东 南 大 学 考 试 卷（ A 卷）

课 程 名 称 计算结构（英文） 考试学期 15-16-2 得分

适 用 专 业 信息学院 考 试 形 式 闭卷 考试时间长度 120 分钟

题目	一（15）	二（10）	三（10）	四（15）	五（8）	六（42）	总 分
得分							
批阅人							

自觉遵守考场纪律 如考试作弊 此答卷无效

姓名

学号

线 封 密

一、 Translate into Chinese (total 15 points)

1. **(5 points)** The basis for the performance advantage of a two-level memory is a principle known as locality of reference. This principle states that memory references tend to cluster. Over a long period of time, the clusters in use change, but over a short period of time, the processor is primarily working with fixed clusters of memory references.

   两级存储器所具有的性能上优势的基础是局部性原理。这个原理表明对存储器的访问趋向于集束的形式。对于长时间的进程，所访问的集束是变化的，但是在短时间，处理器主要访问固定的存储器集束。

2. **(5 points)** A wide variety of addressing modes is used in various instruction sets. These include direct, indirect, register, register indirect, and various forms of displacement, in which a register value is added to an address value to produce the operand address.

   在不同的指令集中使用多种地址模式。这些模式包括直接寻址、间接寻址、寄存器寻址、寄存器间接寻址、以及多种移位寻址。所谓移位寻址是指操作数的地址是一个寄存器内的数值加上地址域的数值。

3. **(3 points)** It is possible to improve pipeline performance by automatically rearranging instructions within a program, so that branch instructions occur later than actually desired.

   通过对程序中的指令自动重新排序，使转移指令的执行晚于程序中的实际设定，有可能提高流水线的性能。

4. **(2 points)** A superscalar processor exploits what is known as instruction-level parallelism, which refers to the degree to which the instructions of a program can be executed in parallel.

   超标量处理器利用了我们所知道的指令层面的并行性，这种并行性是指程序指令能够并行操作的程度。

二、 Fill blanks (total 10 points , 1 points/blank)

1. A computer has a cache and a main memory. If a referenced word is in the cache, 20ns is required to access it. Otherwise, a two-level access is performed, in which an additional 60ns is needed to load the block with the word into the cache. If the cache hit ratio is 0.9, the average time required to access a reference word is (26 ns).

2. A cache is organized as 16K lines of 16 bytes each. Considering a byte addressable main memory of 16 Mbytes (2^{24} = 16M), for direct mapping, the word of address ABCDEF will be loaded in the line numbered (3CDE 或 11 1100 1101 1110 或 15582_{10}) of the cache.

3. The address field refer to the address of a word in memory, which is known as (direct) addressing.

4. If most memory references are relatively near to the instruction being executed, then the use of (relative 或 PC-relative 或 displacement) addressing saves address bits in the instruction.

5. The corresponding reverse Polish expression of "**A-B-C×D"** is (AB-CD×-).

6. (Machine parallelism 或 Machine-level parallelism) is a measure of the ability of the processor to take advantage of instruction-level parallelism.

7. To allow out-of-order issue, it is necessary to decouple decode and execute stages of pipelines. This is done with a buffer referred to as an (instruction window). With this organization, the processor has a lookahead capability, allowing it to identify independent instructions that can be brought into the execute stage.

8. Each instruction cycle is made up of shorter subcycles (e.g., fetch, indirect, execute, interrupt).The execution of each subcycle involves one or more shorter operations called (micro-operations), which are the functional, or atomic, operations of a processor.

9. The (control unit) is the engine that runs the entire computer. It controls everything with a few control signals to points within the processor and a few control signals to the system bus.

10. In a micro-programmed control unit, a set of micro-operations occurring at one time can be described by a (micro-instruction).

三、 Select A, B, C, or D corresponding to the best answer from the given items (total 10 points , 1 points/blank)

1. Computer memory is organized into a hierarchy, where the highest level is (B)
   A. Cache B. Register C. Memory D. Disk

2. The transfer unit between cache an main memory is (D)
   A. Bit B. Byte C. 32-bit word D. Block

3. Among memory access methods, the (D) enables one to make a comparison of desired bit locations within a word for a specified match.
   A. direct access B. random access
   C. sequential access D. associative access

4. An instruction has two address fields: source operand reference and destination operand reference, so the address of the next instruction is (D)
   A. The first address B. The second address
   C. Unknown D. Implicit

5. An instruction of indirect addressing mode is with an address filed containing a decimal value 15. What is the corresponding operand? (B)
   A. Memory location 15
   B. The memory location whose address is in memory location 15
   C. Register 15
   D. The memory location whose address is in register 15

6. The instruction stored in X1 has an address mode of indirect addressing and an address part X2 for operand reference. The effective address of the operand is (C)
   A. X1 B. X2 C. (X2) D. X1+X2

7. There are a number of registers in a processor. The execution time sequence of instructions is controlled by (B)
   A. MAR B. PC C. MBR D. IR

8. In the process of instruction pipeline operation with a branch predictor using dynamic 1-bit history information prediction, for a Loop of 100 iterations, the number of right predictions is (C)
   A. 1 B. 2 C. 98 D. 99

9. RISC organizes its registers into register windows for multilevel procedures. The temporary registers at one level are physically the same as the (A) registers at the next lower level.
   A. parameter B. local C. temporary D. global

10. If we use P_1 to denote instruction-level parallelism and P_2 to denote machine-level parallelism, the actual speed of the superscalar computer is determined by (D)
    A. P_1 B. P_2 C. $P_1 \cup P_2$ D. $P_1 \cap P_2$

四、 Review Questions (total 15 points)

1. **(5 points)** Why is a two-stage instruction pipeline unlikely to cut the instruction cycle time in half, compared with the use of no pipeline?

Answer:

Unequal stage time;
Branch

2. **(5 points)** What is register renaming and what is its purpose?

Answer:

Different physical registers for the same symbolic register;
Resource duplication to avoid unnecessary dependency (W-W, R-W).

3. **(5 points)** What is the difference between horizontal and vertical microinstructions?

Answer:

Wide, more control bits, one bit for a control signal, multiple control signals output at the same time;
Narrow, less control bits, produce more control signals through a decoder, one control signal output at a time.

五、 Answer questions according to given contents (total 8 points)

There is a trade-off among the three key characteristics of memory: namely, capacity, access time, and cost. A variety of technologies are used to implement memory systems, and across this spectrum of technologies, the following relationships hold:

- Faster access time, greater cost per bit
- Greater capacity, smaller cost per bit
- Greater capacity, slower access time

The dilemma facing the designer is clear. The designer would like to use memory technologies that provide for large-capacity memory, both because the capacity is needed

and because the cost per bit is low. However, to meet performance requirements, the designer needs to use expensive, relatively lower-capacity memories with short access times.

The way out of this dilemma is not to rely on a single memory component or technology, but to employ a memory hierarchy. As one goes down the hierarchy, the following occur:

a. Decreasing cost per bit
b. Increasing capacity
c. Increasing access time
d. Decreasing frequency of access of the lower memory

Thus, smaller, more expensive, faster memories are supplemented by larger, cheaper, slower memories. The key to the success of this organization is item (d): decreasing frequency of access. The use of multiple levels of memory to reduce average access time works if the above conditions (a) through (d) apply. Condition (d) is generally valid, and the basis for the validity of condition (d) is a principle known as locality of reference.

(1) What are the key characteristics of memory? **(2 points)**

Answer:

Capacity, access time, and cost.

(2) What is the trouble of memory design? **(2 points)**

Answer:

Dilemma of Capacity and performance

(3) What is the solution of the design trouble? **(2 points)**

Answer:

Memory hierarchy

(4) What makes the condition (d) be always satisfied? **(2 points)**

Answer:

Locality of reference

六、 Problems (total 42 points)

1. **(10 points)** A four-way set-associative cache has lines of 16 bytes and a total size of 8k bytes. The main memory of 16-Mbyte is byte addressable. CPU is to read a data with address ABCDEF from the Cache-Memory structure. Describe the reading process step by step considering the cases of **Hit** and **Miss**.

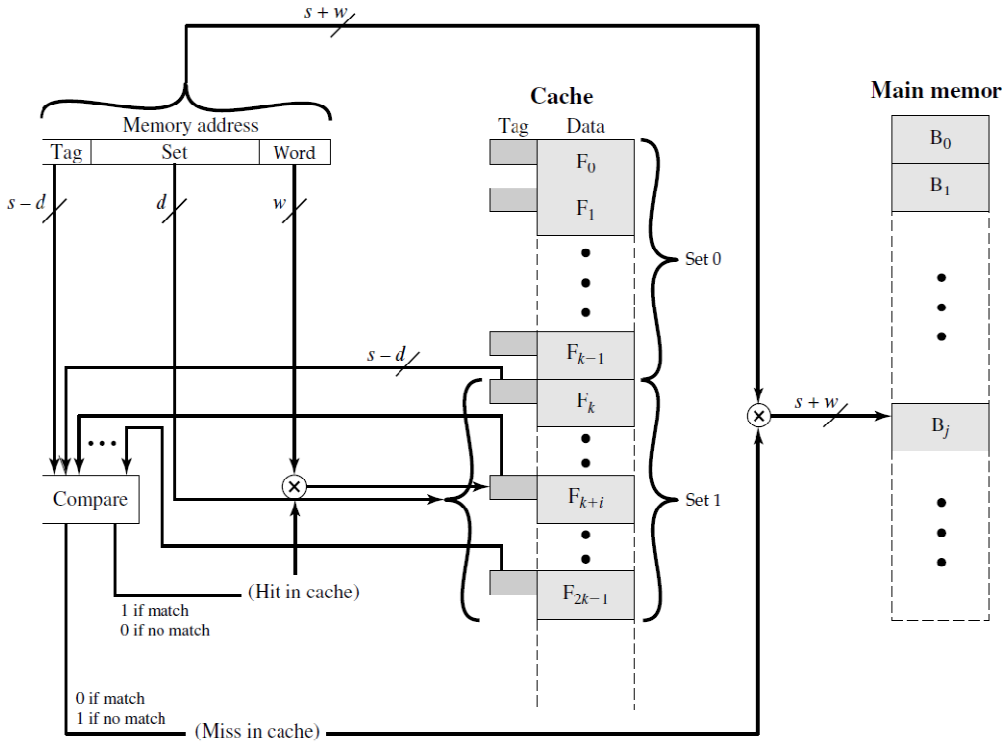

Figure 1 Set Associative Cache Organization

Answer:

For address ABCDEF

a) Address format: 13/7/4
   tag bits: 1010 1011 1100 1 (或 1579_H, 5497_{10})
   set bits: 101 1110 (或 $5E_H$, 94_{10})
   word bits:1111 (或 F_H, 15_{10})
b) Find set 101 1110
c) Compare the tag 1010 1011 1100 1 with the 4 tags of the set
d) If Hit, select the line with the tag 1010 1011 1100 1, and select the Byte with word bit 1111
e) If Miss, search the memory, select the Block including addresses ABCDE0~ABCDEF, put the block onto one line of the set 101 1110 of the cache
f) Read the Byte of address ABCDEF.

2. **(5 points)** Write a program using the stack to compute.

$$X = (A + B * C)/(D - E * F)$$

(The instructions using stack are such as PUSH M, POP M, ADD, SUB, MUL, and DIV etc.)

Answer:

PUSH A
PUSH B
PUSH C
MUL
ADD
PUSH D
PUSH E
PUSH F
MUL
SUB
DIV
POP X

3. **(5 points)** A PC-relative mode branch instruction is 3 bytes long. The address of the instruction, in decimal, is 256028. Determine the branch target address if the signed displacement in the instruction is − 31. (The computer is byte-addressed.)

Answer:

(PC) = 256028+3 =256031
EA = (PC)-31
=256000

4. **(6 points) F**igure 2 illustrates the performance of instruction pipelines without branch, speed up factors vs. instruction numbers (Figure a) and speed up factors vs. instruction stages (Figure b). What can be concluded from the figures?

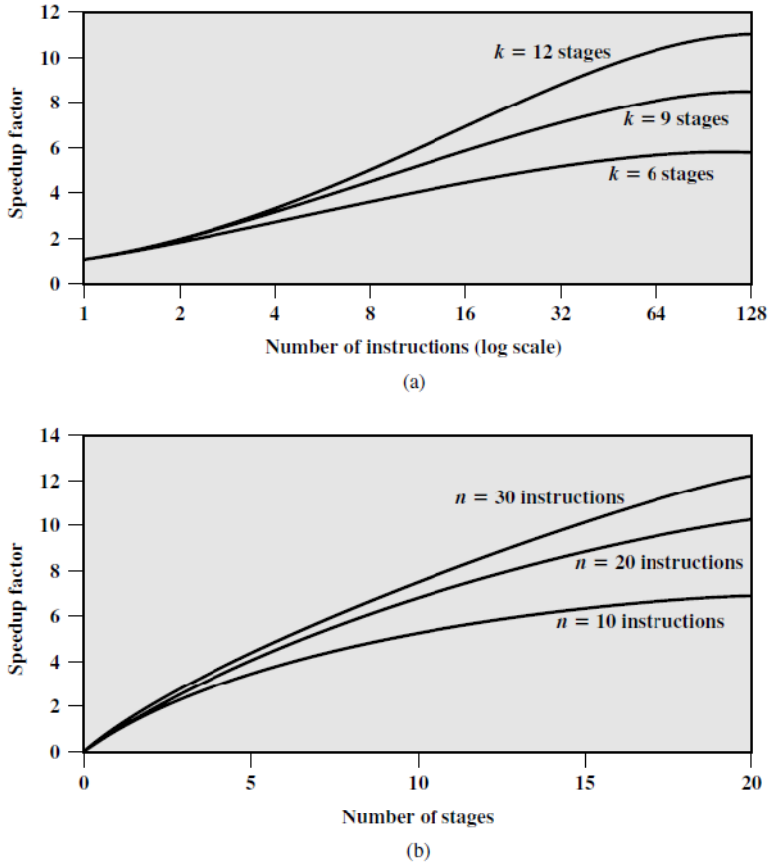

Figure 2 Speedup Factors with Instruction Pipelining

Answer:

Speed up factor increases with stage number; Speed up factor increases with instruction number; Speed up factor approaches the stage number of pipeline for high instruction number.

5. **(10 points)** The instruction “ADD X, Y” includes the following stages:

   a. Instruction Fetch
   b. Load X to AC
   c. ADD Y to AC
   d. Store AC to X

Show the micro-operations of these stages and the corresponding control signals in figure 3.

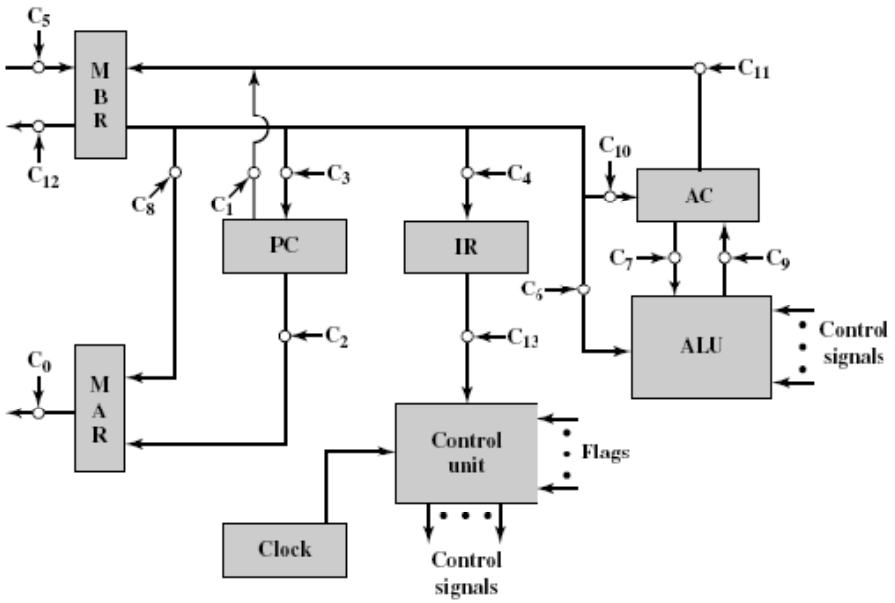

Figure 3 Data Paths and Control Signals

Answer:

a. Instruction Fetch
   MAR←(PC) (C_2) ;
   MBR←Memory (C_5) ;
   IR←(MBR) (C_4) , PC←(PC)+1 ;
b. Load X to AC
   MAR←IR(address1) ;
   MBR←Memory (C_5) ;
   AC←(MBR) (C_{10}) ;
c. ADD Y to AC
   MAR←IR(address2) ;
   MBR←Memory (C_5) ;
   AC←(AC)+(MBR) 或者 ALU←(AC)+(MBR) (C_6, C_7)， AC←(ALU) (C_9);
d. Store AC to X
   MAR←IR(address1) ;
   MBR←AC (C_{11});
   Memory←(MBR) (C_{12}) .

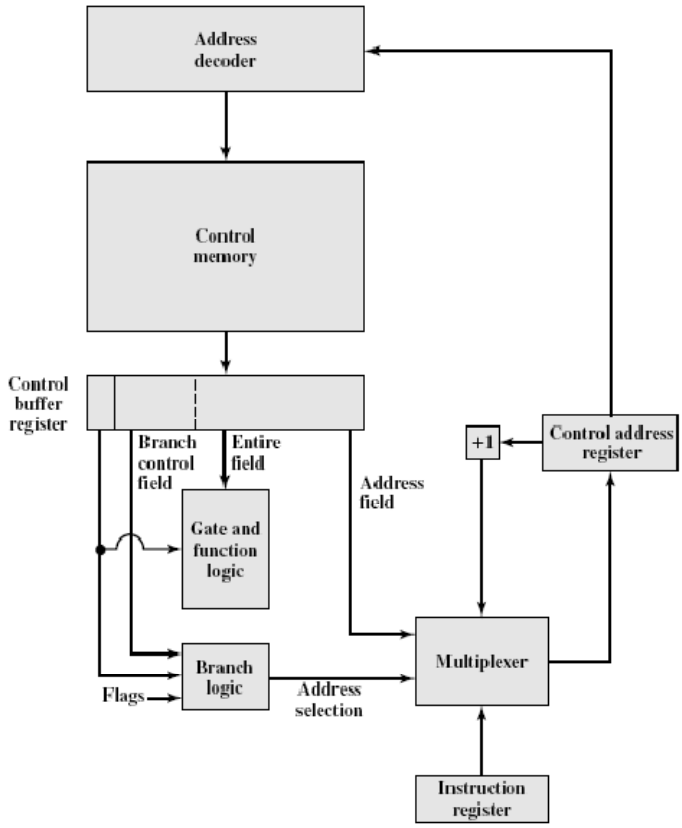

Figure 4 Branch Control Logic: Variable Format

6. **(6 points) F**igure 4 shows a micro-programmed control unit using variable address microinstructions.

   a. What's the format of variable address micro-instructions?
   b. What's the advantage of variable address format?
   c. How to decide the address of the next microinstruction?

Answer:

a) The function of the bits in the address field is variable; A flag bit indicates whether or not the bits in the address field are for address.

b) Save bits and/or produce more control signals.

c) Branch logic selects one address from the multiplexer of three addresses: sequence address, address from the Instruction register, and the address from the address field of the microinstruction.