东 南 大 学 考 试 卷（A卷）

课程名称 计算结构（英文） 考试学期 11-12-2 得分 ____

适用专业 信息学院 考试形式 闭卷 考试时间长度 120分钟

题目	一	二	三	四	总分
得分					
批阅人					

自觉遵守考场纪律 如考试作弊 此答卷无效

装 订 线

姓名 ____ 学号 ____

一、Please write a "T" or "F" in the bracket. (total 10 points)

1. ( ) The speed up factor of a pipeline must not be larger than the stage number of the pipeline.
2. ( ) History bits can be used for branch prediction in the implementation of pipeline.
3. ( ) The delayed branch technique exhibits the same performance in superscalar processing as RISC pipeline.
4. ( ) In register windows the local registers at one level are physically the same as the parameter registers at the next lower level.
5. ( ) An N-window register file can hold N procedure activations without window overlap.
6. ( ) In a superscalar processor, reorder the input instruction helps to improve the speed of instruction execution.
7. ( ) Instruction level parallelism is a measure of the ability of the processor to deal with multiple instructions simultaneously.
8. ( ) Read-write dependency does not affect instruction level parallelism.
9. ( ) Effective address is the address part of a direct addressing instruction.
10. ( ) The outputs from a control unit are divided into two types: Control signals within the processor, Control signals to control bus.

二、Fill in blanks. (1 point / blank, total 12 points)

1. An instruction cycle can be divided into several stages, and, at least, each instruction cycle includes two basic stages: _____, and _____.
2. In designing an instruction pipeline, a variety of approaches can be considered for dealing with conditional branches, such as _____, _____, and _____.
3. There are 152 registers in a computer, 8 of which are left for global use and the others constitute a number of register windows. Each window is consisted of 24 register (8 parameter registers, 8 local registers, and 8 temporary registers). The register window number is _____.
4. RISC is abbreviation of _____.
5. CISC is abbreviation of _____.
6. Convert formula (A+B)+(C×D)+E to reverse Polish _____.
7. There are three possible places for storing the return address for a procedure return, they are _____, _____ and _____.

三. Briefly answer the following questions (**total 18 points**)

1.How does the principle of locality relate to the use of multiple memory levels?

2.Briefly define register addressing.

3.What is a program status word?

4.What are some typical characteristics of a RISC instruction set architecture?

5.What is the essential characteristic of the superscalar approach to processor design?

6.What is the purpose of a control memory? What is the typical sequence in the execution of a mocroprogrammed control unit?

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四. Comprehensive problems (total 60 points)

1. **(8 ponits)** Consider a 16-bit processor in which the following appears in main memory, starting at location 200:

Load to AC	Mode
500	
Next instruction	

The first part of the first word indicates that that instruction loads a value into an accumulator. The mode field specifies an addressing mode and, if appropriate, indicates a source register; assume that when used, the source register is R1, which has a value of 400. There is also a base register that contains the value 100. The value of 500 in location 201 may be part of the address calculation. Assume that location 399 contains the value 999; location 400 contains the value 1000, and so on. Determine the effective address and the operand to be loaded for the following address modes:

a. Immediate
b. Direct
c. Indirect
d. Register

2. **(8 points)** There is a four-stage pipeline with stages of fetch instruction (FI), decode instruction (DI), fetch operands (FO), and execute instruction (EI).

(1) Draw a diagram to show the timing of the instruction pipeline operation for four successive instructions without branch, and

(2) Draw a diagram to show the timing of the instruction pipeline operation for the case of a branch is taken in the 3rd instruction and jumps to instruction 10. (Predict never taken)

3. **(10 points)** Consider the following loop:

```
S := 100;
for K := 1 to 100 do
S := S+K;
```

A generic assembly language would look like

```
    LD   R1, 100
    LD   R2, 1
LP  ADD  R1, R1, R2
    BEQ R2. 100, EXIT
    ADD R2, R2, 1
    JMP LP
```

A compiler for a RISC machine will introduce delay slots into this code so that the processor can employ the delayed branch mechanism. Show the code using delayed branch method to implement the loop.

4.(**12 points**) There are some dependencies in the following code fragment.

a) Point out 4 dependencies of which at least,

b) increase instruction parallelism using register renaming, and

c) Point out dependencies after Register Renaming.

```
I1: R1 ← R3
I2: R3 ← R3 ADD R5
I3: R4 ← R3 + 1
I4: R3 ← R5 + 1
I5: R6 ← R3 SUB R4
```

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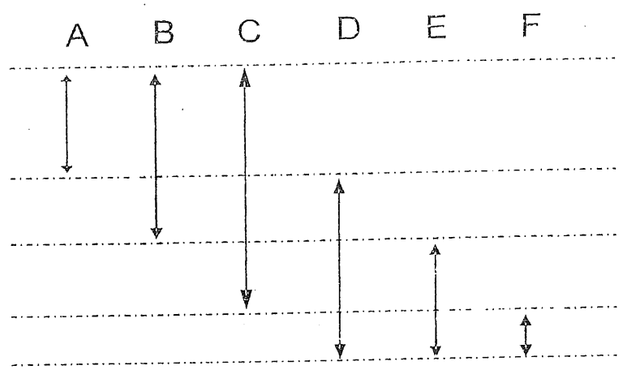
5.(**10 points**) Assume a program with six symbolic registers (A, B, C, D, E, F) to be compiled into three actual registers (R1, R2, R3), the time sequence of active use of each symbolic register is shown in the figure. Give a solution of register assignment.



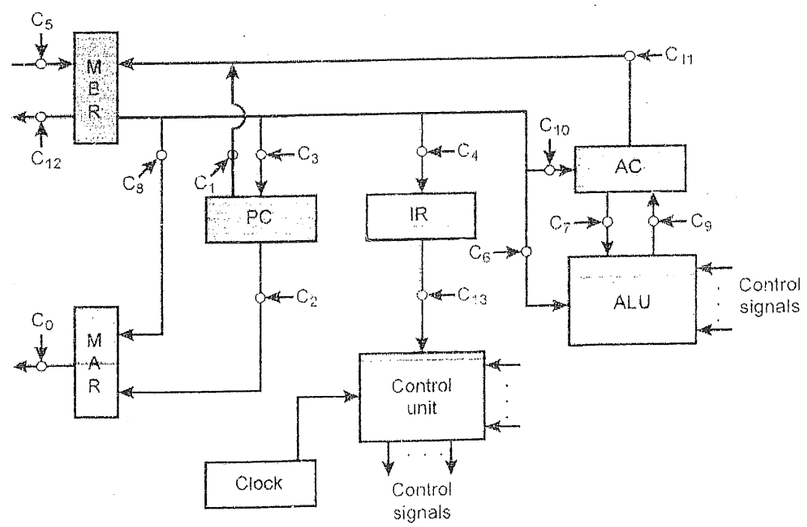


Figure 1

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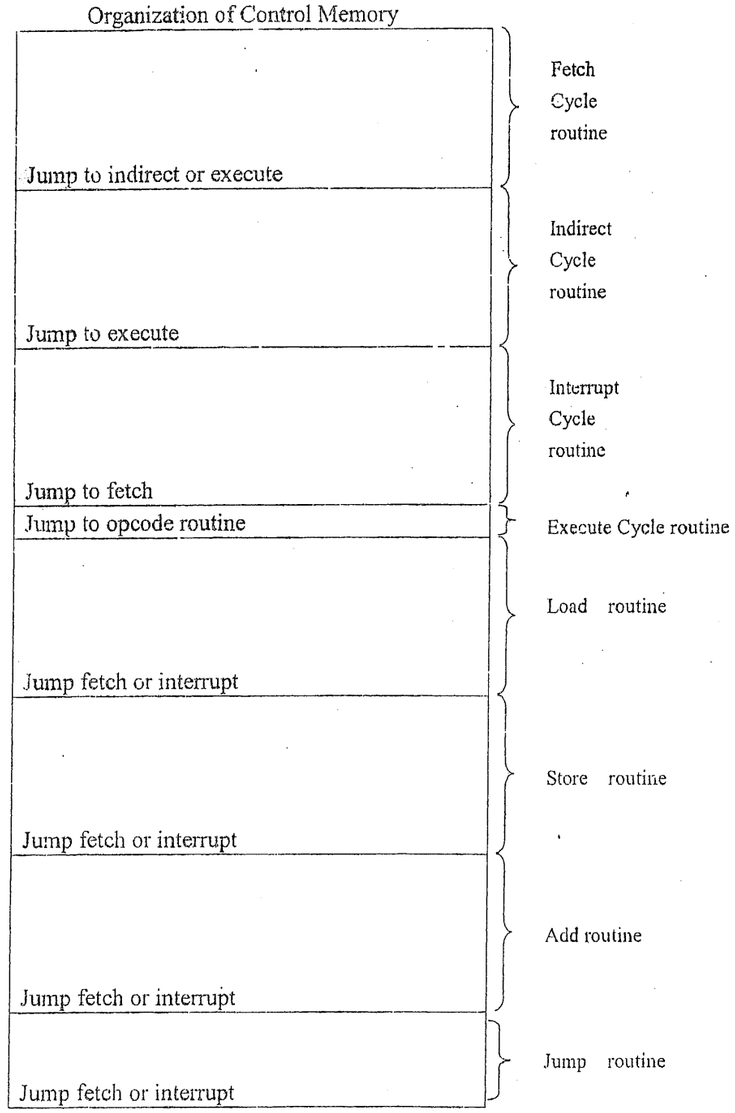
6. **(12 points)** Show the micro-operations(microinstructions) for the processor in figure 1 for the following instructions, including Fetch Cycle, Indirect Cycle and Interrupt Cycle, and then these microinstructions could be arranged in the following control memory.

- Load Accumulator
- Store Accumulator
- Add to Accumulator
- Jump if AC=0

Organization of Control Memory



(4)

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