题目	一（10）	二（10）	三（10）	四（10）	五（10）	六（50）	总分
得分							
批阅人							

自觉遵守考场纪律 如考试作弊 此答卷无效

姓名

学号

一、Translate into Chinese (total 10 points)

1. **(5 points)** The way out of this dilemma (难题，困境) is not to rely on a single memory component or technology, but to employ a memory hierarchy（多级，分层）. Thus, smaller, more expensive, faster memories are supplemented（补充）by larger, cheaper, slower memories. The key to the success of this organization is decreasing frequency of access of the memory by the processor.

2. **(3 points)** A superscalar processor typically fetches multiple instructions at a time and then attempts to find nearby instructions that are independent of one another and can therefore be executed in parallel.

3. **(2 points)** The simple instruction set of a RISC lends itself to efficient pipelining because there are fewer and more predictable operations performed per instruction.

二、Fill blanks (total 10 points , 2 points/blank)

1. In the three mapping methods of caches, the set associative mapping actually includes the other two techniques. For a cache of 1024 lines, if the set size is 1024 line/lines it is associative mapping, and if the set size is 1 line/lines it is direct mapping.
2. The corresponding infix expression of "**AB+CD-×**" is (A+B)×(C-D)
3. There are 136 registers in a computer, 8 of which are left for global use and the others constitute a number of register windows. Each window is consisted of 24 register (8 parameter registers, 8 local registers, and 8 temporary registers). The register window number is 8, and the register window structure supports procedures with depth of 7 at most without window overlap.

三、Fill blanks according to given contents (total 10 points, 2 points/blank)

An alternative to a hardwired control unit is a microprogrammed control unit, in which the logic of the control unit is specified by a microprogram which consists of a sequence of instructions in a microprogramming language. These instructions mentioned above called microinstructions are very simple and they specify micro-operations.

A microprogrammed control unit is a relatively simple logic circuit that is capable of sequencing through microinstructions and generating control signals to execute each microinstruction.

Sequencing in a microprogrammed control unit is implemented by controlling the order of microinstructions to be executed. Microinsturctions are saved in a control memory. The control memory address for the next microinstruction is generated based on the current microinstruction, condition flags, and the contents of the instruction register, and sent to a control address register (CAR).

As in a hardwired control unit, the control signals generated by a microinstruction are used to cause register transfer and ALU operations.

(1) Give a title for the above phases: _____

(2) In the microprogrammed control unit, the microprogram is used to specify _____

_____

(3)In the microprogrammed control unit, micro-operations are determined by _____

_____

(4) The tasks that microprogrammed control unit can do are _____

_____

(5) The control memory address of the next microinstruction is in _____

_____

四、Select A, B, C, or D corresponding to the best answer from the given items (total 10 points , 2 points/blank)

1. When a processor accesses a cache, the reference address is (C)
   A. Register address B. Cache address
   C. Main memory address D. Disk address

2. The degree of instruction-level parallelism is determined by the frequency of (C) and procedure dependency in the code.
   A. Read-Write dependency B. Write-Write dependency
   C. Write-Read dependency D. Resource conflict

3. There are a number of registers in a processor. The execution time sequence of instructions is controlled by (B)
   A. MAR B. PC C. MBR D. IR

4. To perform a sequence of 16 instructions using pipeline, each instruction is divided into 4 stages FI, DI, EI and WO, where each of the stages require **1 cycle**, **1 cycle**, **2 cycles** and **1 cycle** respectively. No branch is in the sequence. The speed up factor of the pipeline is (C)
   A. 5 B. 16/7 C. 4 D. 64/19

5. A vertical formatted microinstruction with a 4-bit control field and an 8-bit address field can produce ( ) different control signals at most.
   A. 16 B. 12 C. 8 D. 4

五、Review Questions (total 10 points)

1. **(5 points) Delayed branch** is a technique used in RISC to improve processor performance. What is a delayed branch? Given the definition and the motivation of the technique.

2. **(5 points)** There are 3 address formats for microinstructions: two-address, one-address, and variable address fields. What is the mean and motivation of the **variable address** format?

六、Problems

1. **(10 points)** Consider a computer with a main memory of 1M bytes addressed at byte level and a cache of 64 Kbytes, where the cache line size is 16 bytes.

   a. Show the address format for direct-mapped cache;

   

   b. Give the **tag**, **line**, and **word offset** values of address CABBE (in hexadecimal) for the direct-mapped cache.

   c. Show the address format for a two-way set-associative mapped cache;

   d. Give the **tag**, **set**, and **word offset** values of address CABBE (in hexadecimal) for the two-way set-associative mapped cache;

   e. Describe the process in accessing the address CABBE of a computer with the two-way set-associative mapped cache.

   Note: The address format above means the distribution of tag bits, line/set bits, and word bits

2. **(10 points)** Given the following instruction sequence:

   I1: R1 = 100
   I2: R1 = R2 + R4
   I3: R2 = R4 – 25
   I4: R4 = R1 + R3
   I5: R1 = R1 + 30

   a. Identify the write-read, write-write, and read-write dependencies in the instruction sequence.

   b. Use register renaming method to improve the independency of the sequence.

   c. Identify dependencies of the instruction sequence after register renaming.

3. **(10 points)** Consider an instruction pipeline of four stages: fetch instruction (FI), decode instruction (DI), fetch operands (FO), and execute instruction (EI).

   a. Draw a diagram to show the timing of the instruction pipeline operation for 5 successive instructions without branch;
   b. Draw a diagram to show the timing of the pipeline for the case that a branch is taken in the 4th instruction after EI and jumps to instruction 10;
   c. Assume 5 effective instructions are performed in both of the above cases. Calculate the speed up factors of the two cases using pipeline.

4. **(10 points)** Assume a program with six symbolic registers (A, B, C, D, E, F) to be compiled into three physical registers (R1, R2, R3), the active time in the program of each symbolic register is as follows. Give a solution of register assignment.

   Active time of symbols:
   A: From Line 1 to Line 10
   B: From Line 2 to Line 13
   C: From Line 8 to Line 15
   D: From Line 11 to Line 20
   E: From Line 12 to Line 100
   F: From Line 16 to Line 124

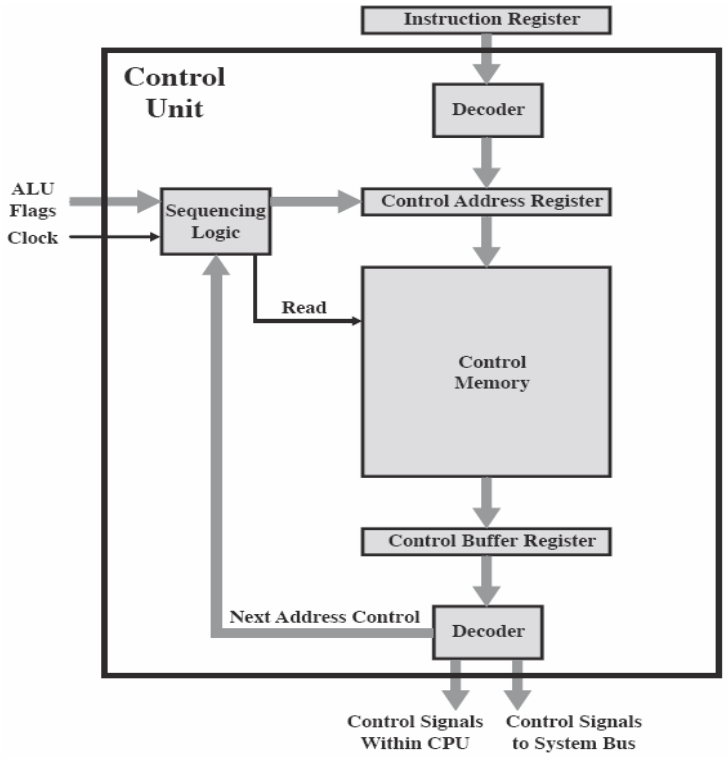

Figure 1. functioning of micro-programmed control unit

5. **(10 Points)** Figure 1. presents the diagram of functioning of micro-programmed control unit. Please try to answer the following questions:

a. What is the purpose of the control memory?

b. What is the difference in function of the upper and the lower **Decoders**?

c. Give the three possible control memory address of the next microinstruction?

d. Describe briefly the work steps of the micro-programmed control unit?