Test Paper Of Computation Structure (A)

PART A

Directions: True or False. Please write a "T" or "F" in the bracket at the head of each problem.

1. (F) All of the addressing techniques need some operations of memory reference.
2. (T) The base-register addressing also takes advantage of the locality of memory references.
3. (T) Most of the control registers, on most machines, are not visible to the user. Some of them may be visible to machine instructions executed in a control or operating system mode.
4. (F) For a 6-stage pipeline, a six times of speed up in the execution of instructions is certainly possible.
5. (F) The horizontal microinstructions have less length than vertical microinstructions.
6. (F) The concept of superscalar is the same as super pipeline.
7. (F) The window scheme in the use of a large register file provides an efficient organization for storing local scalar and ~~global variables~~ in registers.
8. (T) With variable-length instructions, addressing can be provided efficiently and compactly, while the principal price to pay is an increase in the complexity of the CPU.
9. (T) Without register renaming, to duplicate the functional units in a superscalar machine is less effective in the performance improvement.
10. (T) The concept of superscalar design is generally associated with the RISC architecture, so the same superscalar principles can't be applied to a CISC machine.
11. (T) The U and V integer units of Pentium processor are capable of executing two instruction which conform with the pairing rules specified in Pentium's data book, in parallel.
12. (T) In the microprogrammed control circumstance, the execution of a machine instruction is by executing a relevant fragment of the microprogram consisting of a sequence of microinstructions stored in the control memory.
13. (F) The execution of unencoded microinstructions takes longer time than the execution of encoded ones.
14. (T) In practice, microprogrammed control units are not design using a pure unencoded or horizontal microinstruction format. At lease some degree of encoding is used to reduce control memory width to simplify the task of microprogramming.
15. (F) The Pentium is essentially a RISC computer, while the PowerPC is essentially a CISC computer.
16. (T) The user-visible registers in CPU is a kind of which can be referenced by the program written in machine language.
17. (T) It is easier to design in firmware than hardware, but it is more difficult to write a firmware program than a software program.
18. (T) The microinstruction consists of a set of micro-operations occurring at one time.

PART B

Section 1

Directions: Fill in the blanks with given choices, note that the given choices for each problem may not be equal to the blanks.

1. According to the location where an operand lies, the addressing mode is (4) when the operand is in the register; (5) when the reference of the operand is in the register; (1) when the operand is right in the instruction; (3) when the memory address of the operand is in the instruction; (2), (6), (7) when the address of the operand is obtained by the addition of the content of a certain register and the displacement in the instruction.((1)immediate addressing; (2)indexing; (3)indirect addressing; (4)register addressing; (5)indirect register addressing; (6)relative addressing; (7)base-register addressing)
2. In (1) mocroinstruction, every bit in the control field maches to a control line. (2) microinstruction, however, needs decoders to translate its code into individual control signals. The advantage of (2) microinstructions is that they are more compact than (1) microinstructions. Without additional amount of logic, (1) microinstructions are of faster speed. (①horizontal; ②vertical)
3. The following branch prediction techniques can be categorized into two types (1) (2) and (3) are static: they do not depend on the execution history up to the conditional branch instruction; (4) (2) and (5) are dynamic: they depend on the execution history.(①predict never taken; ②the taken/not taken switch; ③predict always taken; ④predict by opcode; ⑤branch history table)
4. An interrupt is generated by (4), and it may occur at (2) during the execution of a program. An (2) is generated from software, and it is provoked by the (6) of an instruction. (①exception; ②random times; ③execution; ④a signal from hardware; ⑤regular times)
5. In register indirect addressing mode, the instruction specifies a register in the CPU whose content is the address of (1) in memory. In other words, the selected register contains (2) of the operand rather than the operand itself. Before using a register indirect addressing mode instruction, the programmer must ensure that (2) of the operand is placed in (3) with a previous instruction. A (5) to the register is then equivalent to specify a memory address. The advantage of this addressing mode is that (6) of the instructions uses fewer bits to select a register than would have been required to specify a memory address directly. In addition, this addressing uses (4) than indirection addressing. (①the operand; ②the address; ③register; ④one less memory reference; ⑤reference; ⑥the address field)
6. The main advantage of the microprogrammed control is the fact that once the hardware configuration is established, there should be no need for further (1). If we want to establish a different control sequence for the system, all we need to do is to specify a (5) for control memory. The hardware configuration (4) (3) for different operations; thing that (5)(4) is the microprogram residing in control memory. (①hardware or wiring changes; ②different set of microinstructions; ③should not be changed; ④must be changed)

Section 2

Directions: Fill in the blanks without given choices.

1. The key elements shared by most RISC designs are a limited and simple instruction set, a large number of general-purpose registers, or the use of compiler technology to optimize register usage, and an emphasis on optimizing the instruction pipeline.
2. There are four common characteristics of RISC architecture: one instruction per circle, register-to-register operations, simple addressing modes, simple instruction formats.
3. The most of techniques to implement the control unit fall into two categories: microprogrammed implementation and hardware implementation. which is essentially a combinatorial circuit.
4. For increasing instruction-level parallelism, five fundamental limitations to the parallelism

must be coped with: true data dependency, antidependency, output dependency, procedural dependency resource conflict. Resource conflict can be overcome by duplication of resources. With register renaming, it is possible for a processor to eliminate antidependency and output dependency. By using an ~~out of order issue~~ branch prediction the process achieves a lookahead capability to identify independent instructions that can be up to the execute stage.

5. The difference between the operations provided in HLLs and those provided in computer architecture is known as semantic gap.
6. A six-window register file can hold up to 15 procedure calls in case of not saving a window.
7. Each entry in the BHT consists of three elements: the address of a branch instruction, some number of history that read the status of use of that instruction information about the target instruction
8. An instruction cycle includes the following subcycles: fetch, execute, interrupt. An indirect subcycle may be needed if the execution of an instructions involves one or more operands in memory. In fact, each of the subcycles involves a series of steps which is referred to as micro-operation.

Section 3

Directions: Give the complete words for each of the following abbreviation.

CAR CBR HLL PSW ALU MBR MAR RISC MESI BHT MMU IR

PART C

Directions: Solve the following comprehensive problems, please give your reasoning process.

1. A PC-relative mode branch instruction is stored in memory at address 620_{10}. The branch is made to location 530_{10}. The address in the instruction is 10 bits long. What is the binary value in the instruction?

EA = A + (pc)
A = EA - (pc)
= 530 - 620
= -90

$(1011010)_2$
= 10100101+1
= 10100110

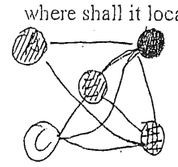
2. Suppose the control unit of a CPU adopts microprogramming, with a control memory of 512 48-bit wide words. The microprogram is able to branch anywhere within the control memory. There are 4 flags used to control the branch and the microinstructions are the horizontal kind. shown as the follows:

Control field	Branch control field	Address-field

How many bits are assigned to each field?

$512 = 2^9$

3. Graph coloring is used in RISC compilers. Assume a program with 5 symbolic registers(A,B,C,D,E) to be compiled into 3 actual registers(R1,R2,R3). The time sequence of active use of each symbolic register is shown in the following figure.
   (a) Please draw the register interference graph that has only been given nodes and show how should the actual registers be assigned to every symbolic register.
   (b) Is there any symbolic registers cannot be assigned with actual registers? If there is any, where shall it locate?



Yes. memory.

A: R1
B: R2
D: R3

4. Show the micro-operations and control signals in the following table for the CPU in following figure(you can refer to Figure 16.5 on page 587 for the clear control signals) for the instructions of ADD to Accumulator (ADD A)with indirect addressing mode.

Instruction sub-cycles	Micro-operations	Active control signal
Fetch	t1:MAR←(PC) t2:MBR←Memory PC←(PC)+1 t3:IR←(MBR)	C_2 C_5, C_R C_4
Indirect	t1:MAR ← IR(address) t2: MBR ← Memory t3: IR(address) ← MBR(address)	C_8 $C_5 . C_R$ C_4
Interrupt:	t1: MBR ← (pc) t2: MAR ← Save-address pc ← Rountine-address t3: Memory ← (MBR)	C_{11} C_{12}, W_W

5. Consider the following symbolic language program fragment:

Address		
200	LOAD	B←Memory
201	STORE	Memory←B+1
202	LOAD	C←Memory
203	STORE	Memory←C+1
204	SUB	X←B-C
205	JUMPZ	300
...		
300		

A register-to-register instruction has the following two phases:

F: Instruction fetch

E: Execute. Performs an ALU operation with register input and output

For load and store operations, three phases are required:

F: Instruction fetch.