TITLE OF THE EXPERIMENT

The proportionality and superposition theorems.

PREREQUISITE KNOWLEDGE

- ❏ OHM’s law
- ❏ Kirchhoff's current law
- ❏ Kirchhoff’s voltage law
- ❏ Calculating effective resistance in series
- ❏ Calculating effective resistance in parallel
- ❏ Mesh current analysis
- ❏ Nodal voltage analysis
- ❏ Thevenin's theorem
- ❏ Norton's theorem

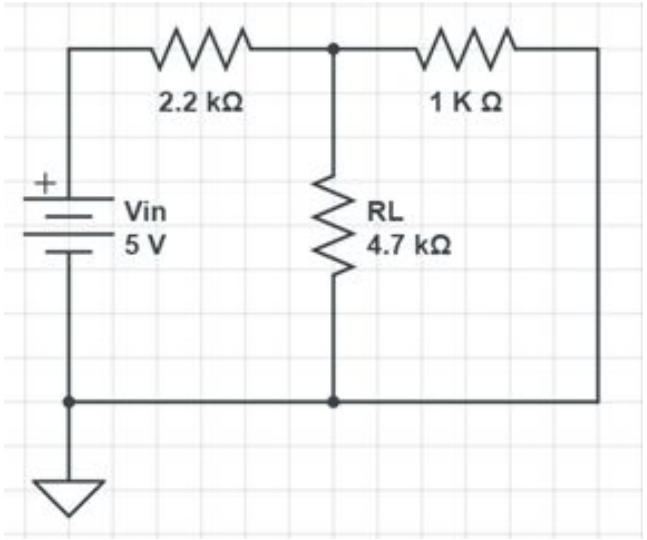
PROPORTIONALITY THEOREM - statement

The Proportionality Theorem states that the response of a circuit is proportional to the source acting on the circuit. This is also known as linearity. The proportionality constant A relates the input voltage to the output voltage as,

$$V_{out} = A \cdot V_{in}$$

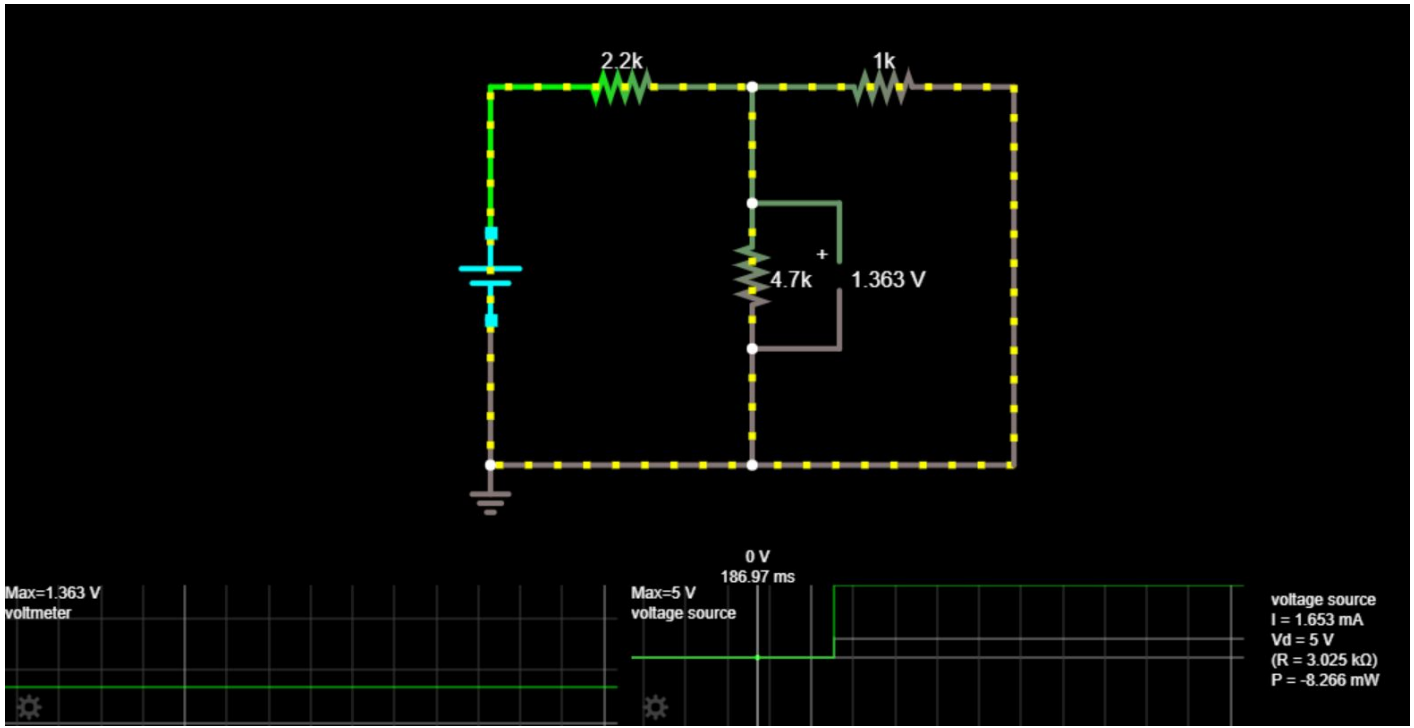
The problem statement

The proportionality factor A is sometimes referred to as the gain of a circuit. For the circuit in the given diagram, the source voltage is $\mathbf{V_{in}}$. The response $\mathbf{V_{out}}$ is across the 4.7kΩ resistor.



Circuit simulation

Link : https://tinyurl.com/ycqfcg4v



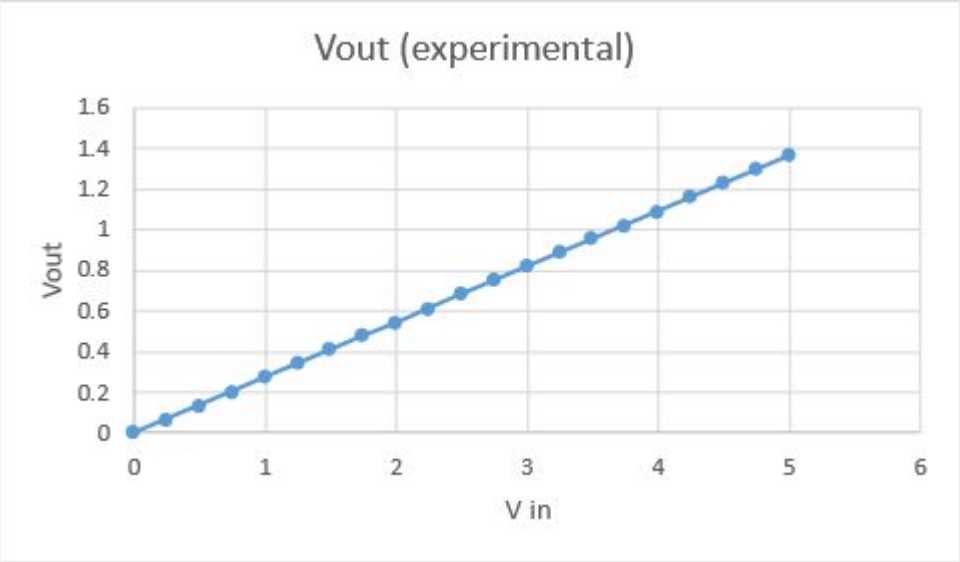
The observation table

SHEET 1 of the given link

https://amritavishwavidyapeetham-my.sharepoint.com/:x:/g/personal/aieb_25672_cb_students_amrita_edu/EQsYVX_pRgpAni2XgHIMwdsB7QOCGvNoDzG1p6QpKNoauA?e=ZNSvlV

Proportionality Theorem- Vout vs Vin Graph

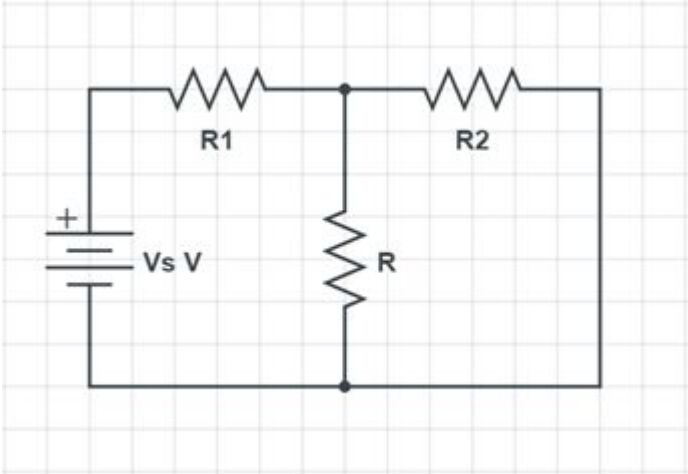
The graph we get on plotting the experimental values



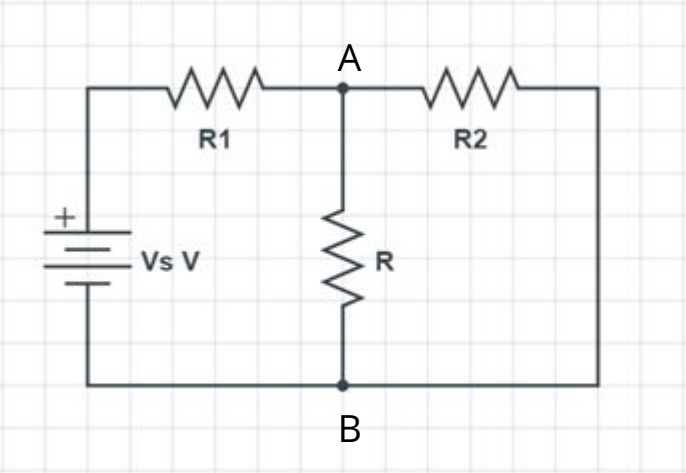
Solving the given problem statement computationally

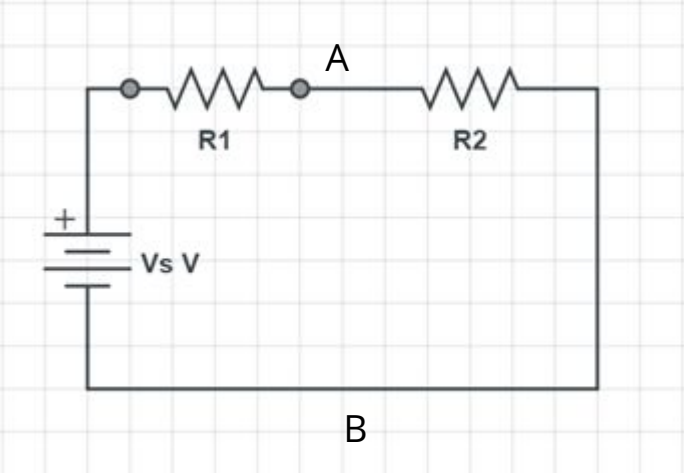
The Thevenin’s theorem states that,

Thevenin's Theorem states that it is possible to simplify any linear circuit, no matter how complex, to an equivalent circuit with just a single voltage source and series resistance connected to a load.



Using the above stated Thevenin's theorem we can simplify the above circuit as the following one,





By observation we can clearly conclude that the two resistance $\mathbf{R_1}$ and $\mathbf{R_2}$ are in parallel, hence the net resistance of the circuit comes out to be,

$$R_{eq} = \frac{R_1 . R_2}{R_1 + R_2}$$

To obtain the net voltage across the wire AB we need to calculate the current flowing through the circuit. For calculating it we can use OHM's law. OHM's law states that the current through a conductor between two points is directly proportional to the voltage across the two points.

From OHM's law, we can relate current with resistance as,

$$I = \frac{V}{R}$$

Here, V is the net voltage of the circuit and **R** is the net resistance of the circuit after removing the joint across AB, hence in the given circuit we can write the current as,

$$I = \frac{V_S}{R_1 + R_2}$$

Now for finding the voltage across AB we can use the Kirchhoff's loop rule. Kirchhoff's loop rule states that the sum of all the electric potential differences around a loop is zero.

Now on applying Kirchhoff's loop rule in the above circuit we get the following,

$$V_{\text{out}} = V_s - \left(\frac{V_S}{R_1 + R_2}\right).R_1$$

And on further simplification we get the following

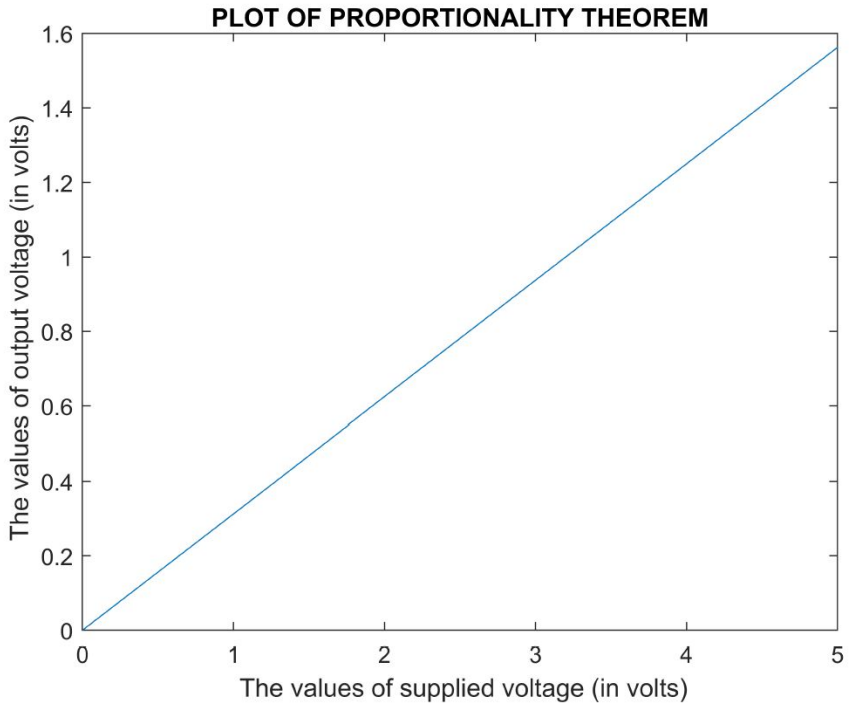
$$\boxed{V_{\text{out}} = V_{\text{in}}\left(\frac{R_2}{R_1 + R_2}\right)}$$

The source voltage is the input voltage that we give. Hence, $\mathbf{V_s} = \mathbf{V_{in}}$.

MATLAB code for computation

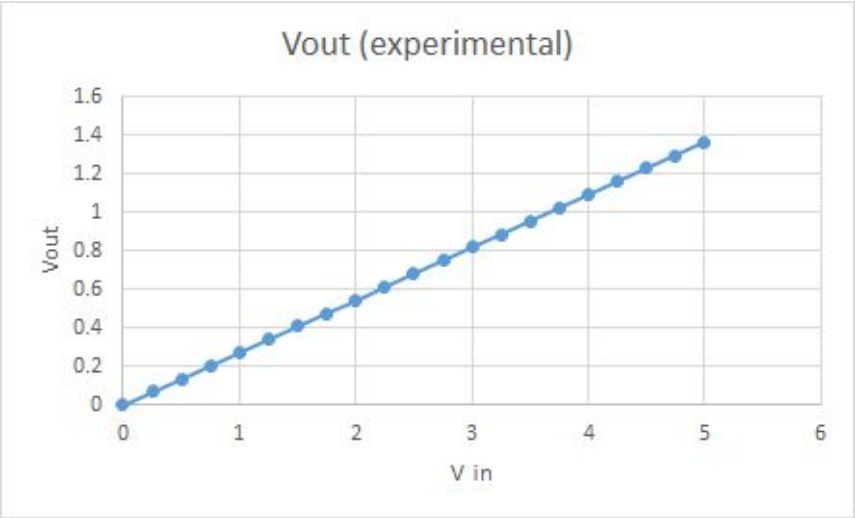
```
Vin = 0:0.25:5;
R1=2.2;
R2=1;
R=R2/(R1+R2);
Vout = Vin*R;
plot(Vin,Vout)
title("PLOT OF PROPORTIONALITY THEOREM")
xlabel(" The values of supplied voltage (in volts)")
ylabel(" The values of output voltage (in volts)")
```

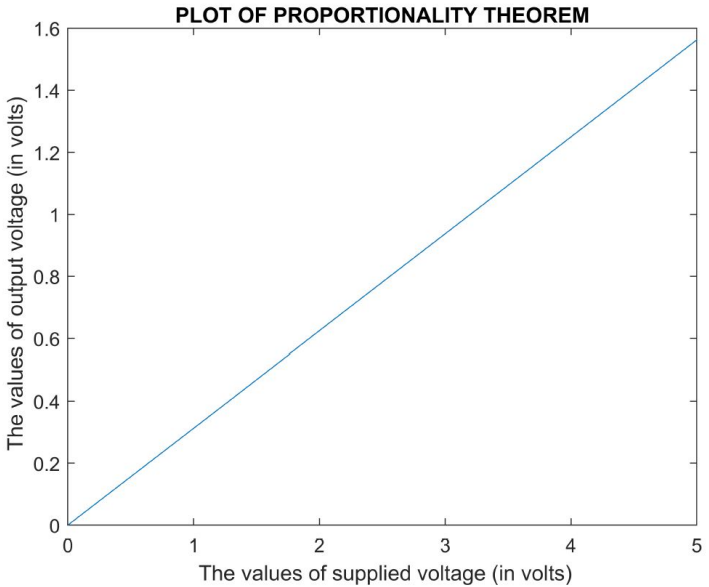
Plot we get as the result



RESULT

Now on plotting a graph of the given values with $\mathbf{V_{in}}$ along x-axis and the experimental and computational values of $\mathbf{V_{out}}$ along y-axis we get the following graphs,





INFERENCE

The value A is calculated by taking the ratio of $\mathbf{V_{out}}$ to $\mathbf{V_{in}}$ or finding the slope of the above graphs i.e.,

$$V_{out} = A \cdot V_{in}$$

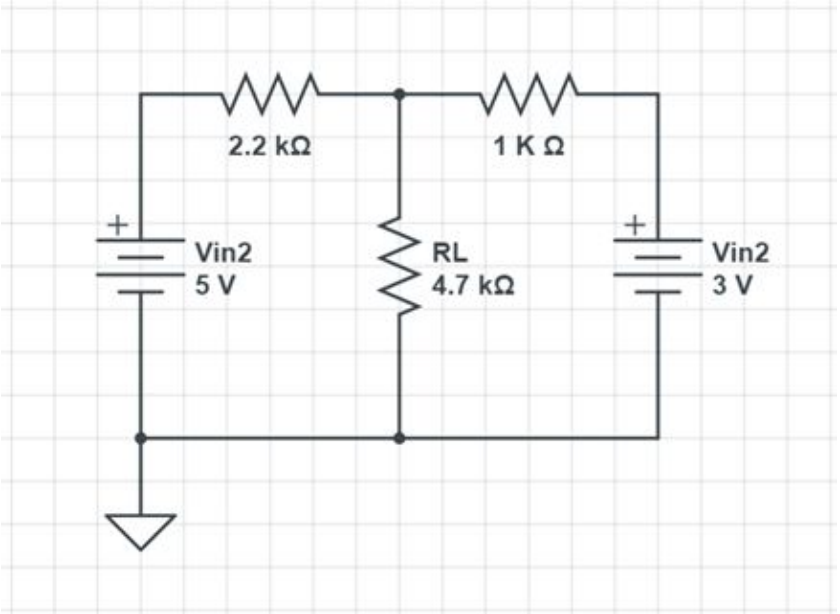
After calculating the value of A, we can observe that it is constant for any value of input voltage $\mathbf{V_{in}}$. This constant A is called the gain of the circuit. Hence, the Proportionality theorem is verified for this circuit.

SUPERPOSITION THEOREM - statement

The Superposition Theorem states that the response of a linear circuit with multiple independent sources can be obtained by adding the individual responses caused by the individual sources acting alone. For an independent source acting alone, all other independent voltage sources in the circuit are replaced by short circuits and all other independent current sources are replaced by open circuits.

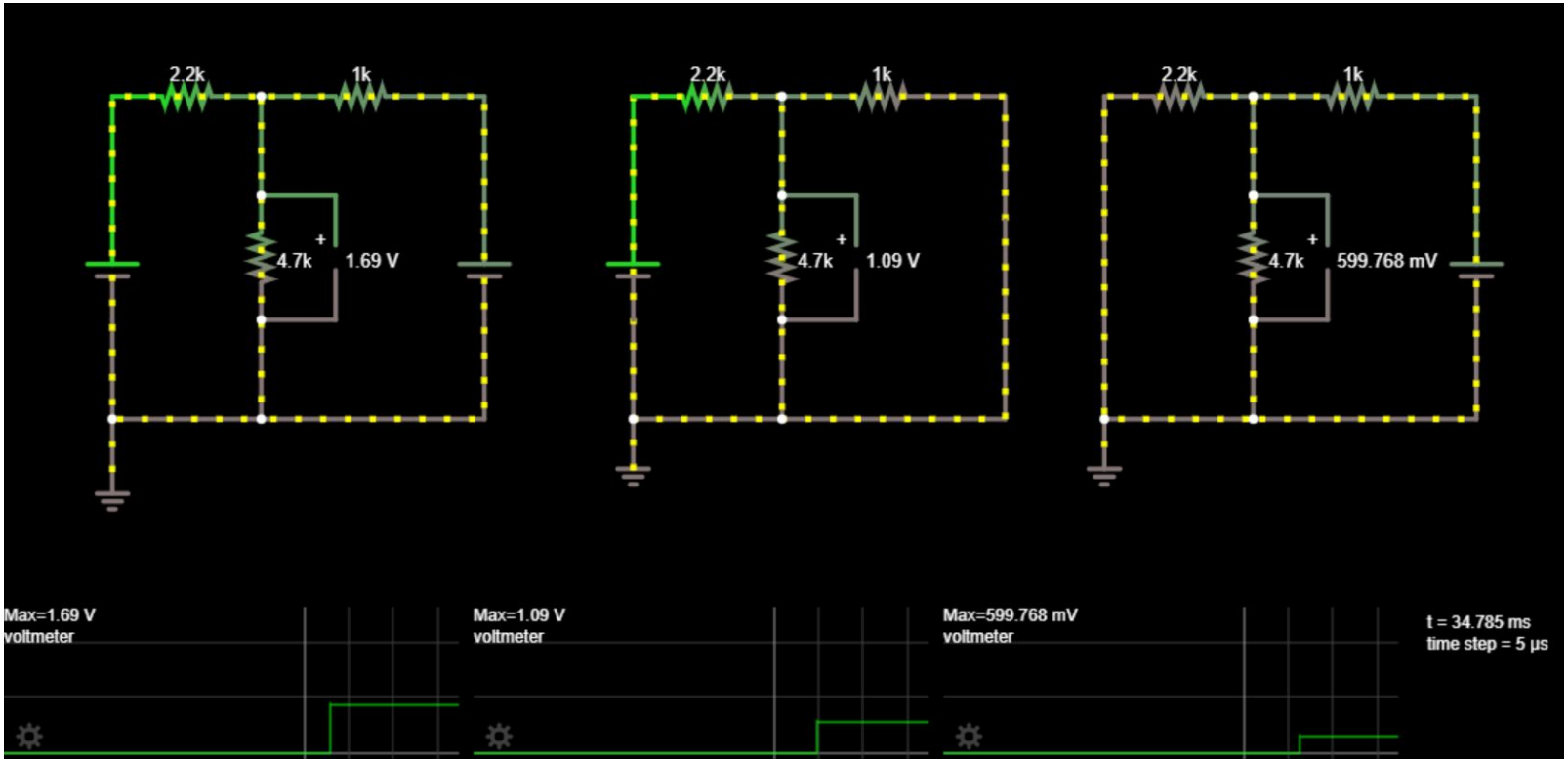
The problem statement

Check whether the given circuit obeys the principle of superposition



Circuit simulation

Link: https://tinyurl.com/ybah4tgt



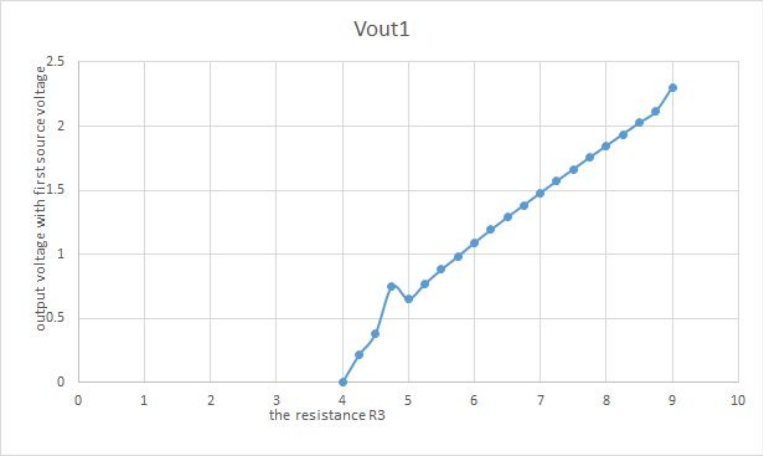
The observation table

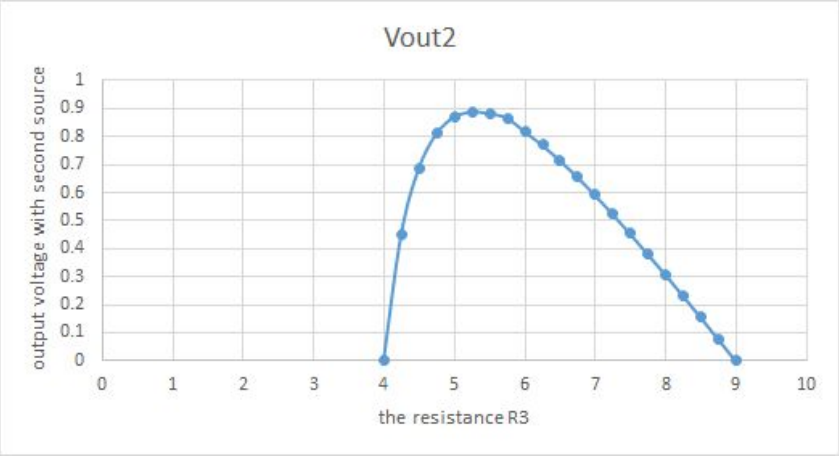
SHEET 2 of the given link

https://amritavishwavidyapeetham-my.sharepoint.com/:x:/g/personal/aieb_25672_cb_students_amrita_edu/EQsYVX_pRgpAni2XgHIMwdsB7QOCGvNoDzG1p6QpKNoauA?e=ZNSvlV

RESULT

Now on plotting a graph of the given values with $\mathbf{R_3}$ along x-axis and the experimental values of $\mathbf{V_{r1}}$, $\mathbf{V_{r2}}$ along y-axis we get the following graphs.

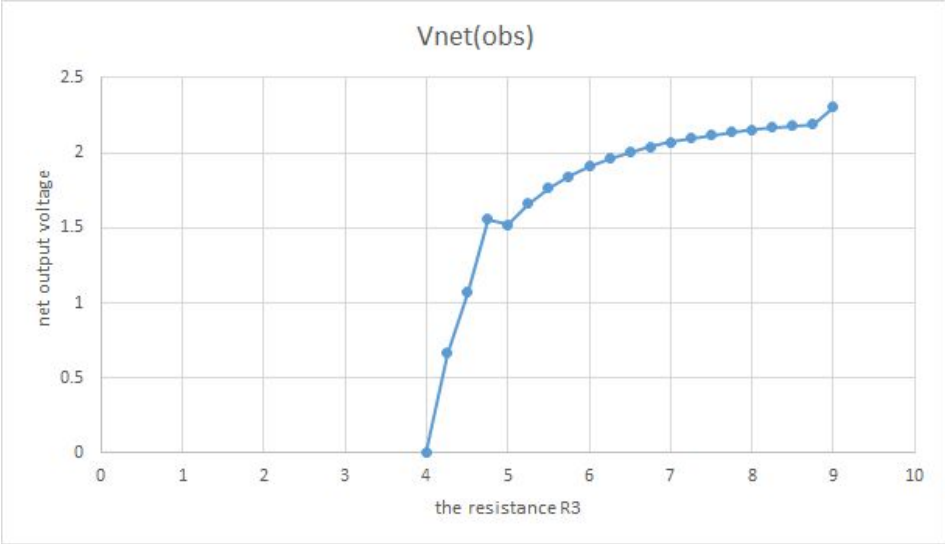




The graph we get on plotting the experimental values.

RESULT - continued

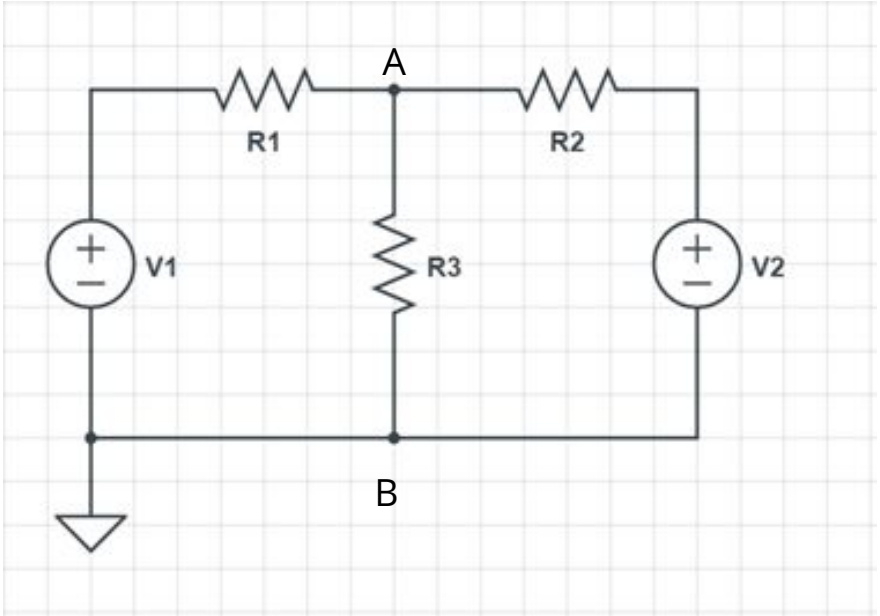
Now on plotting a graph of the given values with $\mathbf{R_3}$ along x-axis and the experimental values of $\mathbf{V_r}$ along y-axis we get the following graph.



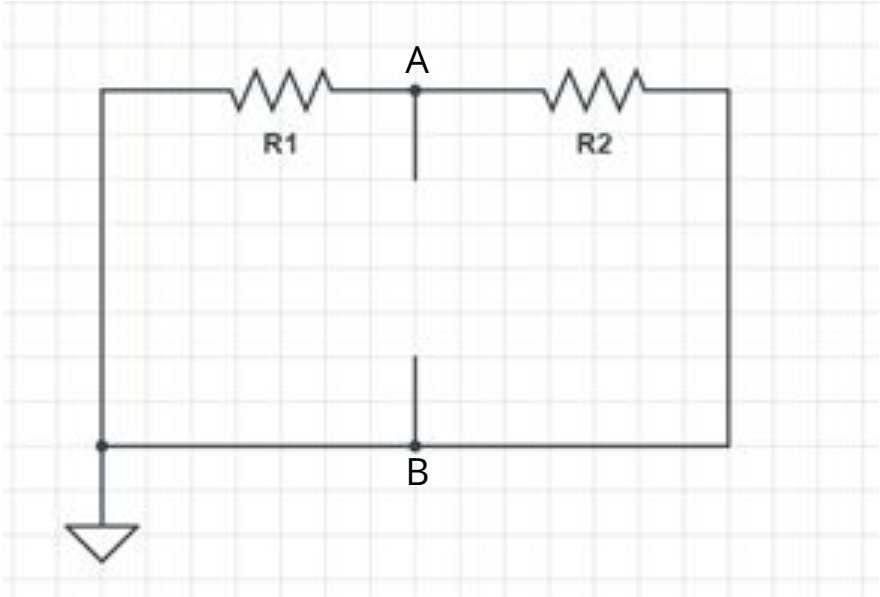
Solving the given problem statement computationally

Let us assume V_1, V_2 as source voltage. Let $V_1 > V_2$.

Case 1 [with 2 source voltage]:

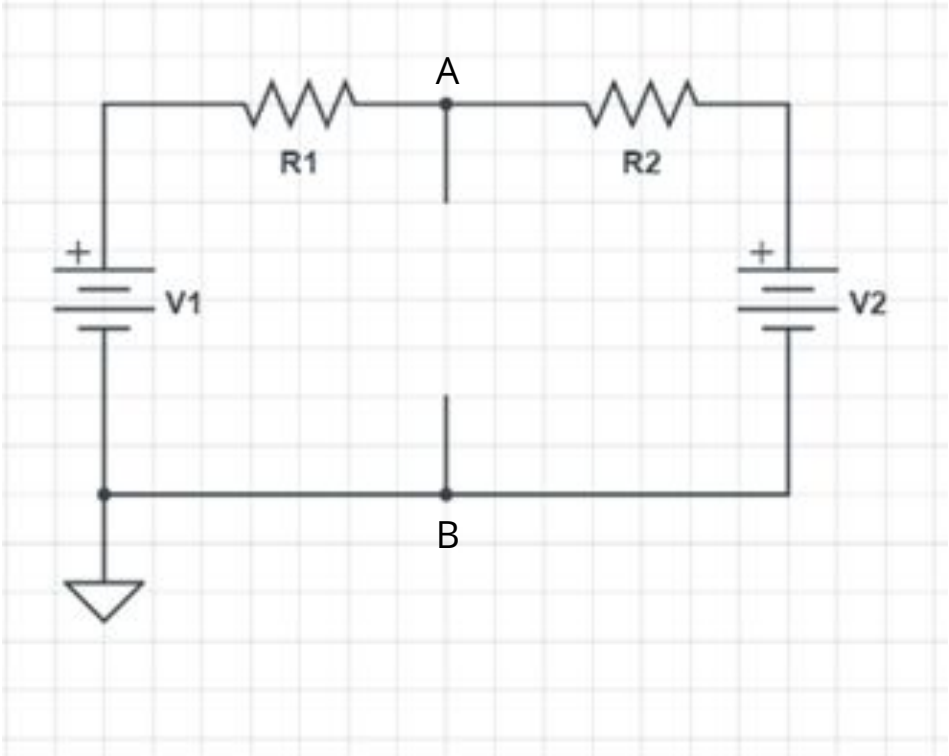


Finding the equivalent resistance, by removing the **'R_3'** resistor. Also, by removing the voltage sources (short circuiting).



$$R_{TH} = \frac{R_1 . R_2}{R_1 + R_2}$$

Finding equivalent voltage [without ' R_3 ' resistor]



By KVL,

$$V_1 - IR_1 - IR_2 - V_2 = 0$$

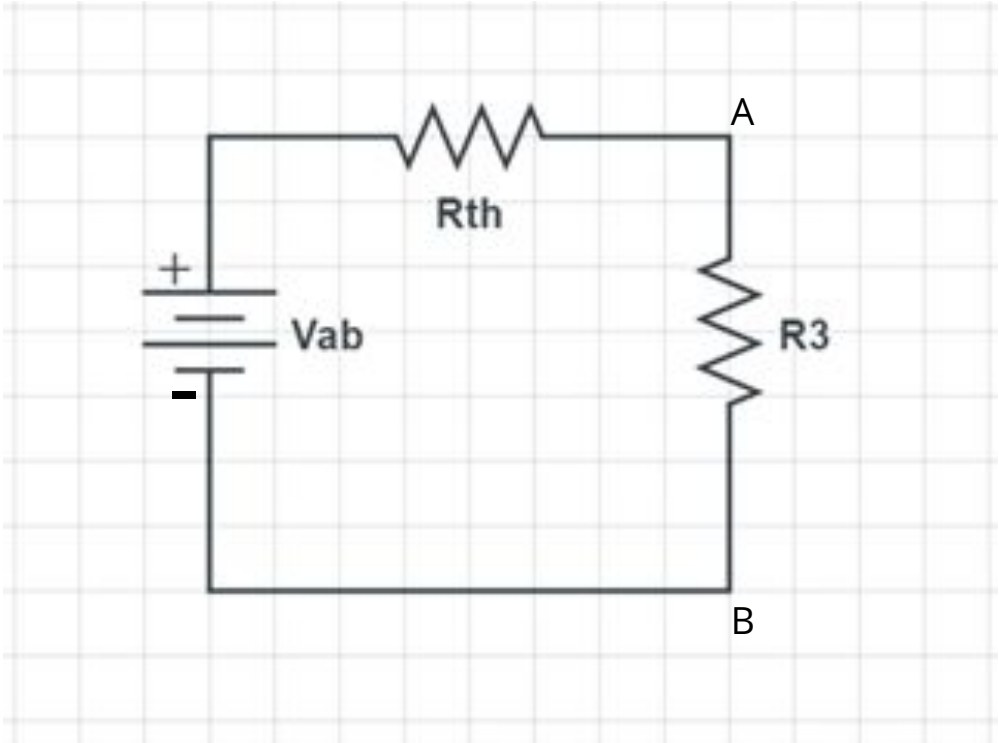
$$I_1 = \frac{V_1 - V_2}{R_1 + R_2} \ ,$$

I $\longrightarrow$ current flowing in the circuit.

Let V_{AB} is the equivalent voltage across A&B,

$$V_{AB} = V_1 - IR_1 = V_2 + IR_2$$

Simplified version of circuit [as per Thevenin's rule]



By applying KVL,

$$V_{AB} - I_1' R_{TH} - I_1' R_3 = 0$$

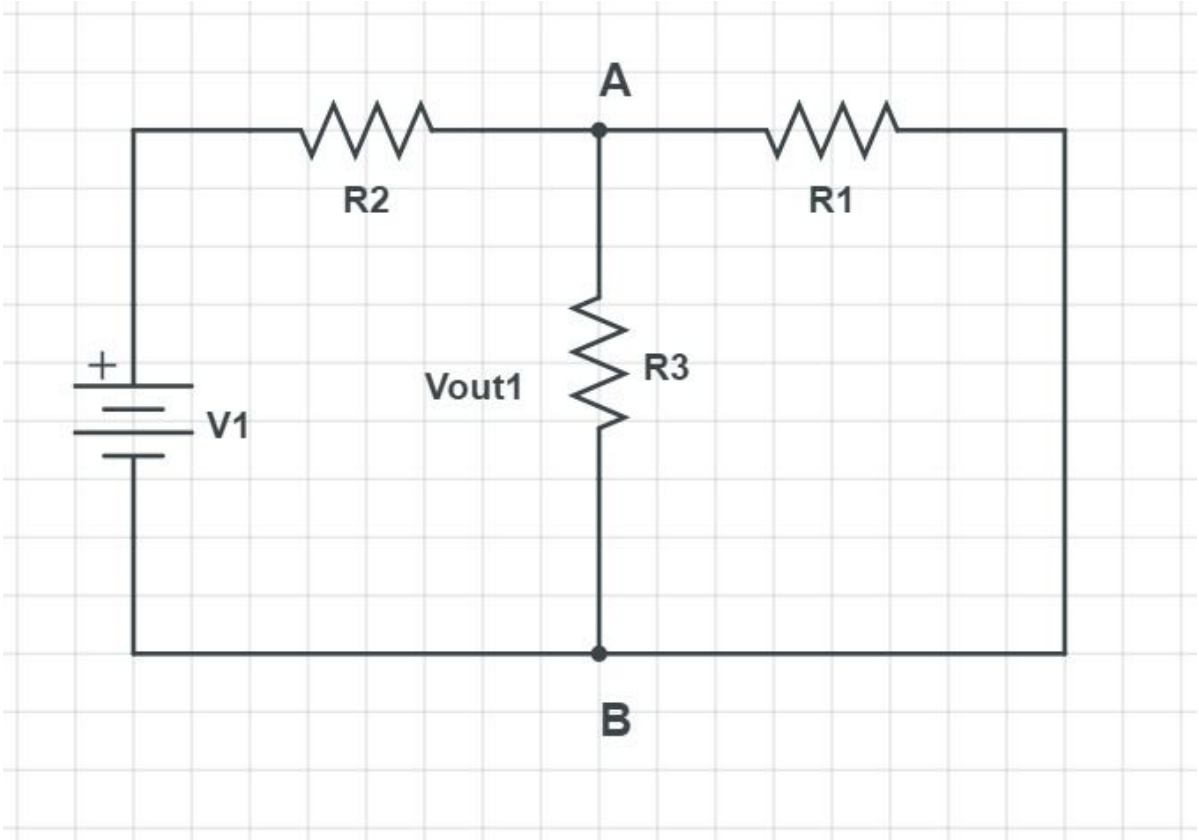
$$I_1' = \frac{V_{AB}}{R_{TH} + R_3}$$

by ohm's law,

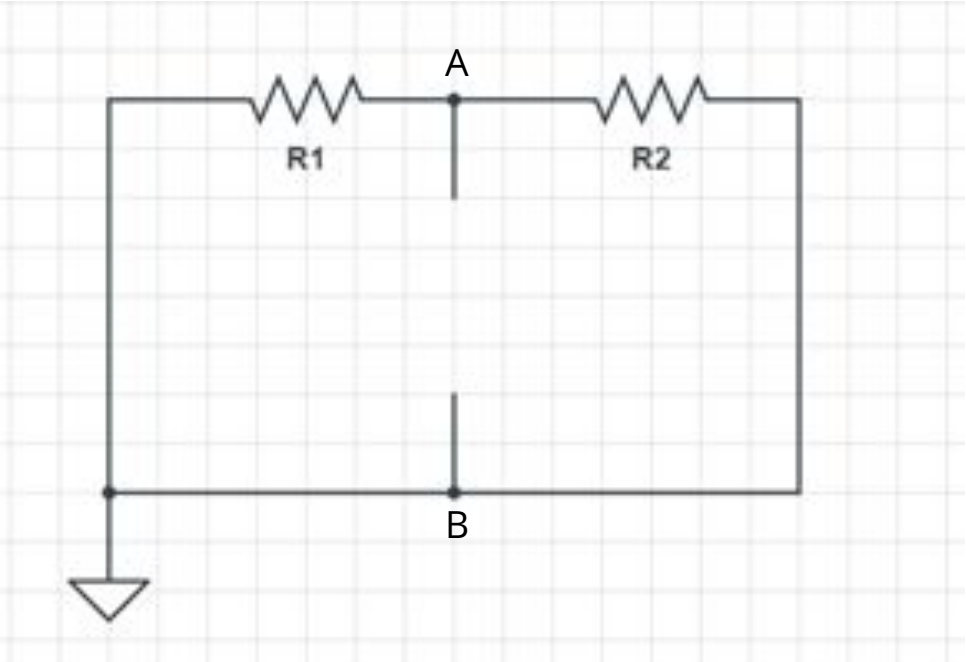
$$V_{out} = I_1' \times R_3$$

where V_{out} is voltage across R_3

Case 2 (with source voltage V_1 and where V_2 is the short circuited)



Finding the equivalent resistance across A&B by removing **'R_3** ' resistor, [also by short circuiting source voltage]



$$R_{TH} = \frac{R_1 . R_2}{R_1 + R_2}$$

finding equivalent voltage across 'A' & 'B'

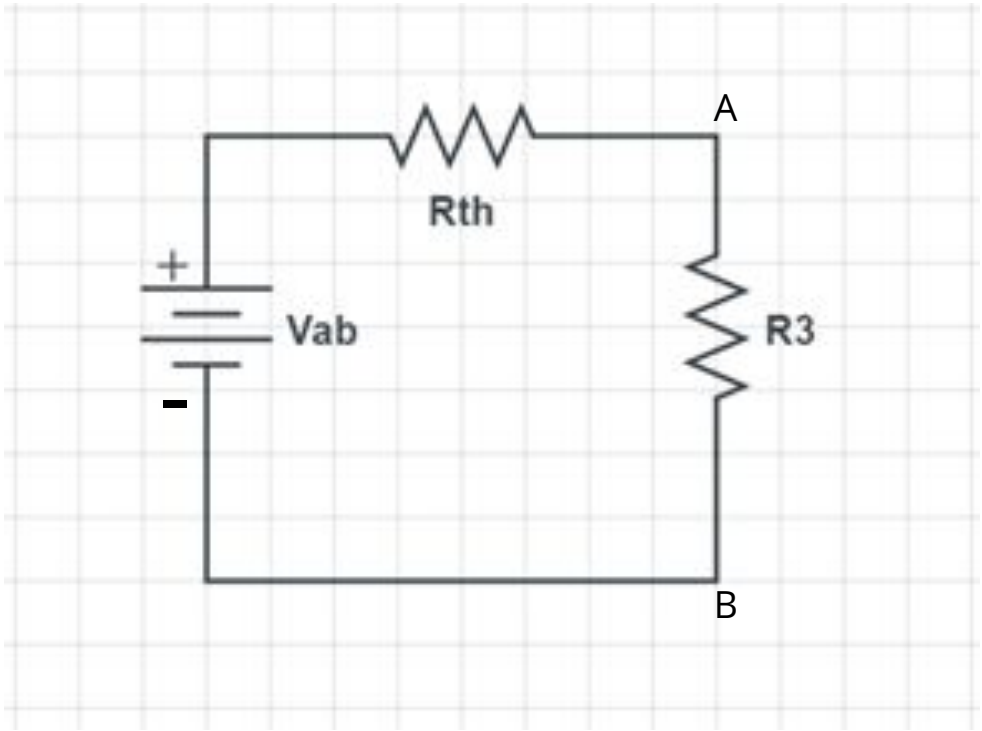
by KVL,

$$V_1 - I_2R_1 - I_2R_2 = 0$$

$$I_2 = \frac{V_1}{R_1 + R_2}$$

$V_{AB} = V_1 - I_2R_1$ where V_{AB} is voltage across A&B

Simplified version of the circuit, [using Thevenin's theorem]



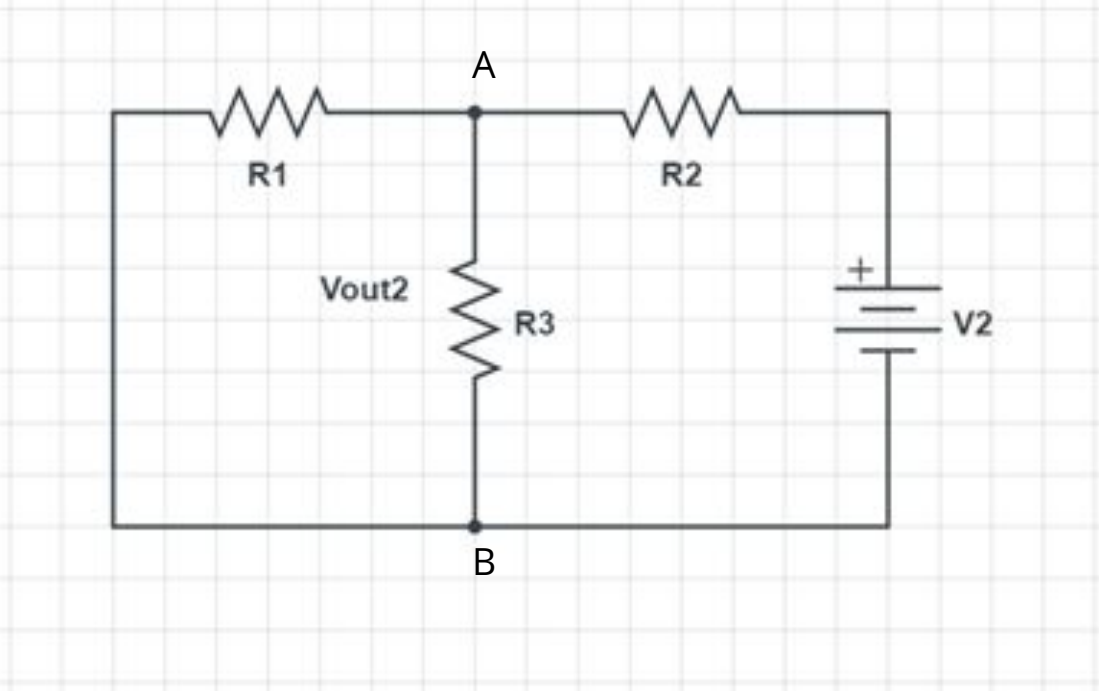
by KVL,

$$V_{AB} - I_2' R_{TH} - I_2' R_3 = 0$$

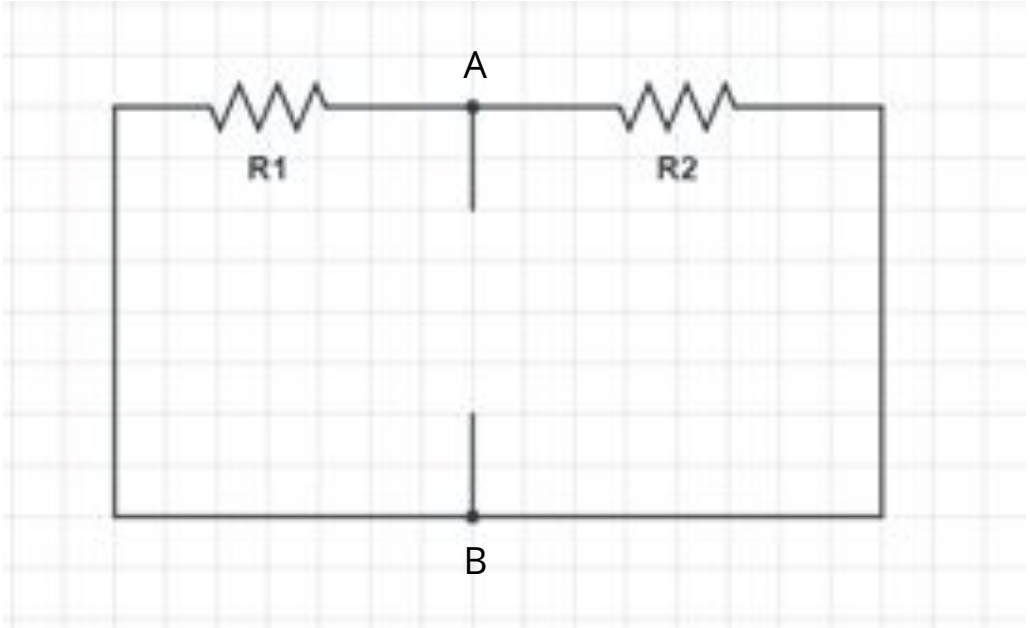
$$I_2' = \frac{V_{AB}}{R_{TH} + R_3}$$

hence, $V_{out\,1} = I_2' R_3 \longrightarrow$ by ohm's law

Case 3 (with source voltage $\mathbf{V_2}$, where $\mathbf{V_1}$ short circuited):

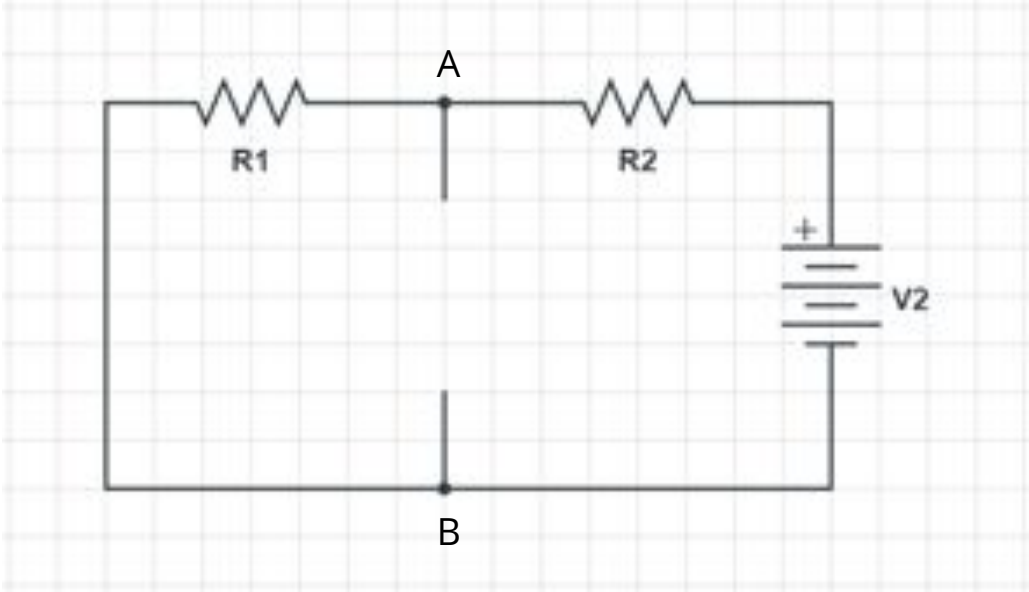


Finding the equivalent resistance across A&B by removing 'R_3' resistor (also by short circuiting source voltage)



$$R_{TH} = \frac{R_1 R_2}{R_1 + R_2}$$

Finding equivalent voltage across A&B



By KVL,

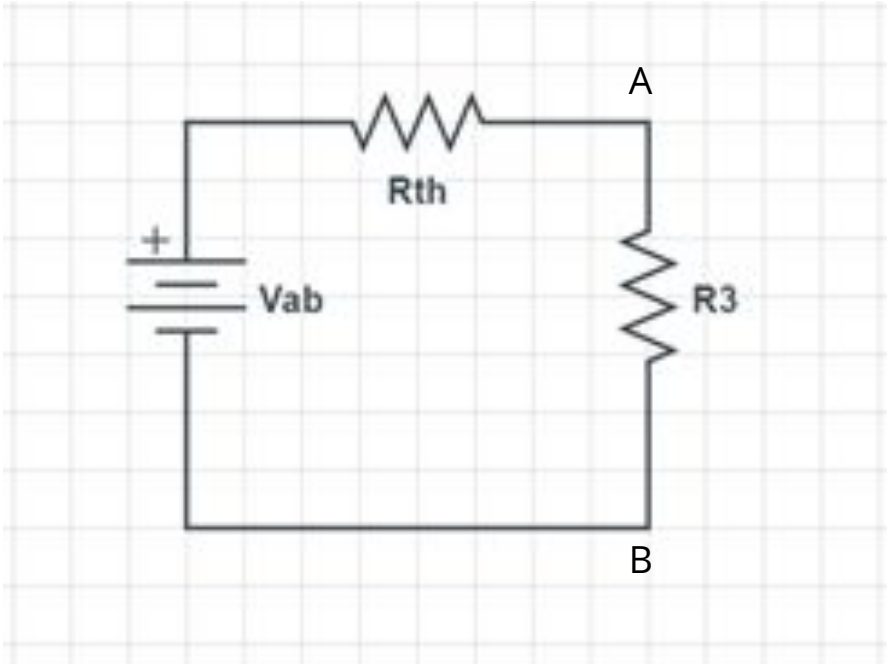
$$V_2 - I_3R_2 - I_3R_1 = 0$$

$$I_3 = \frac{V_2}{R_1 + R_2}$$

$$V_{AB} = V_2 - I_3R_2$$

where V_{AB} is voltage across A&B.

Simplified version of the circuit, (using Thevenin's theorem)



by KVL,

$$V_{AB} - I'_2 R_{TH} - I'_3 R_3 = 0$$

$$I'_3 = \frac{V_{AB}}{R_1 + R_2}$$

hence, $V_{out\,2} = I'_3 R_3$

Now, we can see that,

$$V_{out} = V_{out\,1} + V_{out\,2}$$

Hence, super-position theorem is proved.

also, $I_1' = I_2' + I_3'$

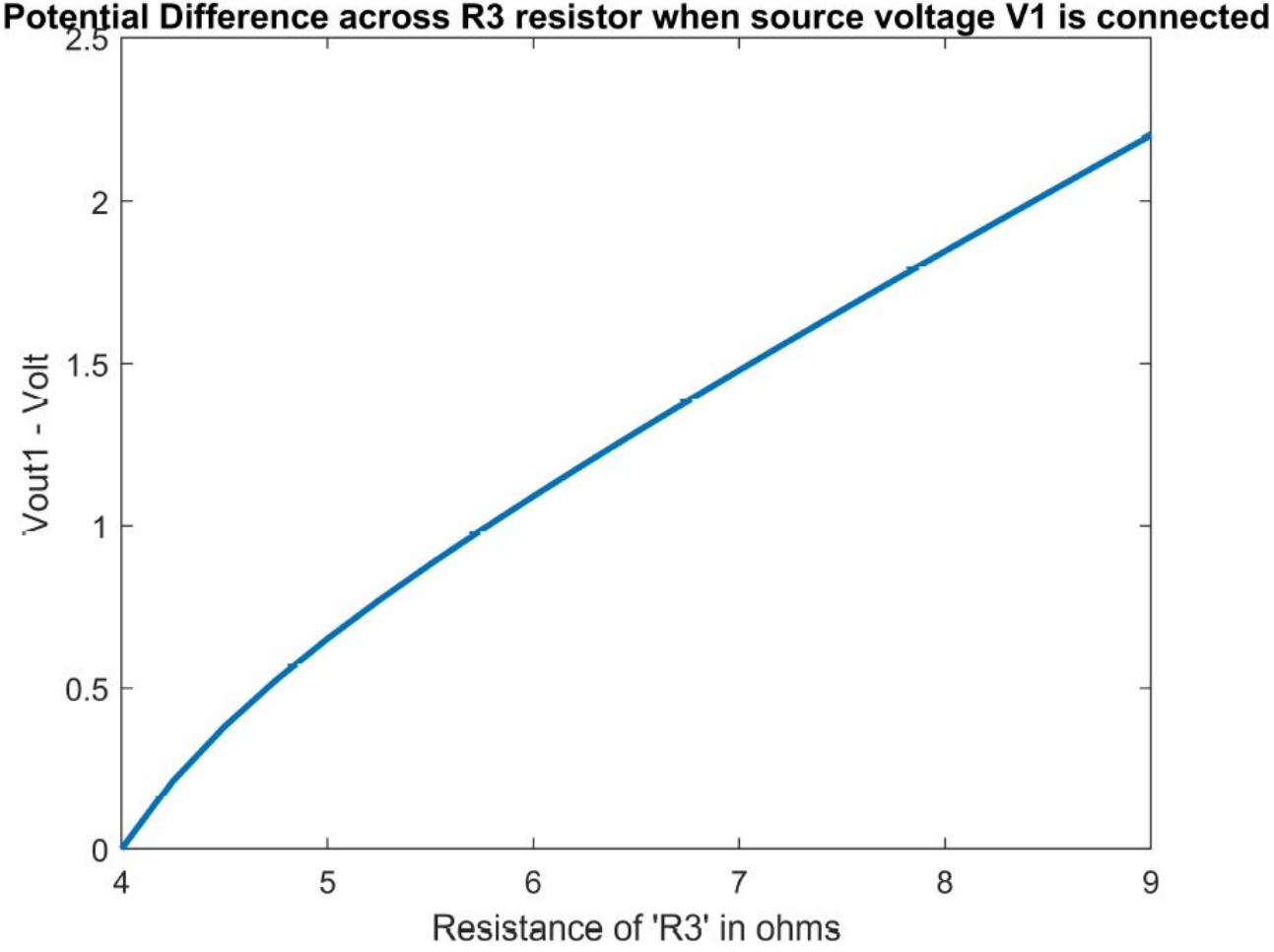
$I_1' \longrightarrow$ current flowing through R_3 when sourcevoltages V1 and V2 are there.

$I_2' \longrightarrow$ current flowing through R_3 when 'V_1' is there.

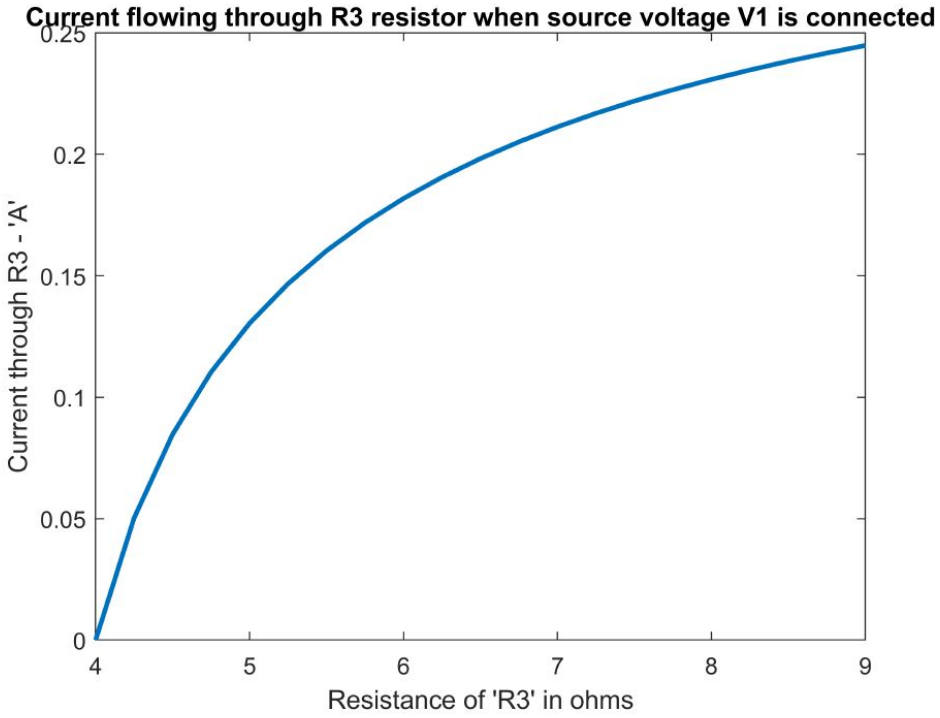
$I_3' \longrightarrow$ current flowing through R_3 when 'V_2' is there.

MATLAB code for computation

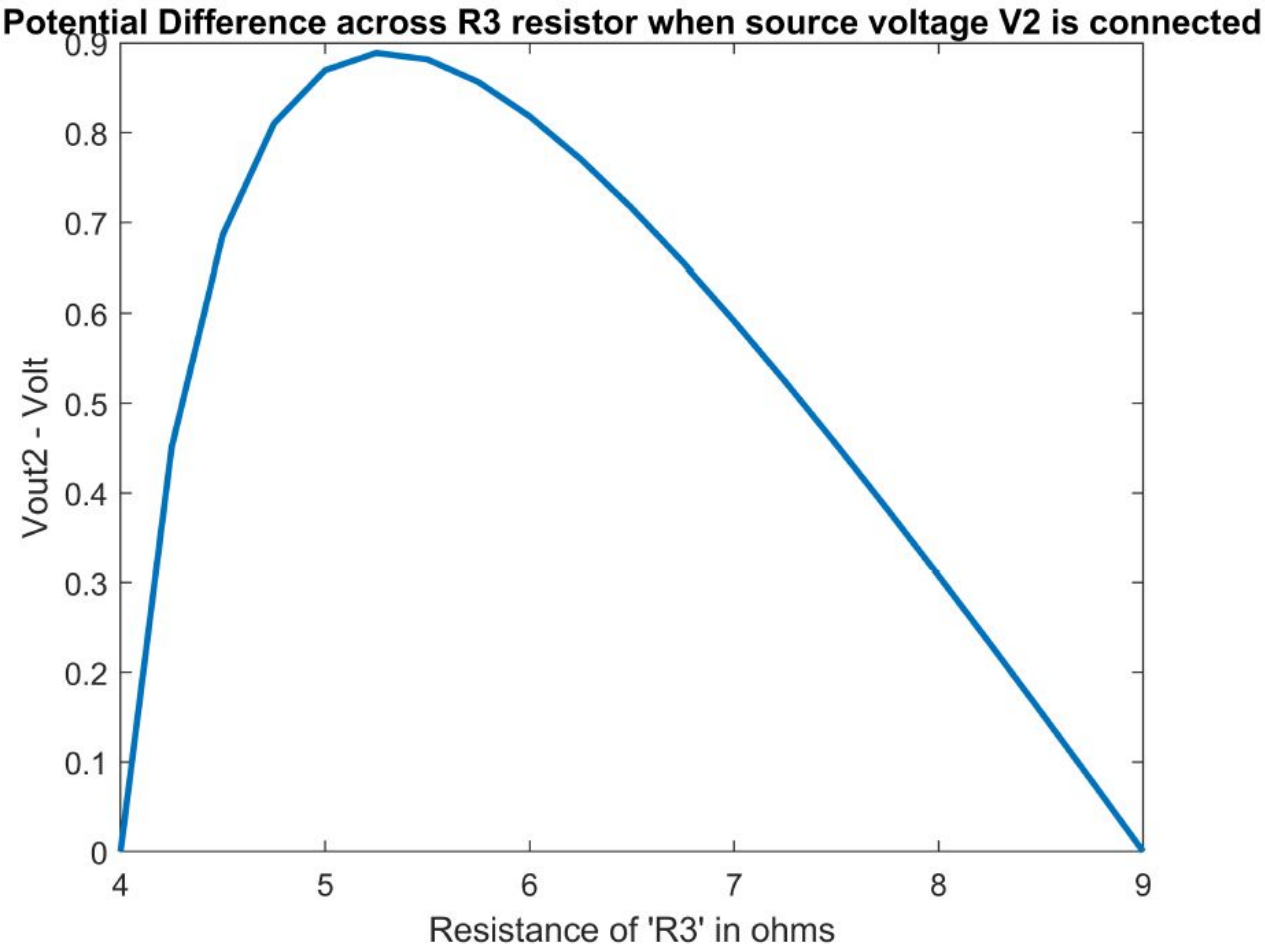
```
clc;
clear all;
close all;

% Resistance Values
R1 = 0:0.25:5;
R2 = 2:0.25:7;
R3 = 4:0.25:9;

% Source Voltages
V1 = 0:0.25:5;
V2 = 5:-0.25:0;

% With source voltage V1
R_TH = R1.*R2 ./ (R1 + R2);
I2 = (V1) ./ (R1 + R2);
V_ab_1 =  V1 - I2.*R1;
IR3_1 = V_ab_1 ./ (R3 + R_TH);
Vout1 = IR3_1 .* R3;
figure
plot(R3,Vout1,"LineWidth",2)
title("Potential Difference across R3 resistor when source voltage V1 is connected")
xlabel("Resistance of 'R3' in ohms")
ylabel("Vout1 - Volt")
```


Potential Difference across R3 resistor when source voltage V1 is connected
Vout1 - Volt
Resistance of 'R3' in ohms
0
0.5
1
1.5
2
2.5
4
5
6
7
8
9

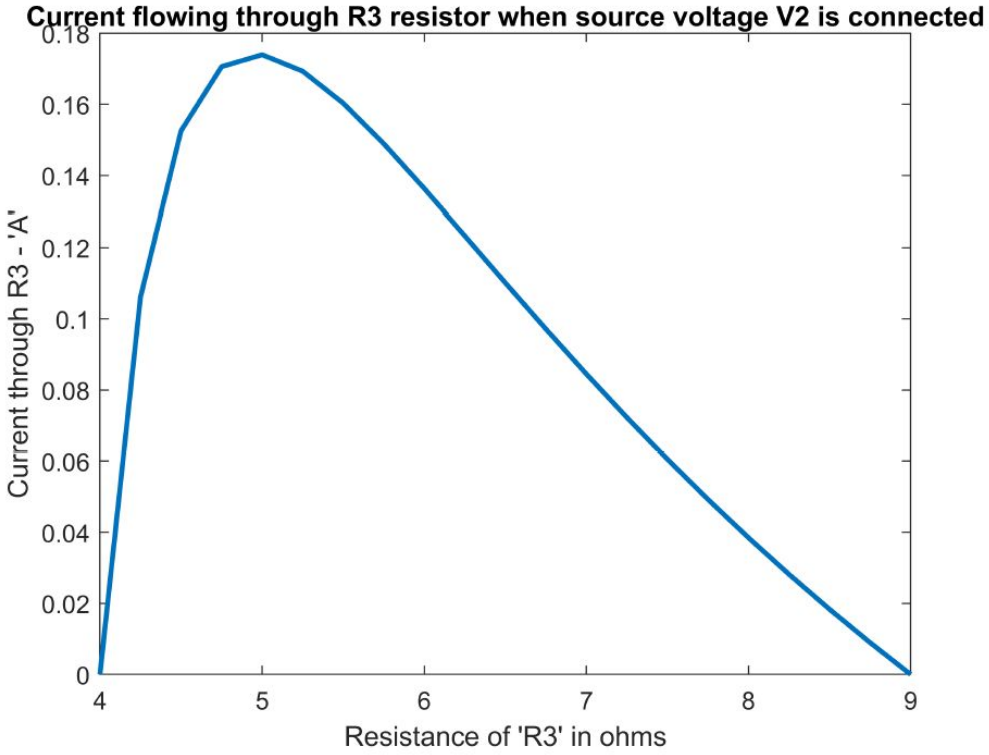
```
plot(R3,IR3_1,"LineWidth",2)
title("Current flowing through R3 resistor when source voltage V1 is connected")
xlabel("Resistance of 'R3' in ohms")
ylabel("Current through R3 - 'A'")
```



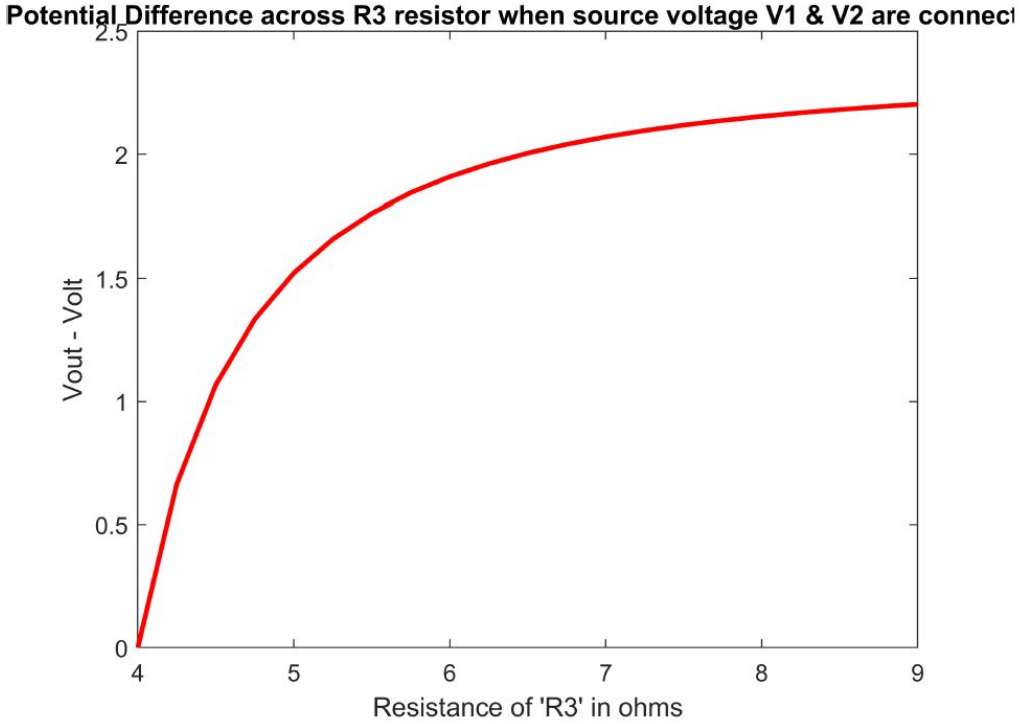
```
% With source voltage V2
R_TH = R1.*R2 ./ (R1 + R2);
I3 = (V2) ./ (R1 + R2);
V_ab_2 =  V2 - I3.*R2;
IR3_2 = V_ab_2 ./ (R3 + R_TH);
Vout2 = IR3_2 .* R3;
figure
plot(R3,Vout2,"LineWidth",2)
title("Potential Difference across R3 resistor when source voltage V2 is connected")
xlabel("Resistance of 'R3' in ohms")
ylabel("Vout2 - Volt")
```


Potential Difference across R3 resistor when source voltage V2 is connected
Vout2 - Volt
0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
4
5
6
7
8
9
Resistance of 'R3' in ohms

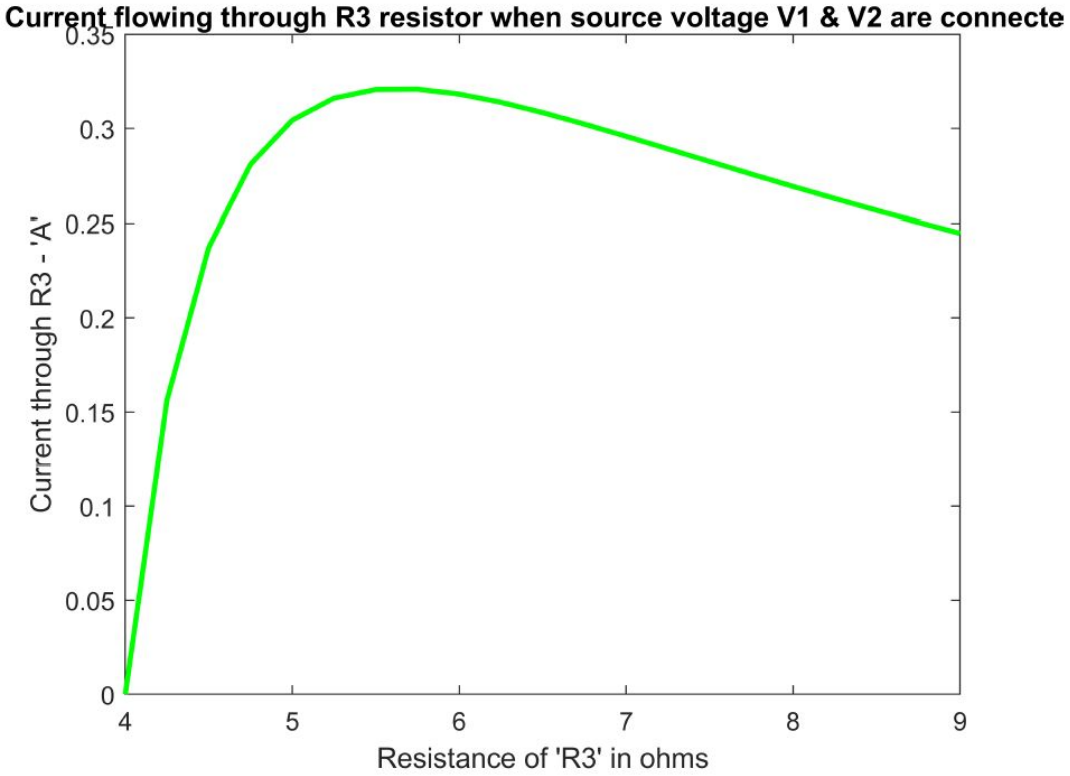
```
plot(R3,IR3_2,"LineWidth",2)
title("Current flowing through R3 resistor when source voltage V2 is connected")
xlabel("Resistance of 'R3' in ohms")
ylabel("Current through R3 - 'A'")
```



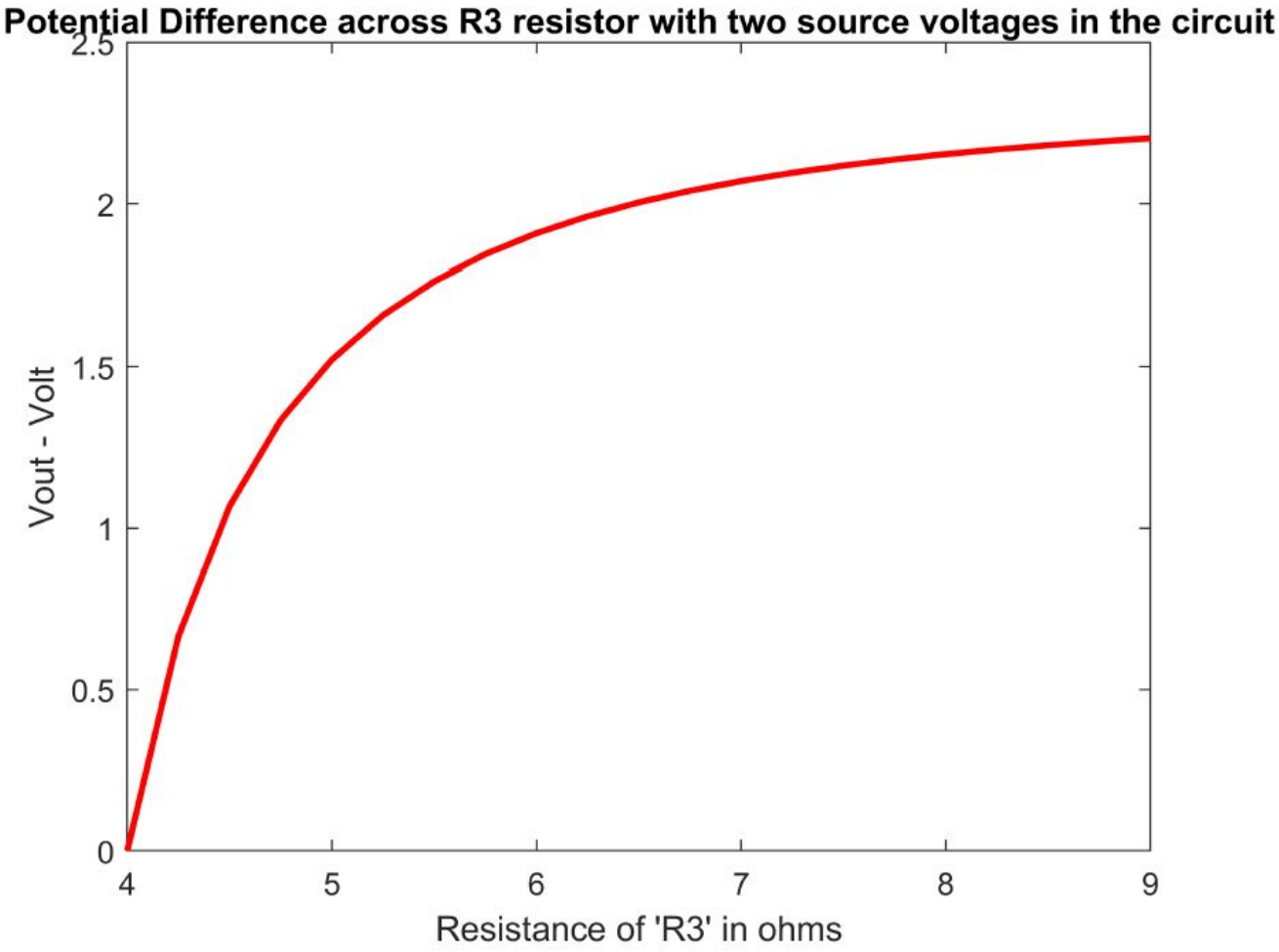
```
Vout = Vout1 + Vout2;
IR3 = IR3_1 + IR3_2;
plot(R3,Vout,"LineWidth",2,"Color",'r')
title("Potential Difference across R3 resistor when source voltage V1 & V2 are connected")
xlabel("Resistance of 'R3' in ohms")
ylabel("Vout - Volt")
```



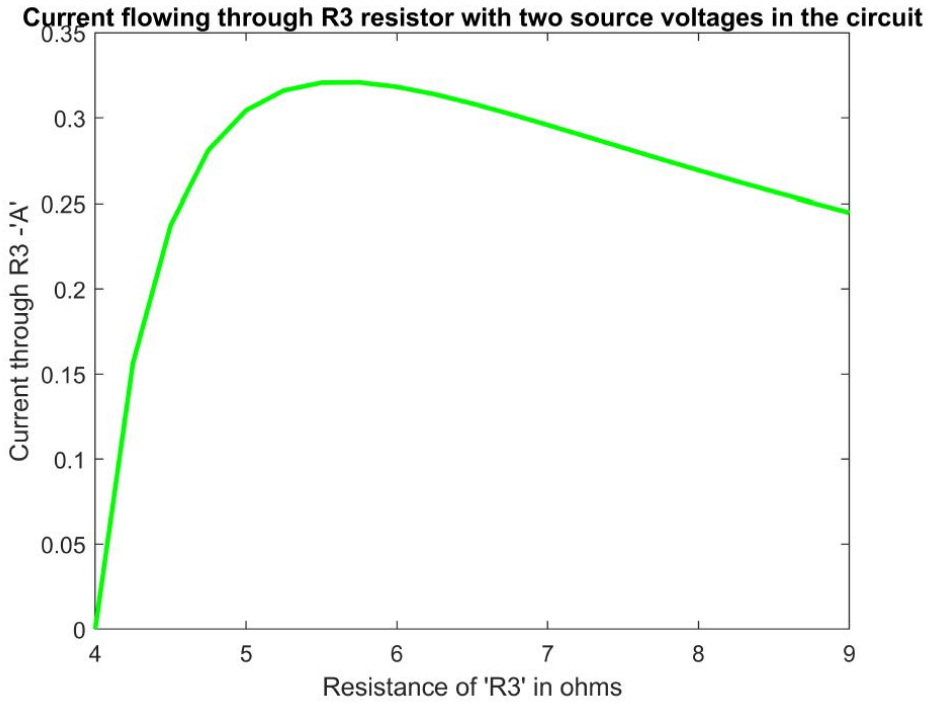
```
plot(R3,IR3,"LineWidth",2,"Color",'green')
title("Current flowing through R3 resistor when source voltage V1 & V2 are connected")
xlabel("Resistance of 'R3' in ohms")
ylabel("Current through R3 - 'A'")
```



```
% With source voltageS V1 and V2
R_TH = R1.*R2 ./ (R1 + R2);
I1 = (V1 - V2) ./ (R1 + R2);
V_ab =  V1 - I1.*R1;
IR3 = V_ab ./ (R3 +R_TH);
Vout = IR3 .* R3;
plot(R3,Vout,"LineWidth",2,"Color",'r')
title("Potential Difference across R3 resistor with two source voltages in the circuit")
xlabel("Resistance of 'R3' in ohms")
ylabel("Vout - Volt")
```


Potential Difference across R3 resistor with two source voltages in the circuit
Vout - Volt
Resistance of 'R3' in ohms
0
0.5
1
1.5
2
2.5
4
5
6
7
8
9

```
plot(R3,IR3,"LineWidth",2,"Color",'green')
title("Current flowing through R3 resistor with two source voltages in the circuit")
xlabel("Resistance of 'R3' in ohms")
ylabel("Current through R3 -'A'")
```



INFERENCE

We can observe that the sum of individual output voltages is equal to the output voltage when both source voltages (V_1 and V_2) are connected in the circuit.

- For $V_{in} = V_1$ and V_2, we get output voltage across resistor $Vr_{\_out}$ and current flowing through the circuit is I_out.
- For $V_{in} = V_1$, we get output voltage across resistor $Vr_{\_out1}$ and current flowing through the circuit is $I_{\_out1}$.
- For $V_{in} = V_2$, we get output voltage across resistor as $Vr_{\_out2}$ and current flowing through the circuit is $I_{\_out2}$.

We observe that:

- $Vr_{\_out} = Vr_{\_out1} + Vr_{\_out2}$
- $I_{\_out} = I_{\_out1} + I_{\_out2}$

Hence, the superposition theorem is proved.

APPLICATION OF SUPERPOSITION IN RC CIRCUIT

Superposition theorem for differential equation:

Suppose y1(t) solves the differential equation, $\frac{dy}{dt} + f(t) = g1(t)$

Suppose y2(t) solves the differential equation, $\frac{dy}{dt} + f(t) = g2(t)$

Then y1 + y2 is a solution to $\frac{dy}{dt} + f(t) = g1(t) + g2(t)$

Proof:

$y = y1 + y2$

$y' = y1' + y2'$

$y1' + y2' + f(t) * [\ y1 + y2\ ] = g1(t) + g2(t)$

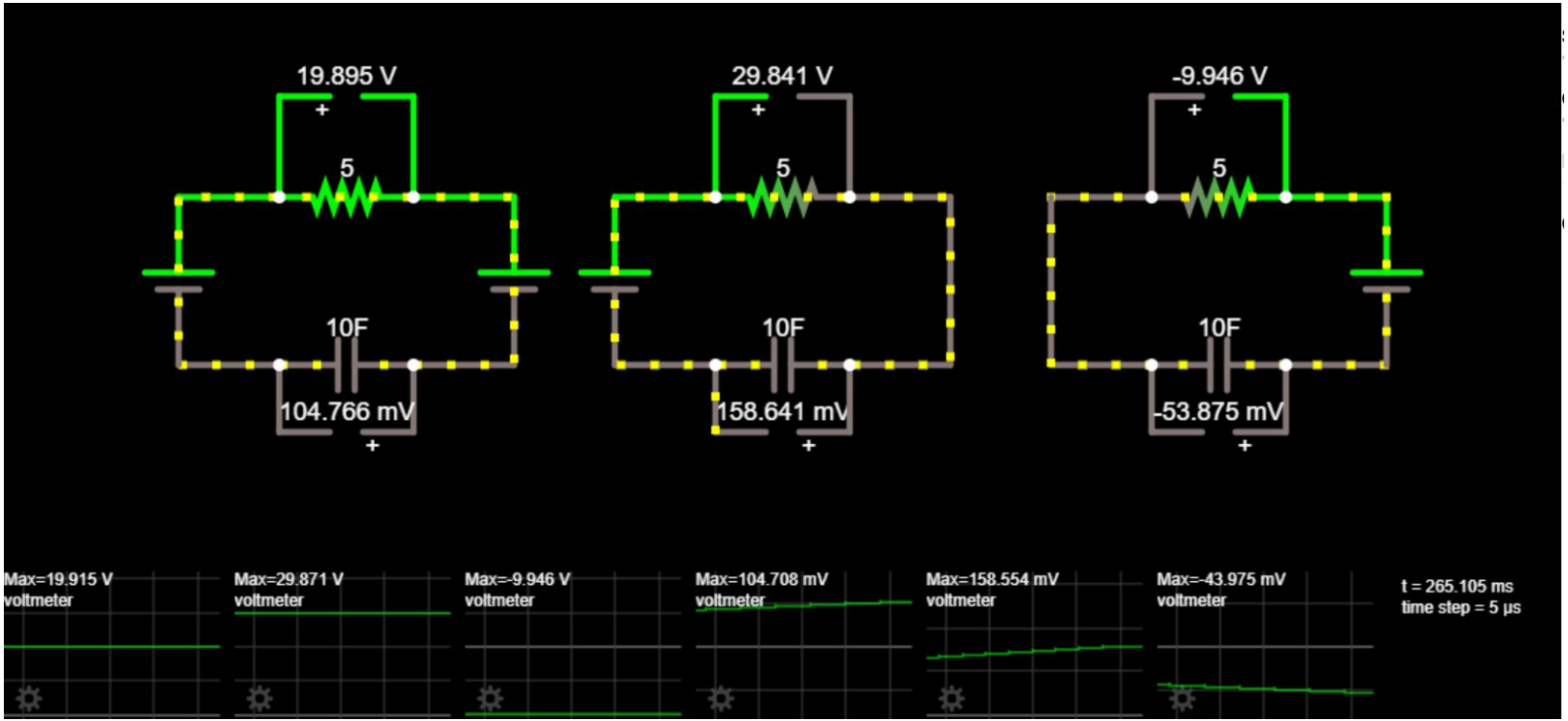
$[\ y1' + f(t) * y1\ ] + [\ y2' + f(t) * y2\ ] = g1(t) + g2(t)$

$g1(t) + g2(t) = g1(t) + g2(t)$

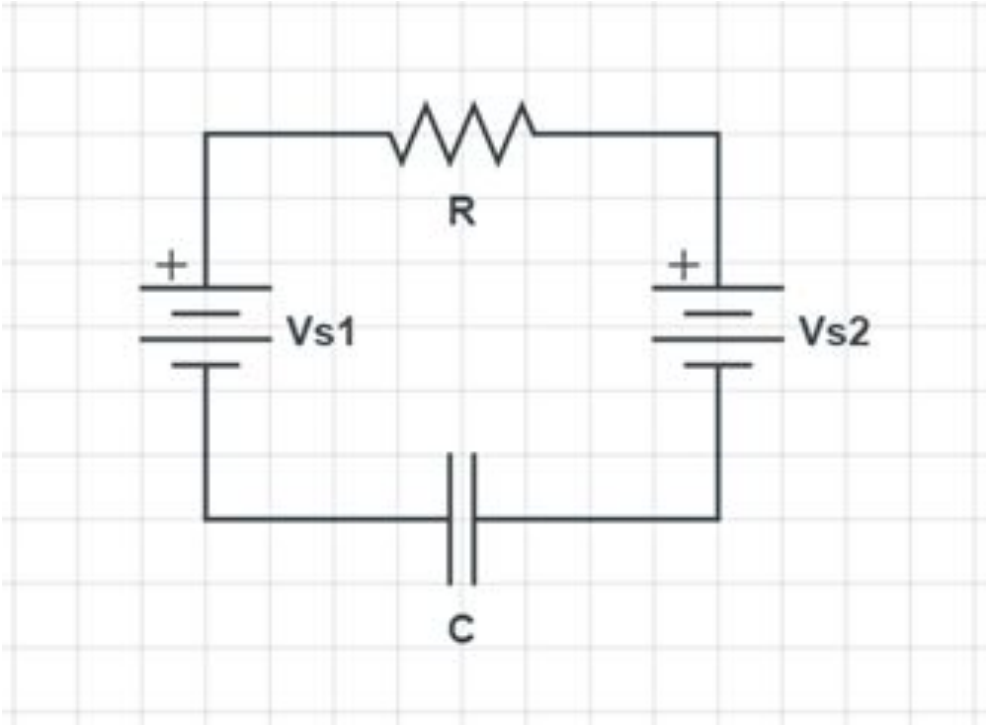
Hence Proved.

Circuit simulation - RC Circuit

Link: https://tinyurl.com/ybm6tyey



Proof of superposition theorem given that two source voltages are **Vs_1** and **Vs_2**



Let Vc be the voltage across the capacitor.

Let Vr be the voltage across the resistor.

Let V_{S1} be source voltage 1.

Let V_{S2} be source voltage 2.

Let R be the resistance of the resistor and C be the capacitance of the capacitor.

Let q(t) be charge on capacitor,

$q(t) = C \times Vc(t)$

$$\frac{dq(t)}{dt} = C \times Vc'(t)$$

$$Vc'(t) = \frac{I(t)}{C} \quad \text{---- (i)}$$

By Ohm's law, $I = \frac{V}{R}$

By, Kirchhoff's voltage law [Sum of voltage around any closed loop is zero],

$Vs1 - Vs2 - Vr - Vc(t) = 0$

$Vr = Vs1 - Vs2 - Vc(t)$ ---- (ii)

Use (ii) in (i),

$$Vc'(t) = \frac{Vs1 - Vs2 - Vc(t)}{R \, x \, C}$$

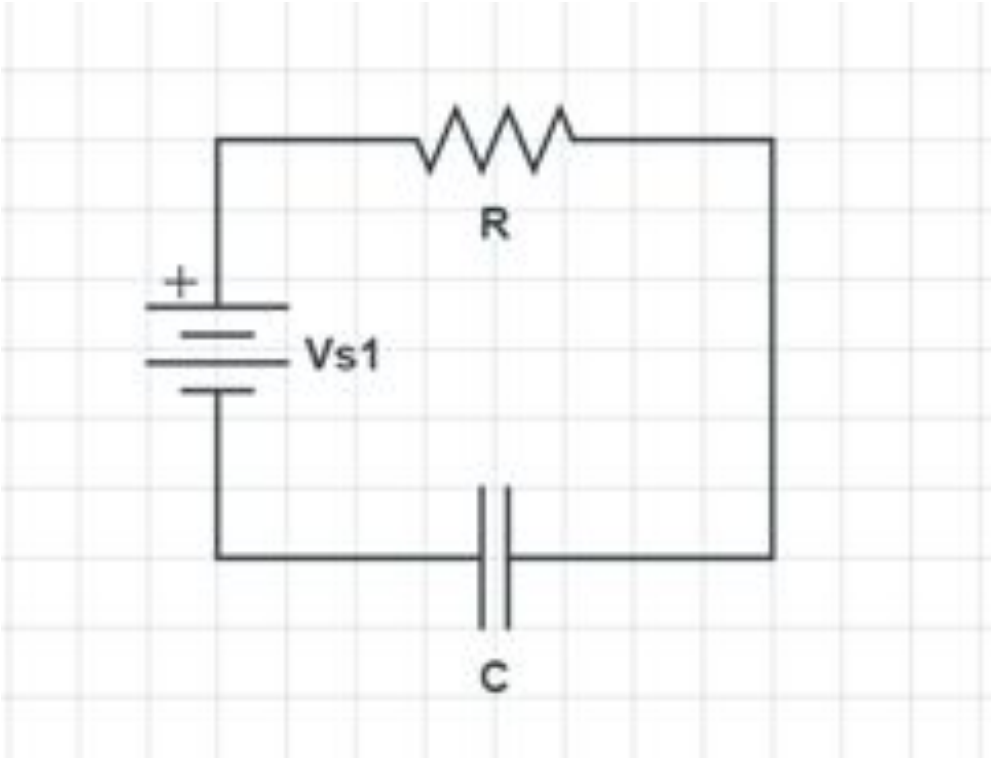
By Euler's method,

$$\mathbf{Vc(n+1) = Vc(n) + \triangle t \; x \; \frac{Vs1 - Vs2 - Vc(n)}{R \, x \, C}}$$

$$\mathbf{I = \frac{Vs1 - Vs2 - Vc(t)}{R}}$$

In this case, let voltage across the resistor, capacitor be Vr_out and Vc_out. Let the total current flowing in the circuit be I_out.

With source voltage $\mathbf{V_{s1}}$



By, Kirchhoff's voltage law [Sum of voltage around any closed loop is zero],

$Vs1 - Vr - Vc(t) = 0$

$Vr = Vs1 - Vc(t)$ → (ii)

Use (ii) in (i),

$$Vc'(t) = \frac{Vs1 - Vc(t)}{R\,x\,C}$$

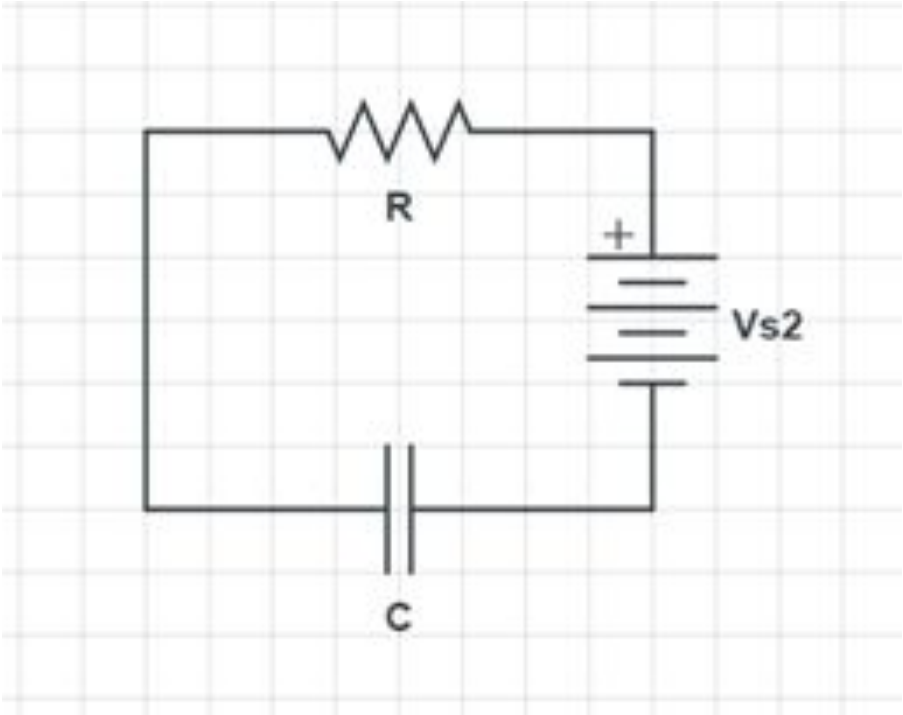
By Euler's method,

$$\mathbf{Vc(n+1) = Vc(n) + \triangle t\ x\ \frac{Vs1 - Vc(n)}{R\,x\,C}}$$

$$\mathbf{I1 = \frac{Vs1 - Vc(t)}{R}}$$

In this case, let voltage across the resistor, capacitor be $\mathbf{Vr_{\_out1}}$ and $\mathbf{Vc_{\_out1}}$. Let the total current flowing in the circuit be $\mathbf{I_1}$.

With source voltage $\mathbf{V_{s2}}$,



By, Kirchhoff's voltage law (Sum of voltage around any closed loop is zero)

$-Vs2 - Vr - Vc(t) = 0$

$Vr = -Vs2 - Vc(t)$ → (ii)

Use (ii) in (i),

$$Vc'(t) = \frac{-Vs2 - Vc(t)}{R \, x \, C}$$

By Euler's method,

$$\mathbf{Vc(n+1) = Vc(n) + \triangle t \; x \; \frac{-Vs2 - Vc(n)}{R \, x \, C}}$$

$$\mathbf{I2 = \frac{-Vs2 - Vc(t)}{R}}$$

In this case, let voltage across the resistor, capacitor be Vr_out2 and Vc_out2. Let the total current flowing in the circuit be I2.

By super-position theorem,

$Vc\_out = Vc\_out1 + Vc\_out2$

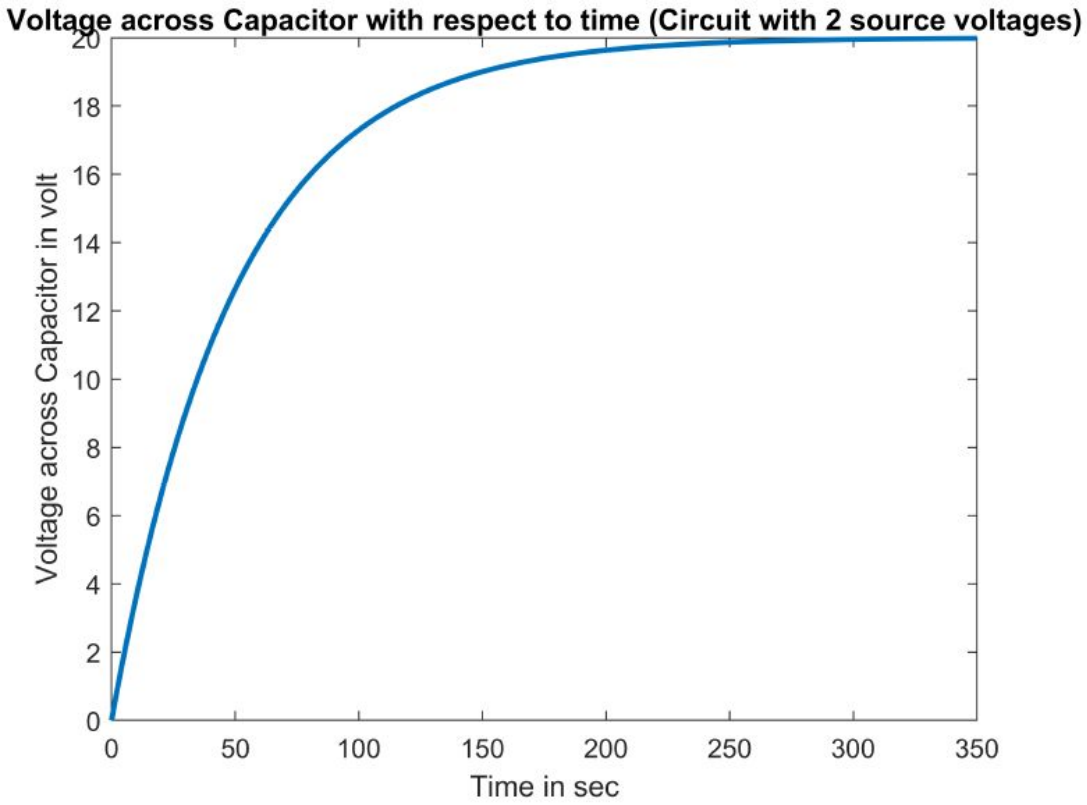
$Vr\_out = Vr\_out1 + Vr\_out2$

$I\_out = I1 + I2$

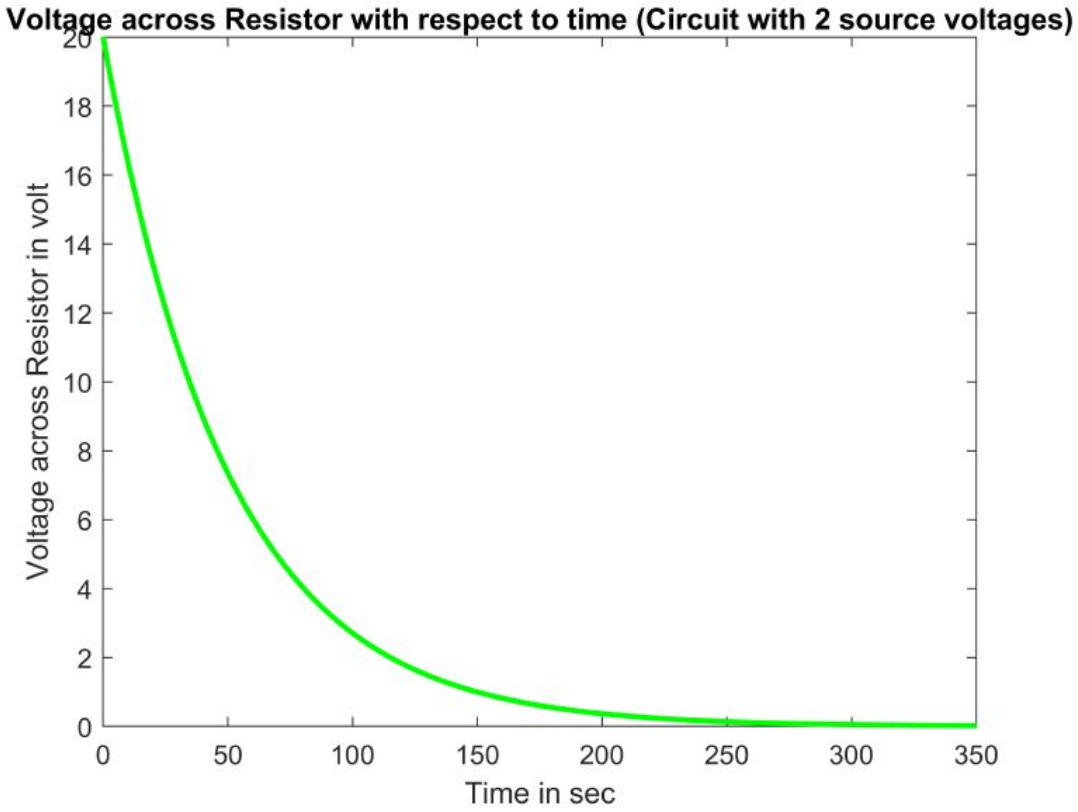
MATLAB code for computation

```
clc;
clear all;
close all;

R = 5;
C = 10;
time_constant = R * C;
% To get a smooth graph we here take 7 times the time constant
% Actually steady state is achieved at 5 times the time constant
T = 7 * time_constant;
dt = 0.01;
t = 0:dt:T;
Vs1 = 30;
Vs2 = 10;
Vc(1) = 0;

for n = 1:(length(t)-1)
Vc(n+1) = Vc(n) + dt*((Vs1 - Vs2 - Vc(n))*(1/(R*C)));
end
Vr = Vs1 - Vs2 - Vc;
I = (Vs1 - Vs2 - Vc) / R;
```

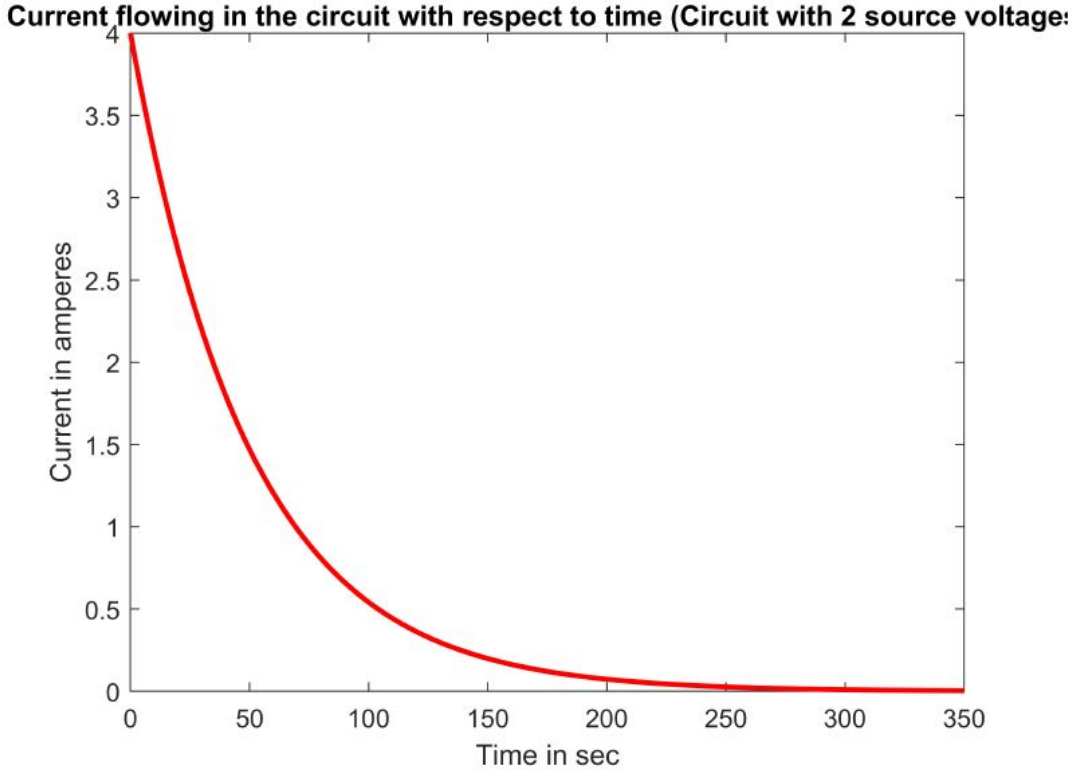
```
% Plotting the graph
plot(t,Vc,"LineWidth",2)
title("Voltage across Capacitor with respect to time (Circuit with 2 source voltages)")
xlabel("Time in sec")
ylabel("Voltage across Capacitor in volt")
```



```
plot(t,Vr,"LineWidth",2,"Color",'green')
title("Voltage across Resistor with respect to time (Circuit with 2 source voltages)")
xlabel("Time in sec")
ylabel("Voltage across Resistor in volt")
```

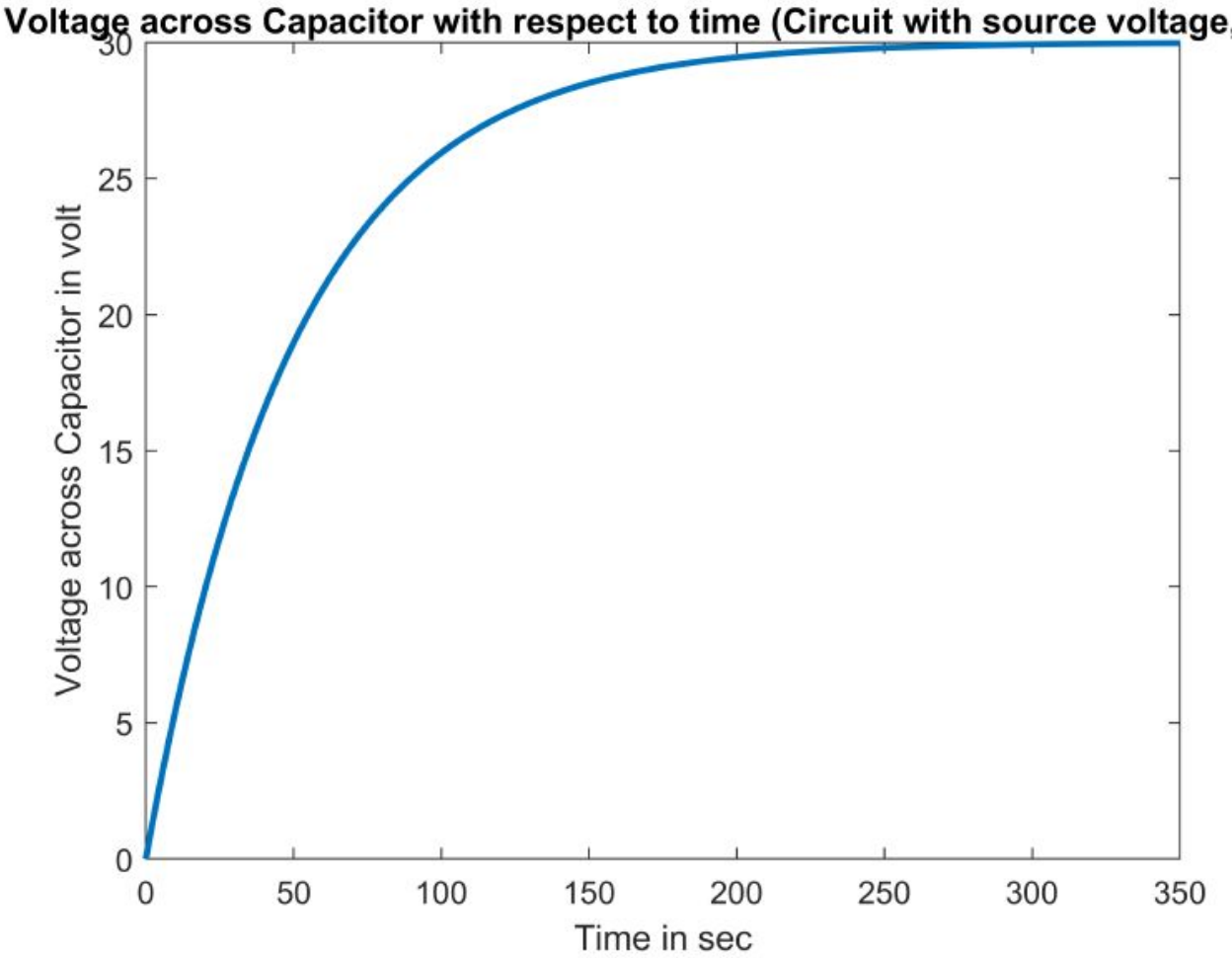


```
plot(t,I,"LineWidth",2,"Color",'r')
title("Current flowing in the circuit with respect to time (Circuit with 2 source voltages)")
xlabel("Time in sec")
ylabel("Current in amperes")
```

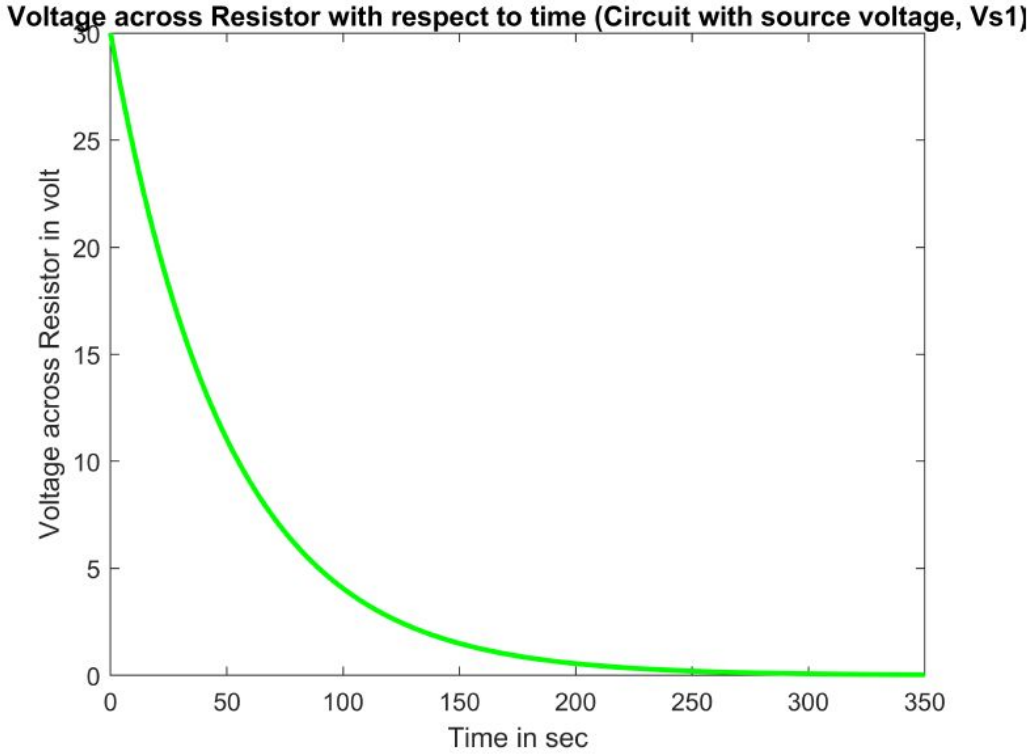


When one source voltage (Vs1) is alone connected

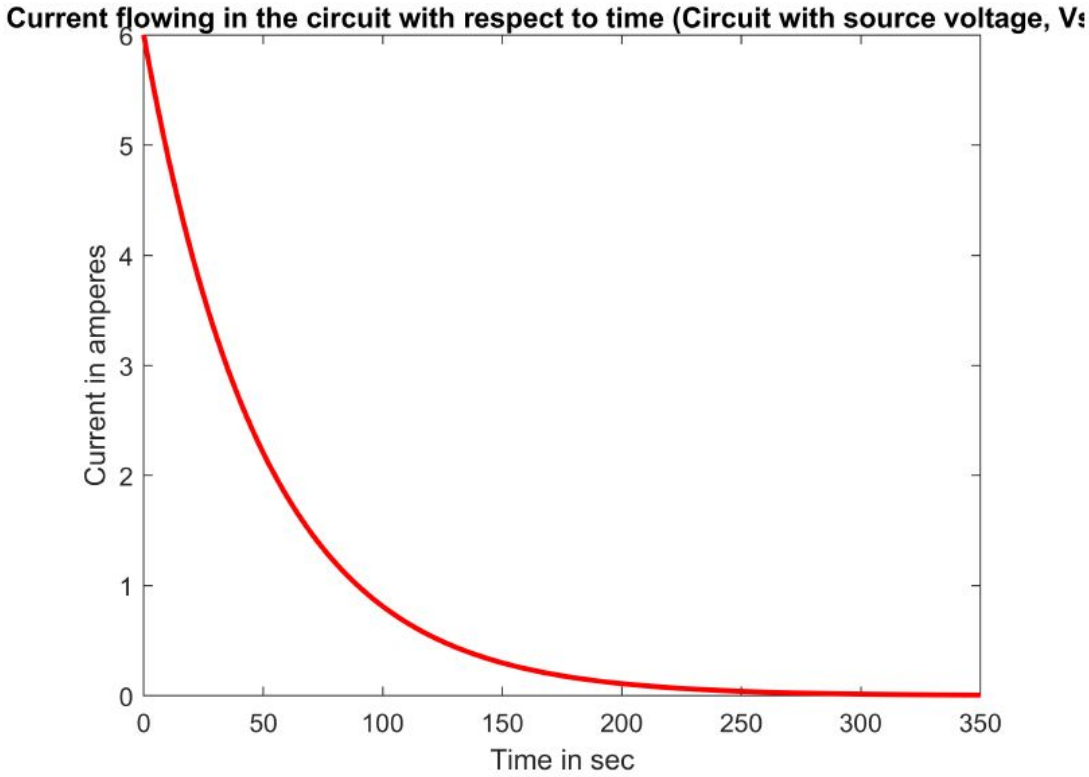
```
Vc_out1(1) = 0;
for i = 1:(length(t)-1)
    Vc_out1(i+1) = Vc_out1(i) + dt*((Vs1 - Vc_out1(i))*(1/(R*C)));
end
Vr_out1 = Vs1 - Vc_out1;
I1 = (Vs1 - Vc_out1) / R;

% Plotting the graph
plot(t,Vc_out1,"LineWidth",2)
title("Voltage across Capacitor with respect to time (Circuit with source voltage, Vs1)")
xlabel("Time in sec")
ylabel("Voltage across Capacitor in volt")
```


Voltage across Capacitor with respect to time (Circuit with source voltage, Vs1
Voltage across Capacitor in volt
Time in sec
0
5
10
15
20
25
30
0
50
100
150
200
250
300
350

```
plot(t,Vr_out1,"LineWidth",2,"Color",'green')
title("Voltage across Resistor with respect to time (Circuit with source voltage, Vs1)")
xlabel("Time in sec")
ylabel("Voltage across Resistor in volt")
```

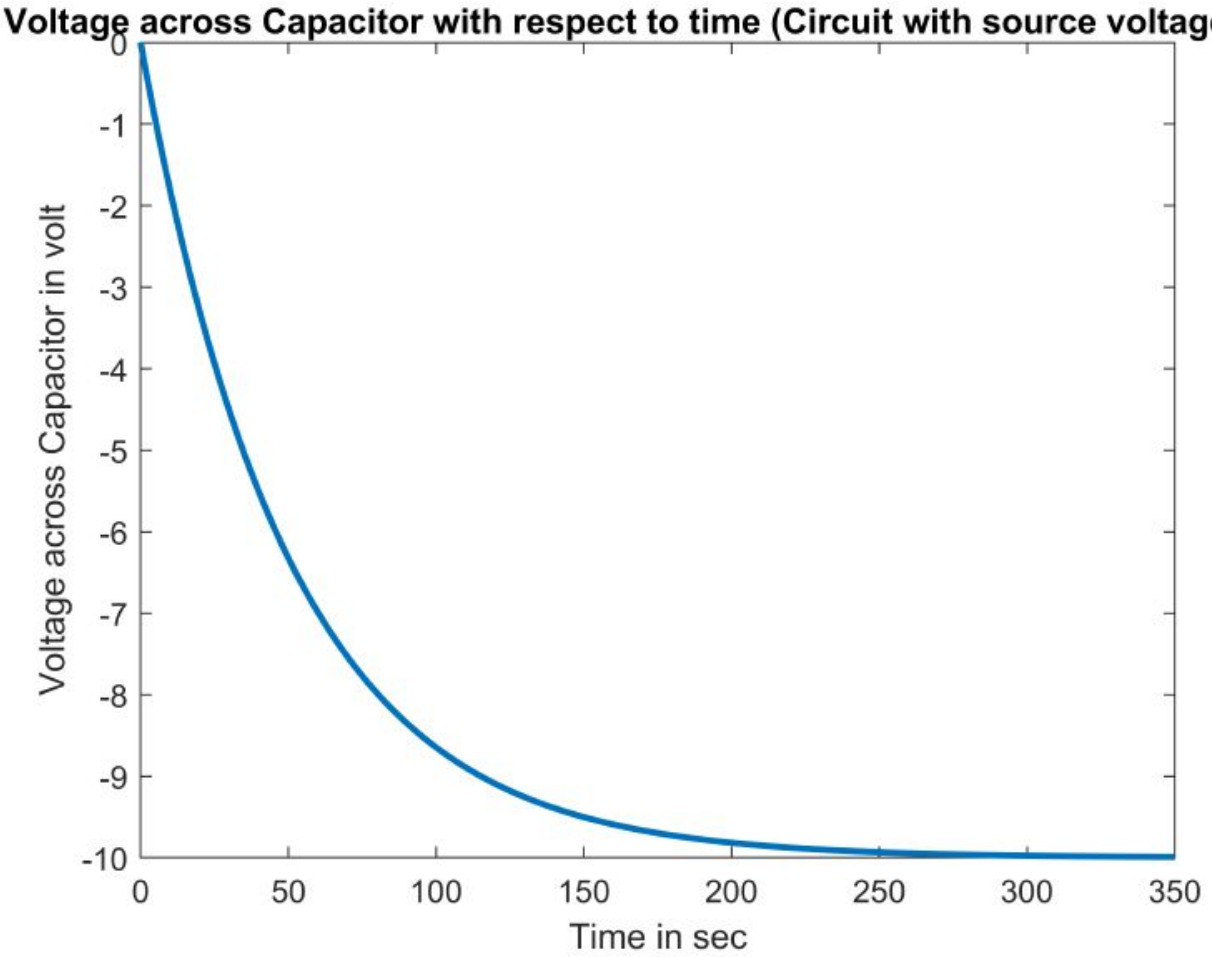


```
plot(t,I1,"LineWidth",2,"Color",'r')
title("Current flowing in the circuit with respect to time (Circuit with source voltage, Vs1)")
xlabel("Time in sec")
ylabel("Current in amperes")
```

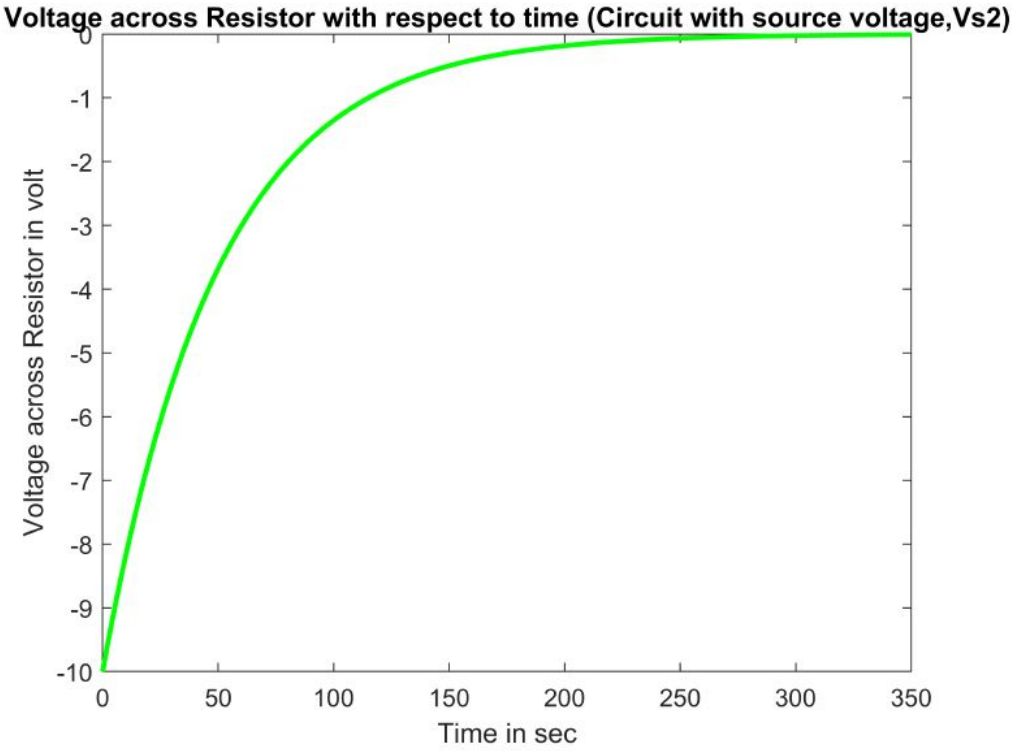


When one source voltage (Vs2) is alone connected

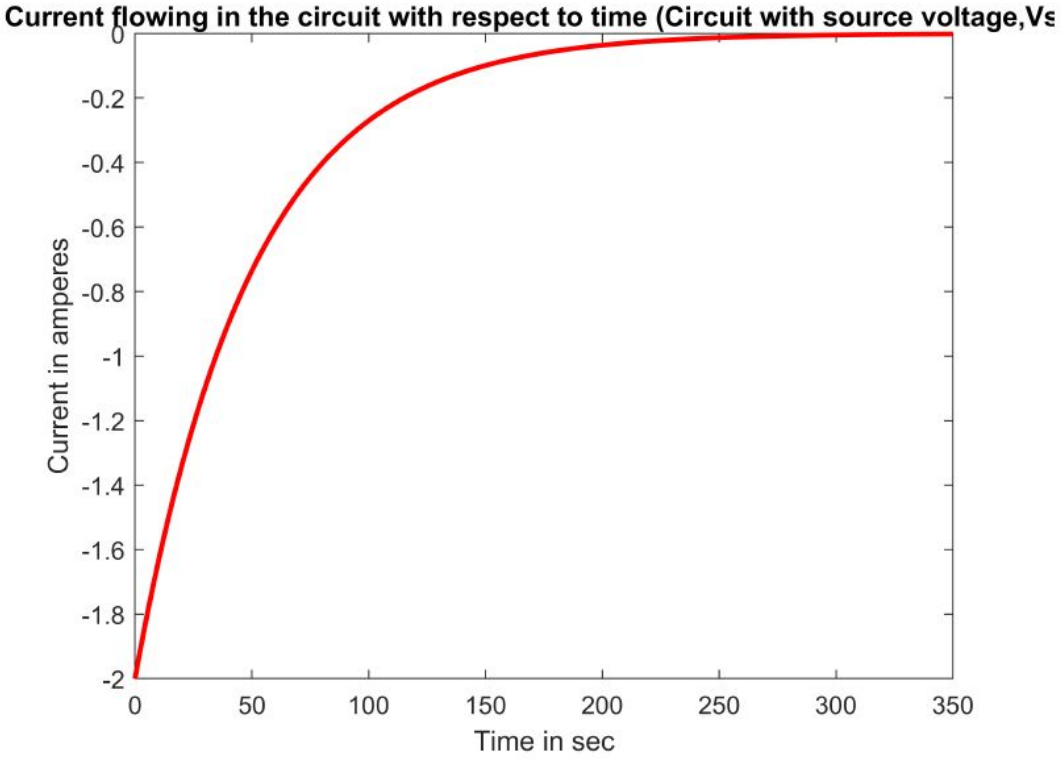
```
Vc_out2(1) = 0;
for j = 1:(length(t)-1)
    Vc_out2(j+1) = Vc_out2(j) + dt*((-Vs2 - Vc_out2(j))*(1/(R*C)));
end
Vr_out2 = -Vs2 - Vc_out2;
I2 = (-Vs2 - Vc_out2) / R;

% Plotting the graph
plot(t,Vc_out2,"LineWidth",2)
title("Voltage across Capacitor with respect to time (Circuit with source voltage,Vs2)")
xlabel("Time in sec")
ylabel("Voltage across Capacitor in volt")
```


Voltage across Capacitor with respect to time (Circuit with source voltage,Vs2
Voltage across Capacitor in volt
0
-1
-2
-3
-4
-5
-6
-7
-8
-9
-10
0
50
100
150
200
250
300
350
Time in sec

```
plot(t,Vr_out2,"LineWidth",2,"Color",'green')
title("Voltage across Resistor with respect to time (Circuit with source voltage,Vs2)")
xlabel("Time in sec")
ylabel("Voltage across Resistor in volt")
```



```
plot(t,I2,"LineWidth",2,"Color",'r')
title("Current flowing in the circuit with respect to time (Circuit with source voltage,Vs2)")
xlabel("Time in sec")
ylabel("Current in amperes")
```



Negative voltage in a circuit is voltage that is more negative in polarity than the ground of the circuit.

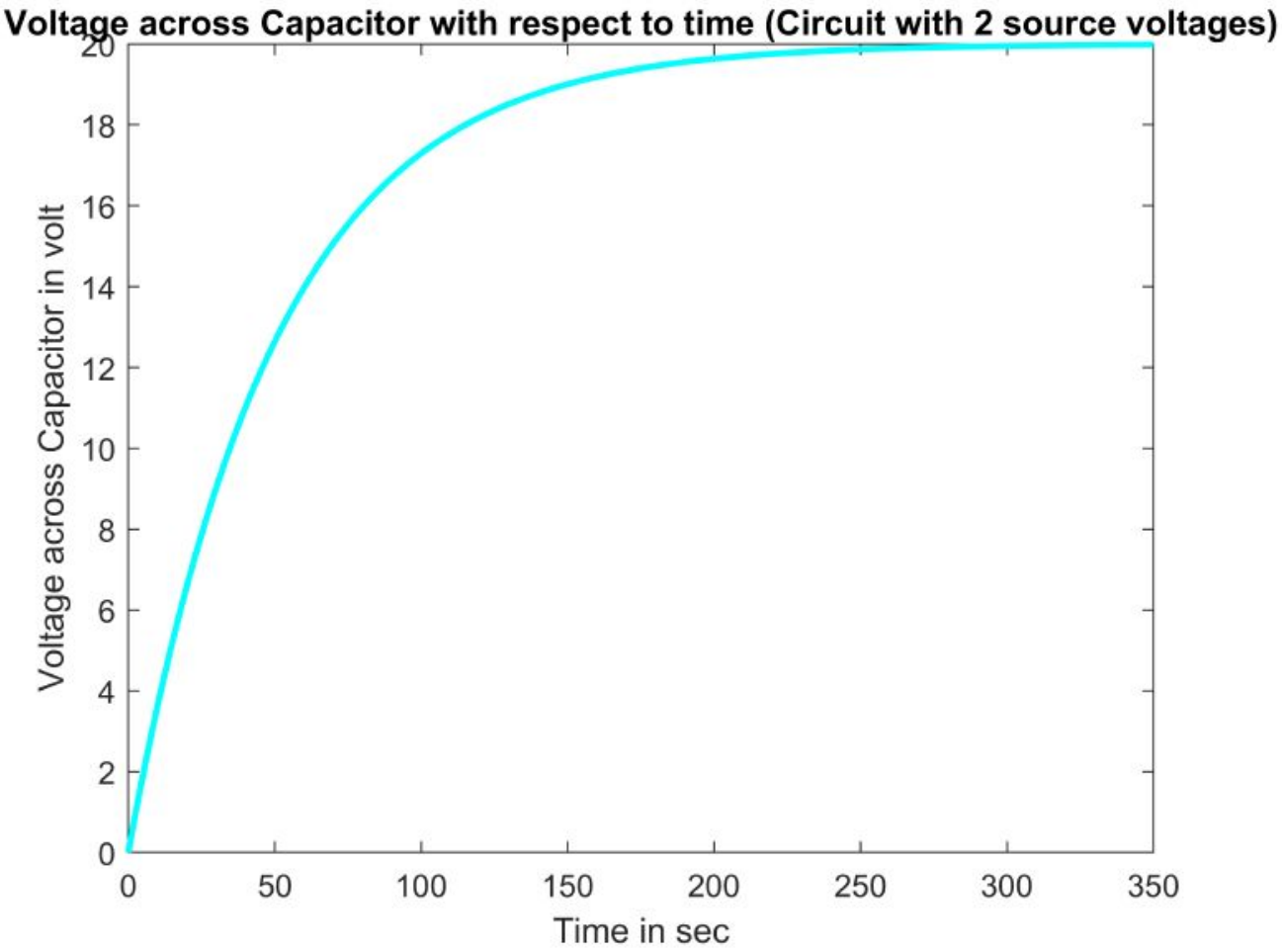
A voltage source has positive or negative polarity depending on its orientation in a circuit. In the case when a voltage across an element has negative voltage, it just means the negative terminal of the voltmeter is connected to the positive side of the circuit and the positive terminal of the voltmeter is connected to the negative side of the circuit.

It just conveys the orientation, but do not make any effect.

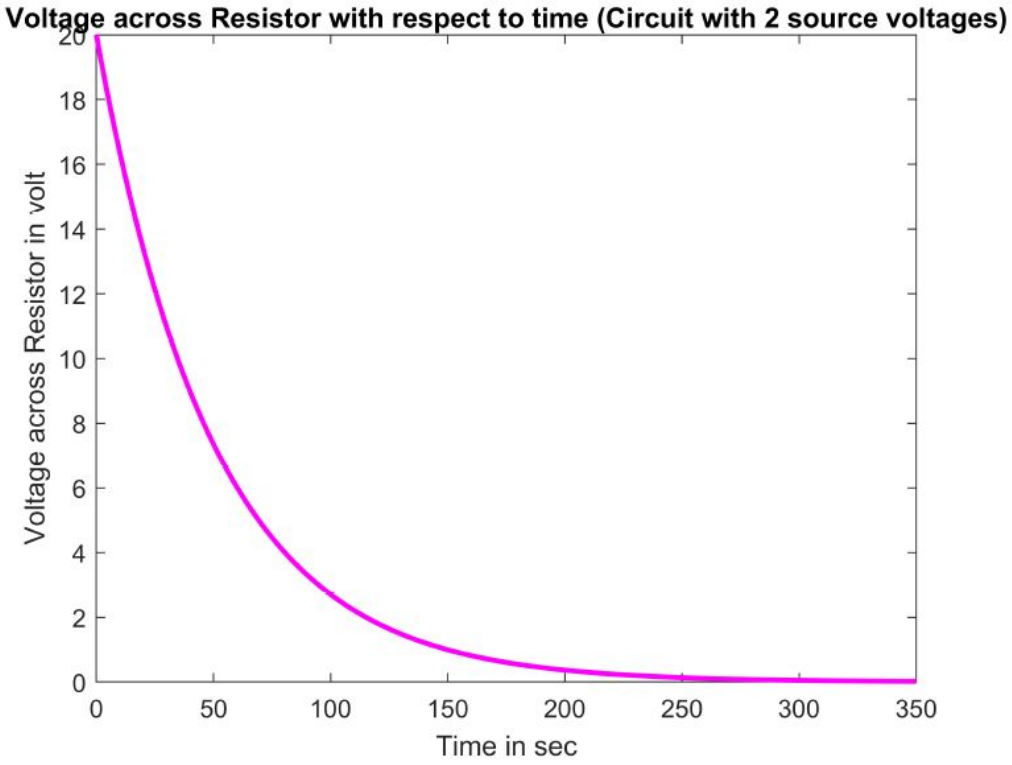
The negative value of current also shows just the opposite direction of flow of current in the circuit. Negative sign tells the direction and not affect magnitude in any way.

Thus, on summing both the functions, as per the super_position theorem,

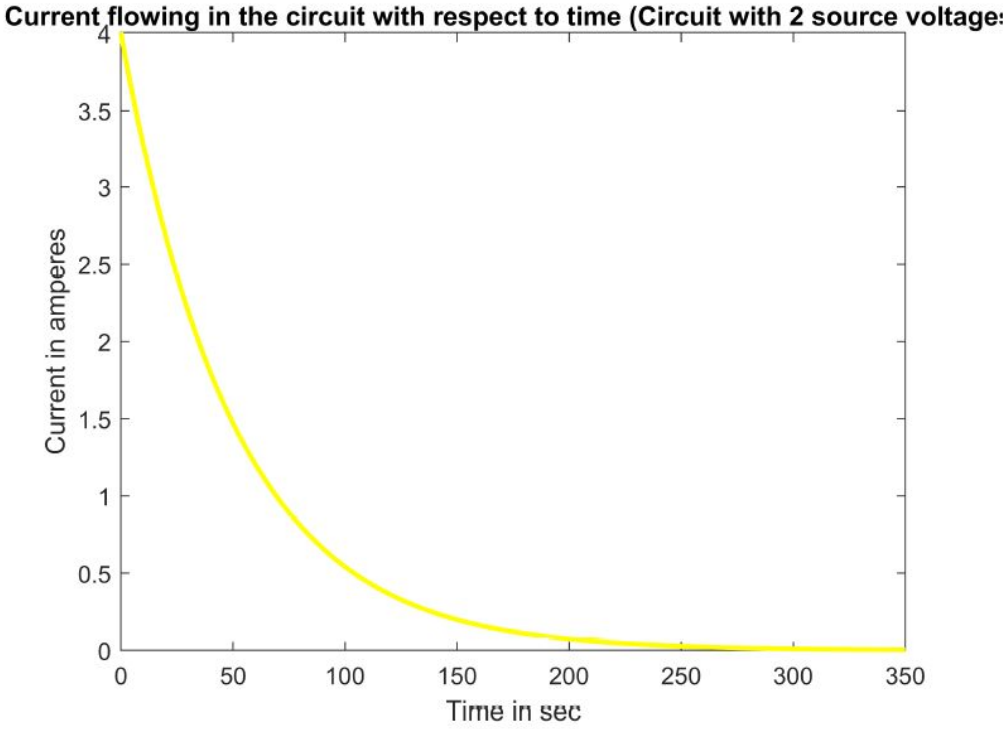
```
Vc_out = Vc_out1 + Vc_out2;
Vr_out = Vr_out1 + Vr_out2;
I_out = I1 + I2;

plot(t,Vc_out,"LineWidth",2,"Color",'c')
title("Voltage across Capacitor with respect to time (Circuit with 2 source voltages)")
xlabel("Time in sec")
ylabel("Voltage across Capacitor in volt")
```


Voltage across Capacitor with respect to time (Circuit with 2 source voltages)
Voltage across Capacitor in volt
Time in sec
0
2
4
6
8
10
12
14
16
18
20
0
50
100
150
200
250
300
350

```
plot(t,Vr_out,"LineWidth",2,"Color",'m')
title("Voltage across Resistor with respect to time (Circuit with 2 source voltages)")
xlabel("Time in sec")
ylabel("Voltage across Resistor in volt")
```



```
plot(t,I_out,"LineWidth",2,"Color",'y')
title("Current flowing in the circuit with respect to time (Circuit with 2 source voltages)")
xlabel("Time in sec")
ylabel("Current in amperes")
```



INFERENCE

We can observe that the sum of individual output voltages is equal to the output voltage when both source voltages (30 V and 10 V) are connected in the circuit.

- For $\mathbf{V_{in}}$ = 30V and 10V, we get output voltage across resistor and capacitor as $\mathbf{Vr_{\_out}}$ and $\mathbf{Vc_{\_out}}$ and current flowing through the circuit is $\mathbf{I_{\_out}}$.
- For $\mathbf{V_{in}}$ = 30V, we get output voltage across resistor and capacitor as $\mathbf{Vr_{\_out1}}$ and $\mathbf{Vc_{\_out1}}$ and current flowing through the circuit is I_out1.
- For $\mathbf{V_{in}}$ = 10V, we get output voltage across resistor and capacitor as $\mathbf{Vr_{\_out2}}$ and $\mathbf{Vc_{\_out2}}$ and current flowing through the circuit is $\mathbf{I_{\_out2}}$.

We observe that:

- $\mathbf{Vr_{\_out} = Vr_{\_out1} + Vr_{\_out2}}$
- $\mathbf{Vc_{\_out} = Vc_{\_out1} + Vc_{\_out2}}$
- $\mathbf{I_{\_out} = I_{\_out1} + I_{\_out2}}$

Hence, the superposition theorem is proved.

Summary of the entire Experiment

REFERENCES

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- https://www.electronics-tutorials.ws/
- https://www.falstad.com/circuit/directions.html
- https://byjus.com/

THANK YOU