



Digital Design ENCS2340

**VERILOG PROJECT**

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**Project Report**

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- This pdf contains the Project Verilog Description, Simulation Screenshots and Quartus Diagram.

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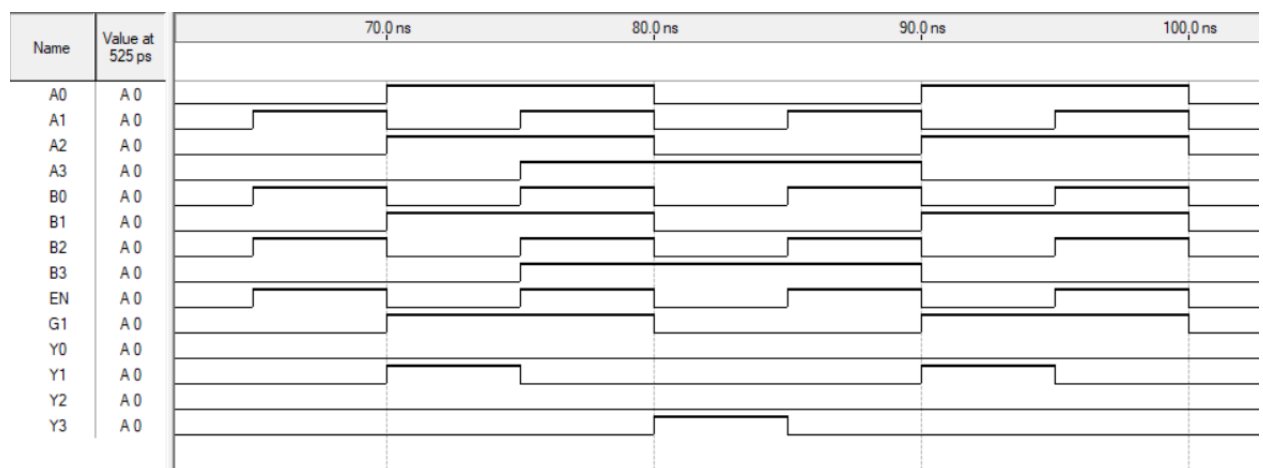
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## 1. Quad\_Mux2x1

### A) Verilog Description:

```
1 module Quad_Mux2x1 (  
2     input EN,  
3     input A0, A1, A2, A3,  
4     input B0, B1, B2, B3,  
5     input G1,  
6     output reg Y0, Y1, Y2, Y3);  
7  
8 always @ (*)begin  
9     if(EN == 0) begin  
10        if (G1 == 0) begin  
11            Y0 = A0;  
12            Y1 = A1;  
13            Y2 = A2;  
14            Y3 = A3;  
15        end else begin  
16            Y0 = B0;  
17            Y1 = B1;  
18            Y2 = B2;  
19            Y3 = B3;  
20        end  
21    end else begin  
22        Y0 = 0;  
23        Y1 = 0;  
24        Y2 = 0;  
25        Y3 = 0;  
26    end  
27 end  
28 endmodule
```

### B) Simulation Screenshot:



## 2. BCD\_7Segment\_Driver

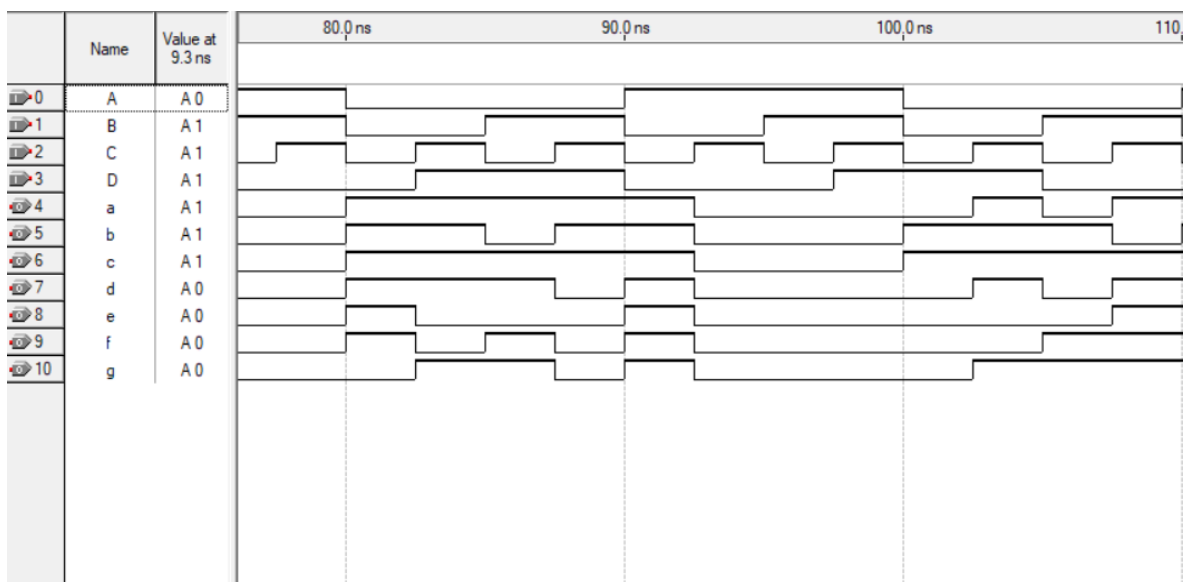
### A) Verilog Description:

```

1  module BCD_7Segment_Driver (A, B, C, D, a, b, c, d, e, f, g);
2      input A, B, C, D;
3      output reg a, b, c, d, e, f, g;
4
5      always @ (A, B, C, D) begin
6          case ({A, B, C, D})
7              4'b0000 :
8                  {a, b, c, d, e, f, g} = 7'b1111110;
9              4'b0001 :
10                 {a, b, c, d, e, f, g} = 7'b0110000;
11             4'b0010 :
12                 {a, b, c, d, e, f, g} = 7'b1101101;
13             4'b0011 :
14                 {a, b, c, d, e, f, g} = 7'b1111001;
15             4'b0100 :
16                 {a, b, c, d, e, f, g} = 7'b0110011;
17             4'b0101 :
18                 {a, b, c, d, e, f, g} = 7'b1011011;
19             4'b0110 :
20                 {a, b, c, d, e, f, g} = 7'b1011111;
21             4'b0111 :
22                 {a, b, c, d, e, f, g} = 7'b1110000;
23             4'b1000 :
24                 {a, b, c, d, e, f, g} = 7'b1111111;
25             4'b1001 :
26                 {a, b, c, d, e, f, g} = 7'b1111011;
27             default :
28                 {a, b, c, d, e, f, g} = 7'b0000000;
29         endcase
30     end
31 endmodule
32

```

### B) Simulation Screenshot:



### 3. Decoder2x4

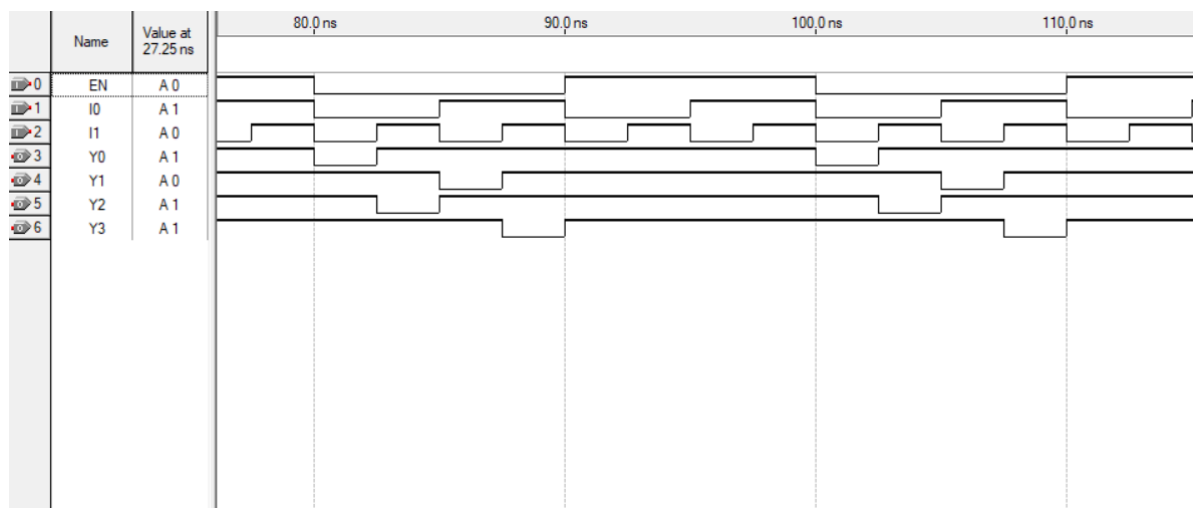
#### A) Verilog Description:

```

1 module Decoder2x4 (
2     input I0, I1, EN,
3     output reg Y0, Y1, Y2, Y3);
4
5     always @ (*) begin
6         if(EN == 0) begin
7             case ({I1, I0})
8             2'b00: begin
9                 Y0 = 0;          Y1 = 1;
10                Y2 = 1;          Y3 = 1;
11            end
12            2'b01: begin
13                Y0 = 1;          Y1 = 0;
14                Y2 = 1;          Y3 = 1;
15            end
16            2'b10: begin
17                Y0 = 1;          Y1 = 1;
18                Y2 = 0;          Y3 = 1;
19            end
20            2'b11: begin
21                Y0 = 1;          Y1 = 1;
22                Y2 = 1;          Y3 = 0;
23            end
24            default : begin
25                Y0 = 1;          Y1 = 1;
26                Y2 = 1;          Y3 = 1;
27            end
28            endcase
29        end else begin
30            Y0 = 1;          Y1 = 1;
31            Y2 = 1;          Y3 = 1;
32        end
33    end
34 endmodule

```

#### B) Simulation Screenshot:



## Quartus Diagram

