Digital Design ENCS2340

VERILOG PROJECT

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Project Report

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- This pdf contains the Project Verilog Description, Simulation Screenshots and Quartus Diagram.

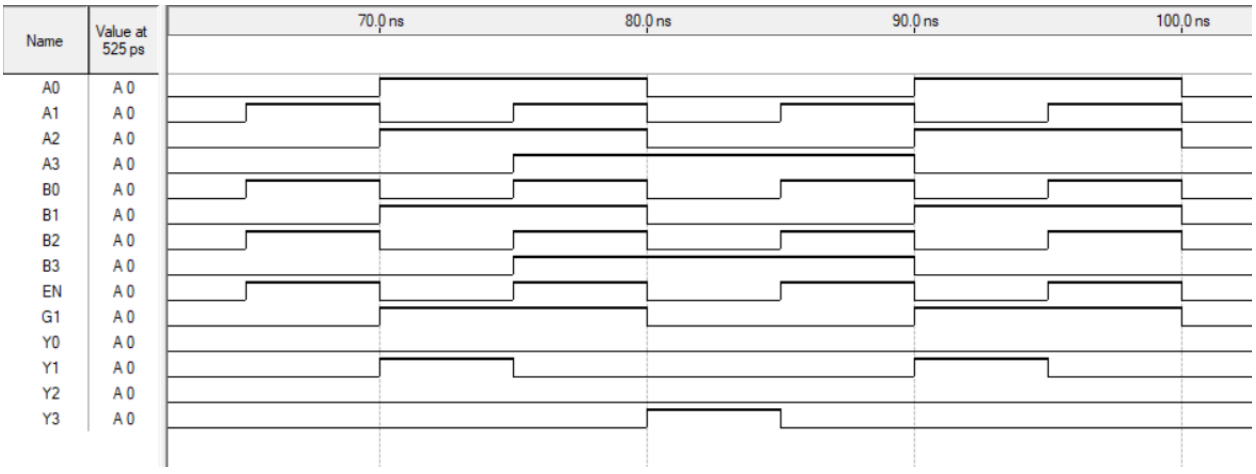
Contents

1. Quad_Mux2x1

A) Verilog Description:

```
1  module Quad_Mux2x1 (
2      input EN,
3      input A0, A1, A2, A3,
4      input B0, B1, B2, B3,
5      input G1,
6      output reg Y0, Y1, Y2, Y3);
7
8  always @ (*)begin
9      if(EN == 0) begin
10         if (G1 == 0) begin
11             Y0 = A0;
12             Y1 = A1;
13             Y2 = A2;
14             Y3 = A3;
15         end else begin
16             Y0 = B0;
17             Y1 = B1;
18             Y2 = B2;
19             Y3 = B3;
20         end
21     end else begin
22         Y0 = 0;
23         Y1 = 0;
24         Y2 = 0;
25         Y3 = 0;
26     end
27 end
28 endmodule
```

B) Simulation Screenshot:



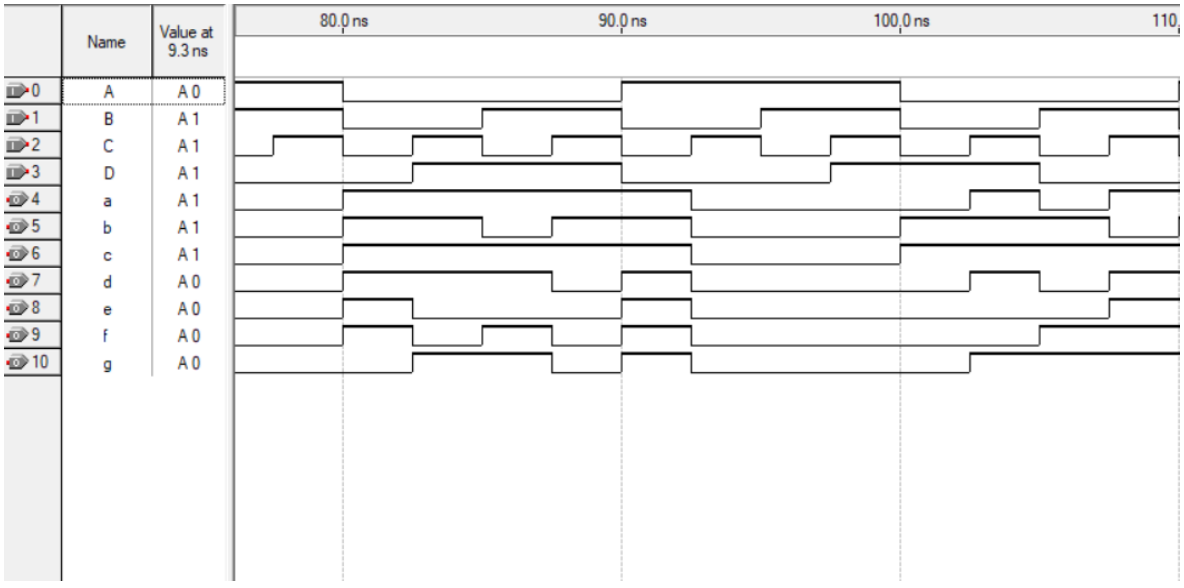
2. BCD_7Segment_Driver

A) Verilog Description:

```
module BCD_7Segment_Driver (A, B, C, D, a, b, c, d, e, f, g);
    input A, B, C, D;
    output reg a, b, c, d, e, f, g;

always @ (A, B, C, D) begin
    case({A, B, C, D})
        4'b0000 :
        {a, b, c, d, e, f, g} = 7'b1111110;
        4'b0001 :
        {a, b, c, d, e, f, g} = 7'b0110000;
        4'b0010 :
        {a, b, c, d, e, f, g} = 7'b1101101;
        4'b0011 :
        {a, b, c, d, e, f, g} = 7'b1111001;
        4'b0100 :
        {a, b, c, d, e, f, g} = 7'b0110011;
        4'b0101 :
        {a, b, c, d, e, f, g} = 7'b1011011;
        4'b0110 :
        {a, b, c, d, e, f, g} = 7'b1011111;
        4'b0111 :
        {a, b, c, d, e, f, g} = 7'b1110000;
        4'b1000 :
        {a, b, c, d, e, f, g} = 7'b1111111;
        4'b1001 :
        {a, b, c, d, e, f, g} = 7'b1111011;
        default :
        {a, b, c, d, e, f, g} = 7'b0000000;
    endcase
end
endmodule
```

B) Simulation Screenshot:



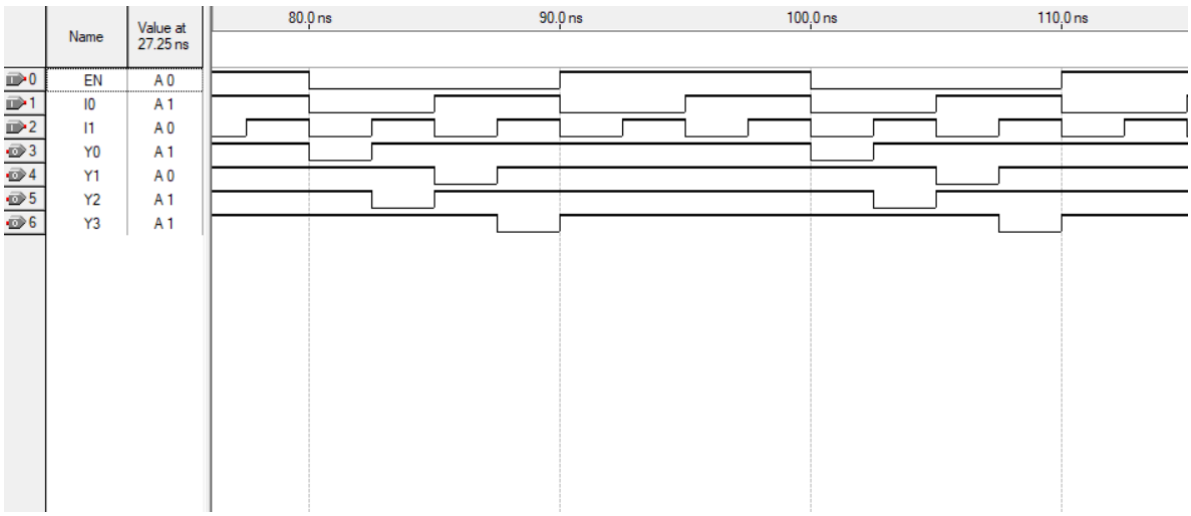
3. Decoder2x4

A) Verilog Description:

```
module Decoder2x4 (
    input I0, I1, EN,
    output reg Y0, Y1, Y2, Y3);

always @ (*) begin
    if(EN == 0) begin
        case ({I1, I0})
        2'b00: begin
        Y0 = 0;          Y1 = 1;
        Y2 = 1;          Y2 = 1;
        end
        2'b01: begin
        Y0 = 1;          Y1 = 0;
        Y2 = 1;          Y3 = 1;
        end
        2'b10: begin
        Y0 = 1;          Y1 = 1;
        Y2 = 0;          Y3 = 1;
        end
        2'b11: begin
        Y0 = 1;          Y1 = 1;
        Y2 = 1;          Y3 = 0;
        end
        default : begin
        Y0 = 1;          Y1 = 1;
        Y2 = 1;          Y3 = 1;
        end
        endcase
    end else begin
        Y0 = 1;          Y1 = 1;
        Y2 = 1;          Y3 = 1;
        end
    end
endmodule
```

B) Simulation Screenshot:



Quartus Diagram