

Cairo University Computer Engineering Department

Faculty of Engineering Credit Hours System

**Computer Architecture**

**CMPN301**

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**Phase 2 Report**

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**Design Changes**

1-Forwarding unit takes from ex stage.

2-The output of the instruction memory is directed to a sign extend in the decode stage for Immediate value use.

3-Added wire from the Control Unit to the PC Control Unit to increment the PC counter by 2 for Immediate Instruction.

4-Out port continues to Write Back stage.

5-Input port is from the fetch stage until the write back stage.

**Hazards**

1- Structural hazard:

Writing on the positive edge and reading on the falling edge (not fully tested).

2- Data Hazard:

Forwarding Unit ALU TO ALU is implemented.

Full Forwarding implemented but not working right.

Forwarding input port signals not working.

Data Hazard Detection Unit is implemented for Load Use. It inserts bubble/NOP after load instruction.