



Department of Computer Science & Engineering
Microprocessor & Computer Architecture
MPCA-Laboratory/Assignment/Hands-on/Project
UE20CS252

Sl. No	Programs
Week No.5	<ol style="list-style-type: none">1. Write a program in ARM7TDMI-ISA to generate Fibonacci Series and store them in an array.2. Write a program in ARM7TDMI-ISA to find smallest number in an array of n 32 bit numbers. Display the element if found.3. Write a program in ARM7TDMI-ISA to add 2 matrices of order3. i.e., Implement $c[i][j] = a[i][j] + b[i][j]$.4. Write a program in ARM7TDMI-ISA to transfer a block of 256 words stored at memory location X to memory location Y using Load Multiple and Store Multiple instructions. The rate of transfer is 32 bytes. <p>Student exercises:</p> <ol style="list-style-type: none">1. Write a program in ARM7TDMI-ISA to multiply 2 matrices of order3. i.e., implement $c[i][j] = c[i][j] + a[i][j] \times b[i][j]$.<ol style="list-style-type: none">a. Use MLA instruction <p>.DATA</p> <p>A: WORD 10,20,30,40,50,60,70,80,90</p> <p>B: WORD 1,2,3,4,5,6,7,8,9</p> <p>C: WORD 0,0,0,0,0,0,0,0,0</p> <p>.TEXT</p> <p>LDR R0,=A</p> <p>LDR R1,=B</p> <p>LDR R2,=C</p> <p>MOV R5,#0</p> <p>MOV R6,#0</p> <p>MOV R7,#0</p> <p>MOV R8,#0</p>

LOOP:

```
LDR R3,[R0],#4
LDR R4,[R1],#12
MLA R8,R3,R4,R8
ADD R5,R5,#1
CMP R5,#3
BNE LOOP
STR R8,[R2],#4
BL L1
```

L1:

```
LDR R3,[R0,#-12]!
LDR R4,[R1,#-32]!
MOV R8,#0
MOV R5,#0
ADD R6,R6,#1
CMP R6,#3
BLT LOOP
```

```
LDR R3,[R0,#12]!
LDR R4,[R1,#-12]!
MOV R8,#0
MOV R5,#0
MOV R6,#0
ADD R7,R7,#1
CMP R7,#3
BNE LOOP
BNE LOOP
SWI 0X011
```

ARMSim - The ARM Simulator Dept. of Computer Science

File View Cache Debug Watch Help

RegistersView

General Purpose | Floating Point

Hexadecimal

Unsigned Decimal

Signed Decimal

R0 : 00000000
R1 : 00000000
R2 : 00000000
R3 : 00000000
R4 : 00000000
R5 : 00000000
R6 : 00000000
R7 : 00000000
R8 : 00000000
R9 : 00000000
R10 (s1) : 00000000
R11 (fp) : 00000000
R12 (ip) : 00000000
R13 (sp) : 00005400
R14 (lr) : 00000000
R15 (pc) : 00001000

CPSR Register

Negative (N) : 0
Zero (Z) : 0
Carry (C) : 0
Overflow (V) : 0
IRQ Disable : 1
FIQ Disable : 1
Thumb (T) : 0
CPU Mode : System

0x000000df

1b.s

```

.DATA
0000108C: A: .WORD 10,20,30,40,50,60,70,80,90
000010B0: B: .WORD 1,2,3,4,5,6,7,8,9
000010D4: C: .WORD 0,0,0,0,0,0,0,0,0

.TEXT
00001000:E59P0078 LDR R0,=A
00001004:E59F1078 LDR R1,=B
00001008:E59F2078 LDR R2,=C
0000100C:E3A05000 MOV R5,#0
00001010:E3A06000 MOV R6,#0
00001014:E3A07000 MOV R7,#0
00001018:E3A08000 MOV R8,#0

.LOOP:
0000101C: LDR R3,[R0],#4
0000101D:E4913004 LDR R4,[R1],#12
00001020:E491400C MLA R8,R3,R4,R8
00001024:E0288493 ADD R5,R5,#1
00001028:E2855001 CMP R5,#3
0000102C:E3550003 BNE LOOP
00001030:1AFFFFF9 STR R8,[R2],#4
00001034:E4828004 BL L1
00001038:EDFFFFFF

```

MemoryView1

Word Size: 8Bit 16Bit 32Bit

000010D4

StackView

000053AC:81818181
000053B0:81818181
000053B4:81818181
000053B8:81818181
000053BC:81818181
000053C0:81818181
000053C4:81818181
000053C8:81818181
000053CC:81818181
000053D0:81818181
000053D4:81818181
000053D8:81818181
000053DC:81818181
000053E0:81818181
000053E4:81818181
000053E8:81818181
000053EC:81818181
000053F0:81818181
000053F4:81818181
000053F8:81818181
000053FC:81818181
00005400:81818181
00005404:81818181
00005408:81818181
0000540C:81818181
00005410:81818181
00005414:81818181
00005418:81818181
0000541C:81818181
00005420:81818181
00005424:81818181
00005428:81818181
0000542C:81818181
00005430:81818181
00005434:81818181
00005438:81818181
0000543C:81818181
00005440:81818181
00005444:81818181
00005448:81818181
0000544C:81818181
00005450:81818181

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File View Cache Debug Watch Help

RegistersView

General Purpose | Floating Point

Hexadecimal

Unsigned Decimal

Signed Decimal

R0 : 000010b0
R1 : 000010b0
R2 : 000010f8
R3 : 00000001
R4 : 00000001
R5 : 00000000
R6 : 00000000
R7 : 00000003
R8 : 00000000
R9 : 00000000
R10 (s1) : 00000000
R11 (fp) : 00000000
R12 (ip) : 00000000
R13 (sp) : 00005400
R14 (lr) : 0000103c
R15 (pc) : 0000107c

CPSR Register

Negative (N) : 0
Zero (Z) : 1
Carry (C) : 1
Overflow (V) : 0
IRQ Disable : 1
FIQ Disable : 1
Thumb (T) : 0
CPU Mode : System

0x600000df

1b.s

```

00001038:EDFFFFFF BL L1

.L1:
0000103C: LDR R3,[R0,#-12]!
00001040:E5314020 LDR R4,[R1,#-32]!
00001044:E3A08000 MOV R8,#0
00001048:E3A05000 MOV R5,#0
0000104C:E2866001 ADD R6,R6,#1
00001050:E3660003 CMP R6,#3
00001054:BAFFFFFFO BLT LOOP

00001058:E5B0300C LDR R3,[R0,#12]!
0000105C:E531400C LDR R4,[R1,#-12]!
00001060:E3A08000 MOV R8,#0
00001064:E3A05000 MOV R5,#0
00001068:E3A06000 MOV R6,#0
0000106C:E2877001 ADD R7,R7,#1
00001070:E3570003 CMP R7,#3
00001074:1AFFFFF9 BNE LOOP
00001078:1AFFFEED BNE LOOP
0000107C:EF000011 SWI 0X011

```

MemoryView1

Word Size: 8Bit 16Bit 32Bit

000010D4

StackView

000053AC:81818181
000053B0:81818181
000053B4:81818181
000053B8:81818181
000053BC:81818181
000053C0:81818181
000053C4:81818181
000053C8:81818181
000053CC:81818181
000053D0:81818181
000053D4:81818181
000053D8:81818181
000053DC:81818181
000053E0:81818181
000053E4:81818181
000053E8:81818181
000053EC:81818181
000053F0:81818181
000053F4:81818181
000053F8:81818181
000053FC:81818181
00005400:81818181
00005404:81818181
00005408:81818181
0000540C:81818181
00005410:81818181
00005414:81818181
00005418:81818181
0000541C:81818181
00005420:81818181
00005424:81818181
00005428:81818181
0000542C:81818181
00005430:81818181
00005434:81818181
00005438:81818181
0000543C:81818181
00005440:81818181
00005444:81818181
00005448:81818181
0000544C:81818181
00005450:81818181

b. Use MUL instruction

.DATA

A: .WORD 10,20,30,40,50,60,70,80,90

B: .WORD 1,2,3,4,5,6,7,8,9

C: .WORD 0,0,0,0,0,0,0,0,0

.TEXT

LDR R0,=A

LDR R1,=B

LDR R2,=C

MOV R5,#0

MOV R6,#0

MOV R7,#0

MOV R8,#0

MOV R9,#0

LOOP:

LDR R3,[R0],#4

LDR R4,[R1],#12

MUL R8,R3,R4

ADD R9,R9,R8

ADD R5,R5,#1

CMP R5,#3

BNE LOOP

STR R9,[R2],#4

BL L1

L1:

LDR R3,[R0,#-12]!

LDR R4,[R1,#-32]!

MOV R8,#0

MOV R9,#0

MOV R5,#0

ADD R6,R6,#1

CMP R6,#3

BLT LOOP

LDR R3,[R0,#12]!

LDR R4,[R1,#-12]!

MOV R8,#0

MOV R9,#0

MOV R5,#0

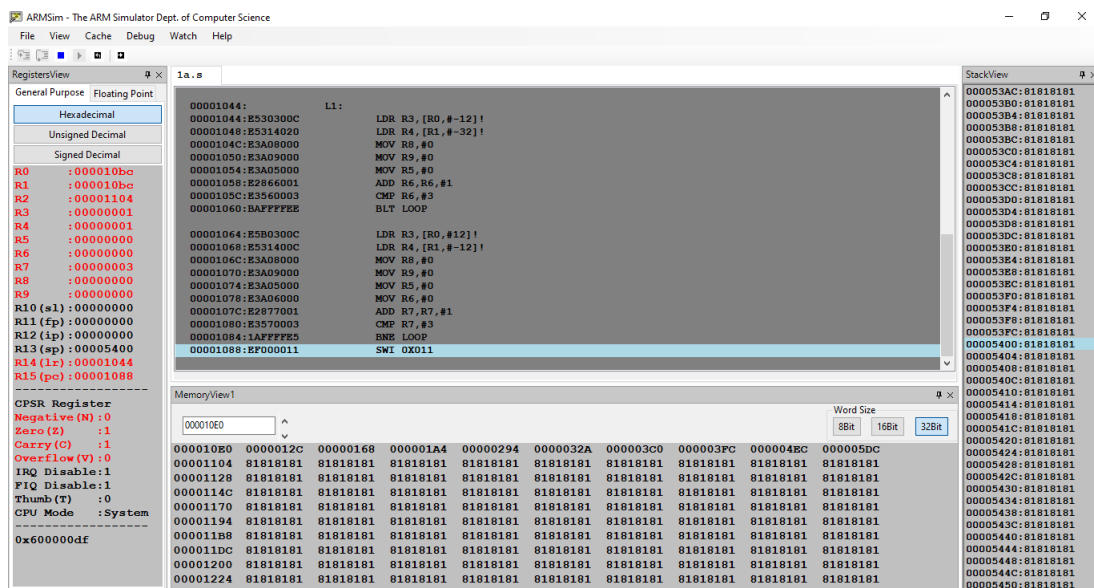
MOV R6,#0

ADD R7,R7,#1

CMP R7,#3

BNE LOOP

SWI 0X011



```
.DATA
    MATRIX:.WORD 1, 2, 3, 4, 5, 6, 7, 8, 9
    R:.WORD 3
    C:.WORD 3
    ROWSUM:.WORD 0, 0, 0

.TEXT
    LDR R0,=MATRIX
    LDR R1,=R
    LDR R2,=C
```

LDR R9,=ROWSUM

LDR R3,[R0]

LDR R4,[R1]

LDR R5,[R2]

MOV R6,#1

L1:

MOV R7,#1

MOV R8,#0

L2:

ADD R8,R8,R3

LDR R3,[R0,#4]!

ADD R7,R7,#1

CMP R7,R5

BLE L2

STR R8,[R9],#4

ADD R6,R6,#1

CMP R6,R4

BLE L1

SWI 0X011

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File View Cache Debug Watch Help

RegistersView

General Purpose Floating Point

Hexadecimal

Unsigned Decimal

Signed Decimal

R0 : 00000000

R1 : 00000000

R2 : 00000000

R3 : 00000000

R4 : 00000000

R5 : 00000000

R6 : 00000000

R7 : 00000000

R8 : 00000000

R9 : 00000000

R10 (s1) : 00000000

R11 (fp) : 00000000

R12 (ip) : 00000000

R13 (sp) : 00005400

R14 (lr) : 00000000

R15 (pc) : 00001000

CPSR Register

Negative (N) : 0

Zero (Z) : 0

Carry (C) : 0

Overflow (V) : 0

IRQ Disable : 1

FIQ Disable : 1

Thumb (T) : 0

CPU Mode : System

0x000000df

3. s

.DATA

00001060: MATRIX: .WORD 1, 2, 3, 4, 5, 6, 7, 8, 9

00001084: R1: .WORD 3

00001088: C1: .WORD 3

0000108C: ROWSUM: .WORD 0, 0, 0

.TEXT

00001000: E59F0048 LDR R0,=MATRIX

00001004: E59F1048 LDR R1,=R

00001008: E59F2048 LDR R2,=C

0000100C: E59F9048 LDR R9,=ROWSUM

00001010: E5903000 LDR R3,[R0]

00001014: E5914000 LDR R4,[R1]

00001018: E5925000 LDR R5,[R2]

0000101C: E3A06001 L1: MOV R6,#1

00001020: MOV R7,#1

00001024: E3A08000 L2: MOV R8,#0

00001028: ADD R8,R8,R3

StackView

000053AC: 81818181

000053B0: 81818181

000053B8: 81818181

000053C0: 81818181

000053C8: 81818181

000053D0: 81818181

000053D8: 81818181

000053E0: 81818181

000053E8: 81818181

000053F0: 81818181

000053F8: 81818181

00005400: 81818181

00005408: 81818181

00005410: 81818181

00005418: 81818181

00005420: 81818181

00005428: 81818181

00005430: 81818181

00005438: 81818181

00005440: 81818181

00005448: 81818181

00005450: 81818181

MemoryView 1

0000108C

Word Size

8Bit 16Bit 32Bit

0000108C 00000000 00000000 00000000 81818181 81818181 81818181 81818181 81818181 81818181

00001090 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181

00001094 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181

00001098 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181

00001102 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181

00001106 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181

00001110 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181

00001114 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181

00001118 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181

00001122 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181

00001126 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181

00001130 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181

00001134 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181

00001138 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181

00001142 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181

00001146 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181

00001150 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181

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File View Cache Debug Watch Help

RegistersView 3.s

General Purpose Floating Point

Hexadecimal
Unsigned Decimal
Signed Decimal

R0 : 00001084
R1 : 00001084
R2 : 00001088
R3 : 00000003
R4 : 00000003
R5 : 00000003
R6 : 00000004
R7 : 00000004
R8 : 00000004
R9 : 00000018
R10 (s1) : 00000000
R11 (fp) : 00000000
R12 (ip) : 00000000
R13 (sp) : 00005400
R14 (lr) : 00000000
R15 (pc) : 0000104c

CPSR Register
Negative (N) : 0
Zero (Z) : 0
Carry (C) : 1
Overflow (V) : 0
IRQ Disable : 1
Thumb (T) : 0
CPU Mode : System
0x200000df

00001010: E5903000 LDR R3, [R0]
00001014: E5914000 LDR R4, [R1]
00001018: E5925000 LDR R5, [R2]
0000101C: E3A06001 L1: MOV R6, #1
00001020: MOV R7, #1
00001020: E3A07001 MOV R7, #1
00001024: E3A08000 MOV R8, #0
00001028: L2: ADD R8, R8, R3
00001028: E0888003
0000102C: E5B03004 LDR R3, [R0, #4]!
00001030: E2877001 ADD R7, R7, #1
00001034: E1570005 CMP R7, R5
00001038: DAFFFFFA BLE L2
0000103C: DA898004 STR R8, [R9], #4
00001040: E2866001 ADD R6, R6, #1
00001044: E1560004 CMP R6, R4
00001048: DAFFFFFA BLE L1
0000104C: EF000011 SWI 0X011

MemoryView1

Word Size
8Bit 16Bit 32Bit

0000108C 00000006 0000000F 00000018 81818181 81818181 81818181 81818181 81818181 81818181
000010B0 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181
000010D4 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181
000010F8 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181
0000111C 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181
00001140 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181
00001164 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181
00001188 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181
000011AC 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181
000011D0 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181

StackView

000053AC: 81818181
000053B0: 81818181
000053B4: 81818181
000053B8: 81818181
000053BC: 81818181
000053C0: 81818181
000053C4: 81818181
000053C8: 81818181
000053CC: 81818181
000053D0: 81818181
000053D4: 81818181
000053D8: 81818181
000053DC: 81818181
000053E0: 81818181
000053E4: 81818181
000053E8: 81818181
000053EC: 81818181
000053F0: 81818181
000053F4: 81818181
000053F8: 81818181
000053FC: 81818181
00005400: 81818181
00005404: 81818181
00005408: 81818181
0000540C: 81818181
00005410: 81818181
00005414: 81818181
00005418: 81818181
0000541C: 81818181
00005420: 81818181
00005424: 81818181
00005428: 81818181
0000542C: 81818181
00005430: 81818181
00005434: 81818181
00005438: 81818181
0000543C: 81818181
00005440: 81818181
00005444: 81818181
00005448: 81818181
0000544C: 81818181
00005450: 81818181