Implementation of Digital Phase Locked Loop using CMOS Technology

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ABSTRACT: The requirement for low power and rapid circuits are expanding in present day hardware. The generation of carrier and locking of phase have become significant for transceiver circuits. The frequency divider which is dependent on the phase locked loop (PLL) is a fundamental building block of the transceiver. The frequency divider that produces the carrier for the down-conversion/up-conversion functions, it works at high frequency and it expends a massive portion of the whole power of the circuit. The frequency divider dependent on phase locked loop (PLL) comprises voltage controlled oscillator (VCO), phase detector, loop filter and frequency divider.

KEYWORDS: CMOS, VCO.

Fig2 : Implemented Digital Phase locked Loop

INTRODUCTION

A phase lock loop is a negative feedback system consisting of a phase detector, low pass filter and voltage controlled oscillator (VCO). Its purpose is to synchronize an output signal with a reference or input signal in frequency as well as in phase. Classification of PLL is Analog PLL Digital PLL and All digital PLL The major application of PLL is frequency synthesis for frequency multiplier and frequency divider. In frequency synthesis, If we want 1Ghz from the 100 Mhz reference voltage so there we use PLL. and Also used in clock data recovery data[1].

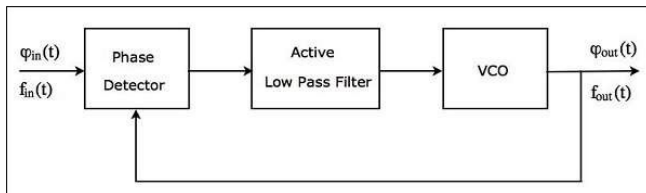### OUTPUT WAVEFORM

Fig 4: Output waveform of PLL

Fig1: Block Diagram of PLL [1]

Applied to the Phase detector. In a phase detector there are two input signals one is a reference signal or input signal and the second is a feedback signal or an output of the oscillator signal. Phase detector is basically a comparator circuit that compares both the input and the output to detect the phase difference between input signal and feedback signal. Means output of the phase detector is an error voltage that is proportional to the phase difference between input signal and oscillator frequency[2].
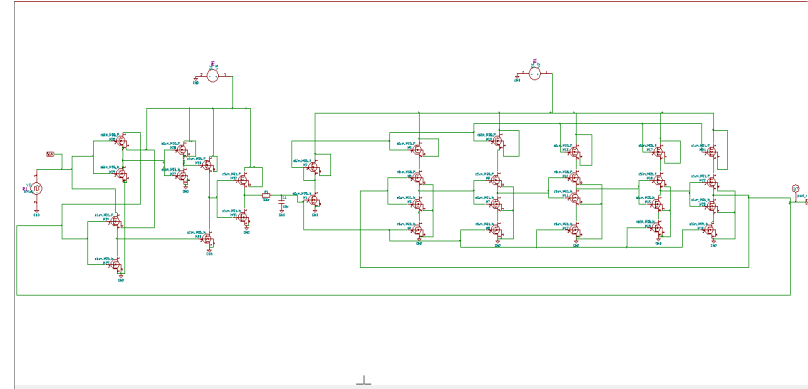
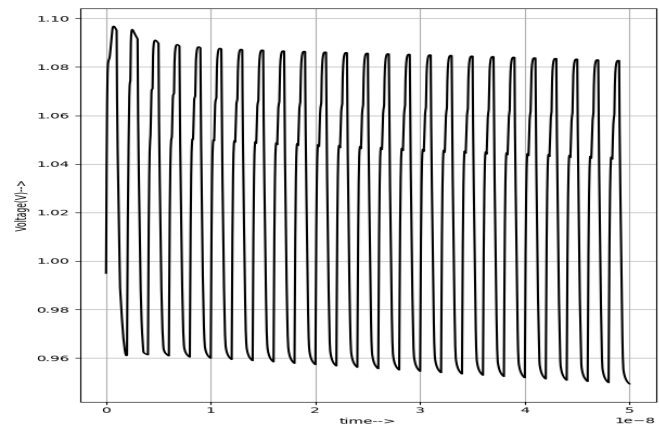## Reference

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