The documentation and process conversion measures necessary to comply with this revision shall be completed by 18 September 2018.

INCH-POUND

MIL-PRF-19500/371J
18 June 2018
SUPERSEDING
MIL-PRF-19500/371H
13 December 2013

PERFORMANCE SPECIFICATION SHEET

* TRANSISTOR, NPN, SILICON, HIGH POWER, TYPES 2N3902 AND 2N5157, JAN, JANTX, AND JANTXV

This specification is approved for use by all Departments and Agencies of the Department of Defense.

The requirements for acquiring the product described herein shall consist of this specification sheet and MIL-PRF-19500.

1. SCOPE

* 1.1 Scope. This specification covers the performance requirements for NPN silicon, high-power transistors. Three levels of product assurance (JAN, JANTX, and JANTXV) are provided for each encapsulated device.

* 1.2 Package outlines. The device package outlines are as follows: Modified TO-204AA (similar to TO-3) in accordance with figure 1, TO-254AA in accordance with figure 2, and TO-257AA in accordance with figure 3 for all encapsulated device types.

1.3 Maximum ratings. Unless otherwise specified, T_A = +25°C.

Type	P_T	P_T (1) T_C = +25°C	$R_{\theta JC}$ (2)	V_{CBO}	V_{CEO}	V_{EBO}	I_B	I_C	T_J and T_{STG}
	W	W	°C/W	V dc	V dc	V dc	A dc	A dc	°C
2N3902	5.0	125	1.25	700	400	5.0	2.0	3.5	-65 to +200
2N3902T1	6.0	175	1.00	700	400	5.0	2.0	3.5	-65 to +200
2N3902T3	4.0	(3) 125	1.30	700	400	5.0	2.0	3.5	-65 to +200
2N5157	5.0	125	1.25	700	500	6.0	2.0	3.5	-65 to +200
2N5157T1	6.0	175	1.00	700	500	6.0	2.0	3.5	-65 to +200
2N5157T3	4.0	(3) 125	1.30	700	500	6.0	2.0	3.5	-65 to +200

(1) See figures 4, 5, and 6 for temperature-power derating curves.
(2) For thermal impedance curves, see figures 7, 8, and 9.
(3) For TO-257 devices with typical mounting and small footprint, conservatively rated at 125 W and 1.3°C/W only.

Comments, suggestions, or questions on this document should be addressed to DLA Land and Maritime, ATTN: VAC, P.O. Box 3990, Columbus, OH 43218-3990, or emailed to Semiconductor@dla.mil. Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at https://assist.dla.mil/.

AMSC N/A

FSC 5961

1.4 Primary electrical characteristics. Unless otherwise specified, T_A = +25°C.

	h_{FE1} (1) V_{CE} = 5 V dc I_C = 0.5 A dc	h_{FE2} (1) V_{CE} = 5 V dc I_C = 1.0 A dc	$V_{CE(SAT)1}$ I_C = 1.0 A dc I_B = 0.1 A dc	$V_{BE(SAT)1}$ I_C = 1.0 A dc I_B = 0.1 A dc	C_{obo} V_{CB} = 10 V dc I_E = 0 100 kHz ≤ f ≤ 1 MHz	$\|h_{fe}\|$ V_{CE} = 10 V dc I_C = 0.2 A dc f = 1 MHz	Switching	
							t_{on}	t_{off}
			V dc	V dc	pF		µs	µs
Min	25	30				2.5		
Max		90	0.8	1.5	250	25	0.8	1.7

(1) Pulsed (see 4.5.1).

* 1.5 Part or Identifying Number (PIN). The PIN is in accordance with MIL-PRF-19500, and as specified herein. See 6.4 for PIN construction example and 6.5 for a list of available PINs.

* 1.5.1 JAN certification mark and quality level for encapsulated devices. The quality level designators for encapsulated devices that are applicable for this specification sheet from the lowest to the highest level are as follows: "JAN", "JANTX", and "JANTXV".

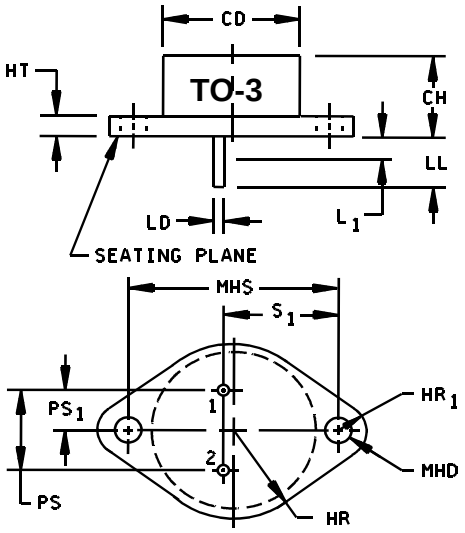
* 1.5.2 Device type. The designation system for the device types of transistors covered by this specification sheet are as follows.

* 1.5.2.1 First number and first letter symbols. The transistors of this specification sheet use the first number and letter symbols "2N".

* 1.5.2.2 Second number symbols. The second number symbols for the transistors covered by this specification sheet are as follows: "3902", and "5717".

* 1.5.2.3 Suffix letters. No suffix letters are used on devices that are packaged in the TO-3 similar package of figure 1. The suffix letters "T1" are used on devices that are packaged in the TO-254AA package of figure 2. The suffix letters "T3" are used on devices packaged in the TO-257AA package of figure 3.

* 1.5.3 Lead finish. The lead finishes applicable to this specification sheet are listed on QPDSIS-19500.

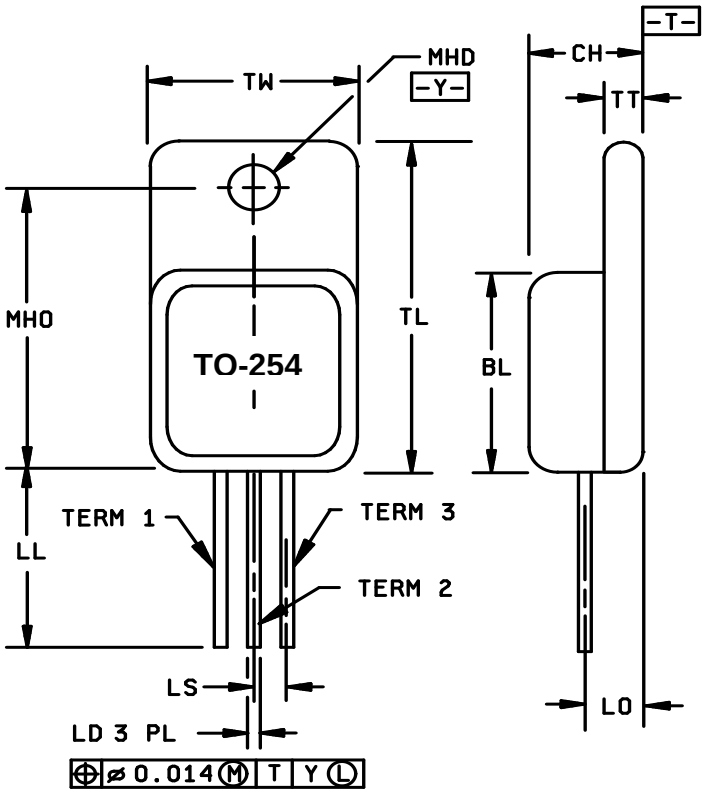


Ltr	Dimensions				Notes
	Inches		Millimeters		
	Min	Max	Min	Max	
CD		.875		22.22	3
CH	.250	.328	6.35	8.33	
HR	.495	.525	12.57	13.34	
HR_1	.131	.188	3.33	4.78	6
HT	.060	.135	1.52	3.43	
LD	.038	.043	0.97	1.09	4, 5, 9
LL	.312	.500	7.92	12.70	4, 5, 9
L_1		.050		1.27	5, 9
MHD	.151	.161	3.84	4.09	7
MHS	1.177	1.197	29.90	30.40	
PS	.420	.440	10.67	11.18	
PS_1	.205	.225	5.21	5.72	5
S_1	.655	.675	16.64	17.15	

NOTES:
1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. Body contour is optional within zone defined by CD.
4. These dimensions shall be measured at points .050 inch (1.27 mm) to .055 inch (1.40 mm) below seating plane. When gauge is not used, measurement shall be made at seating plane.
5. Both terminals.
6. At both ends.
7. Two holes.
8. Terminal 1 is the emitter, terminal 2 is base. The collector shall be electrically connected to the case.
9. LD applies between L_1 and LL. Lead diameter shall not exceed twice LD within L_1.
10. In accordance with ASME Y14.5M, diameters are equivalent to ϕx symbology.
11. The seating plane of the header shall be flat within .001 inch (0.03 mm) concave to .004 inch (0.10 mm) convex inside a .930 inch (23.62 mm) diameter circle on the center of the header and flat within .001 inch (0.03 mm) concave to .006 inch (0.15 mm) convex overall.

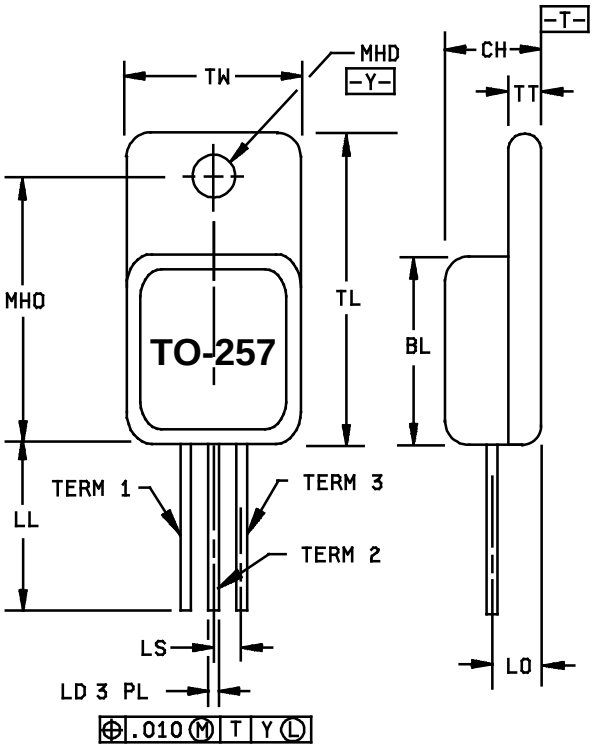
* FIGURE 1. Physical dimensions, 2N3902, 2N5157 (modified TO-204AA, similar to TO-3).

Symbol	Dimensions			
	Inches		Millimeters	
	Min.	Max.	Min.	Max.
BL	.535	.545	13.59	13.84
CH	.249	.260	6.32	6.60
LD	.035	.045	0.89	1.14
LL	.510	.570	12.95	14.48
LO	.150 BSC		3.81 BSC	
LS	.150 BSC		3.81 BSC	
MHD	.139	.149	3.53	3.78
MHO	.665	.685	16.89	17.40
TL	.790	.800	20.07	20.32
TT	.040	.050	1.02	1.27
TW	.535	.545	13.59	13.84
TERM 1	Base			
TERM 2	Collector			
TERM 3	Emitter			



NOTES:
1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. All terminals are isolated from case.
4. Methods used for electrical isolation of the terminals feedthroughs shall employ materials that contain a minimum of 90 percent AL2O3 (ceramic).
5. In accordance with ASME Y14.5M, diameters are equivalent to ϕx symbology.

FIGURE 2. Physical dimensions, 2N3902T1, 2N5157T1 (TO-254AA).



Ltr	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
BL	.410	.430	10.41	10.92
CH	.190	.200	4.83	5.08
LD	.025	.035	0.64	0.89
LL	.500	.750	12.70	19.05
LO	.120 BSC		3.05 BSC	
LS	.100 BSC		2.54 BSC	
MHD	.140	.150	3.56	3.81
MHO	.527	.537	13.39	13.63
TL	.645	.665	16.38	16.89
TT	.035	.045	0.89	1.14
TW	.410	.420	10.41	10.67
Term 1	Base			
Term 2	Collector			
Term 3	Emitter			

NOTES:
1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. All terminals are isolated from case.
4. Methods used for electrical isolation of the terminals feedthroughs shall employ materials that contain a minimum of 90 percent AL2O3 (ceramic).
5. In accordance with ASME Y14.5M, diameters are equivalent to ϕx symbology.

FIGURE 3. Physical dimensions, 2N3902T3, 2N5157T3 (TO-257AA).

2. APPLICABLE DOCUMENTS

* 2.1 General. The documents listed in this section are specified in sections 3 and 4 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections 3 and 4 of this specification, whether or not they are listed.

2.2 Government documents.

2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATIONS

MIL-PRF-19500 - Semiconductor Devices, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-750 - Test Methods for Semiconductor Devices.

* (Copies of these documents are available online at http://quicksearch.dla.mil/).

2.3 Order of precedence. Unless otherwise noted herein or in the contract, in the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 General. The individual item requirements shall be as specified in MIL-PRF-19500 and as modified herein.

3.2 Qualification. Devices furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturer's list (QML) before contract award (see 4.2 and 6.3).

3.3 Abbreviations, symbols, and definitions. Abbreviations, symbols, and definitions used herein shall be as specified in MIL-PRF-19500.

3.4 Interface and physical dimensions. The interface and physical dimensions shall be as specified in MIL-PRF-19500, figure 1 (TO-3), figure 2 (TO-254AA), and figure 3 (TO-257AA) herein.

3.4.1 Lead finish. Lead finish shall be solderable in accordance with MIL-PRF-19500, MIL-STD-750, and herein. Where a choice of lead finish is desired, it shall be specified in the acquisition document (see 6.2).

3.5 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in 1.3, 1.4 and table I herein.

3.6 Electrical test requirements. The electrical test requirements shall be as specified in table I.

3.7 Marking. Marking shall be in accordance with MIL-PRF-19500. At the option of the manufacturer, marking of the country of origin may be omitted from the body of the transistor but shall be retained on the initial container.

3.8 Workmanship. Semiconductor devices shall be processed in such a manner as to be uniform in quality and shall be free from other defects that will affect life, serviceability, or appearance.

4. VERIFICATION

4.1 Classification of inspections. The inspection requirements specified herein are classified as follows:

a. Qualification inspection (see 4.2).

b. Screening (see 4.3).

c. Conformance inspection (see 4.4 and table I).

4.2 Qualification inspection. Qualification inspection shall be in accordance with MIL-PRF-19500 and as specified herein.

4.2.1 Group E qualification. Group E inspection shall be performed for qualification or re-qualification only. In case qualification was awarded to a prior revision of the specification sheet that did not request the performance of table II tests, the tests specified in table II herein that were not performed in the prior revision shall be performed on the first inspection lot of this revision to maintain qualification.

* 4.3 Screening (JANTX and JANTXV level). Screening shall be in accordance with table E-IV of MIL-PRF-19500, and as specified herein. The following measurements shall be made in accordance with table I herein. Devices that exceed the limits of table I herein shall not be acceptable.

Screen (see table E-IV of MIL-PRF-19500)	Measurement JANTX and JANTXV only
(1) 3c	Thermal impedance (transient), method 3131 of MIL-STD-750 (see 4.3.2)
10	V_{CB} = 80 percent of maximum rated
11	h_{FE2} and I_{CEX1}
12	See 4.3.1
* 13	ΔI_{CEX1} = 100 percent of initial value or 2 μA dc, whichever is greater. Δh_{FE2} = 25 percent of initial value
* 17	For TO-254AA and TO-257AA packages: Method 1081 of MIL-STD-750 (see 4.3.3), Endpoints: Subgroup 2 of table I herein.

(1) Thermal impedance limits shall not exceed as shown in figures 7, 8, and 9. This test shall be performed anytime after temperature cycling, screen 3a, and does not need to be repeated in screening requirements.

4.3.1 Power burn-in conditions. Power burn-in conditions are as follows: T_A = room ambient as defined in the general requirements of 4.5 of MIL-STD-750; V_{CB} = 10-30 V dc, T_J = +175°C minimum.

4.3.2 Thermal impedance. The thermal impedance measurements shall be performed in accordance with method 3131 of MIL-STD-750 using the guidelines in that method for determining I_M, I_H, t_H, t_{MD}, t_{SW}, (and V_H where appropriate). The thermal impedance limit used in screen 3c of 4.3 herein and table I shall comply with the thermal impedance graph in figure 7, 8, and 9 (less than or equal to the curve value at the same t_H time) and shall be less than the process determined statistical maximum limit as outlined in method 3131.

4.3.3 Dielectric withstanding voltage.

a. Magnitude of test voltage……..900 V dc.

b. Duration of application of test voltage……..15 seconds (min).

c. Points of application of test voltage……...All leads to case (bunch connection).

d. Method of connection……..Mechanical.

e. Kilovolt-ampere rating of high voltage source…….1,200 V/1.0 mA (min).

f. Maximum leakage current……...1.0 mA.

g. Voltage ramp up time.....500 V/second.

4.4 Conformance inspection. Conformance inspection shall be in accordance with MIL-PRF-19500.

* 4.4.1 Group A inspection. Group A inspection shall be conducted in accordance with MIL-PRF-19500, and table I herein.

* 4.4.2 Group B inspection. Group B inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-VIB (JAN, JANTX, and JANTXV) of MIL-PRF-19500 and herein.

Subgroup	Method	Condition
B3	1037	V_{CB} = 10-30 V dc, $t_{on} = t_{off}$ = 3 minutes, 2,000 cycles.

* 4.4.3 Group C inspection. Group C inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-VII of MIL-PRF-19500, and as follows.

Subgroup	Method	Condition
C2	2036	Test condition A, weight = 10 pounds, t = 15 s.
C5	3131	See 4.5.2, $R_{\theta JC}$ = 1.25°C/W for 2N3902, 2N5157; $R_{\theta JC}$ = 1.0°C/W for 2N3902T1, 2N5157T1; and $R_{\theta JC}$ = 1.30°C/W for 2N3902T3 and 2N5157T3.
C6	1037	V_{CB} = 10-30 V dc, $t_{on} = t_{off}$ = 3 minutes, 6,000 cycles.

* 4.4.4 Group E inspection. Group E inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-IX of MIL-PRF-19500 and as specified in table II herein.

4.5 Method of inspection. Methods of inspection shall be as specified in the appropriate tables and as follows:

4.5.1 Pulse measurements. Conditions for pulse measurement shall be as specified in section 4 of MIL-STD-750.

4.5.2 Thermal resistance. The thermal resistance measurements shall be performed in accordance with method 3131 of MIL-STD-750 using the guidelines in that method for determining I_M, I_H, t_H, t_{SW} (and V_H where appropriate). Measurement delay time (t_{MD}) = 70 μs max. See MIL-PRF-19500, table E-IX, group E, subgroup 4.

TABLE I. Group A inspection.

Inspection 1/ 2/	MIL-STD-750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
Subgroup 1						
Visual and mechanical examination	2071					
Subgroup 2						
Thermal impedance 3/	3131	See 4.3.2	$Z_{\theta JX}$			°C/W
Collector to emitter cutoff current	3041	V_{BE} = -1.5 V dc; V_{CE} = 700 V dc	I_{CEX1}		20	µA dc
Emitter to base cutoff current	3061	Bias condition D	I_{EBO1}			
2N3902, 2N3902T1, 2N3902T3		V_{EB} = 5.0 V dc			200	µA dc
2N5157, 2N5157T1, 2N5157T3		V_{EB} = 6.0 V dc			200	µA dc
Collector to emitter cutoff current	3041	Bias condition D	I_{CEO}			
2N3902, 2N3902T1, 2N3902T3		V_{CE} = 400 V dc			100	µA dc
2N5157, 2N5157T1, 2N5157T3		V_{CE} = 500 V dc			100	µA dc
Base emitter voltage (saturated)	3066	Test condition A; I_C = 1.0 A dc; I_B = 0.1 A dc; pulsed (see 4.5.1)	$V_{BE(SAT)1}$		1.5	V dc
Base emitter voltage (saturated)	3066	Test condition A; I_C = 3.5 A dc; I_B = 0.7 A dc; pulsed (see 4.5.1)	$V_{BE(SAT)2}$		2.0	V dc
Collector to emitter saturated voltage	3071	I_C = 1.0 A dc; I_B = 0.1 A dc; pulsed (see 4.5.1)	$V_{CE(sat)1}$		0.8	V dc
Collector to emitter saturated voltage	3071	I_C = 3.5 A dc; I_B = 0.7 A dc; pulsed (see 4.5.1)	$V_{CE(sat)2}$		2.5	V dc
Forward-current transfer ratio	3076	V_{CE} = 5.0 V dc; I_C = 0.5 A dc; pulsed (see 4.5.1)	h_{FE1}	25		

See footnotes at end of table.

TABLE I. Group A inspection – Continued.

Inspection 1/ 2/	MIL-STD-750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
Subgroup 2 – Continued						
Forward-current transfer ratio	3076	V_{CE} = 5.0 V dc; I_C = 1.0 A dc; pulsed (see 4.5.1)	h_{FE2}	30	90	
Forward-current transfer ratio	3076	V_{CE} = 5.0 V dc; I_C = 2.5 A dc; pulsed (see 4.5.1)	h_{FE3}	10		
Forward-current transfer ratio	3076	V_{CE} = 5.0 V dc; I_C = 3.5 A dc; pulsed (see 4.5.1)	h_{FE4}	5		
Collector to emitter sustaining voltage		I_C = 100 mA dc	$V_{CEO(SUS)}$			
2N3902, 2N3902T1, 2N3902T3				325		V dc
2N5157, 2N5157T1, 2N5157T3				400		V dc
Subgroup 3						
High-temperature operation:		T_A = +150°C				
Collector to emitter cutoff current	3041	Bias condition A; V_{BE} = -1.5 V dc	I_{CEX2}			
2N3902, 2N3902T1, 2N3902T3		V_{CE} = 400 V dc			300	µA dc
2N5157, 2N5157T1, 2N5157T3		V_{CE} = 500 V dc			300	µA dc
Low-temperature operation:		T_A = -55°C				
Forward-current transfer ratio	3076	V_{CE} = 5.0 V dc; I_C = 1.0 A dc; pulsed (see 4.5.1)	h_{FE5}	10		

See footnotes at end of table.

TABLE I. Group A inspection – Continued.

Inspection 1/ 2/	MIL-STD-750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
Subgroup 4						
Pulse response	3251	Test condition A, except test circuit and pulse requirements in accordance with figure 10 herein.				
Turn-on time		V_{CC} = 125 V dc; I_C = 1.0 A dc; I_{B1} = 0.1 A dc	t_{on}		0.8	µs
Turn-off time		V_{CC} = 125 V dc; I_C = 1.0 A dc; I_{B1} = 0.1 A dc; $-I_{B2}$ = 0.50 A dc	t_{off}		1.7	µs
Small-signal short-circuit forward-current transfer ratio	3306	V_{CE} = 10 V dc; I_C = 0.2 A dc; f = 1 MHz	$\|h_{fe}\|$	2.5	25	
Open circuit output capacitance	3236	V_{CB} = 10 V dc; I_E = 0; 100 kHz ≤ f ≤ 1 MHz	C_{obo}		250	pF
Subgroup 5						
Safe operating area (continuous dc)	3051	T_C = +25°C; t ≥ 1 s; (see figure 11)				
Test 1		V_{CE} = 28.6 V dc; I_C = 3.5 A dc				
Test 2		V_{CE} = 70 V dc; I_C = 1.43 A dc				
Test 3						
2N3902, 2N3902T1, 2N3902T3		V_{CE} = 325 V dc; I_C = 55 mA dc				
2N5157, 2N5157T1, 2N5157T3		V_{CE} = 400 V dc; I_C = 35 mA dc				

See footnotes at end of table.

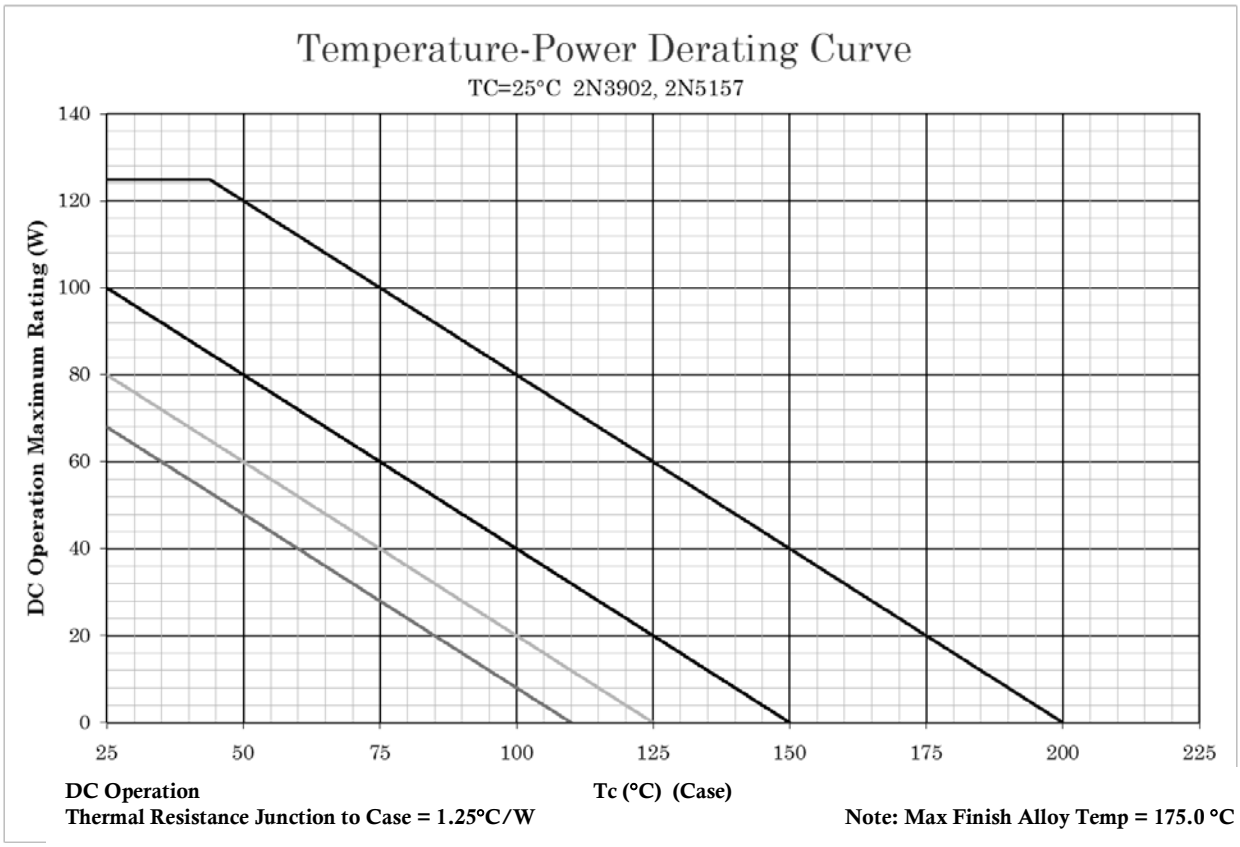
TABLE I. Group A inspection – Continued.

Inspection 1/ 2/	MIL-STD-750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
Subgroup 5 continued						
Safe operating area (switching)	3053	Load condition C (unclamped inductive load) (see figures 11 and 12), T_C = +25°C; duty cycle ≤ 10 percent, R_S = 0.1 Ω (see 4.5.1)				
Test 1		t_p approximately 3 ms (vary to obtain I_C); R_{BB1} = 20 Ω; V_{BB1} = 10 V dc; R_{BB2} = 3 kΩ; V_{BB2} = 1.5 V dc; I_C = 3.5 A dc, V_{CC} = 50 V dc; L = 60 mH; R = 3 Ω; R_L ≤ 14 Ω.				
Test 2		t_p approximately 3 ms (vary to obtain I_C); R_{BB1} = 100 Ω; V_{BB1} = 10 V dc; R_{BB2} = 3 kΩ; V_{BB2} = 1.5 V dc; I_C = 0.6 A dc; V_{CC} = 50 V dc; L = 200 mH; R = 8 Ω; R_L ≤ 83 Ω.				
Safe operating area (switching)	3053	Clamped inductive load (see figures 11, 12, and 13); T_C = +25°C; duty cycle ≤ 10 percent; t_p = approximately 30 ms (vary to obtain I_C); R_S = 0.1 Ω; R_{BB1} = 20 Ω; V_{BB1} = 10 V dc; R_{BB2} = 100 ohms; V_{BB2} = 1.5 V dc; V_{CC} = 50 V dc; I_C = 3.5 A dc; (see figure 11); R_L ≥ 0 Ω; L = 60 mH; R = 3 Ω A suitable clamping circuit or diode can be used (see 4.5.1).				
2N3902, 2N3902T1, 2N3902T3		Clamp voltage = 400 +0, -5 V dc				
2N5157, 2N5157T1, 2N5157T3		Clamp voltage = 500 +0, -5 V dc (clamped voltage must be reached)				
Electrical measurements		See table I, subgroup 2				

1/ For sampling plan, see MIL-PRF-19500.
2/ Electrical characteristics and tests in this table apply to all package styles.
* 3/ For end-point measurements, this test is required for the following subgroups:
Group B, subgroups 2 and 3 (JAN, JANTX and JANTXV).
Group C, subgroups 2 and 6.
Group E, subgroup 1.

TABLE II. Group E inspection (all quality levels) for qualification and re-qualification only.

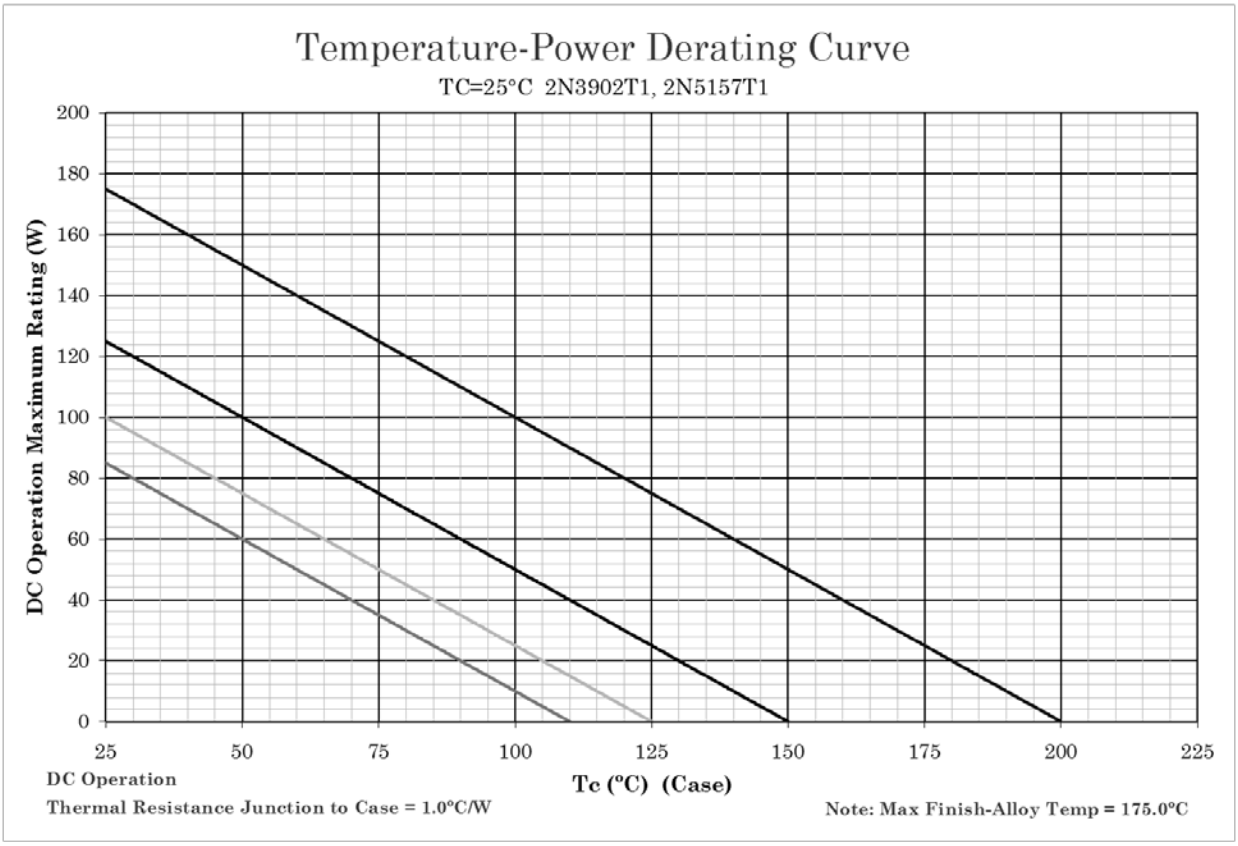
Inspection	MIL-STD-750		Sample plan
	Method	Conditions	
Subgroup 1			45 devices c = 0
Temperature cycling	1051	500 cycles minimum.	
Hermetic seal Fine leak Gross leak	1071		
Electrical measurements		See table I, subgroup 2 herein.	
Subgroup 2			45 devices c = 0
Blocking life	1048	Test temperature = +125°C; V_{CB} = 80 percent of rated; t = 1,000 hours.	
Electrical measurements		See table I, subgroup 2 herein.	
Subgroup 4			Sample size N/A
Thermal impedance curves		See MIL-PRF-19500.	
Subgroup 5			15 devices c = 0
Barometric pressure	1001	Condition C; see 1.3.	
Subgroup 8			45 devices c = 0
Reverse stability	1033	Condition A.	



NOTES:

1. Top curve is thermal runaway loci and cannot be used as a derate design curve since it exceeds the maximum ratings for this part. Operating under this curve using these mounting conditions assures the device will not have a thermal runaway. This is the true inverse of the worst case thermal resistance value extrapolated out to the thermal runaway point.
2. Derate design curve constrained by the maximum junction temperature ($T_J \leq +200°C$) and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at $T_J \leq +150°C$, where the maximum temperature of electrical test is performed.
4. Derate design curves chosen at $T_J \leq +125°C$, and +110°C to show power rating where most users want to limit T_J in their application.

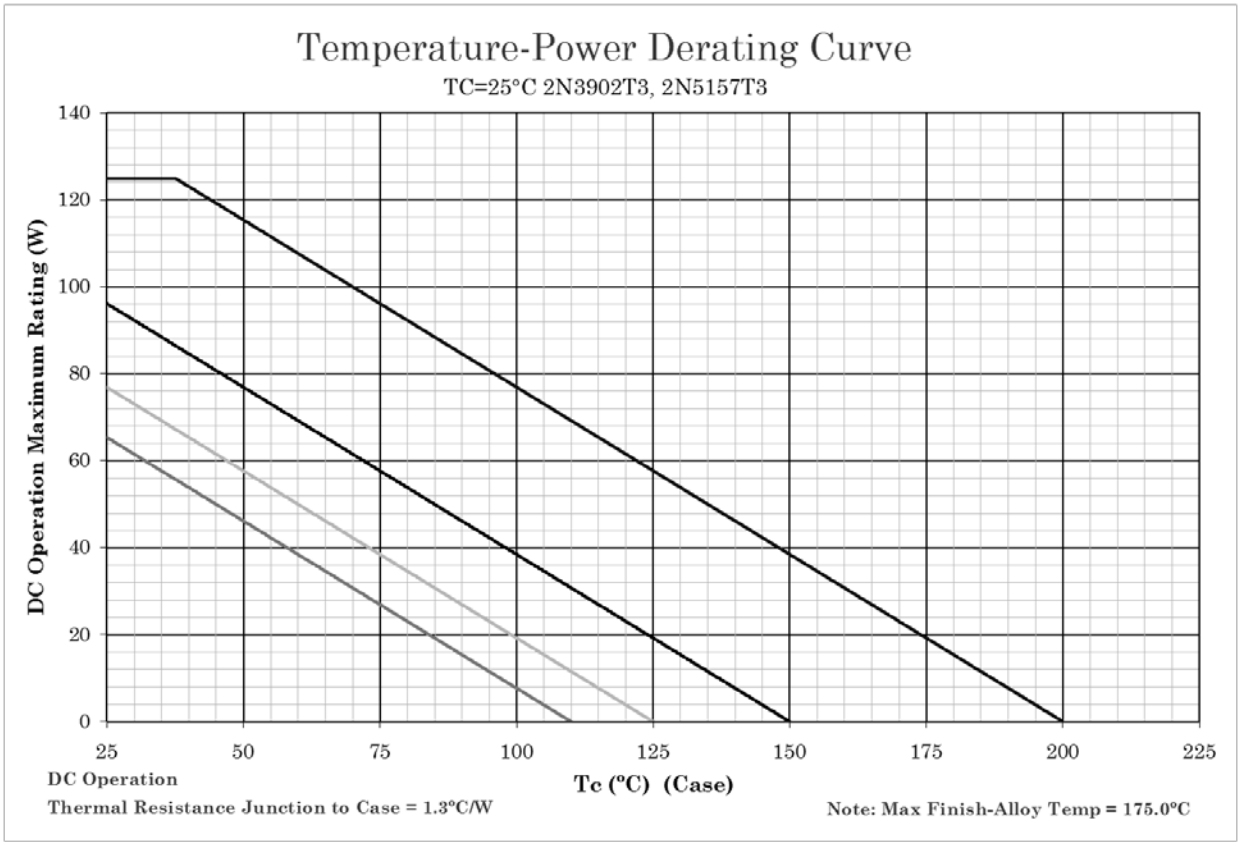
FIGURE 4. Temperature-power derating graph (TO-3), 2N3902 and 2N5157.



NOTES:

1. Top curve is thermal runaway loci and cannot be used as a derate design curve since it exceeds the maximum ratings for this part. Operating under this curve using these mounting conditions assures the device will not have a thermal runaway. This is the true inverse of the worst case thermal resistance value extrapolated out to the thermal runaway point.
2. Derate design curve constrained by the maximum junction temperature ($T_J \leq +200°C$) and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at $T_J \leq +150°C$, where the maximum temperature of electrical test is performed.
4. Derate design curves chosen at $T_J \leq +125°C$, and +110°C to show power rating where most users want to limit T_J in their application.

FIGURE 5. Temperature-power derating graph (TO-254), 2N3902T1 and 2N5157T1.

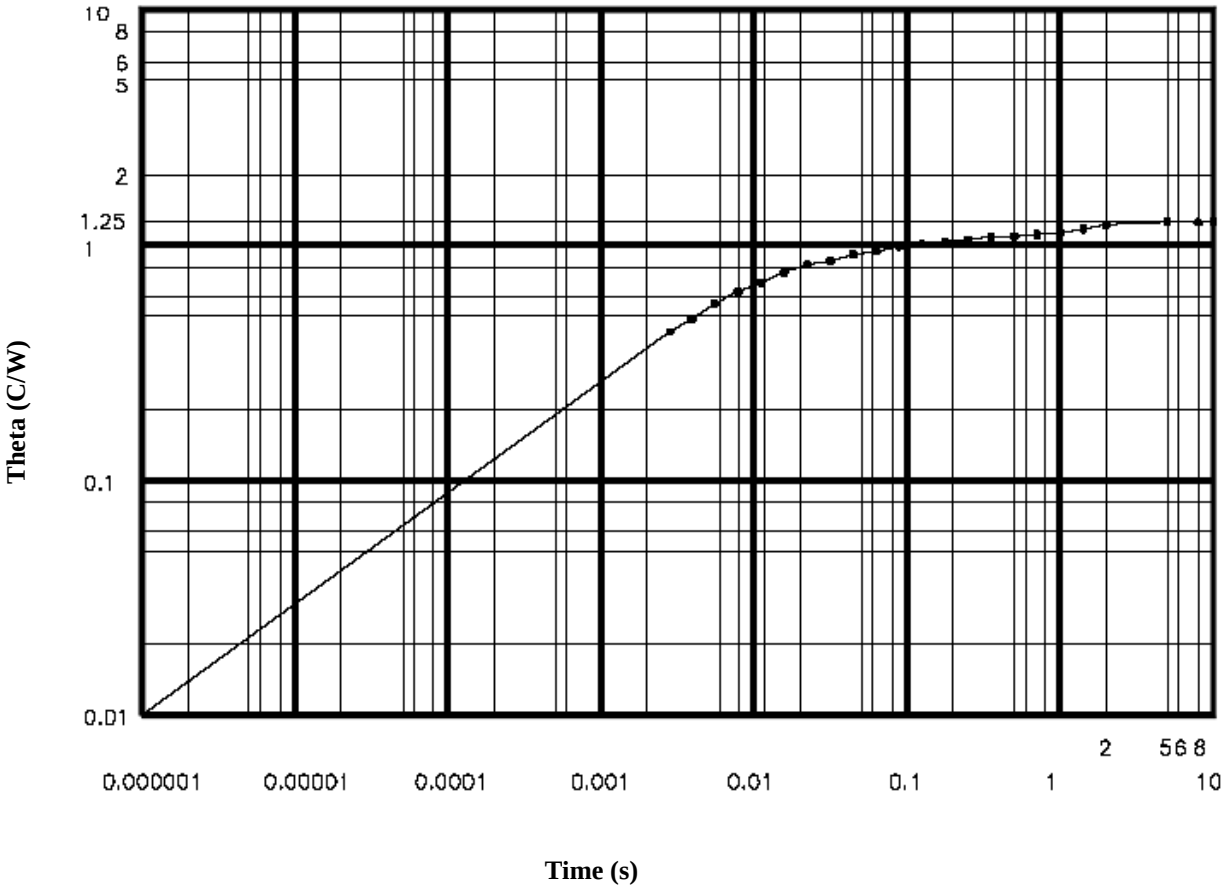


NOTES:

1. Top curve is thermal runaway loci and cannot be used as a derate design curve since it exceeds the maximum ratings for this part. Operating under this curve using these mounting conditions assures the device will not have a thermal runaway. This is the true inverse of the worst case thermal resistance value extrapolated out to the thermal runaway point.
2. Derate design curve constrained by the maximum junction temperature ($T_J \leq +200°C$) and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at $T_J \leq +150°C$, where the maximum temperature of electrical test is performed.
4. Derate design curves chosen at $T_J \leq +125°C$, and +110°C to show power rating where most users want to limit T_J in their application.

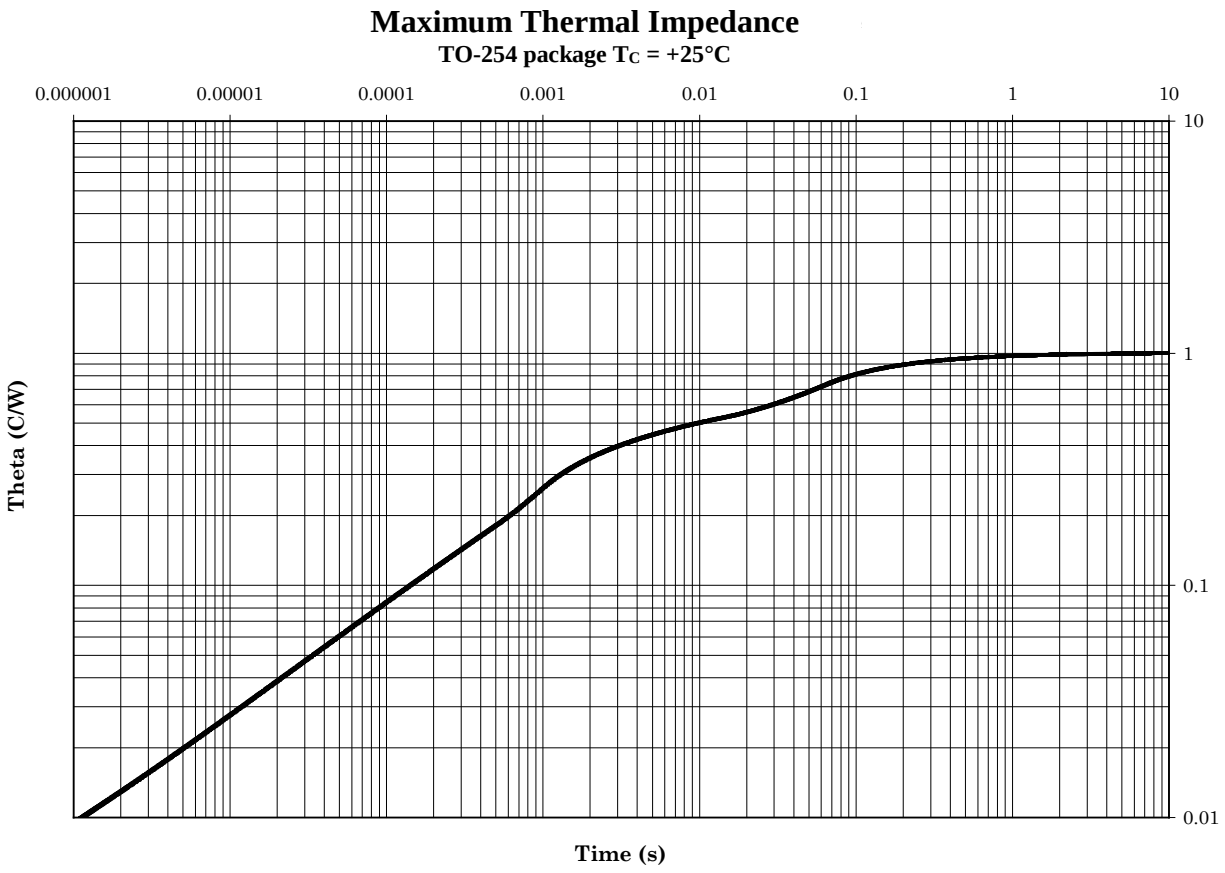
FIGURE 6. Temperature-power derating graph (TO-257), 2N3902T3 and 2N5157T3.

Maximum Thermal Impedance
TO-3 package T_C = +25°C



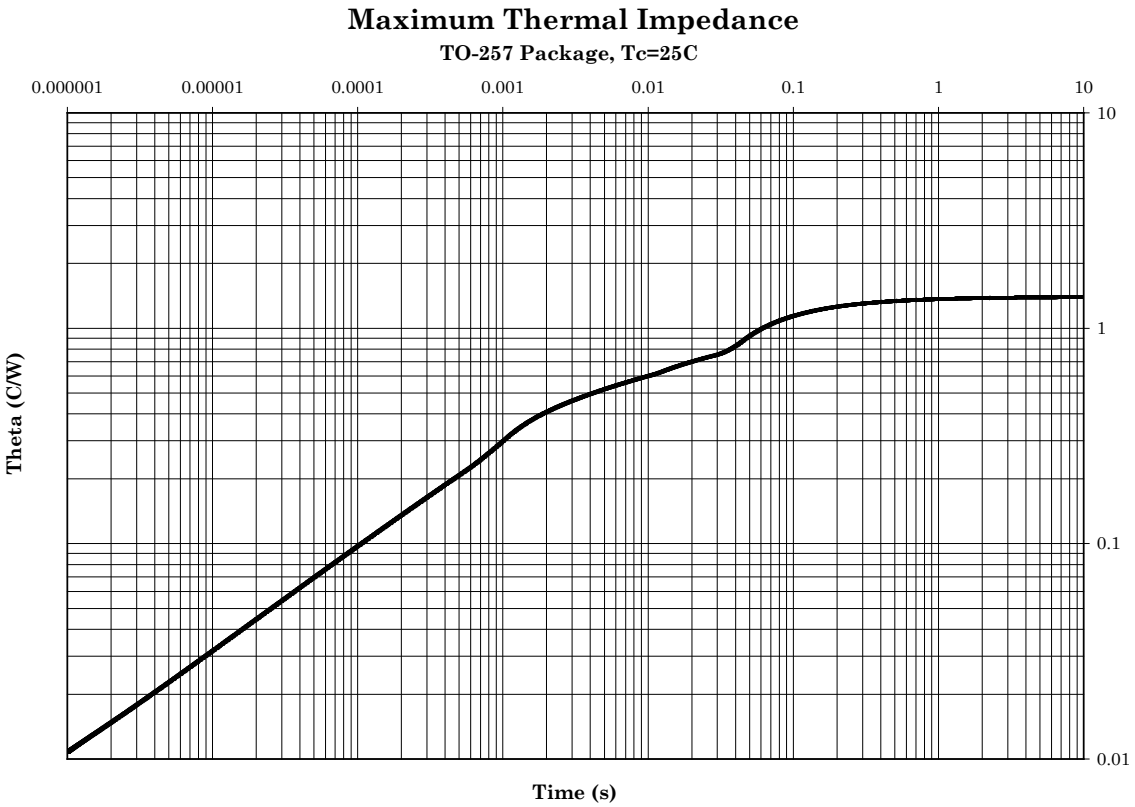
$R_{\theta JC}$ = 1.25°C/W max.

FIGURE 7. Thermal impedance graph (2N3902 and 2N5157).



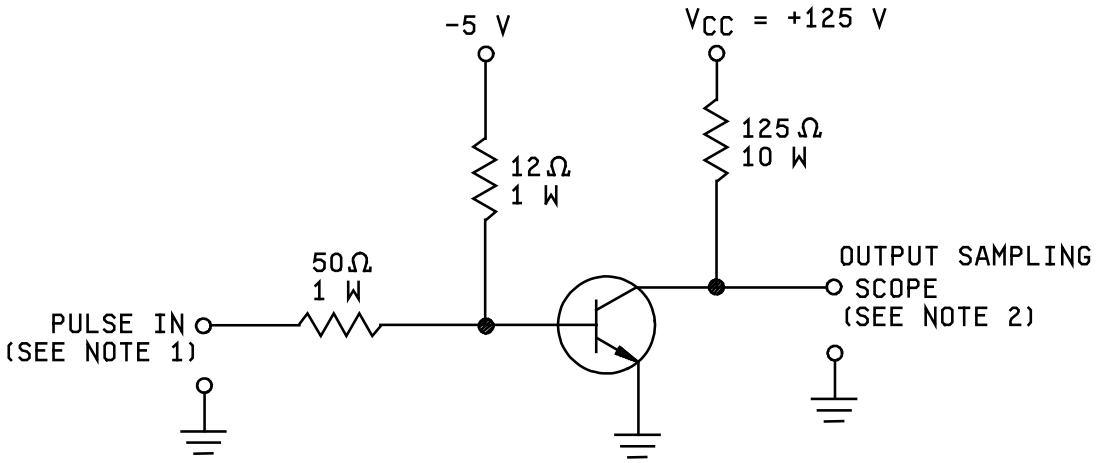
$R_{\theta JC}$ = 1.0°C/W max.

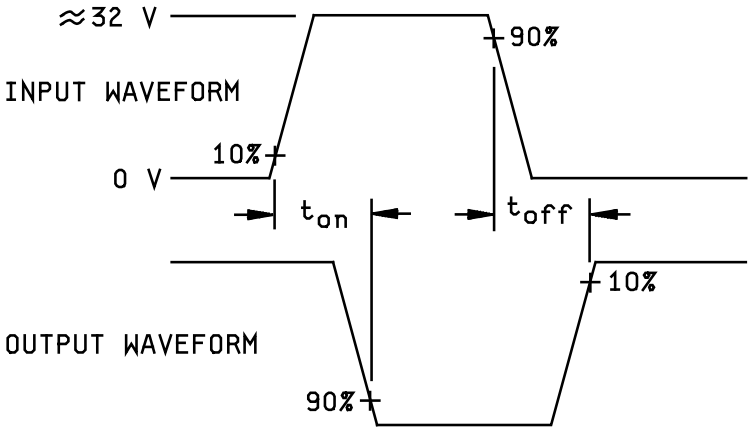
FIGURE 8. Thermal impedance graph (2N3902T1 and 2N5157T1).



$R_{\theta JC}$ = 1.3°C/W max.

FIGURE 9. Thermal impedance graph (2N3902T3, and 2N5157T3).





NOTES:

1. The rise time (t_r) and fall time (t_f) of the applied pulse shall be each ≤ 20 ns; duty cycle ≤ 5 percent; generator source impedance shall be 50Ω; pulse width = 5 μs.
2. Output sampling oscilloscope: Z_{in} ≥ 100 kΩ; C_{in} ≤ 50 pF; rise time ≤ 2.0 ns.

FIGURE 10. Pulse response test circuit.

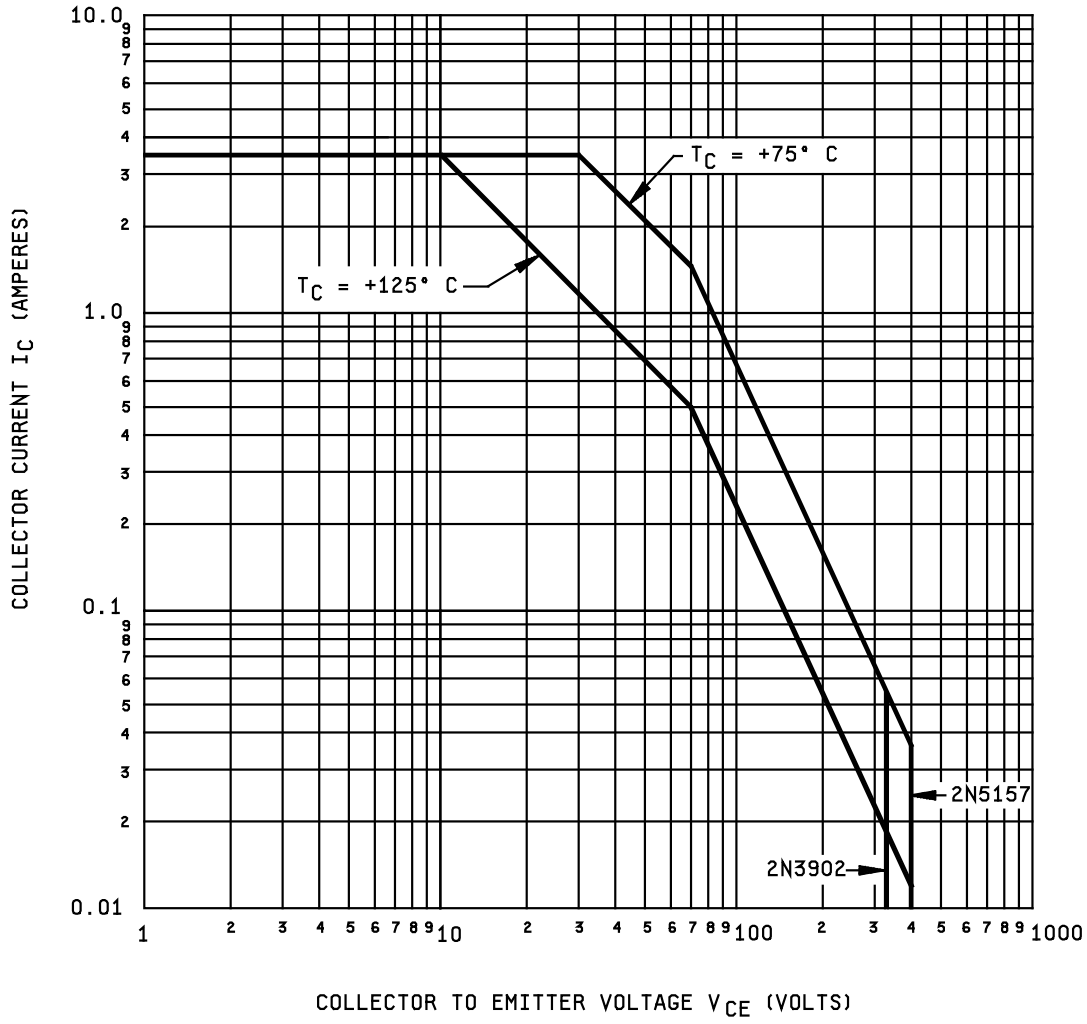


FIGURE 11. Maximum safe operating graph for all parts (continuous dc).

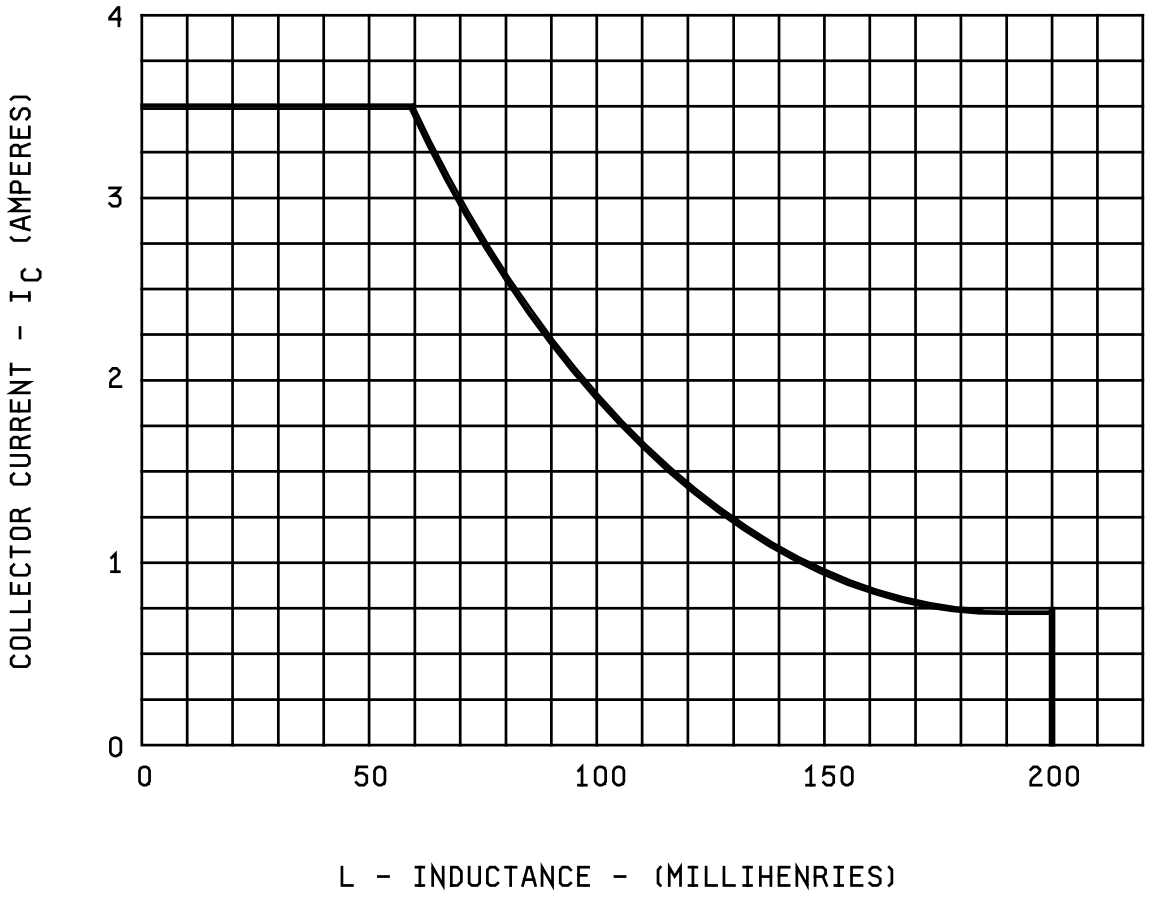


FIGURE 12. Safe operating area for switching between saturation and cutoff for all parts (unclamped inductive load).

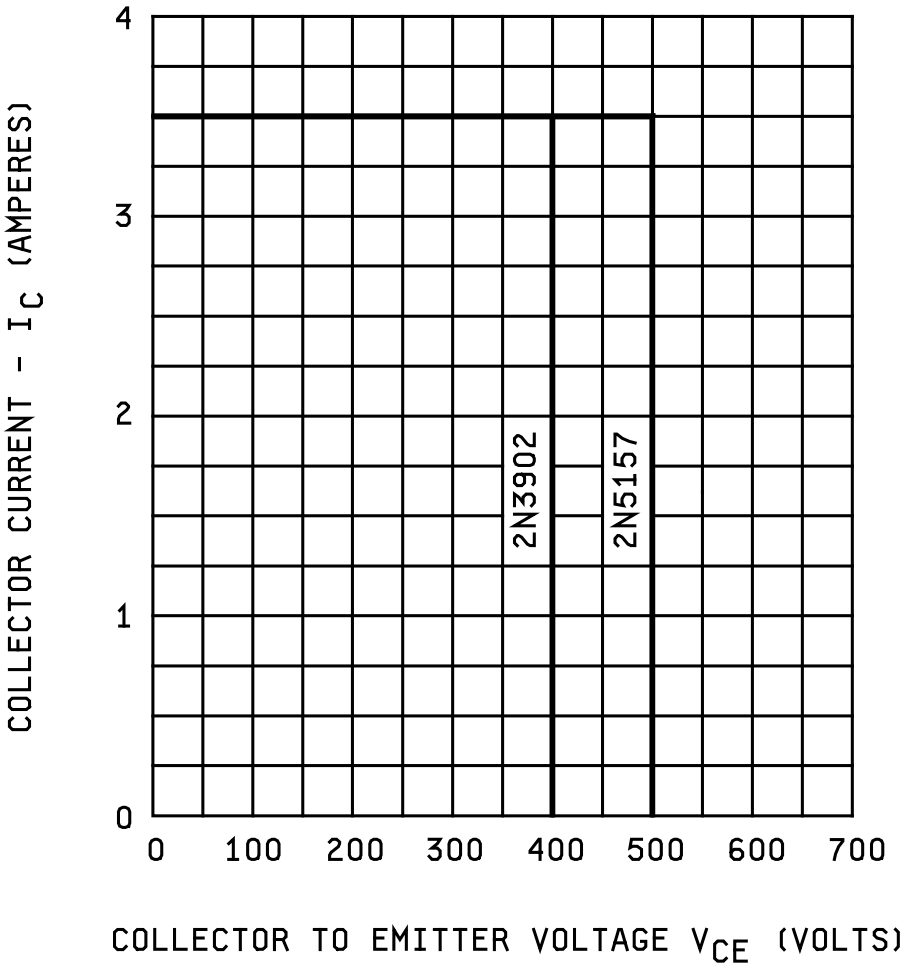


FIGURE 13. Safe operating area for switching between saturation and cutoff for all parts (clamped inductive load).

5. PACKAGING

5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activities within the Military Service or Defense Agency, or within the Military Service's system commands. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory. The notes specified in MIL-PRF-19500 are applicable to this specification.)

6.1 Intended use. Semiconductors conforming to this specification are intended for original equipment design applications and logistic support of existing equipment.

6.2 Acquisition requirements. Acquisition documents should specify the following:

a. Title, number, and date of this specification.

b. Packaging requirements (see 5.1).

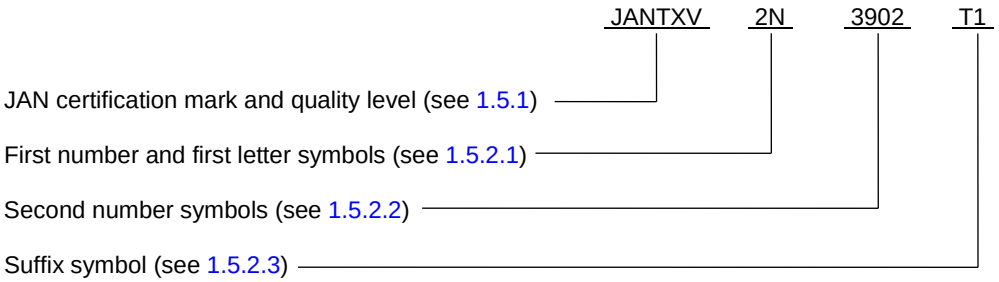
c. Lead finish (see 3.4.1).

* d. The complete PIN, see 1.5 and 6.5.

* 6.3 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers List (QML 19500) whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from DLA Land and Maritime, ATTN: VQE, P.O. Box 3990, Columbus, OH 43218-3990 or e-mail vqe.chief@dla.mil. An online listing of products qualified to this specification may be found in the Qualified Products Database (QPD) at http://qpldocs.dla.mil.

* 6.4 PIN construction example.

* 6.4.1 Encapsulated devices The PINs for encapsulated devices are constructed using the following form.



* 6.5 List of PINs. The following is a list of possible PINs available on this specification sheet.

PINs for types2N3902	PINs for types 2N5157
JAN2N3902	JAN2N5157
JAN2N3902T1	JAN2N5157T1
JAN2N3902T3	JAN2N5157T3
JANTX2N3902	JANTX2N5157
JANTX2N3902T1	JANTX2N5157T1
JANTX2N3902T3	JANTX2N5157T3
JANTXV2N3902	JANTXV2N5157
JANTXV2N3902T1	JANTXV2N5157T1
JANTXV2N3902T3	JANTXV2N5157T3

* 6.6 Request for new types and configurations. Requests for new device types or configurations for inclusions in this specification sheet should be submitted to: DLA Land and Maritime, ATTN: VAC, Post Office Box 3990, Columbus, OH 43218-3990 or by electronic mail at Semiconductor@dla.mil or by facsimile (614) 692-6939 or DSN 850-6939.

6.7 Changes from previous issue. The margins of this specification are marked with asterisks to indicate where changes from the previous issue were made. This was done as a convenience only and the Government assumes no liability whatsoever for any inaccuracies in these notations. Bidders and contractors are cautioned to evaluate the requirements of this document based on the entire content irrespective of the marginal notations and relationship to the last previous issue.

Custodians:
Army - CR
Navy - EC
Air Force - 85
NASA - NA
DLA - CC

Review activities:
Air Force - 19, 99
Navy - AS, MC

Preparing activity:
DLA - CC

(Project: 5961-2018-060)

NOTE: The activities listed above were interested in this document as of the date of this document. Since organizations and responsibilities can change, you should verify the currency of the information above using the ASSIST Online database at https://assist.dla.mil.