The documentations and process conversion measures necessary to comply with this revision shall be completed by 14 August 2014.

INCH-POUND

MIL-PRF-19500/711A
14 May 2014
MIL-PRF-19500/711
6 June 2003

PERFORMANCE SPECIFICATION

SEMICONDUCTOR DEVICE, FIELD EFFECT
TRANSISTORS, N-CHANNEL, SILICON TYPES 2N7541T3, 2N7542U3, 2N7543T3 AND 2N7544U3
JAN, JANTX, JANTXV, JANHC AND JANKC

This specification is approved for use by all Departments and Agencies of the Department of Defense.

The requirements for acquiring the product described herein shall consist of this specification sheet and MIL-PRF-19500.

1. SCOPE

1.1 Scope. This specification covers the performance requirements for an N-channel, enhancement-mode, MOSFET power transistor. Four levels of product assurance are provided for each packaged device type and two levels of product assurance are provided for each unpackaged device type, as specified in MIL-PRF-19500, with avalanche energy maximum rating (E_{AS}) and maximum avalanche current (I_{AS}).

1.2 Physical dimensions. See figure 1, TO-257AA (T3), figure 2, SMD.5 TO-276AA (U3), figure 3 and 4 for JANHC and JANKC die dimensions.

1.3 Maximum ratings. Unless otherwise specified, T_A = +25°C.

Type (1)	P_T (1) T_C = +25°C	P_T T_A = +25°C (free air)	V_{DS}	V_{DG}	V_{GS}	I_{D1} (2) T_C = +25°C	I_{D2} T_C = +100°C	I_S	I_{DM} (3)	T_J and T_{STG}
	W	W	V dc	V dc	V dc	A dc	A dc	A dc	A(pk)	°C
2N7541T3	75	1.56	55	55	±20	18	18	18	72	-55 to +150
2N7542U3	75	1.56	55	55	±20	22	22	22	88	
2N7543T3	75	1.56	100	100	±20	18	16	18	72	
2N7544U3	75	1.56	100	100	±20	22	16	22	88	

(1) Derate linearly 0.6 W/°C for T_C > +25°C;
(2) The following formula derives the maximum theoretical I_D Limit. I_D is also limited by package and internal wires.

$$I_D = \sqrt{\frac{T_J \max - T_C}{(R_{\Theta JC}) x (R_{DS_{on}} at\, T_{Jmax})}}$$

(3) I_{DM} = 4 X I_{D1} as calculated in footnote (2).

* Comments, suggestions, or questions on this document should be addressed to DLA Land and Maritime, ATTN: VAC, P.O. Box 3990, Columbus, OH 43218-3990, or emailed to Semiconductor@dla.mil. Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at https://assist.dla.mil.

AMSC N/A

FSC 5961

1.4 Primary electrical characteristics at T_C = +25°C.

Type	Min $V_{(BR)DSS}$ V_{GS} = 0 I_D = 1.0 mA dc	$V_{GS(TH)}$ $V_{DS} \geq V_{GS}$ I_D = 1.0 mA dc		Max I_{DSS1} V_{GS} = 0 V_{DS} = 100 percent of rated V_{DS}	Max $r_{DS(ON)}$ (1) V_{GS} = 12 V dc		$R_{\theta JC}$ max	E_{AS} at I_{D1}	I_{AS}
					T_J = +25°C at I_{D2}	T_J = +150°C at I_{D2}			
	V dc	V dc		µA dc	ohm	ohm	°C/W	mJ	A
		Min	Max						
2N7541T3	55	2.0	4.0	25	0.029	0.061	1.67	160	18
2N7542U3	55	2.0	4.0	25	0.016	0.034	1.67	160	22
2N7543T3	100	2.0	4.0	25	0.058	0.122	1.67	225	16
2N7544U3	100	2.0	4.0	25	0.052	0.109	1.67	200	16

(1) Pulsed (see 4.5.1).

2. APPLICABLE DOCUMENTS

* 2.1 General. The documents listed in this section are specified in sections 3 or 4 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections 3 or 4 of this specification, whether or not they are listed.

2.2 Government documents.

* 2.2.1 The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATIONS

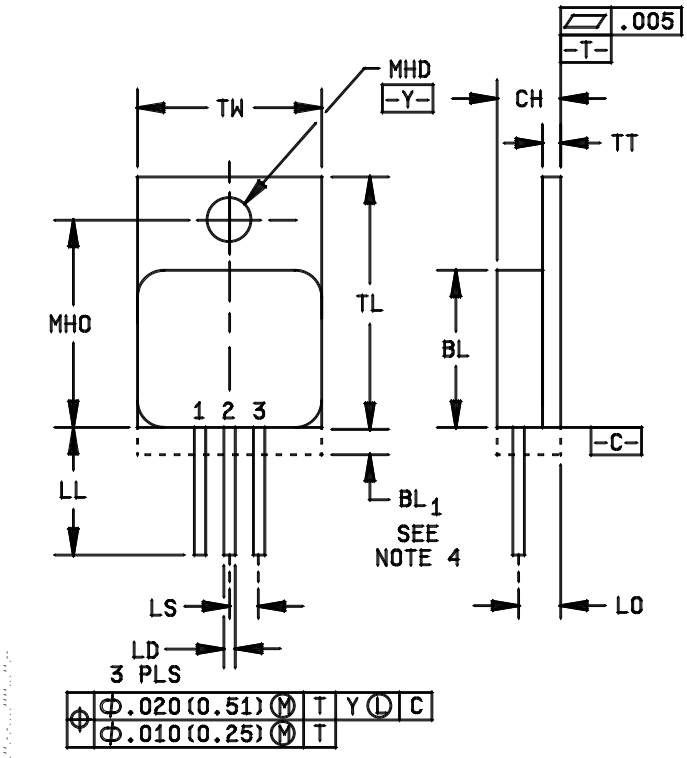
MIL-PRF-19500 - Semiconductor Devices, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-750 - Test Methods for Semiconductor Devices.

* (Copies of these documents are available online at http://quicksearch.dla.mil/

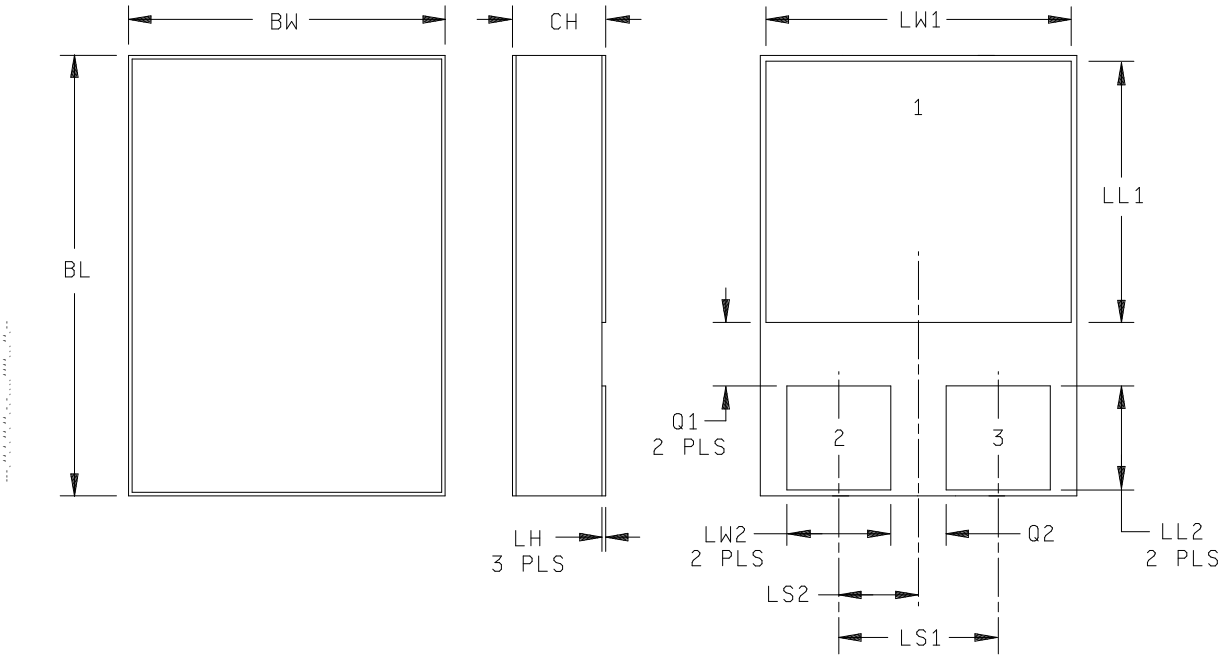
* 2.3 Order of precedence. Unless otherwise noted herein or in the contract, in the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.



Ltr	Inches		Millimeters	
	Min	Max	Min	Max
L	.410	.430	10.41	10.92
L_1		.028		0.71
H	.190	.200	4.83	5.08
D	.025	.035	0.64	0.89
L	.500	.625	12.70	15.88
O	.120 BSC		3.05 BSC	
S	.100 BSC		2.54 BSC	
HD	.140	.150	3.56	3.81
HO	.527	.537	13.39	13.64
L	.645	.665	16.38	16.89
T	.035	.045	0.89	1.14
W	.410	.420	10.41	10.67
erm 1	Drain			
erm 2	Source			
erm 3	Gate			

NOTES:
1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. All terminals are isolated from the case.
4. This area is for the lead feed-thru eyelets (configuration is optional, but will not extend beyond this zone).
5. In accordance with ASME Y14.5M, diameters are equivalent to ϕx symbology.

* FIGURE 1. Physical dimensions for TO-257AA (2N7541T3 and 2N7543T3).

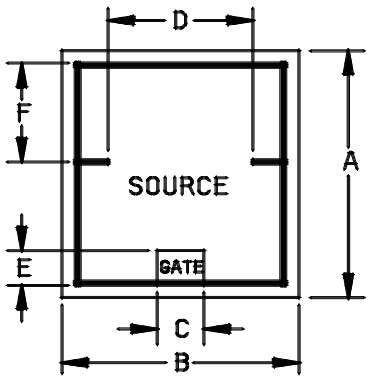


Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
BL	.395	.405	10.03	10.29
BW	.291	.301	7.39	7.65
CH	.108	.121	2.74	3.07
LH	.010	.020	0.25	0.51
LL1	.220	.230	5.59	5.84
LL2	.115	.125	2.92	3.18
LS1	.150 BSC		3.81 BSC	
LS2	.075 BSC		1.91 BSC	
LW1	.281	.291	7.14	7.39
LW2	.090	.100	2.29	2.54
Q1	.030		0.76	
Q2	.030		0.76	
Term 1	Drain			
Term 2	Gate			
Term 3	Source			

NOTES:
1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. Dimensions and tolerancing shall be in accordance with ASME Y14.5M.

* FIGURE 2. Physical dimensions for SMD.5 TO-276AA (2N7542U3 and 2N7544U3).

2N7541 OR 2N7542



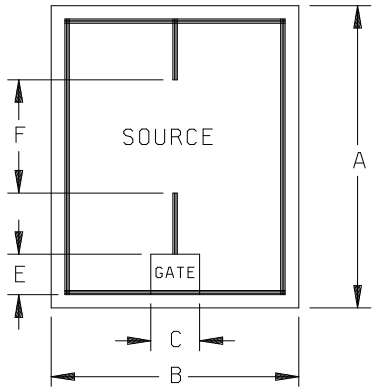
Letter	Dimensions			
	Inches		Millimeter	
	Min	Max	Min	Max
A	.142	.158	3.708	3.912
B	.126	.142	3.298	3.502
C	.024	.026	0.615	0.665
D	.076	.078	1.935	1.985
E	.0195	.0205	0.497	0.523
F	.056	.058	1.425	1.475

* NOTES:

1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. The physical characteristics of the die are:
   Back metals are Chromium, Nickel and silver.
   Top metal is Aluminum.
   Back contact is the Drain.
4. The die thickness is .0187 inch (0.474 mm), the tolerance is ±.005 inch (±0.13 mm).
5. Unless otherwise specified, tolerance is .0005 inch (0.13 mm).
6. In accordance with ASME Y14.5M, diameters are equivalent to ϕx symbology.

* FIGURE 3. JANHCA & JANKCA die dimensions.

2N7543 OR 2N7544



Letter	Dimensions			
	Inches		Millimeter	
	Min	Max	Min	Max
A	.152	.168	3.857	4.263
B	.120	.136	3.047	3.453
C	.024	.026	0.615	0.665
E	.0205	.0215	0.517	0.543
F	.059	.061	1.495	1.545

NOTES:
1. Dimensions are in inches.
2. Millimeters equivalents are given for general information only.
3. The physical characteristics of the die are:
   Back metals are Chromium, Nickel and silver.
   Top metal is Aluminum.
   Back contact is the Drain.
4. The die thickness is .0187 inch (0.474 mm), the tolerance is ±.005 inch (±0.13 mm).
5. Unless otherwise specified, tolerance is .0005 inch (0.13 mm).
6. In accordance with ASME Y14.5M, diameters are equivalent to ϕx symbology.

* FIGURE 4. JANHCB & JANKCB die dimensions.

3. REQUIREMENTS

3.1 General. The individual item requirements shall be as specified in MIL-PRF-19500 and as modified herein.

3.2 Qualification. Devices furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturer's list (QML) before contract award (see 4.2 and 6.3).

3.3 Abbreviations, symbols, and definitions. Abbreviations, symbols, and definitions used herein shall be as specified in MIL-PRF-19500.

3.4 Interface and physical dimensions. The interface and physical dimensions shall be as specified in MIL-PRF-19500 and on figures 1 (T3, TO-257AA) and 2 (U3, surface mount SMD.5 TO-276AA) herein.

3.4.1 Lead finish. Lead finish shall be solderable in accordance with MIL-PRF-19500, MIL-STD-750, and herein. Where a choice of lead finish is desired, it shall be specified in the acquisition document (see 6.2).

3.4.2 Lead material. Lead material shall be Kovar or Alloy 52 for the TO - 257AA; a copper core or plated core is permitted.

3.4.3 Internal construction. Multiple chip construction shall not be permitted to meet the requirements of this specification.

3.5 Electrostatic discharge protection. The devices covered by this specification require electrostatic discharge protection.

* 3.5.1 Handling. MOS devices must be handled with certain precautions to avoid damage due to the accumulation of static charge. The following handling procedures shall be followed:

a. Devices shall be handled on benches with conductive handling devices.

b. Ground test equipment, tools, and personnel handling devices.

c. Do not handle devices by the leads.

d. Store devices in conductive foam or carriers.

e. Avoid use of plastic, rubber, or silk in MOS areas.

f. Maintain relative humidity above 50 percent, if practical.

g. Care should be exercised, during test and troubleshooting, to apply not more than maximum rated voltage to any lead.

h. Gate must be terminated to source, $R \leq 100$ k, whenever bias voltage is to be applied drain to source.

3.6 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.7 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table I herein.

3.8 Marking. Marking shall be in accordance with MIL-PRF-19500. At the option of the manufacturer, marking may be omitted from the body, but shall be retained on the initial container.

3.9 Workmanship. Semiconductor devices shall be processed in such a manner as to be uniform in quality and shall be free from other defects that will affect life, serviceability, or appearance.

4. VERIFICATION

4.1 Classification of inspections. The inspection requirements specified herein are classified as follows:

a. Qualification inspection (see 4.2).

b. Screening (see 4.3).

c. Conformance inspection (see 4.4 and tables I and II).

4.2 Qualification inspection. Qualification inspection shall be in accordance with MIL-PRF-19500 and as specified herein.

* 4.2.1 Qualification of JANHC and JANKC die. The qualification inspection of JANHC and JANKC die shall be in accordance with MIL–PRF–19500.

* 4.2.2 Group E qualification. Group E inspection shall be performed for qualification or re-qualification only. In case qualification was awarded to a prior revision of the specification sheet that did not request the performance of table II tests, the tests specified in table II herein that were not performed in the prior revision shall be performed on the first inspection lot of this revision to maintain qualification.

* 4.3 Screening.

* 4.3.1 Screening of encapsulated devices (JANTX and JANTXV). Screening of packaged devices shall be in accordance with table E–IV of MIL–PRF–19500 and as specified herein. The following measurements shall be made in accordance with table I herein. Devices that exceed the limits of table I herein shall not be acceptable.

Screen (see table E-IV of MIL-PRF-19500) (1) (2)	Measurement
	JANTX and JANTXV level
(3)	Method 3470 of MIL-STD-750, E_{AS} (see 4.3.1.4)
(3) 3c	Method 3161 of MIL-STD-750, thermal impedance (see 4.3.1.3)
(3)	Gate stress test (see 4.3.1.5)
(1) 9	Not applicable
10	Method 1042 of MIL-STD-750, test condition B
11	Subgroup 2 of table I herein; I_{GSSF1}, I_{GSSR1}, I_{DSS1}, $r_{DS(on)1}$, $V_{GS(TH)1}$
12	Method 1042 of MIL-STD-750, test condition A, OR T_A = +175°C, t = 48 hours.
13	Subgroups 2 and 3 of table I herein; ΔI_{GSSF1} = ± 20 nA dc or ±100 percent of initial value, whichever is greater. ΔI_{GSSR1} = ± 20 nA dc or ± 100 percent of initial value, whichever is greater. ΔI_{DSS1} = ± 10 μA dc or ± 100 percent of initial value, whichever is greater. $\Delta r_{DS(on)1}$ = ± 20 percent of initial value. $\Delta V_{GS(TH)1}$= ± 20 percent of initial value.
* 17	For TO–257AA packages: Method 1081 of MIL-STD-750 (see 4.3.1.1), Endpoints: Subgroup 2 of table I herein

(1) At the end of the test program, I_{GSSF1} and I_{GSSR1} are measured.
(2) An out-of-family program to characterize I_{GSSF1} and I_{GSSR1} shall be invoked.
* (3) Shall be performed anytime after temperature cycling, screen 3a; JANTXV level does not need to be repeated in screening requirements.

* 4.3.1.1 Dielectric withstanding voltage.

a. Magnitude of test voltage……800 V dc.

b. Duration of application of test voltage……..15 seconds (min).

c. Points of application of test voltage……..All leads to case (bunch connection).

d. Method of connection……..Mechanical.

e. Kilovolt-ampere rating of high voltage source…….1,200 V/1.0 mA (min).

f. Maximum leakage current……...1.0 mA.

g. Voltage ramp up time.....500 V/second.

* 4.3.1.2 Thermal resistance. Thermal resistance measurements shall be performed in accordance with method 3161 of MIL-STD-750. The maximum limit of $R_{\theta JC(max)}$ = 1.67°C/W. The following parameter measurements shall apply:

a. Measuring current (I_M) .....10 mA.

b. Drain heating current (I_H) .....4.2 A.

c. Heating time (t_H) .....Steady-state (see method 3161 of MIL-STD-750 for definition).

d. Drain-source heating voltage (V_H).....12 V.

e. Measurement time delay (t_{MD}) .....30 μs to 60 μs.

f. Sample window time (t_{SW}).....10 μs maximum.

* 4.3.1.3 Thermal impedance. The thermal impedance measurements shall be performed in accordance with method 3161 of MIL-STD-750 using the guidelines in that method for determining I_M, I_H, t_H, t_{SW}, (and V_H where appropriate). Measurement delay time (t_{MD}) = 70 μs maximum. See table II, group E, subgroup 4 herein.

* 4.3.1.4 Single pulse avalanche energy (E_{AS}).

a. Peak current (I_{AS}).. ..... $I_{AS(max)}$.

b. Peak gate voltage (V_{GS}) ..... 10 V.

c. Gate to source resistor (R_{GS}) ..... $25\Omega \leq R_{GS} \leq 200\Omega$.

d. Initial case temperature (T_C) ..... +25°C +10°C, -5°C.

e. Inductance (L) ..... $\left[\frac{2E_{AS}}{(I_{D1})^2}\right]\frac{[(V_{BR}-V_{DD})]}{V_{BR}}$ *mH minimum.*

f. Number of pulses to be applied ..... 1 pulse minimum.

g. Supply voltage (V_{DD}) ..... 50 V.

* 4.3.1.5 Gate stress test.

a. V_{GS} = 24 V minimum.

b. t = 250 μs minimum.

* 4.3.2 Screening of unencapsulated die (JANHC and JANKC). Screening of JANHC and JANKC unencapsulated die shall be in accordance with appendix G of MIL–PRF–19500.

* 4.4 Conformance inspection. Conformance inspection shall be in accordance with MIL-PRF-19500, and as specified herein.

* 4.4.1 Group A inspection. Group A inspection shall be conducted in accordance with MIL-PRF-19500 and table I herein. End-point electrical measurements shall be in accordance with table I, subgroup 2 herein.

* 4.4.2 Group B inspection. Group B inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-VIB (JANTX and JANTXV) of MIL-PRF-19500, and as follows. Electrical measurements (end-points) shall be in accordance with table I, subgroup 2 herein.

4.4.2.1 Group B inspection, table E-VIB (JANTX & JANTXV) of MIL-PRF-19500.

	Subgroup	Method	Inspection
	B2	1051	Test condition G, 25 cycles. (45 total, including 20 cycles performed in screening).
*	B3	1042	Test condition D. No heat sink nor forced-air cooling on the device shall be permitted during the on cycle. The heating cycle shall be 60 seconds minimum.
*	B3	2037	Test condition D. All internal bond wires for each device shall be pulled separately.
	B4	2075	See 3.4.2 herein.
	B4	2077	Not applicable.
	B5 and B6		Not applicable.

* 4.4.3 Group C inspection. Group C inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-VII of MIL-PRF-19500 and as follows. Electrical measurements (end-points) shall be in accordance with table I, subgroup 2 herein.

	Subgroup	Method	Inspection
	C2	1056	Test condition B.
	C2	2036	Test condition A, weight = 10 lbs, t = 10 seconds (applicable to TO-257AA only).
	C2	1021	Omit initial conditioning.
	C5	3161	$R_{\theta JC}$ = 1.67 °C/W maximum. See 4.3.1.3.
*	C6	1042	Test condition D. No heat sink nor forced-air cooling on the device shall be permitted during the on cycle. The heating cycle shall be 60 seconds minimum.
*	C7	1018	

4.4.4 Group E inspection. Group E inspection shall be conducted in accordance with the conditions specified for subgroup testing in appendix E, table E-IX of MIL-PRF-19500 and as specified herein. Electrical measurements (end-points) and delta measurements shall be in accordance with table I, subgroup 2 herein.

4.5 Methods of inspection. Methods of inspection shall be as specified in the appropriate tables and as follows.

4.5.1 Pulse measurements. Conditions for pulse measurement shall be as specified in section 4 of MIL-STD-750.

TABLE I. Group A inspection.

Inspection 1/	MILSTD750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
Subgroup 1						
Visual and mechanical inspection	2071					
Subgroup 2						
Thermal impedance 2/	3161	See 4.3.1.3	$Z_{\theta JC}$			
2N7541T3, 2N7543T3					1.5	°C/W
2N7542U3, 2N7544U3					1.3	°C/W
Breakdown voltage, drain to source	3407	V_{GS} = 0 V dc, I_D = 250 µA dc, bias condition C	$V_{(BR)DSS}$			
2N7541T3, 2N7542U3				55		V dc
2N7543T3, 2N7544U3				100		V dc
Gate to source voltage (threshold)	3403	$V_{DS} \geq V_{GS}$, I_D = 250 µA dc	$V_{GS(TH)1}$	2.0	4.0	V dc
Gate reverse current	3411	V_{GS} = 20 V dc and +20 V dc, bias condition C, V_{DS} = 0	I_{GSS1}		±100	nA dc
Drain current	3413	V_{GS} = 0 V dc, bias condition C, V_{DS} = 100% of rated V_{DS}	I_{DSS1}		25	µA dc
Static drain to source onstate resistance	3421	V_{GS} = 10 V dc, condition A, pulsed (see 4.5.1), $I_D = I_{D2}$	$r_{DS(on)}1$			
2N7541T3					0.029	Ω
2N7542U3					0.016	Ω
2N7543T3					0.058	Ω
2N7544U3					0.052	Ω
Forward voltage	4011	Pulsed (see 4.5.1), $I_D = I_{D1}$, V_{GS} = 0 V dc	V_{SD}		1.3	V
Subgroup 3						
High temperature operation:		$T_C = T_J$ = +125°C				
Gate reverse current	3411	V_{GS} = 20 V dc and +20 V dc, bias condition C, V_{DS} = 0	I_{GSS2}		± 200	nA dc
Drain current	3413	V_{GS} = 0 V dc, bias condition C, V_{DS} = 80 percent of rated V_{DS}	I_{DSS2}		250	µA dc
Static drain to source on state resistance	3421	V_{GS} = 10 V dc, condition A, pulsed (see 4.5.1), $I_D = I_{D2}$	$r_{DS(on)}3$			
2N7541T3					0.052	Ω
2N7542U3					0.029	Ω
2N7543T3					0.116	Ω
2N7544U3					0.104	Ω

See footnotes at end of table.

TABLE I. Group A inspection - Continued.

Inspection 1/	MIL-STD-750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
Subgroup 3 - Continued						
Gate to source voltage (threshold)	3403	$V_{DS} \geq V_{GS}$, I_D = 250 µA dc	$V_{GS(TH)2}$	1.0		V dc
Low temperature operation:		$T_C = T_J$ = 55°C				
Gate to source voltage (threshold)	3403	$V_{DS} \geq V_{GS}$, I_D = 250 µA dc	$V_{GS(TH)3}$		5.0	V dc
Subgroup 4						
Forward transconductance	3475	I_D = rated I_{D2}, V_{DD} = 15 V (see 4.5.1)	g_{FS}			
2N7541T3, 2N7542U3				22		S
2N7543T3, 2N7544U3				11		S
Switching time test	3472	I_D = rated I_{D1}, V_{GS}= 10 V dc, R_G = 5.1Ω, V_{DD} = 50 percent of rated V_{DS}				
Turn on delay time			$t_{d(on)}$			
2N7541T3					18	ns
2N7542U3					23	ns
2N7543T3					17	ns
2N7544U3					24	ns
Rise time			t_r			
2N7541T3					78	ns
2N7542U3					141	ns
2N7543T3					83	ns
2N7544U3					125	ns
Turn-off delay time			$t_{d(off)}$			
2N7541T3					55	ns
2N7542U3					60	ns
2N7543T3					61	ns
2N7544U3					86	ns
Fall time			t_f			
2N7541T3					63	ns
2N7542U3					98	ns
2N7543T3					51	ns
2N7544U3					82	ns
Subgroup 5						
Safe operating area test (high voltage)	3474	See figures 6 and 7; t_p = 10 ms, V_{DS} = 80 percent of rated V_{DS}				
Electrical measurements		See table I, subgroup 2 herein.				

See footnotes at end of table.

TABLE I. Group A inspection - Continued.

Inspection 1/	MIL-STD-750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
Subgroup 6						
Not applicable						
Subgroup 7						
Gate charge	3471	Condition B	$Q_{G(on)}$			
2N7541T3					45	nC
2N7542U3					101	nC
2N7543T3 and 2N7544U3					104	nC
On-state gate charge			Q_{GS}			
2N7541T3					16	nC
2N7542U3					19	nC
2N7543T3 and 2N7544U3					20	nC
Gate to drain charge			Q_{GD}			
2N7541T3					34	nC
2N7542U3					41	nC
2N7543T3 and 2N7544U3					43	nC
Reverse recovery time	3473	Condition A, di/dt ≤ 100A/μs, $V_{DD} \leq 50$ V, $I_D = I_{D1}$	t_{rr}			
2N7541T3 and 2N7542U3					104	ns
2N7543T3 and 2N7544U3					240	ns

1/ For sampling plan, see MIL-PRF-19500.
2/ This test is required for the following end-point measurements only (not intended for screen 13): Group B, subgroups 2 and 3 (JANTXV); group C, subgroup 6; group E, subgroup 1.

* TABLE II. Group E inspection (all quality levels) for qualification only.

Inspection	MIL-STD-750		Qualification and large lot quality conformance inspection
	Method	Conditions	
Subgroup 1			45 devices c = 0
Thermal shock (temperature cycling)	1051	Test condition G, 500 cycles	
Hermetic seal Fine leak Gross leak	1071		
Electrical measurements		See table I, subgroup 2	
Subgroup 2 1/			45 devices c = 0
Steady-state reverse bias	1042	Condition B, 1,000 hours	
Electrical measurements		See table I, subgroup 2	
Steady-state gate bias	1042	Condition A, 1,000 hours	
Electrical measurements		See table I, subgroup 2	
Subgroup 4			Sample size N/A
Thermal impedance curves		See MIL-PRF-19500.	
Subgroup 5			15 devices c = 0
Not Applicable			
Subgroup 6			
ESD	1020		
Subgroup 7			22 devices c = 0
Commutating diode for safe operating area test procedure for measuring dv/dt during reverse recovery of power MOSFET transistors or insulated gate bipolar transistors	3476	Test conditions shall be derived by the manufacturer	

1/ A separate sample for each test shall be pulled.

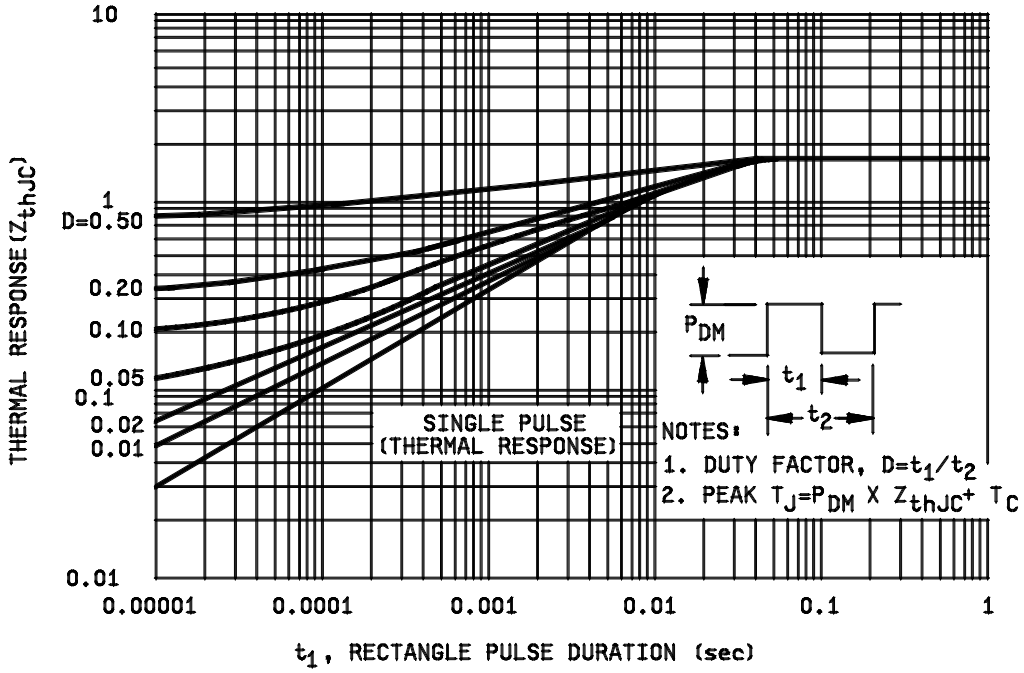


FIGURE 5. Thermal impedance curves.

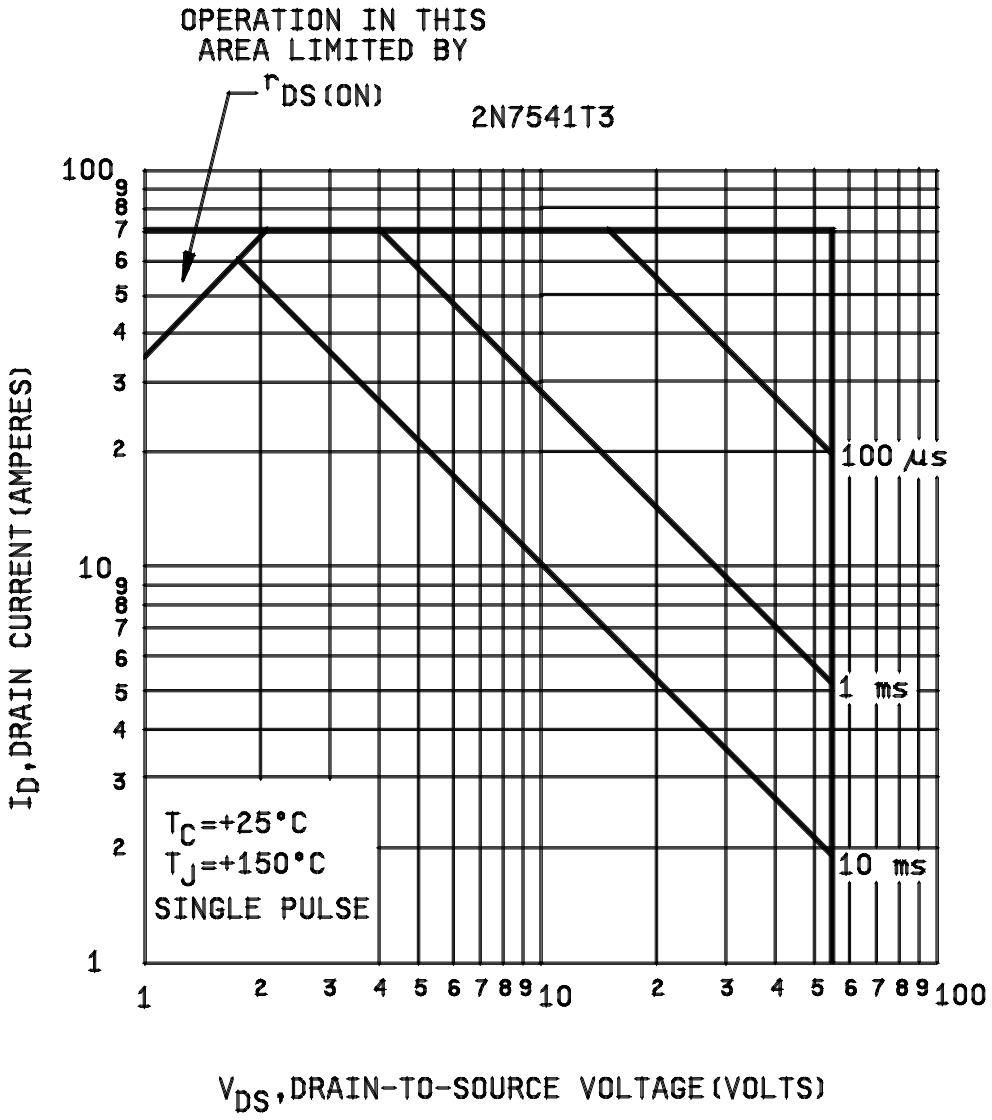


FIGURE 6. Safe operating area graph.

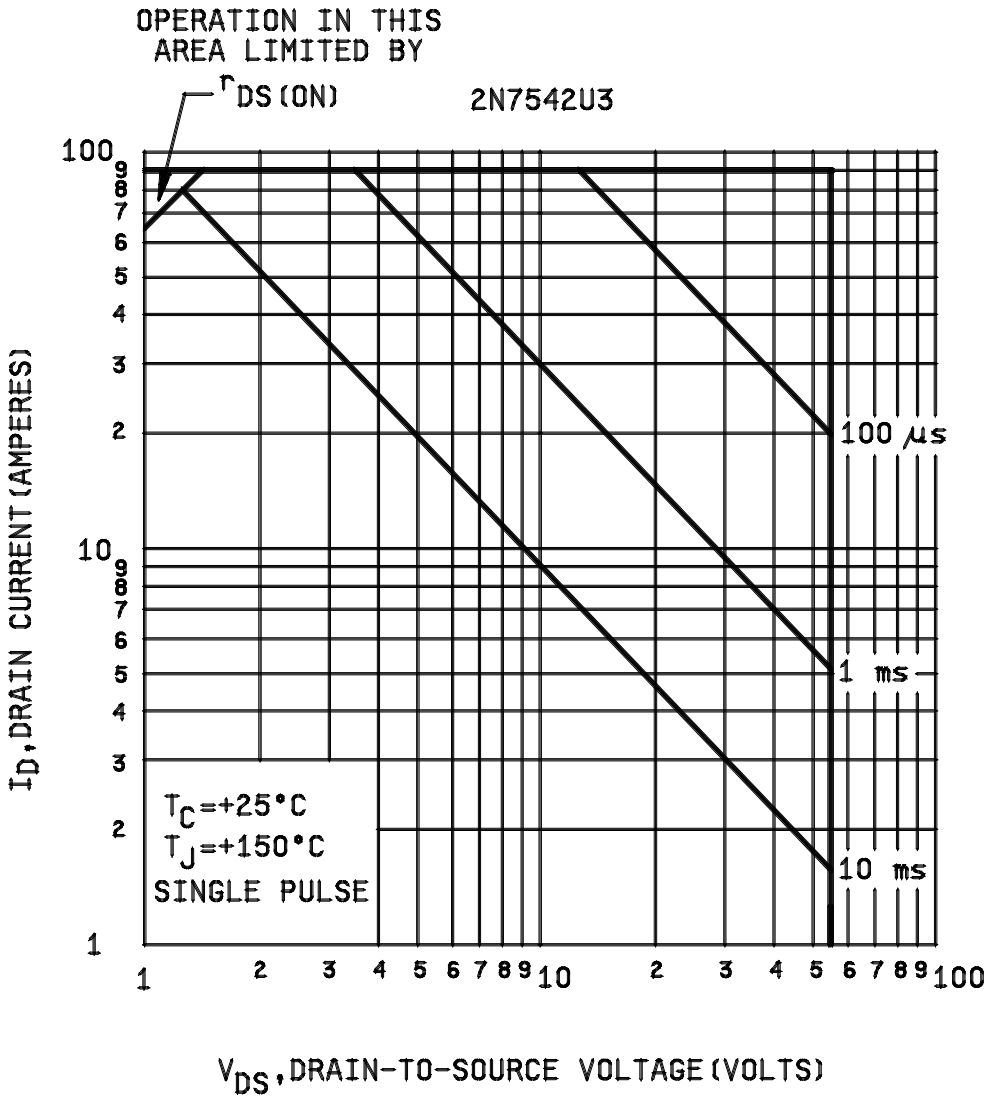


FIGURE 6. Safe operating area graph Continued.

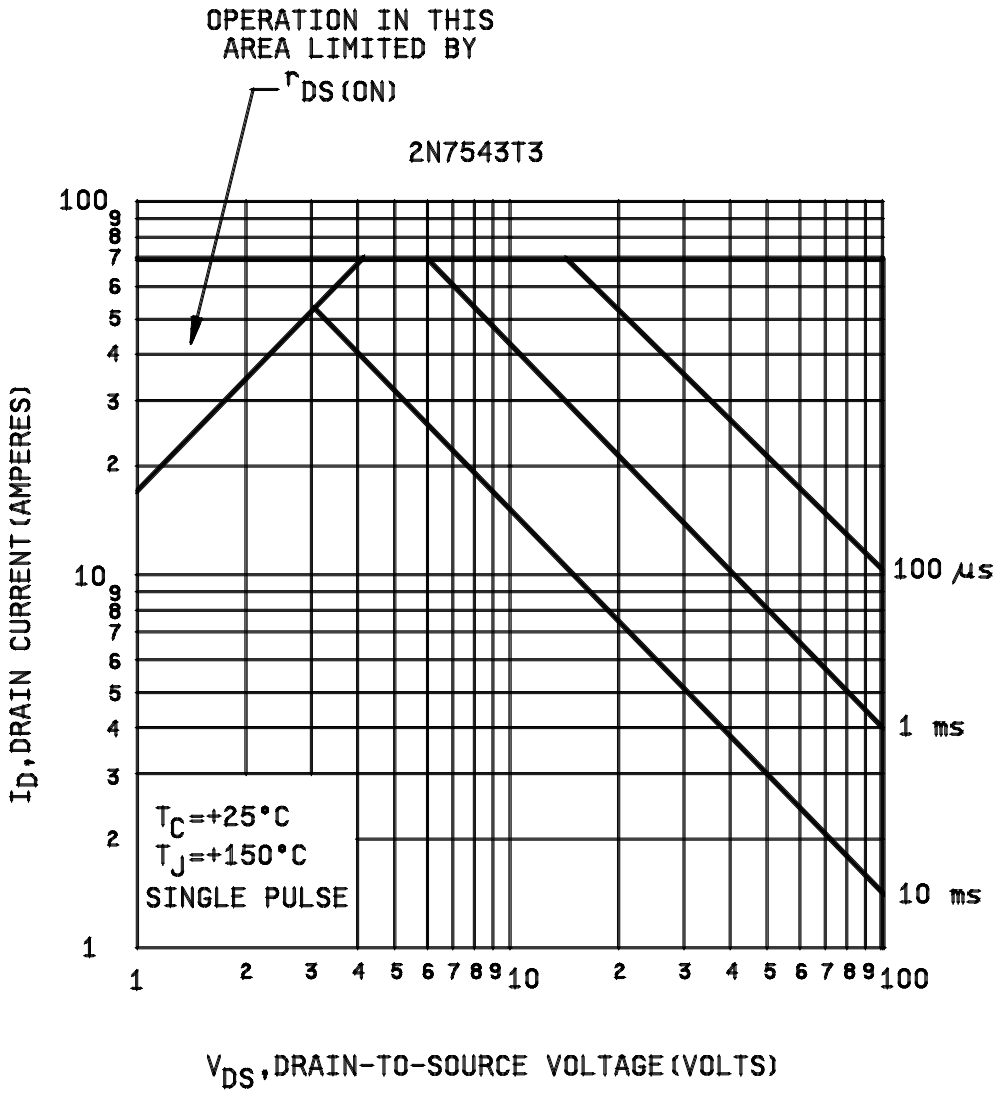


FIGURE 7. Safe operating area graph.

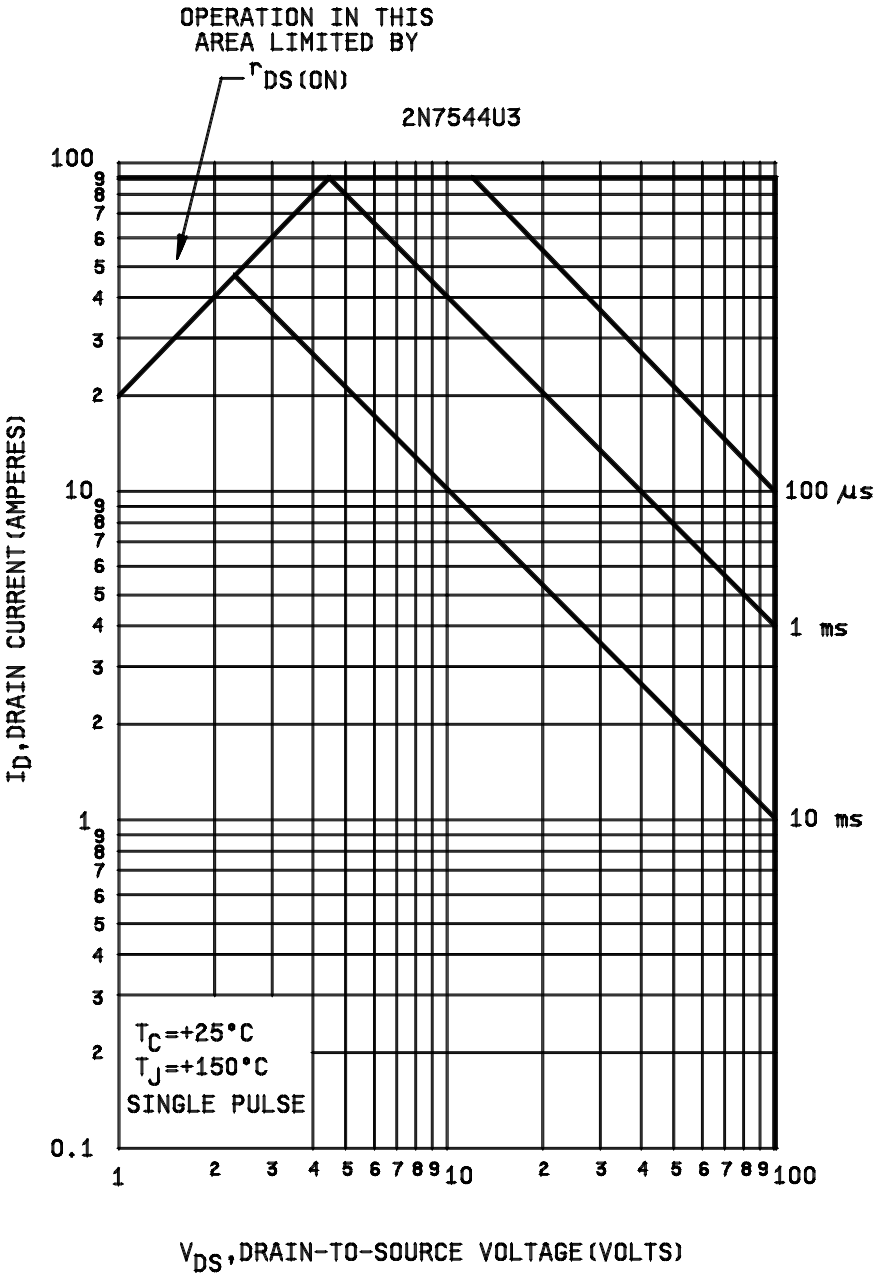


FIGURE 7. Safe operating area graph Continued.

5. PACKAGING

* 5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activities within the Military Service or Defense Agency, or within the Military Service's system commands. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

* 6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory. The notes specified in MIL-PRF-19500 are applicable to this specification.)

6.1 Intended use. Semiconductors conforming to this specification are intended for original equipment design applications and logistic support of existing equipment.

6.2 Acquisition requirements. Acquisition documents must specify the following:

a. Title, number, and date of this specification.

b. Packaging requirements (see 5.1).

c. Lead finish (see 3.4.1).

d. The complete Part or Identifying Number (PIN), see title and section 1.

* 6.3 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers List (QML 19500) whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from DLA Land and Maritime, ATTN: VQE, P.O. Box 3990, Columbus, OH 43218-3990 or e-mail vqe.chief@dla.mil. An online listing of products qualified to this specification may be found in the Qualified Products Database (QPD) at https://assist.dla.mil.

6.4 Substitution information. Devices covered by this specification are substitutable for the manufacturer's and user's Part or Identifying Number (PIN). This information in no way implies that manufacturer's PIN's are suitable for the military PIN.

Preferred types (military PIN)	Commercial PIN	
	TO-257AA	TO-276AA (SMD.5)
2N7541T3	IRF5YZ48	
2N7542U3		IRF5NJZ48
2N7543T3	IRF5Y540	
2N7544U3		IRF5NJ540

* 6.5 Changes from previous issue. The margins of this specification are marked with asterisks to indicate where changes from the previous issue were made. This was done as a convenience only and the Government assumes no liability whatsoever for any inaccuracies in these notations. Bidders and contractors are cautioned to evaluate the requirements of this document based on the entire content irrespective of the marginal notations and relationship to the previous issue.

Custodians:
Army – CR
Navy – EC
Air Force – 85
NASA – NA
DLA – CC

Review activities:
Army – AR, MI

Preparing activity:
DLA - CC

(Project 5961-2014-077)

* NOTE: The activities listed above were interested in this document as of the date of this document. Since organizations and responsibilities can change, you should verify the currency of the information above using the ASSIST Online database at https://assist.dla.mil/.