Faculty of Electronics, Telecommunications and Information Technology

TECHNICAL UNIVERSITY OF CLUJ-NAPOCA ROMANIA

COMPUTER AIDED DESIGN

PULSE WIDTH MODULATION GENERATOR

Coordinator: Fizeşan Raul, PhD

Student: Gherman Teodora Ștefania

Group 2023

Year 2

1. Introduction

Pulse-width modulation (PWM) is a modulation process or technique used in most communication systems for encoding the amplitude of a signal right into a pulse width or duration of another signal, usually a carrier signal, for transmission. Although PWM is also used in communications, its main purpose is actually to control the power that is supplied to various types of electrical devices, most especially to inertial loads such as AC/DC motors. [2]

Pulse-width modulation (PWM) is used for controlling the amplitude of digital signals in order to control devices and applications requiring power or electricity. It essentially controls the amount of power, in the perspective of the voltage component, that is given to a device by cycling the on-and-off phases of a digital signal quickly and varying the width of the "on" phase or duty cycle. To the device, this would appear as a steady power input with an average voltage value, which is the result of the percentage of the on time. The duty cycle is expressed as the percentage of being fully (100%) on.[2]

A very powerful benefit of PWM is that power loss is very minimal. Compared to regulating power levels using an analog potentiometer to limit the power output by essentially choking the electrical pathway, thereby resulting in power loss as heat, PWM turns off the power output rather than limits it. Applications range from controlling DC motors and light dimming to heating elements. [2]

The term *duty cycle* describes the proportion of 'on' time to the regular interval or 'period' of time; a low duty cycle corresponds to low power, because the power is off for most of the time. Duty cycle is expressed in percent, 100% being fully on. When a digital signal is on half of the time and off the other half of the time, the digital signal has a duty cycle of 50% and resembles a "square" wave. When a digital signal spends more time in the on state than the off state, it has a duty cycle of >50%. When a digital signal spends more time in the off state than the on state, it has a duty cycle of <50%.[2]

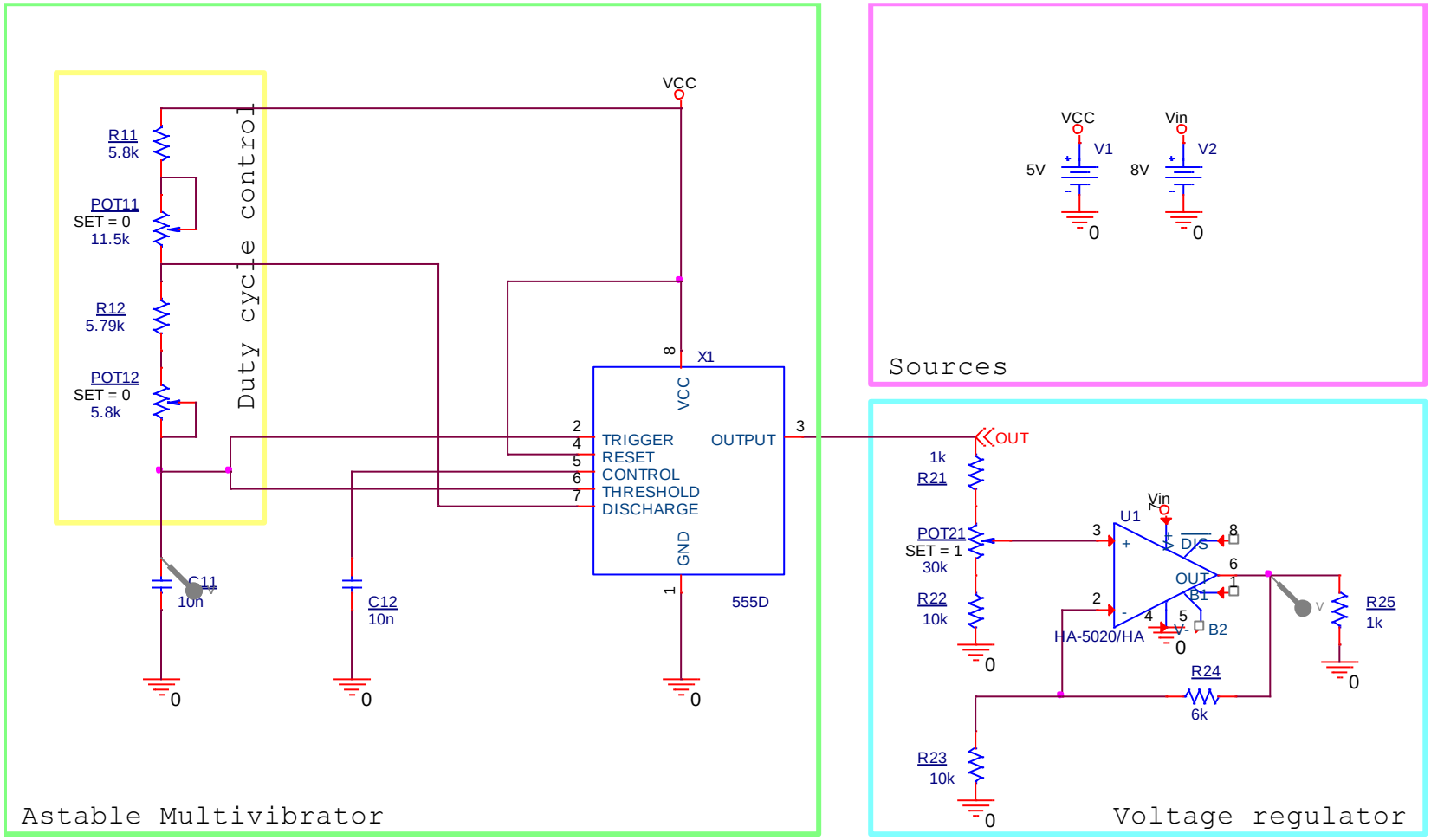


Figure 1. Pulse width modulation generator

2. Circuit structure and operation

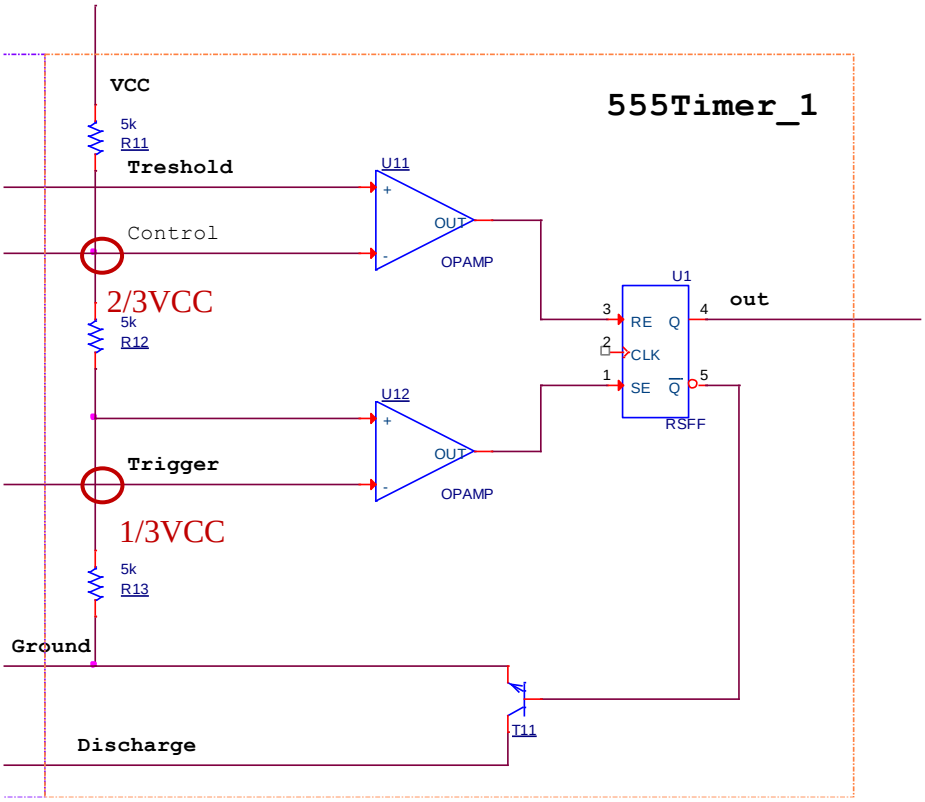


Figure 2. Internal structure of the 555 timer.

The voltage references for U11 and U12 comparators are set by the R11 - R12 - R13 network that divides the VCC voltage into 3 equal parts: $\frac{2}{3}$ VCC for the noninverting comparator U11 and $\frac{1}{3}$VCC for the inverting comparator U12 such that:

v_{Tresh}	$v_{Trigger}$	R	S	Q	$\overline{Q}$	T	Out
$< \frac{2}{3} V_{CC}$	$< \frac{1}{3} V_{CC}$	L	H	H	L	off	V_{OH}
$> \frac{2}{3} V_{CC}$	$> \frac{1}{3} V_{CC}$	H	L	L	H	sat	V_{OL}
$< \frac{2}{3} V_{CC}$	$> \frac{1}{3} V_{CC}$	L	L	previous state		previous state	previous state

Figure 3. Table of states.

2.1. Astable multivibrator

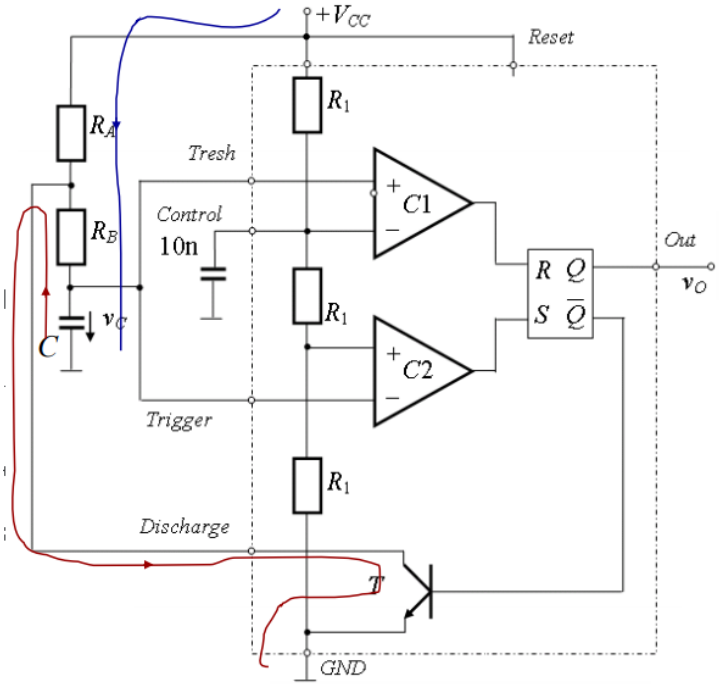


Figure 4. Astable multivibrator [3]

In astable configuration, the 555 timer puts out a continuous stream of rectangular pulses having a specific frequency. The astable configuration is usually implemented using two resistors, R_{11} and R_{12}, and one capacitor C_{11}. In this configuration, the control pin is not used, thus it is connected to ground through a 10 nF decoupling capacitor to shunt electrical noise. The threshold and trigger pins are connected to the capacitor C_{11}, thus they have the same voltage. Initially, the capacitor C_{11} is not charged, thus the trigger pin receives zero voltage which is less than third of the supply voltage. Consequently, the trigger pin causes the output to go high and the internal discharge transistor to go to cut-off mode. Since the discharge pin is no longer short circuited to ground, the current flows through the two resistors, R_{11} and R_{12} to the capacitor charging it. The capacitor C_{11} starts charging until the voltage becomes two-thirds of the supply voltage. At this instance, the threshold pin causes the output to go low and the internal discharge transistor to go into saturation mode. Consequently, the capacitor starts discharging through R_{12} till it becomes less than third of the supply voltage, in which case, the trigger pin causes the output to go high and the internal discharge transistor to go to cut-off mode once again. And the cycle repeats. [1]

In the first pulse, the capacitor charges from zero to two-thirds of the supply voltage, however, in later pulses, it only charges from one-third to two-thirds of the supply voltage. Consequently, the first pulse have a longer high time interval compared to later pulses. Moreover, the capacitor charges through both resistors but only discharges through R_{12}, thus the high interval is longer than the low interval. This is shown in the following equations. [1]

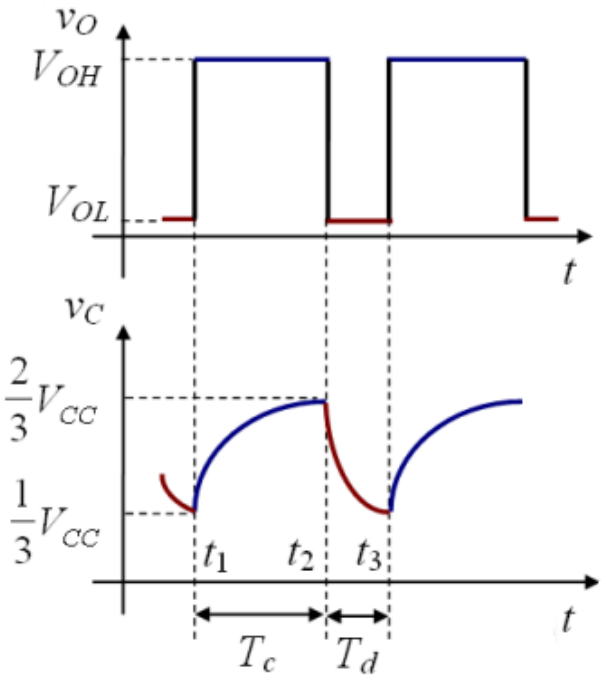


Figure 5. Output signal and the signal given by the charging and discharging of the capacitor

The high time interval of each pulse is given by the formula: [3]

$$T_c = (R_a + R_b) \cdot C \cdot ln2 \approx 0.69 \cdot (R_a + R_b) \cdot C \quad (1)$$

The low time interval of each pulse is given by the formula: [3]

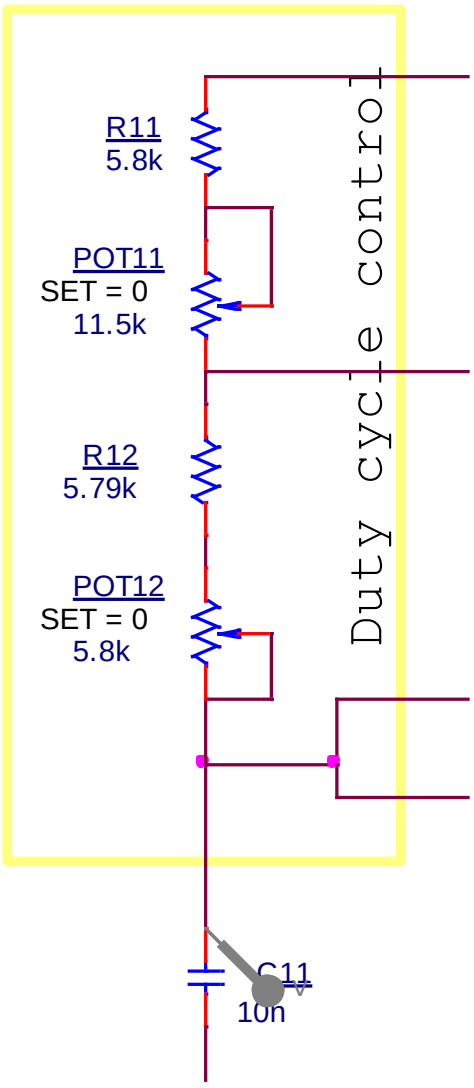
$$T_d = R_b \cdot C \cdot ln2 \approx 0.69 \cdot R_b \cdot C \quad (2)$$

Hence, the frequency f of the pulse is given by: [3]

$$f = \frac{1}{T} = \frac{1}{T_d + T_c} = \frac{1}{ln2 \cdot (R_a + 2R_b) \cdot C} \quad (3)$$

2.2. Duty cycle control

In order to have a modifiable duty cycle, I used a potentiometer next to each resistance.



I first chose C_{11} to be 10nF and then I calculated the period of the signal using formula $Tc = (R_a + R_b) \cdot C \cdot ln2 \approx 0.69 \cdot (R_a + R_b) \cdot C$ (1).

$$T = \frac{1}{f} = \frac{1}{5kHz} = 0.2\,ms = 200\,\mu s$$

By finding 60% and 80% out of the period, I also found the values for T_c and T_d for both values of the duty cycle.

$$T_{c1} = 60\% \cdot 200\,\mu s = 120\,\mu s$$

$$T_{d1} = 40\% \cdot 200\,\mu s = 80\,\mu s$$

$$T_{c2} = 80\% \cdot 200\,\mu s = 160\,\mu s$$

$$T_{d2} = 20\% \cdot 200\,\mu s = 40\,\mu s$$

Next I found the value for R12 by using formula $Td = R_b \cdot C \cdot ln2 \approx 0.69 \cdot R_b \cdot C$ (2) and R11 from formula $Tc = (R_a + R_b) \cdot C \cdot ln2 \approx 0.69 \cdot (R_a + R_b) \cdot C$ (1) for 60% duty cycle:

$$T_{d1} = 80\,\mu s = 0.69 \cdot R_{12} \cdot C$$

$$R_{12} = \frac{80 \cdot 10^{-6}}{0.69 \cdot 10 \cdot 10^{-9}} = 11.59kOhm$$

$$T_{c1} = 120\,\mu s = 0.69 \cdot (R_{11} + R_{12}) \cdot C$$

Figure 6. Duty cycle control

$$R_{11} = \frac{120 \cdot 10^{-6}}{0.69 \cdot 10 \cdot 10^{-9}} - 11.59 \cdot 10^3 = 5.8\,kOhm$$

The same has been done for the 80% duty cycle and I obtained R_{11} equal to 17.3 kOhm and R_{12} equal to 5.79 kOhm.

In order to be able to use both values for R_{11} and R_{12}, I used a potentiometer which would add up to the existing resistance. Therefore, I calculated POT_{11} to be equal with 11.5kOhm and POT_{12}

equal with 5.8kOhm. When both potentiometers are set to 0 we can see the 80% duty. When the potentiometers are set to 1, we can see the 60% duty.

To better see the duty cycle, I applied a Time domain analysis to the circuit with the following settings:

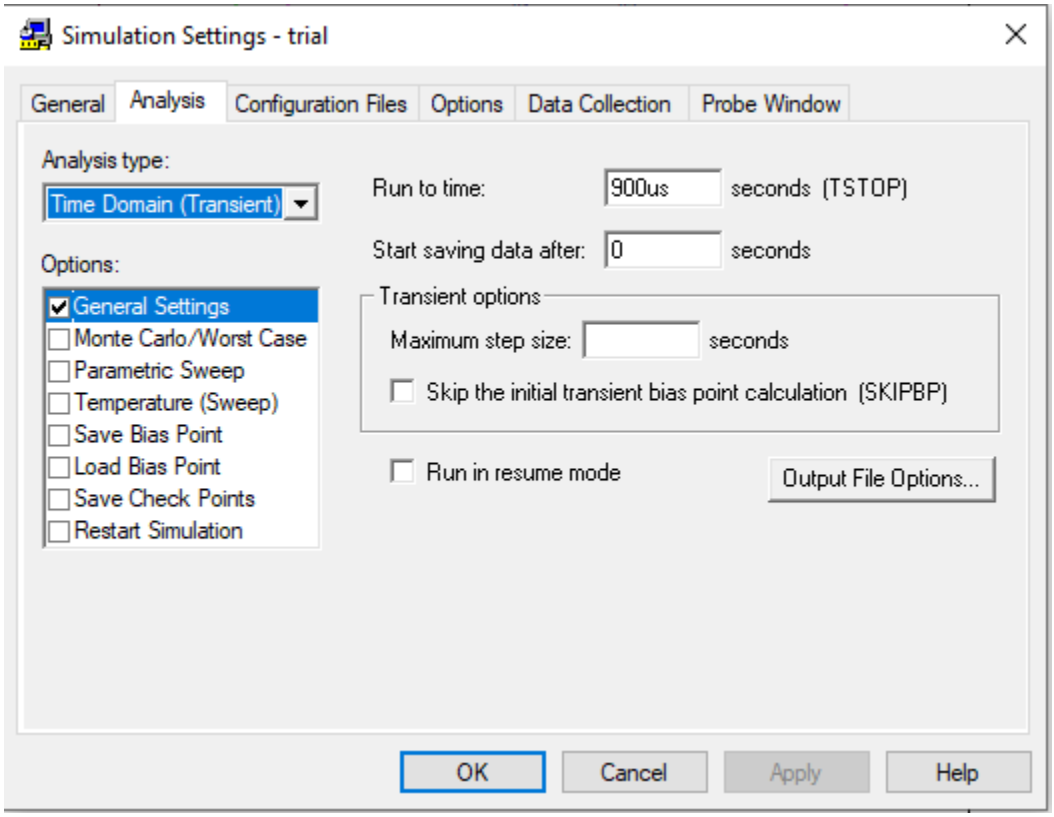


Figure 7. Profile simulation settings

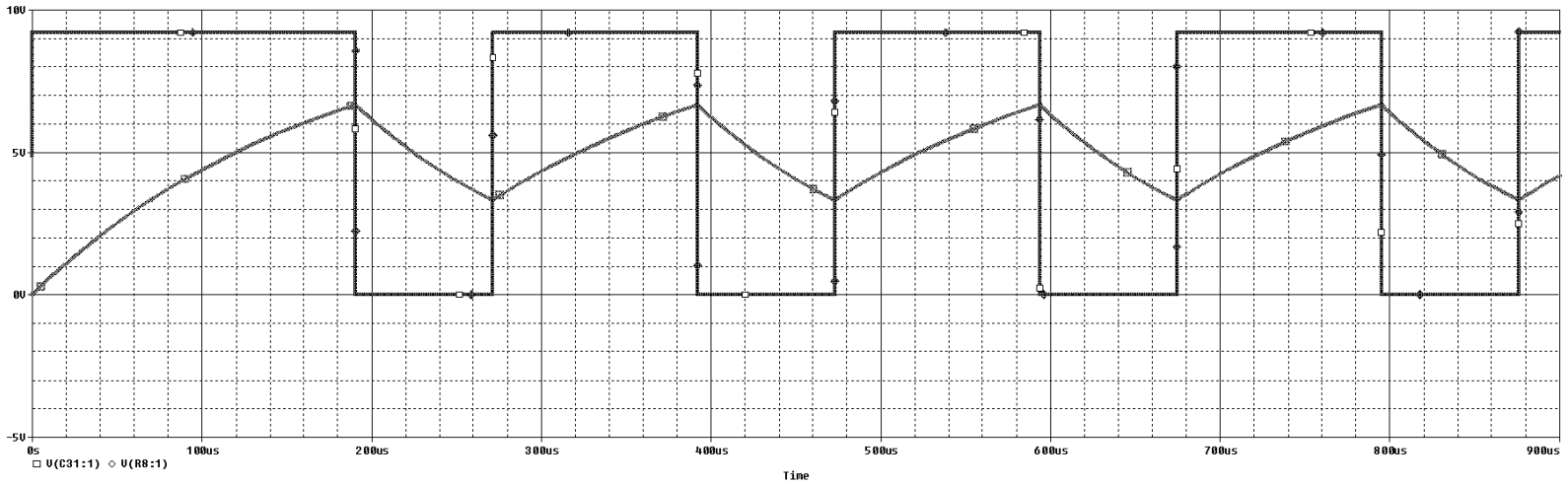


Figure 8. 60% duty cycle without using the voltage regulator

Trace Color	Trace Name	Y1	Y2	Y1 - Y2
	X Values	793.665u	593.818u	199.847u

Figure 9. Period measured with the PSpice cursors for 60% duty cycle

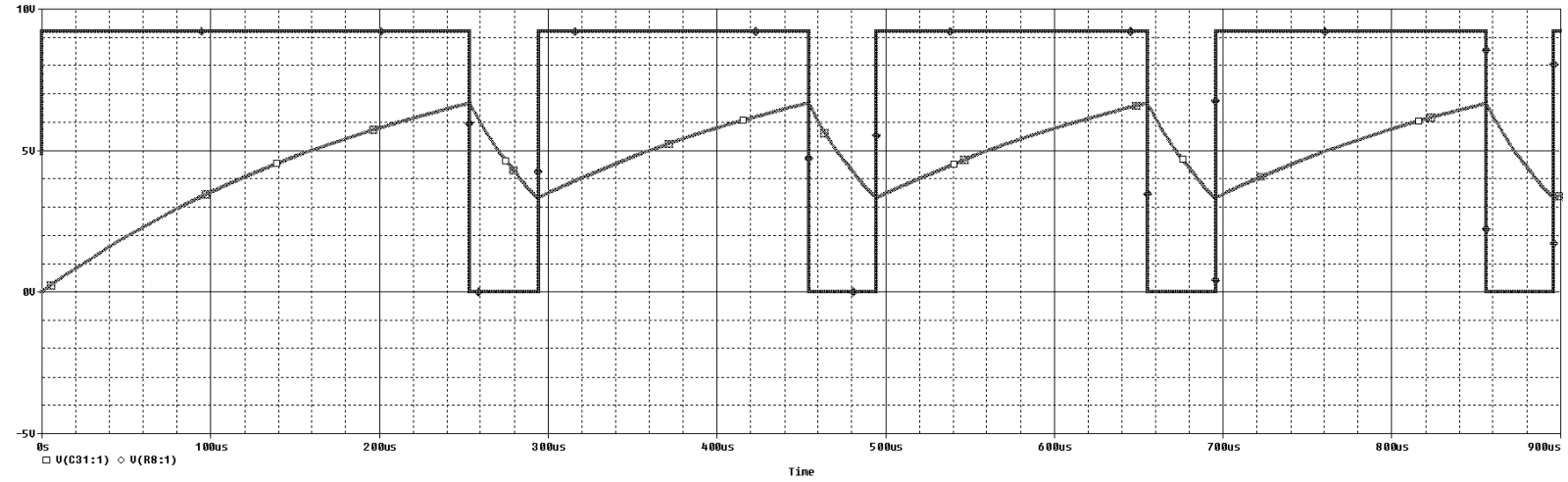


Figure 10. 80% duty cycle without using the voltage regulator

Trace Color	Trace Name	Y1	Y2	Y1 - Y2
	X Values	896.062u	695.087u	200.975u

Figure 11. Period measured with the PSpice cursors for 80% duty cycle

2.3. Amplitude control

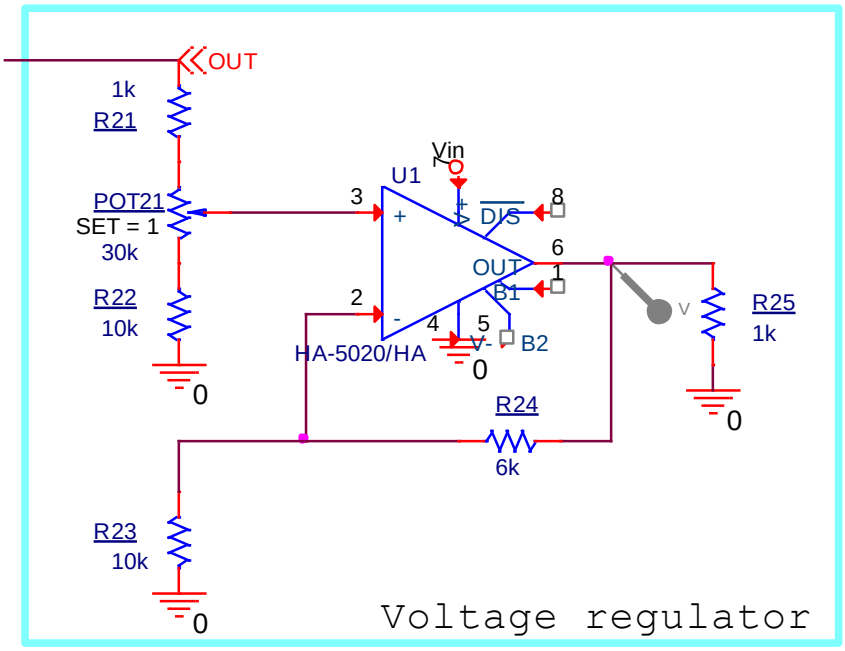


Figure 12. Voltage regulator

In order to modify the amplitude of the output signal between 2V and 8V, I used a voltage regulator.

A voltage regulator is a system designed to automatically maintain a constant voltage level. A voltage regulator may use a simple feed-forward design or may include negative feedback. It may use an electromechanical mechanism, or electronic components. Depending on the design, it may be used to regulate one or more AC or DC voltages. [6]

Electronic voltage regulators are found in devices such as computer power supplies where they stabilize the DC voltages used by the processor and other elements. In automobile alternators and central power station generator plants, voltage regulators control the output of the plant. In an electric power distribution system, voltage regulators may be installed at a substation or along distribution lines so that all customers receive steady voltage independent of how much power is drawn from the line. [6]

The negative feedback helps us by giving equal inputs of the operational ($V_- = V_+$). I chose the operational amplifier HA-5020/HA in the HARRIS library because of its 100MHz bandwidth and high slew rate (800V/μs).

$$V_+ = \frac{k \cdot POT_{21} + R_{22}}{POT_{21} + R_{22}} (4)$$

$$V_- = \frac{R_{23}}{R_{23} + R_{24}} (5)$$

$$V_- = V_+ (6)$$

By making a system of equations from $V_+ = \frac{k \cdot POT_{21} + R_{22}}{POT_{21} + R_{22}}$(4), $V_- = \frac{R_{23}}{R_{23} + R_{24}}$ (5) and $V_- = V_+$ (6) I got the values [3]:

$$POT_{21} = 30kOhm$$
$$R_{22} = 10kOhm$$
$$R_{23} = 10kOhm$$
$$R_{24} = 6kOhm$$

For R21 and R25 I picked the standard value of 1kOhm since their value is not important.

By running the same Time domain analysis, when POT21 is set to 0, we have an amplitude of 2V and when it's set at 1, we have a 8V amplitude.

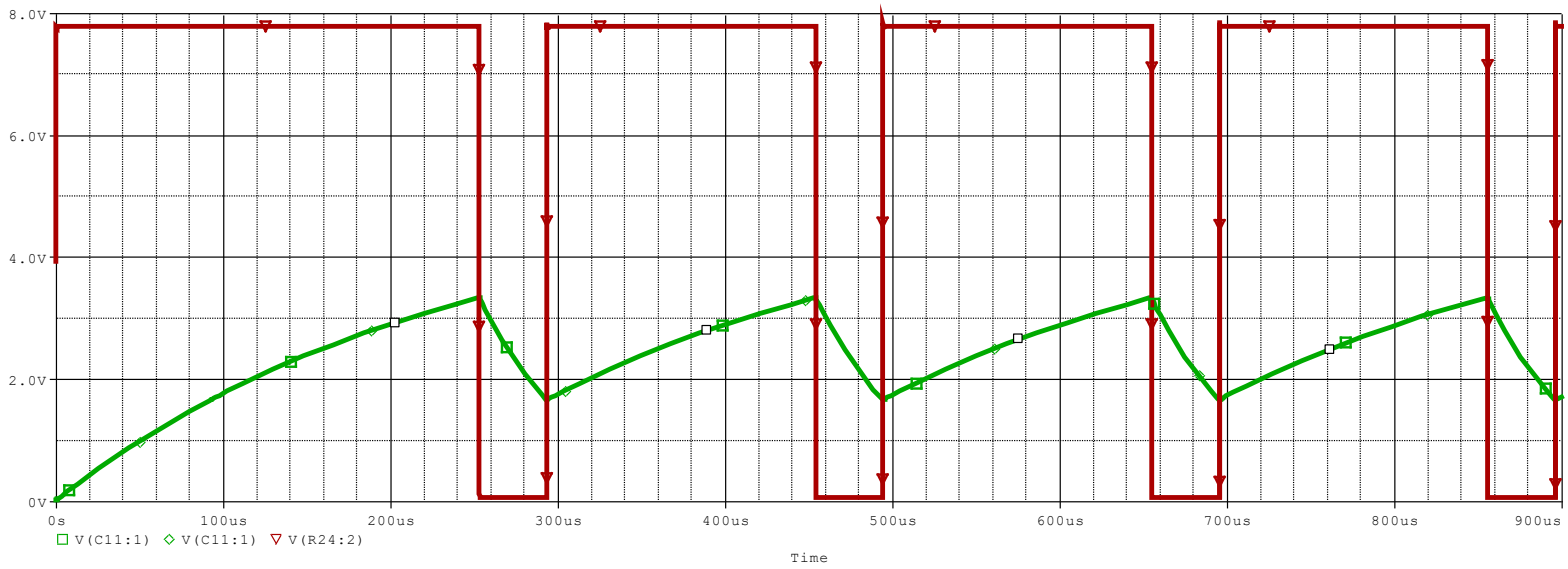


Figure 13. 8 V amplitude

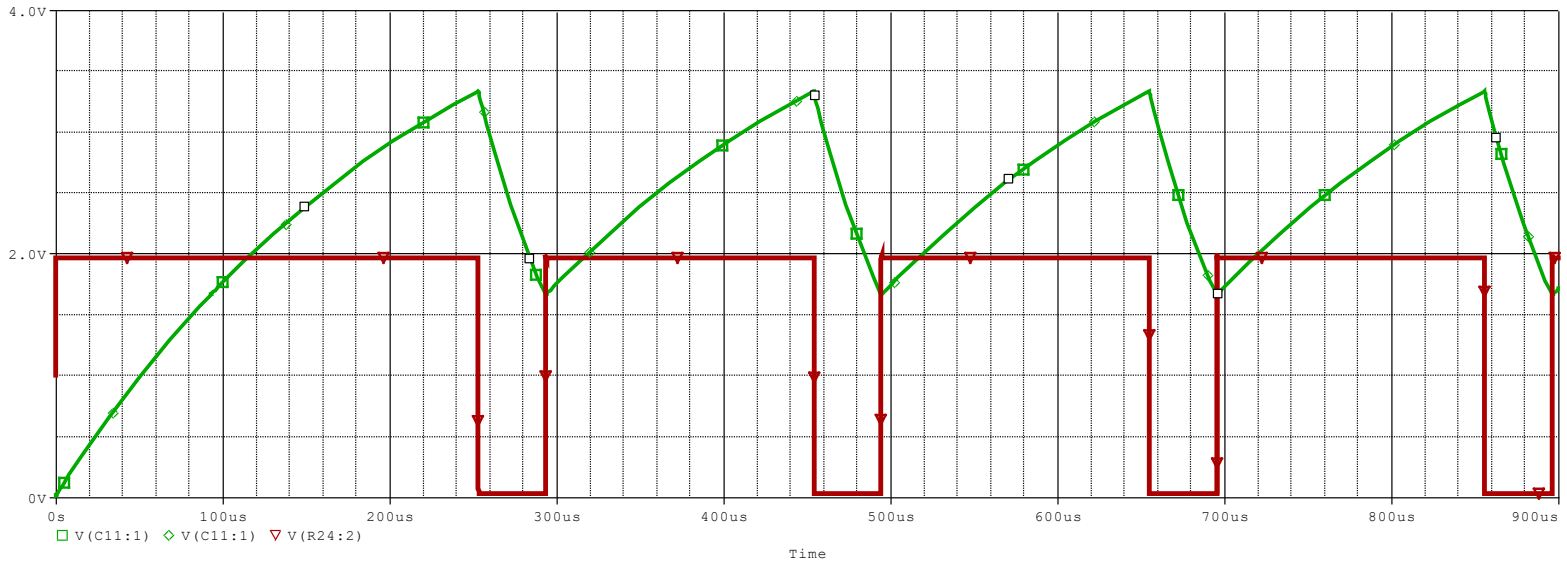


Figure 14. 2V amplitude

4. Standardization

In the standardization process, I tried choosing the closest real values to the calculated values. I started with the potentiometers, since they come in a smaller variety. For the potentiometer used by the Voltage Regulator I had to compute the value for R_{22} again (Figure 1). Also I realized I did not need the R_{21} resistor from Figure 1. I took into account the power dissipated on each component (it can be checked by enabling the Bias Power Display button at the top of the Capture CIS window).

CALCULUS	STANDARD VALUES	PROPERTIES
R_{11} = 5.8k Ω	5.76k Ω	Metal Film Resistors - Through Hole 400mW 5.76Kohms 1% SFR55 Historical p/n
R_{12} = 5.79k Ω	5.76k Ω	Metal Film Resistors - Through Hole 400mW 5.76Kohms 1% SFR55 Historical p/n
POT_{11} = 11.5k Ω	11k Ω	Potentiometers 11K 3/4" Single Turn
POT_{12} = 5.8k Ω	5k Ω	Potentiometers 5K 10% 12.5MM SQ CONTROL
C_{11} = 10nF	10nF	Multilayer Ceramic Capacitors MLCC - Leaded .010µF 25.0V
C_{12} = 10nF	10nF	Multilayer Ceramic Capacitors MLCC - Leaded .010µF 25.0V
R_{21} = 10k Ω	10k Ω	RES 10K OHM 1/4W 5% AXIAL
R_{22} = 10k Ω	10k Ω	RES 10K OHM 1/4W 5% AXIAL
R_{23} = 6k Ω	6k Ω	RES 6K OHM 3W 5% AXIAL
R_{24} = 1k Ω	1k Ω	RES 1K OHM 1/4W 5% AXIAL
POT_{21} = 30k Ω	30k Ω	Trimmer Resistors - Through Hole 3/8" 30Kohms 10% 0.5Watts Square
C_{12} = 10nF	10nF	Multilayer Ceramic Capacitors MLCC - Leaded .010UF 25.0V

Table 1. Standardization of the passive components

After standardization with real values, I obtained a 1.5% smaller period for 60% duty cycle and a 5% smaller period for 80% duty cycle. This is due to the difference between the standardized value and the computed value for POT_{11} and POT_{12}. The 80% duty cycle is now with 0.38% smaller (79.69%) with the computed values, and the 60% duty cycle with 0.86% bigger (60.52%).

Duty cycle	Computed values	Standardized values
60%	R_1 = 5.8 k Ω	R_1 = 5.76 k Ω
	R_2 = 11.59k Ω	R_2 = 10.76 k Ω
80%	R_1' = 17.3 k Ω	R_1' = 16.76 k Ω
	R_2' = 5.8 k Ω	R_2' = 5.76 k Ω

Table 2. Modifications that occurred after the standardization process

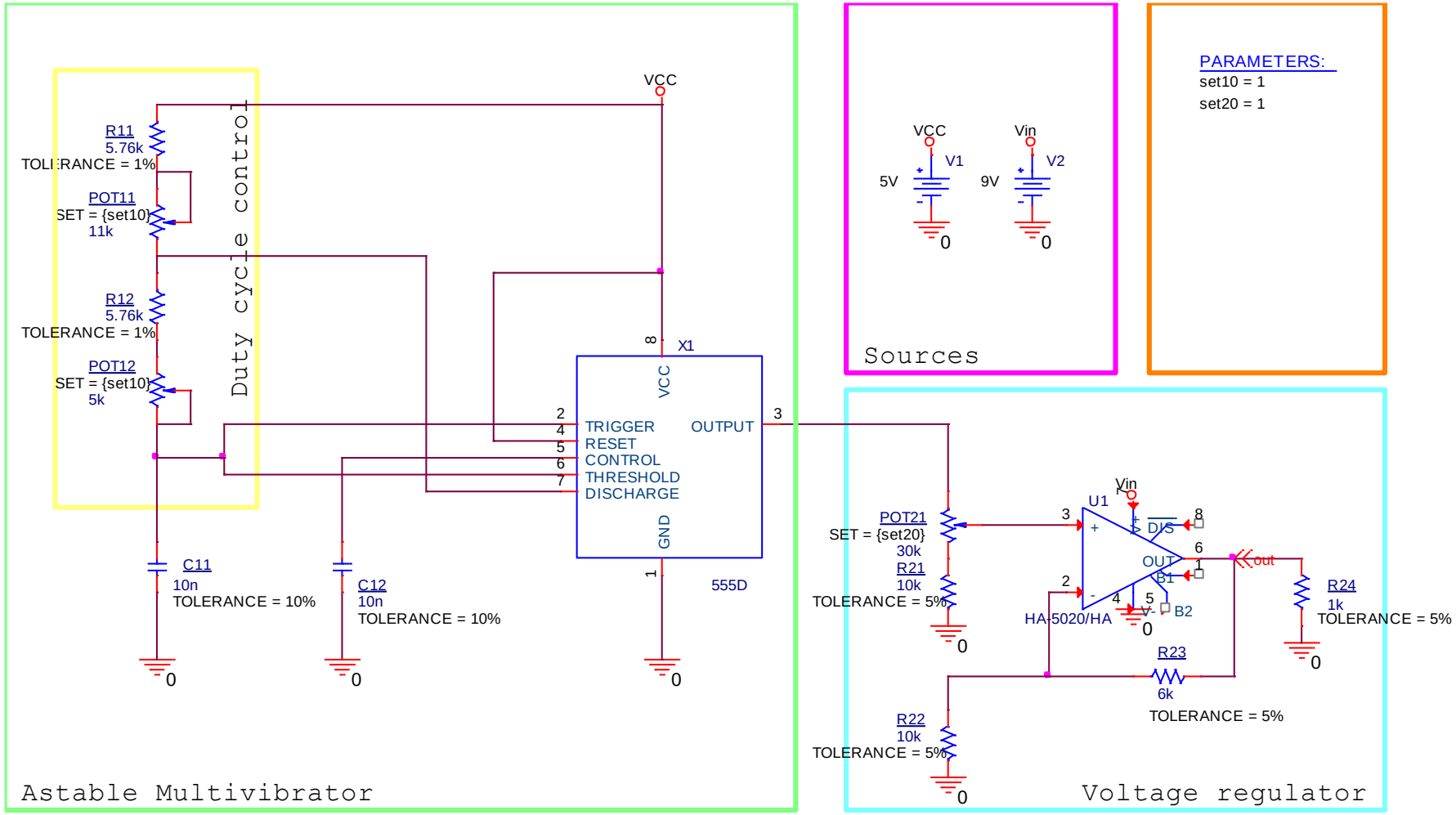


Figure 15. Circuit after standardization

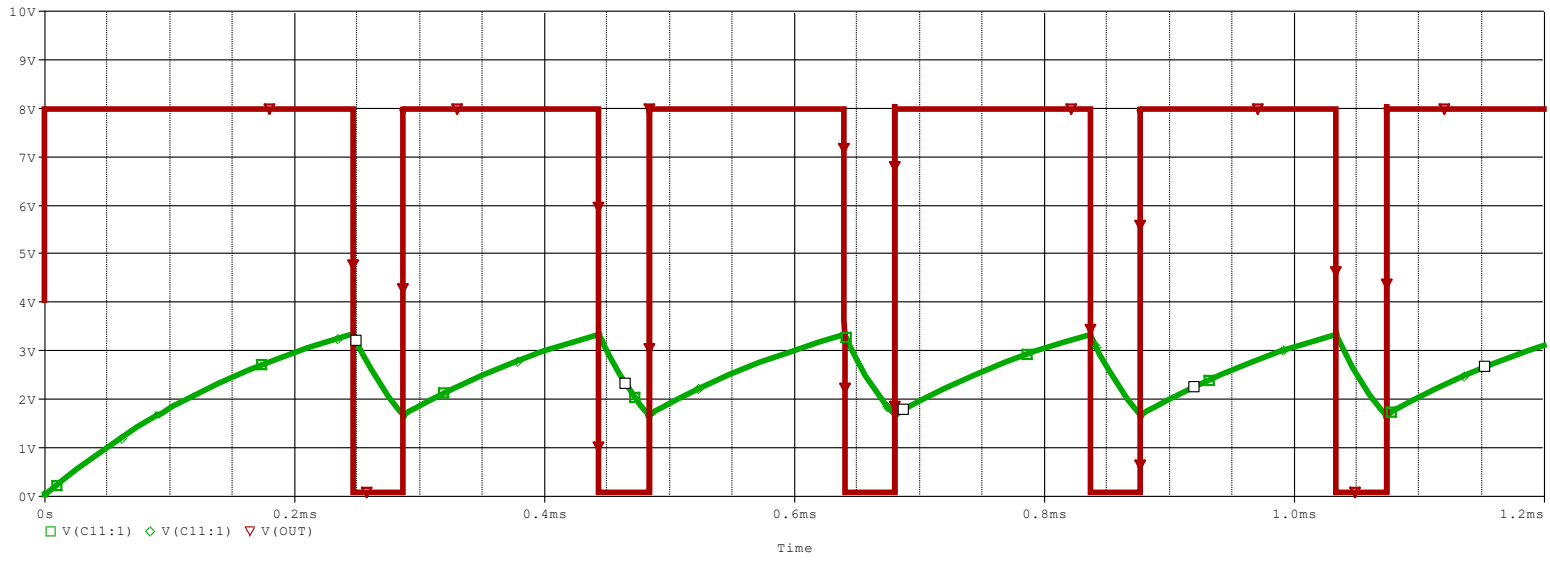


Figure 16. POT11 and POT12 are set to 0 (80% duty cycle) and POT21 set to 1 (8V amplitude)

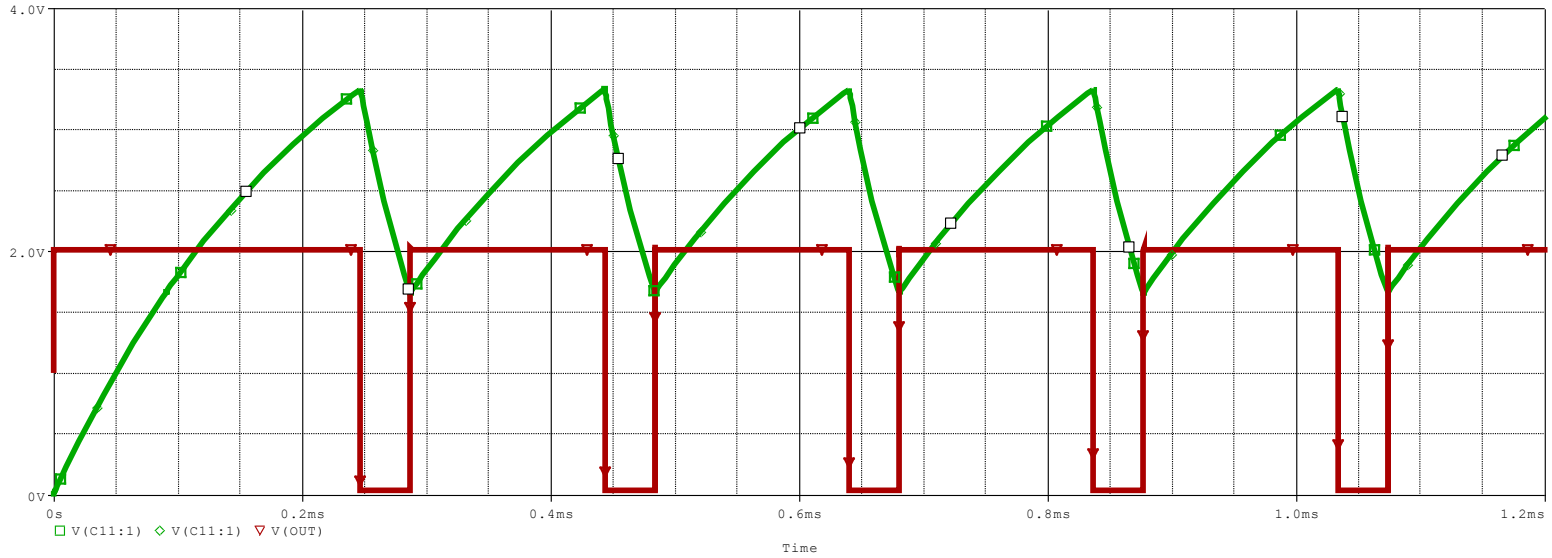


Figure 17. POT11 and POT12 are set to 0 (80% duty cycle) and POT21 set to 0 (2V amplitude)

Trace Color	Trace Name	Y1	Y2	Y1 - Y2
	X Values	877.002u	680.557u	196.445u

Figure 18. Period measured with the PSpice cursors for 80% duty cycle

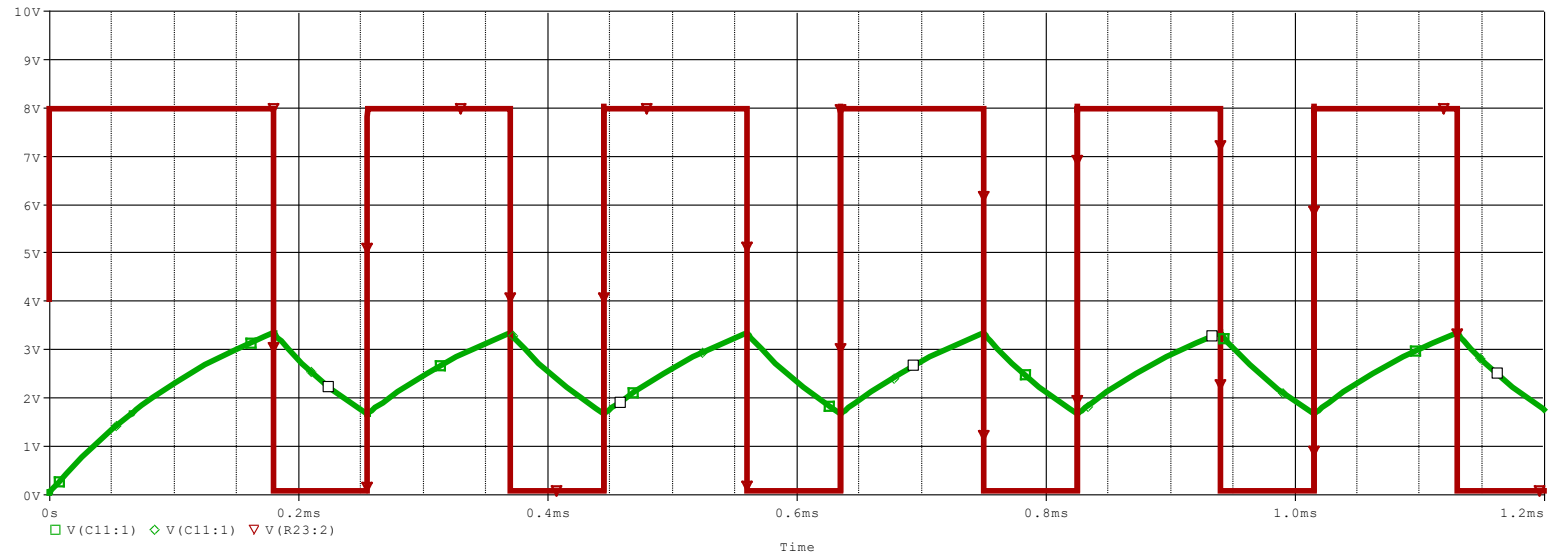


Figure 19. POT11 and POT12 are set to 1 (60% duty cycle) and POT21 set to 1 (8V amplitude)

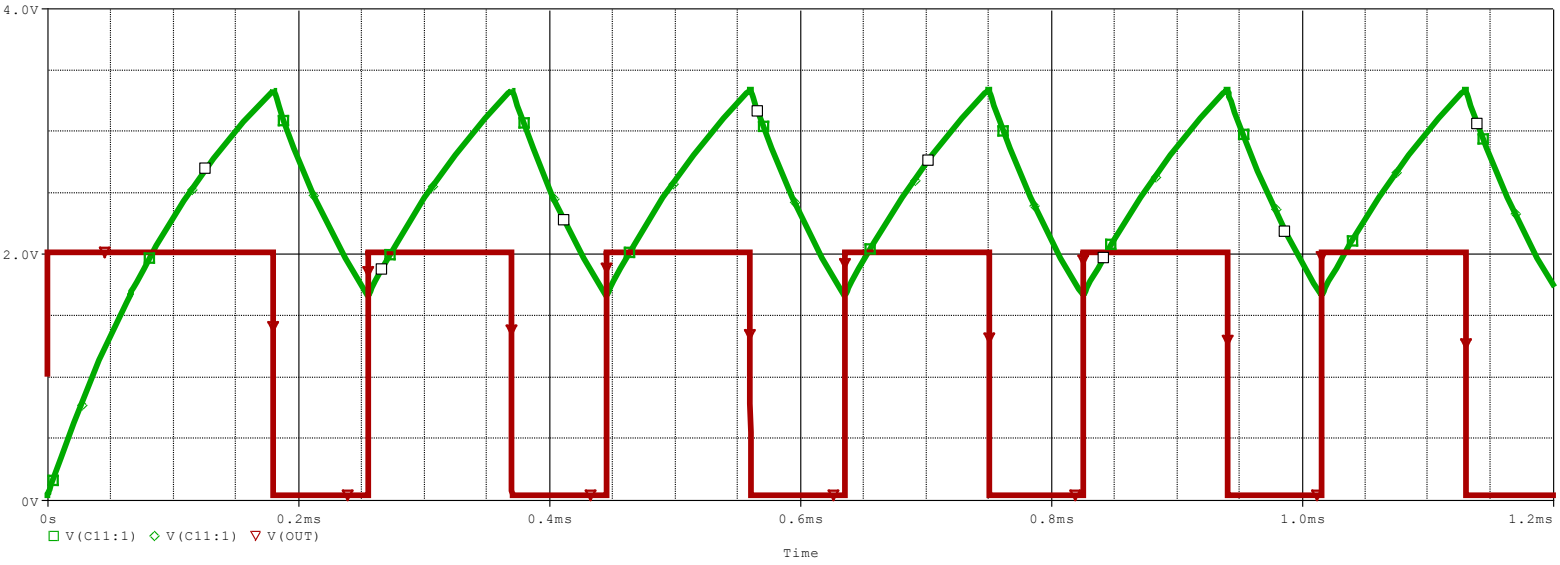


Figure 20. POT11 and POT12 are set to 1 (60% duty cycle) and POT21 set to 0 (2V amplitude)

Trace Color	Trace Name	Y1	Y2	Y1 - Y2
	X Values	825.499u	635.294u	190.204u

Figure 21. Period measured with the PSpice cursors for 60% duty cycle

I modified the simulation such that there would be visible approximately 6 periods of the signal.

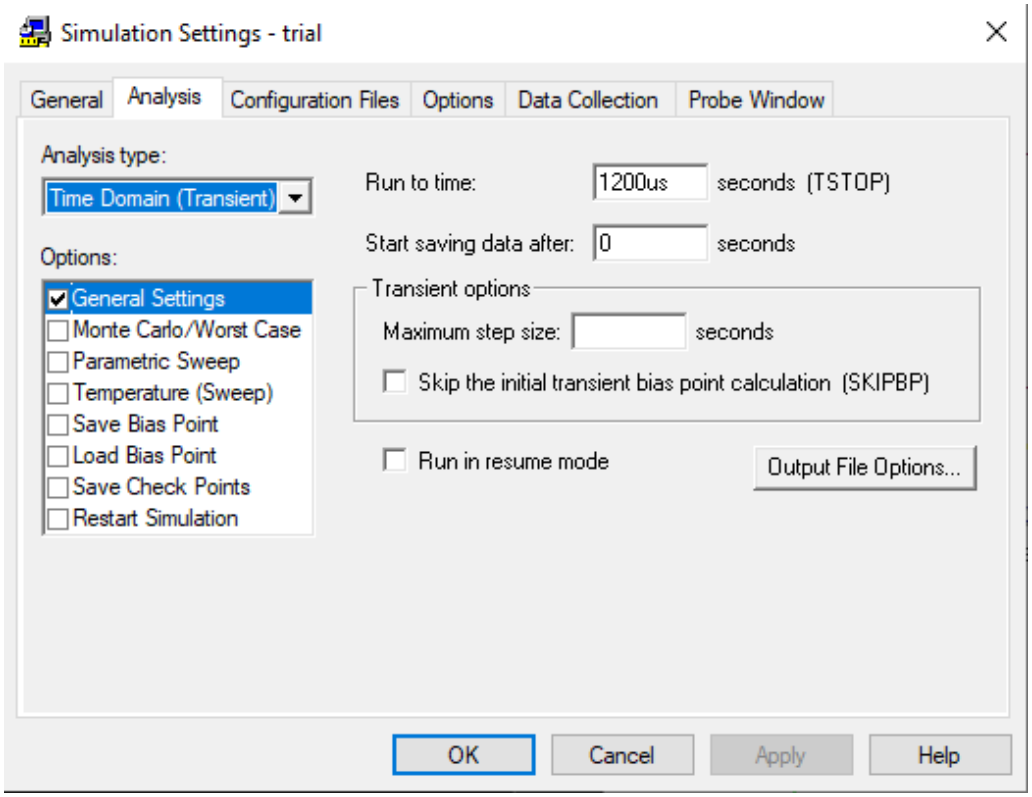


Figure 22. Time domain profile simulation settings

As for the video amplifier HA-5020/HA from the HARRIS library with the following features:

Features

- Wide Unity Gain Bandwidth 100MHz
- Slew Rate. 800V/μs
- Output Current . . . . . ±30mA (Min)
- Drives 3.5V into 75Ω
- Differential Gain 0.03%
- Differential Phase. . . . . .0.03°
- Low Input Voltage Noise . . . . . 4.5nV/$\sqrt{Hz}$
- Low Supply Current . . . . . 10mA (Max)
- Wide Supply Range . . . . . ±5V to ±15V
- Output Enable/Disable
- High Performance Replacement for EL2020
- Pb-Free Plus Anneal Available (RoHS Compliant)

Figure 23. Features taken from the datasheet [7]

The real-life equivalent has been discontinued and cannot be bought anymore, but I searched for one with the same characteristics, if not maybe a little bit better and I found the THS4061CD - High Speed Operational Amplifiers 180MHz High Speed. It is manufactured by Texas Instruments™ and sold by Mouser™.

Product Attribute	Attribute Value	Search Similar
Manufacturer:	Texas Instruments	☐
Product Category:	High Speed Operational Amplifiers	☑
RoHS:	RoHS Details	
Series:	THS4061	☐
Number of Channels:	1 Channel	☐
GBP - Gain Bandwidth Product:	100 MHz	☐
SR - Slew Rate:	400 V/us	☐
Voltage Gain dB:	78.06 dB	☐
CMRR - Common Mode Rejection Ratio:	70 dB to 110 dB	☐
Output Current per Channel:	115 mA	☐
Ib - Input Bias Current:	6 uA	☐
Vos - Input Offset Voltage:	8 mV	☐
Supply Voltage - Max:	33 V	☐
Supply Voltage - Min:	9 V	☐
Operating Supply Current:	10.5 mA	☐
Minimum Operating Temperature:	- 40 C	☐
Maximum Operating Temperature:	+ 85 C	☐
Mounting Style:	SMD/SMT	☐
Package/Case:	SOIC-8	☐
Packaging:	Tube	☐
Amplifier Type:	Voltage Feedback	
Height:	1.58 mm	
Length:	4.9 mm	
Product:	Operational Amplifiers	
Width:	3.91 mm	
Brand:	Texas Instruments	
Topology:	Voltage Feedback	
en - Input Voltage Noise Density:	14.5 nV/sqrt Hz	
Operating Supply Voltage:	33 V	
Pd - Power Dissipation:	740 mW	
Product Type:	Op Amps - High Speed Operational Amplifiers	
PSRR - Power Supply Rejection Ratio:	70 dB	

Figure 24. Properties taken from the THS4061CD Mouser product page.

For a real-life component of the IC555 timer with the specification in Figure 25, I chose the SE555QS-13 with the specifications in Figure 26.

ELECTRICAL CHARACTERISTICS(T_A =+25°C)

Symbol	Parameter	Test Conditions	Guaranteed Limits		Unit
			Min	Max	
I_{CC}	Supply Current	V_{CC}=5.0 V, R_L =∞ V_{CC}=15 V, R_L=∞		6.0 15	mA
	Timing Error	R=1.0 kΩ to 100 kΩ Initial Accuracy C = 0.1 µF V_{CC}=5.0 V and V_{CC}=15 V		4	%
V_{th}	Threshold Voltage	V_{CC}=5.0 V V_{CC}=15 V	2.6 9	4.0 11	V
V_T	Trigger Voltage	V_{CC}=5.0 V V_{CC}=15 V	1.1 4.5	2.2 5.6	V
I_T	Trigger Current	V_{02}=0 V, V_{CC}=15 V V_{02}=15 V, V_{CC}=15 V		-2 0.5	µA
V_R	Reset Voltage	V_{CC}=15 V	0.4	1.0	V
I_R	Reset Current	V_{04}=0 V, V_{CC}=15 V V_{04}=15 V, V_{CC}=15 V		-0.4 0.5	mA µA
I_{th}	Threshold Current (Note 1)	V_{06}=0 V, V_{CC}=15 V V_{06}=10 V, V_{CC}=15 V		-0.5 0.25	µA
I_{dis}	Discharge Leakage Current (Pin 7)	V_{CC}=15 V, V_{07}=15 V		100	nA
V_{REF}	Control Voltage Level	V_{CC}=15 V V_{CC}=5.0 V	9.0 2.6	11 4.0	V
V_{OL}	Output Voltage Low	(V_{CC}=15 V) I_{sink}=10 mA, I_{sink}=50 mA, I_{sink}=100 mA, V_{CC}=5.0 V, I_{sink}=5.0 mA		 0.25 0.75 2.3 0.35	V
V_{OH}	Output Voltage High	I_{source}=200 mA,V_{CC}=15 V I_{source}=100 mA, V_{CC}=15 V I_{source}=100 mA, V_{CC}=5.0 V	12 12.75 2.75		V
t_{OLH}	Rise Time of Output	V_{CC}=15 V		150	ns
t_{OHL}	Fall Time of Output	V_{CC}=15 V		150	ns

Note 1. This will determine the maximum value of R_A + R_B for 15 V operation.
The maximum total R=20 MΩ.

Figure 25. Electrical characteristics of the PSpice model of the IC555 timer[8]

Electrical Characteristics (V_{CC} = 5V to 15V, T_A = +25°C, unless otherwise stated.)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
V_{TH}	Threshold Voltage Level	V_{CC} = 15V	8.8	10	11.2	V
		V_{CC} = 5V	2.4	3.3	4.2	
I_{TH}	Threshold Current (Note 9)	—	—	30	250	nA
V_{TR}	Trigger Voltage Level	V_{CC} = 15V	4.5	5	5.6	V
		V_{CC} = 5V	1.1	1.67	2.2	
I_{TR}	Trigger Current	TRIG at 0V	—	0.5	2	µA
V_{RST}	RESET Voltage Level	—	0.3	0.7	1	V
I_{RST}	RESET Current	RESET at V_{CC}	—	0.1	0.4	mA
		RESET at 0V	—	-0.4	-1.5	
I_{DIS}	DISCH Switch Off-state Current	—	—	20	100	nA
V_{DIS}	DISCH Saturation Voltage with Output Low (Note 10)	V_{CC} = 15V, I_{DIS} = 15mA	—	180	480	mV
		V_{CC} = 5V, I_{DIS} = 4.5mA	—	80	200	
V_{CON}	CONT Voltage (Open Circuit)	V_{CC} = 15V	9	10	11	V
		V_{CC} = 5V	2.6	3.3	4	

Symbol	Parameter	Test conditions		Min	Typ.	Max	Unit
V_{OL}	Low Level Output Voltage	V_{CC} = 15V, I_{OL} = 10mA		—	0.1	0.25	V
		V_{CC} = 15V, I_{OL} = 50mA		—	0.4	0.75	
		V_{CC} = 15V, I_{OL} = 100mA		—	2	2.5	
		V_{CC} = 15V, I_{OL} = 200mA		—	2.5	—	
		V_{CC} = 5V, I_{OL} = 5mA		—	0.1	0.35	
		V_{CC} = 5V, I_{OL} = 8mA		—	0.15	0.4	
V_{OH}	High Level Output Voltage	V_{CC} = 15V, I_{OH} = -100mA		12.75	13.3	—	V
		V_{CC} = 15V, I_{OH} = -200mA		—	12.5	—	
		V_{CC} = 5V, I_{OH} = -100mA		2.75	3.3	—	
I_{CC}	Supply Current	Output low, no load	V_{CC} = 15V	—	10	15	mA
			V_{CC} = 5V	—	3	6	
		Output high, no load	V_{CC} = 15V	—	9	13	
			V_{CC} = 5V	—	2	5	
T_{ER}	Initial Error of Timing Interval (Note 11)	Each time, monostable (Note 12)	—	—	1	3	%
		Each time, astable (Note 13)		—	2.25	—	
T_{TC}	Temperature Coefficient of Timing Interval	Each time, monostable (Note 12)	T_A = full range	—	50	—	ppm/°C
		Each time, astable (Note 13)		—	150	—	
T_{VCC}	Supply Voltage Sensitivity of Timing Interval	Each time, monostable (Note 12)	—	—	0.1	0.5	%/V
		Each time, astable (Note 13)		—	0.3	—	
t_{RI}	Output Pulse Rise Time		C_L = 15pF	—	100	300	ns
t_{FA}	Output Pulse Fall Time		C_L = 15pF	—	100	300	ns

Figure 26. Electrical characteristic of the chosen SE555QS-13 component [9]

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Item	Quantity	Reference	Part	Value	Manufacturer	Vendor	Description
1	2	C11,C12	10n	KEMET	Mouser electronics		Multilayer Ceramic Capacitors MLCC - Leaded .010UF 25.0V
2	1	POT11	11k	Bourns	Mouser Electronics		Potentiometers 11K 3/4" Single Turn
3	1	POT12	5k	Bourns	Mouser electronics		Potentiometers 5K 10% 12.5MM SQ CONTROL
4	1	POT21	30k	Bourns	Mouser electronics		Trimmer Resistors - Through Hole 3/8" 30Kohms 10% 0.5Watts Square
5	2	R11,R12	5.76k	Vishay / BC Components	Mouser electronics		Metal Film Resistors - Through Hole 400mW 5.76Kohms 1% SFR55 Historical p/n
6	2	R21,R22	10k	Kamaya Inc. DigiKey	RES 10K OHM 1/4W 5% AXIAL		
7	1	R23	6k	Stackpole Electronics Inc.	DigiKey	RES 6K OHM 3W 5% AXIAL	
8	1	R24	1k	Kamaya Inc. DigiKey	RES 1K OHM 1/4W 5% AXIAL		
9	1	U1	HA-5020/HA	Texas Instruments	Mouser electronics		High Speed Operational Amplifiers 180MHz High Speed
10	1	X1	555D	Diodes Incorporated	Mouser electronics		Timers & Support Products Automotive Grade Precision Timer

Figure 27. Bill of materials

4. Simulations

4.1. Parametric sweep

Parametric analysis performs multiple iterations of a specified standard analysis while varying a global parameter, model parameter, component value, or operational temperature. The effect is the same as running the circuit several times, once for each value of the swept variable. [10]

As parameters I chose the ‘set’ values of the potentiometers in order to show how they influence the circuit and the range of results we can get from different sections on the potentiometer.

Through the simulation in Figure 31 I mean to show how the duty cycle changes depending on POT_{11} and POT_{12}. I chose an increment of 0.33 so that the first and last plot do not overlap and in Figure 30 are displayed the values of set10 as the increment grows.

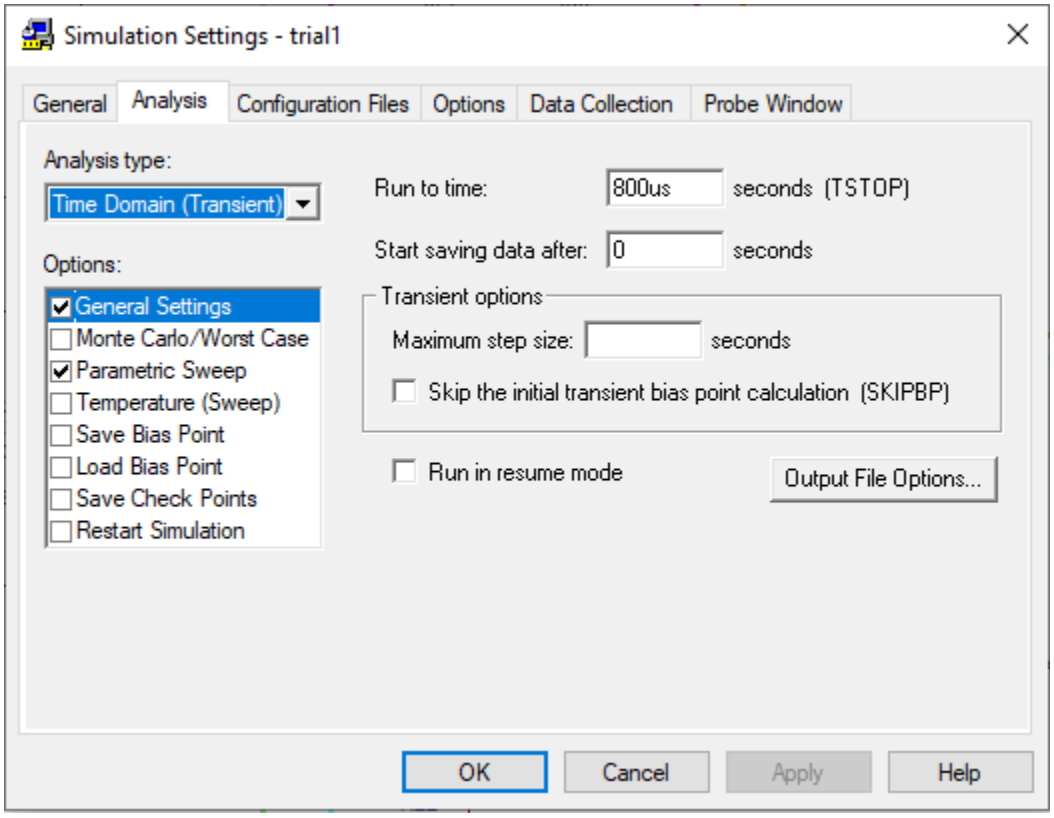

Figure 28. Time domain simulation settings

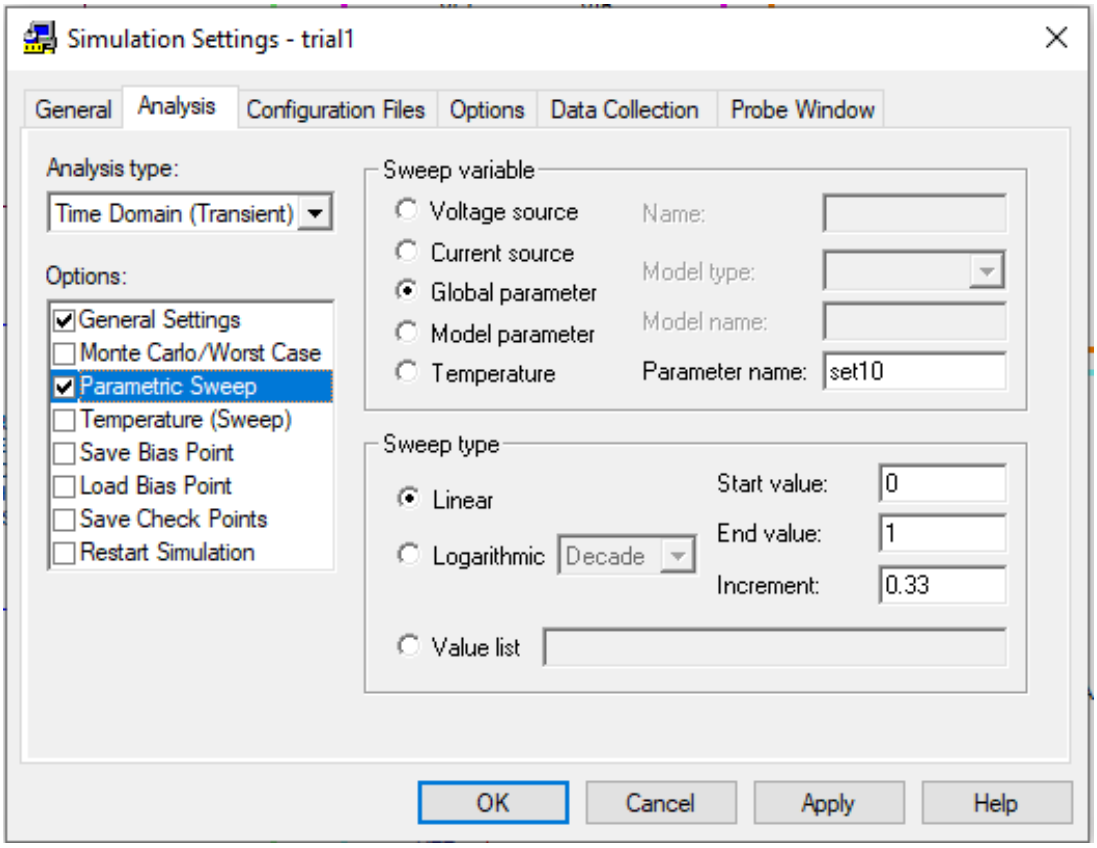

Figure 29. Parametric sweep simulation settings

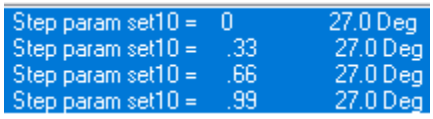

Figure 30. Available sections

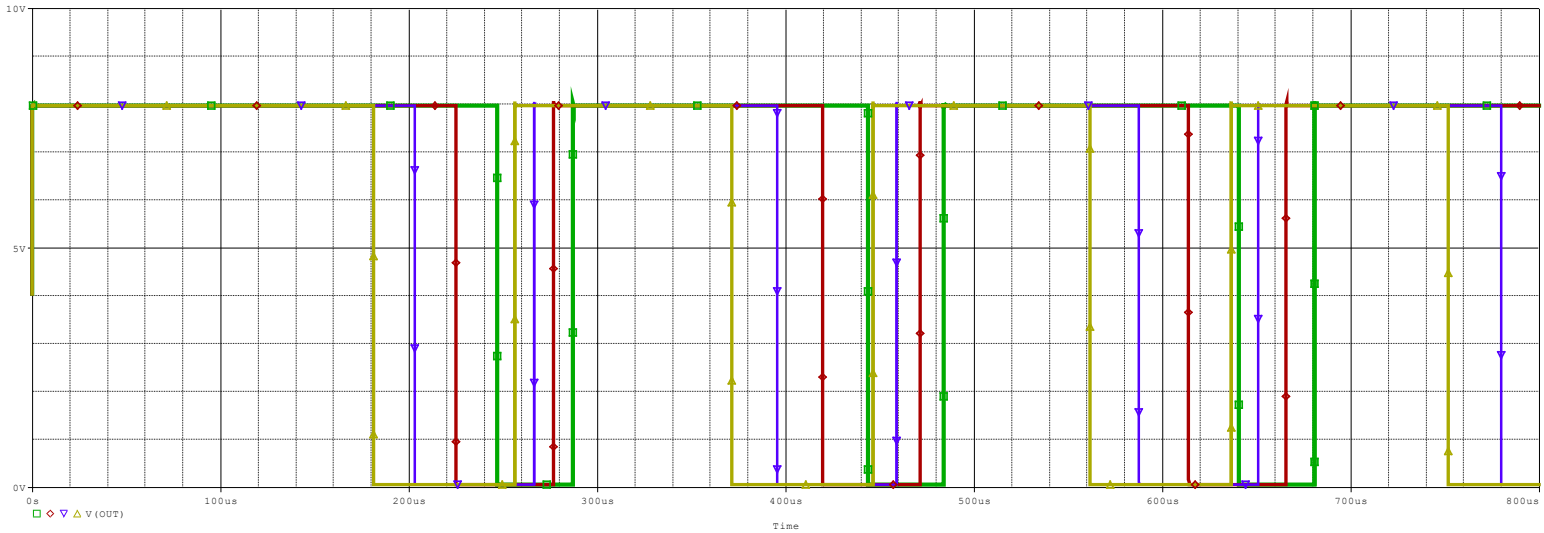

Figure 31. The variation of the output with respect to the value of set10

In Figure 36 I wanted to show how one can change the amplitude of the circuit through POT_{21}. I chose an increment of 0.25 such that the simulation would display 3 more values, after each quarter of the potentiometer. In Figure 34 are the values of the amplitude measured in PSpice for each value of set20 from figure Figure 35.

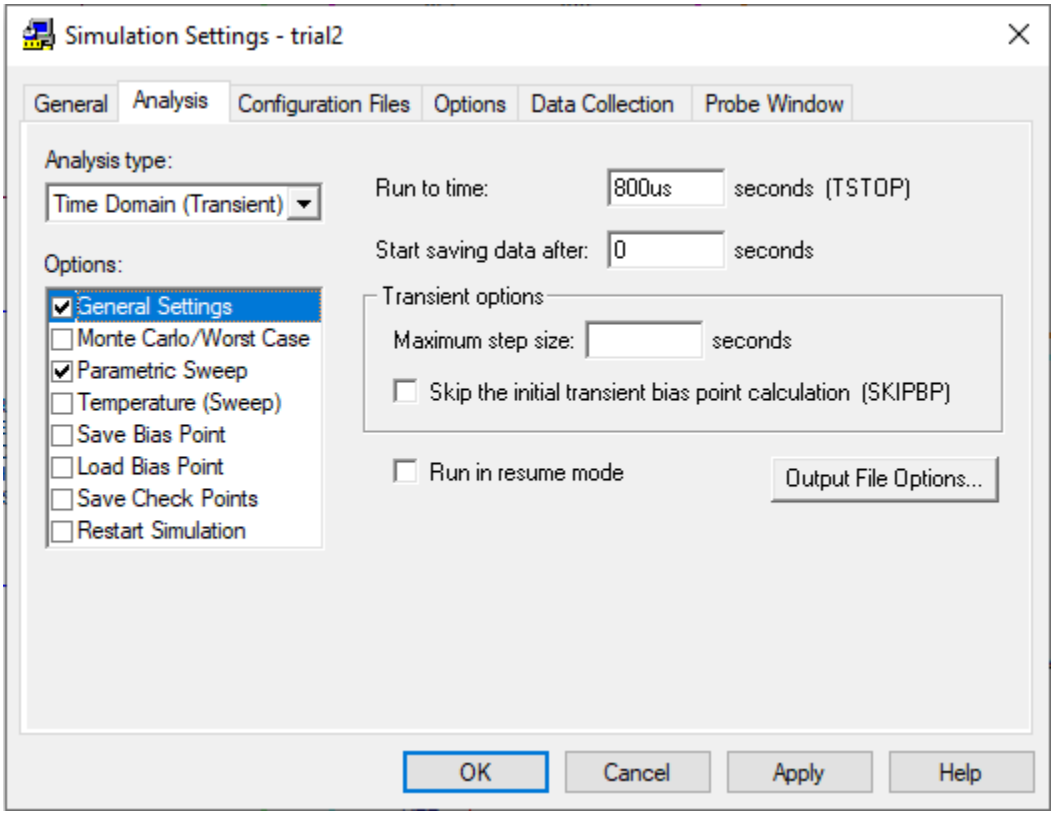

Figure 32. Time domain simulation settings

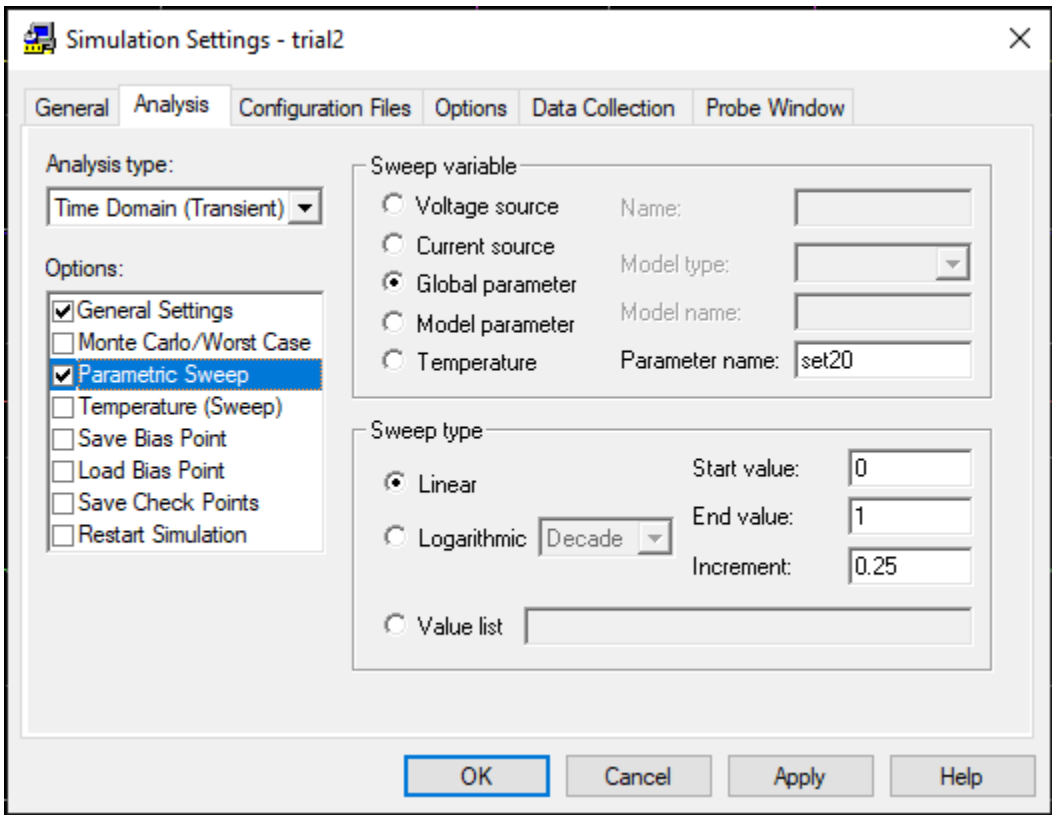

Figure 33. Parametric sweep simulation settings

```
Step param set20 =   0      27.0 Deg
Step param set20 =   .25    27.0 Deg
Step param set20 =   .5     27.0 Deg
Step param set20 =   .75    27.0 Deg
Step param set20 =   1      27.0 Deg
```

Figure 35. Available sections

Trace Color	Trace Name	Y1
	X Values	141.011u
CURSOR 1,2	V(OUT)	2.0117
	V(OUT)	3.4867
	V(OUT)	4.9710
	V(OUT)	6.4651
	V(OUT)	7.9697

Figure 34. The amplitudes we can obtain with a 0.25 increment

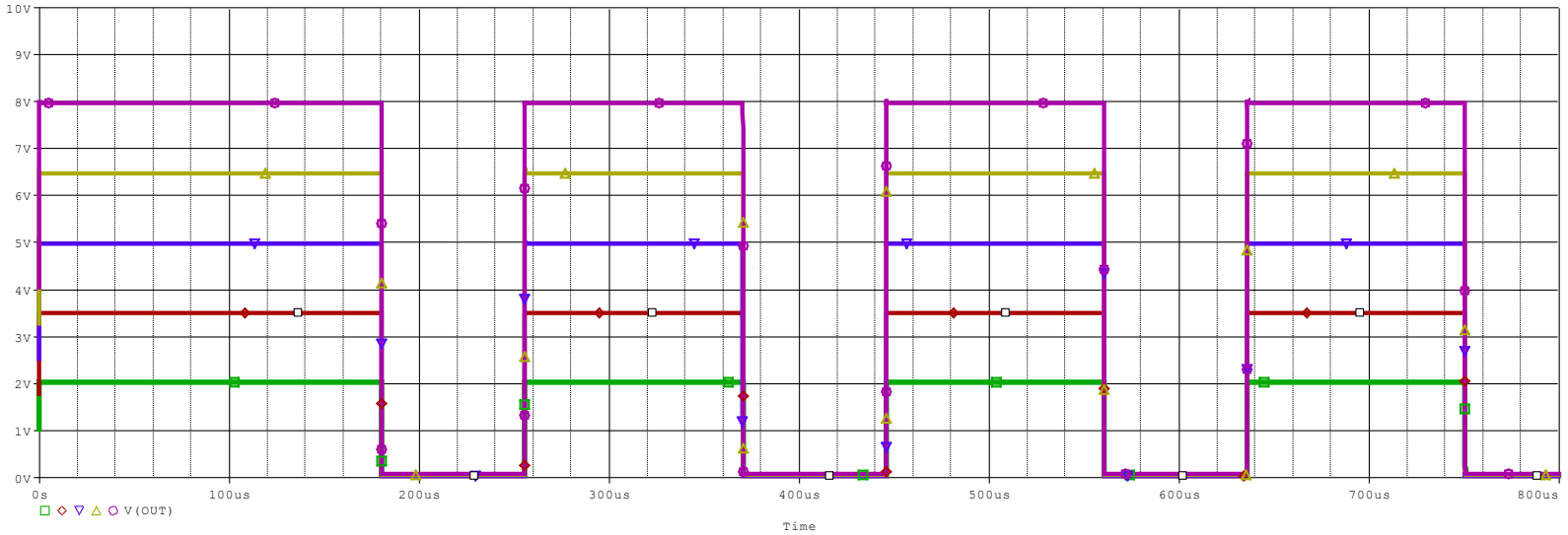

Figure 36. The variation of the output with respect to the value of set20

5. Conclusion

The PWM generator is used to control and adjust the total power delivered to a load, in other words, controlling the output voltage of the converter by modulating the width of the pulse of the output waveform. [11]

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