



## **Faculty of Engineering**

# **Computer Engineering Department**

# **Computer Architecture Project**

# Supervised by

Dr. Mayada Hadhood

## By

Giath Ajam
Ahmed Hamdy Nossir
Ahmed Sayed Saif
Yousef Atef Elshabrawy

## 1) Instruction format

Instruction Bits details

There will be 2 types of instructions : -

#### o 16 bit instruction

Т		operat	ion	func		rd		rs		rt		хххх
15	15	/14	13	/12	10	0/9	7	/6	4/3	3	1	0

## o 32 bit instruction

		func	rd	rs	хххх	Offset/immediate
Т	operation					
31	31/30	29/28 20	6/25 2	23/22 2	0/19 1	6/15 0

## • Opcode of each instruction

#### o 16 bit instruction

T (instruction type)	Correspond to
0	16 bit instruction
1	32 bit instruction

operation	Correspond to	
0 0	1 – operand	
0 1	2 – operand	
1 0	Memory	
1 1	Branch	

Reg addresses	Correspond to
000	R0
001	R1
010	R2
011	R3
100	R4
101	R5
110	R6
111	R7

Operation type	function	Op code
1- operand	NOP	000
1- operand	HLT	001
1- operand	SETC	010
1- operand	NOT Rdst	011
1- operand	INC Rdst	100
1- operand	OUT Rdst	101
1 - operand	IN Rdst	110
2- operand	MOV	000
2- operand	ADD	001
2- operand	SUB	010

2- operand	AND	011	
memory	PUSH	000	
memory	POP	001	
branch	JZ	000	
branch	JN	001	
branch	JC	010	
branch	JMP	011	
branch	CALL	100	
branch	RET	101	
branch	INT	110	
branch	RTI	111	

#### o 32 bit instruction

The op code will be the same except some changes

Operation op code	Correspond to
X 0	2- operand
X 1	memory

Operation type	function	Op code
2- operand	IADD	000
Memory	LDM	000
Memory	LDD	001
Memory	STD	010



