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NATIONAL INSTITUTE OF TECHNOLOGY SILCHAR

CACHAR, ASSAM

LABORATORY EXERCISE BOOK

B.TECH. IIIRD SEM.

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SCH. ID.: 1912160

BRANCH: CSE - 'B'

SUBJECT: CIRCUIT AND SWITCHING LAB

CODE : EC-222

09/12/2020
Experiment-07

AIM: ANALYSIS AND SYNTHESIS OF SEQUENTIAL CIRCUITS USING BASIC FLIP-FLOPS.

THEORY:

The logic circuits whose outputs at any instant of time depend not only on the present input ~~by~~ but also on the past outputs are called sequential circuits. The simplest kind of sequential circuit which is capable of storing one bit of information is called latch. The operation of basic latch can be modified, by providing an additional control input that determines, when the state of the circuit is to be changed. The latch with additional control input is called the flip-flop. The additional control input is either the clock or enable input. There are four basic types of flip-flops:

1) SR flipflop
2) JK flipflop
3) D flipflop
4) T flipflop

1) SR flipflops: The SR flipflop basically consists of two NOR gates and also two NAND gates. It can also be made using only NAND gates.

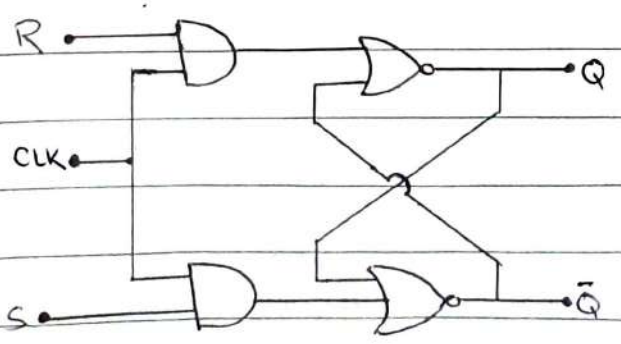

fig. 7.1: Clocked NOR based SR flipflop

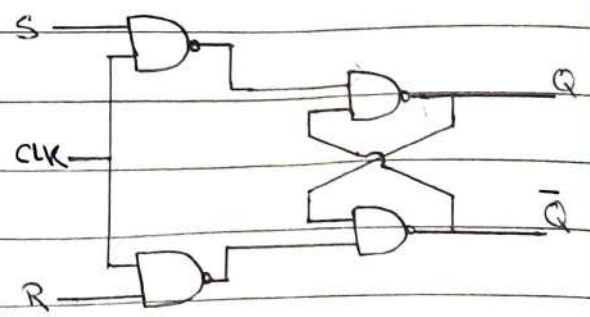

fig. 7.2: Clocked NAND based SR Flipflop

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S	R	Q_{t+1}
0	0	Q_t
0	1	0
1	0	1
1	1	Not Used

fig. 7.3: Truth Table of SR flipflop

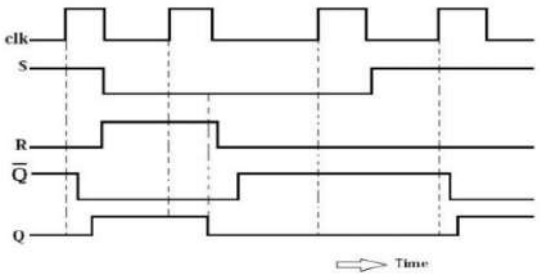

fig. 7.4: Typical Waveform in SR Flipflop

2) JK Flipflop: The JK flipflop is basically a gated SR flipflop with the addition of a clock input circuitry.

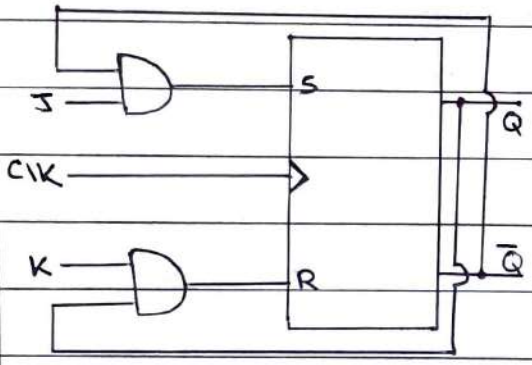

fig. 7.5: JK flipflop using SR flipflop

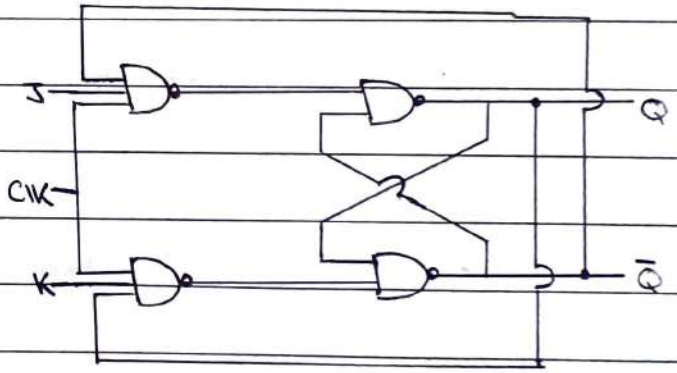

fig. 7.6: NAND based JK flipflop

J	K	Q_{t+1}
0	0	Q_t
0	1	0
1	0	1
1	1	$\bar{Q}_t$

fig. 7.7: Truth table of JK flipflop

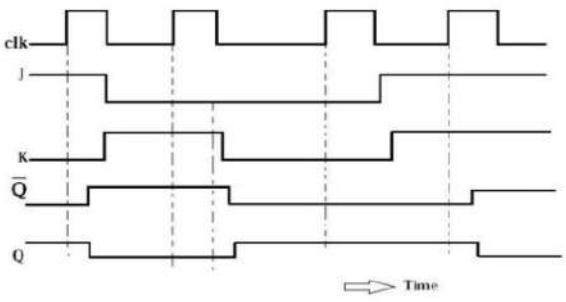

fig. 7.8: Typical Waveform in JK Flipflop

3) D flipflops: D flipflop captures the D-input value at the specified edge (ie, rising or falling) of the clock.

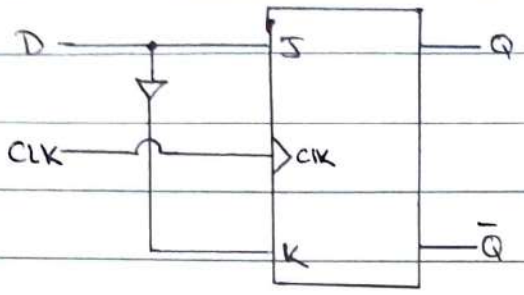

fig: 7.9: D flipflop using JK flipflop

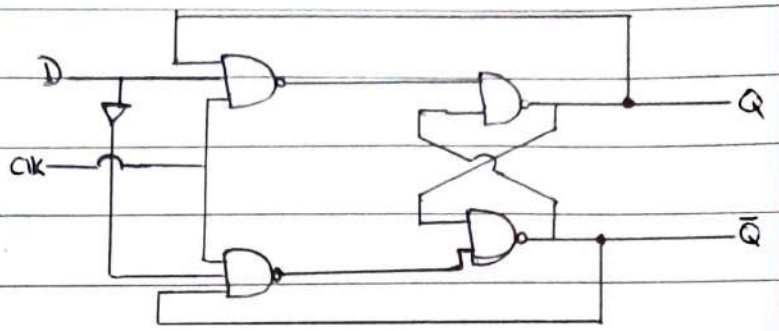

fig. 7.10: NAND-Based D flipflop

D	Q_{t+1}
0	1
1	1

fig: 7.11: Truthtable of D flipflop

Synthesis using flipflop:

We can verify the operation of a serial (sequential) adder (1 bit full adder) carry output of a one bit full adder can be fed back to the input of a D flipflop. The output of this flipflop can be fed back to the carry input of that adder.

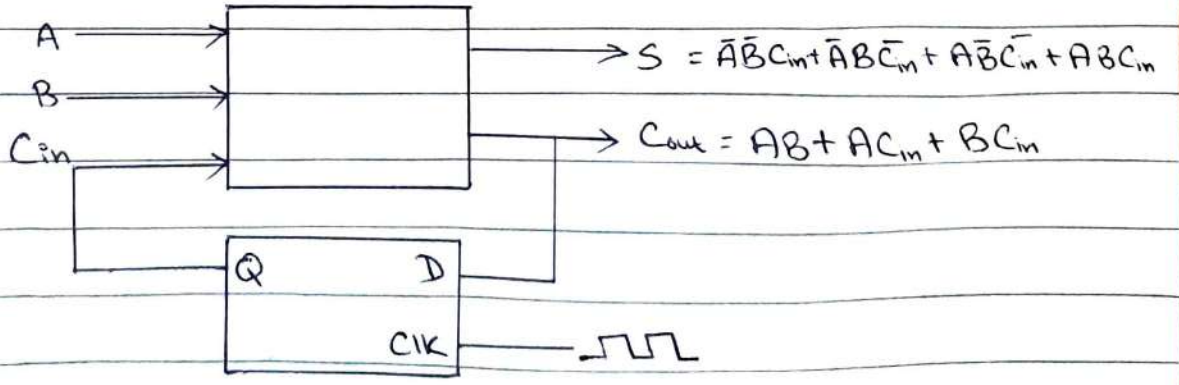

fig. 7.12: Verification of the functionality of a combinational circuit using sequential element (flipflop)

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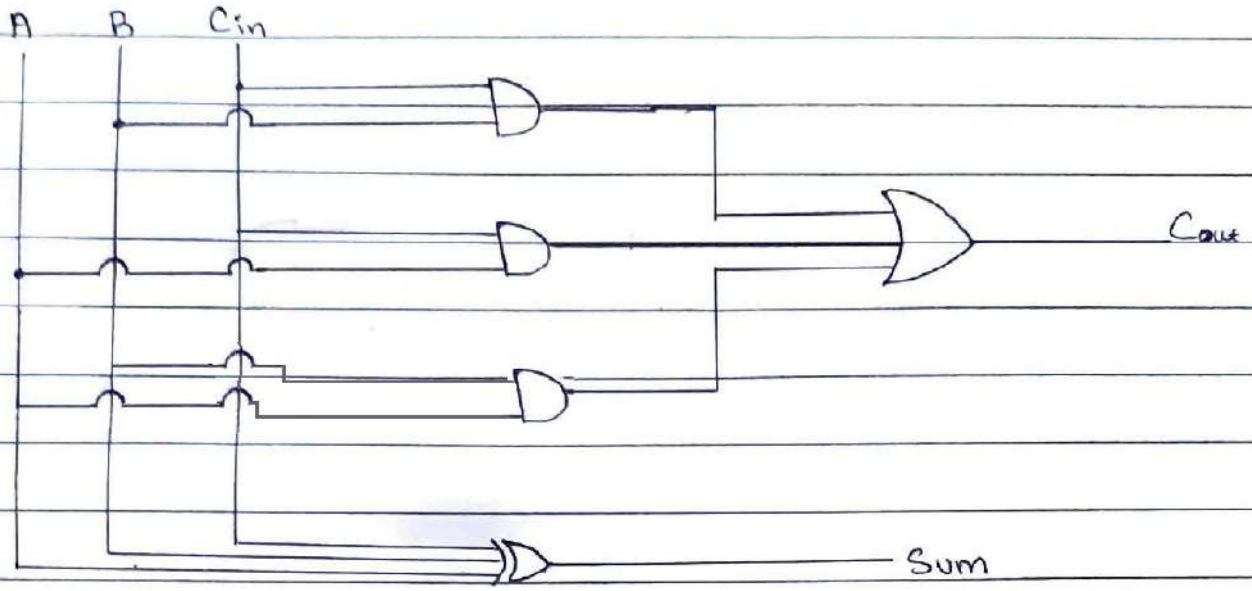

fig. 7.13: Gate diagram of Combinational Circuit (1 bit full adder)

A	B	Cin	Sum	Cout
0	0	0	0	0
0	1	0	1	0
1	0	0	1	0
1	1	0	0	1
0	0	1	1	0
0	1	1	0	1
1	0	1	0	1
1	1	1	1	1

fig. 7.14: Truth table of a 1 bit full adder.

Circuit Diagram

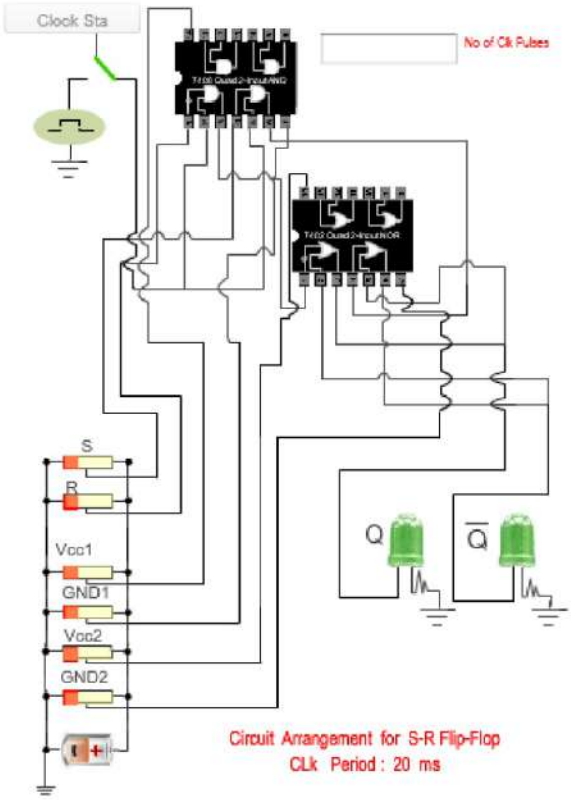

fig. 7.15: Circuit Diagram of SR FlipFlop

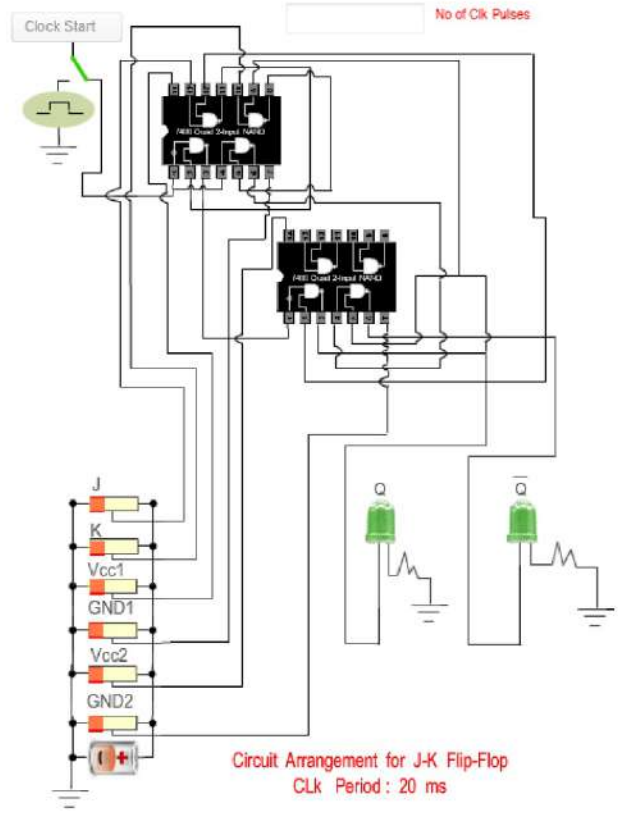

fig. 7.16: Circuit Diagram of JK FlipFlop

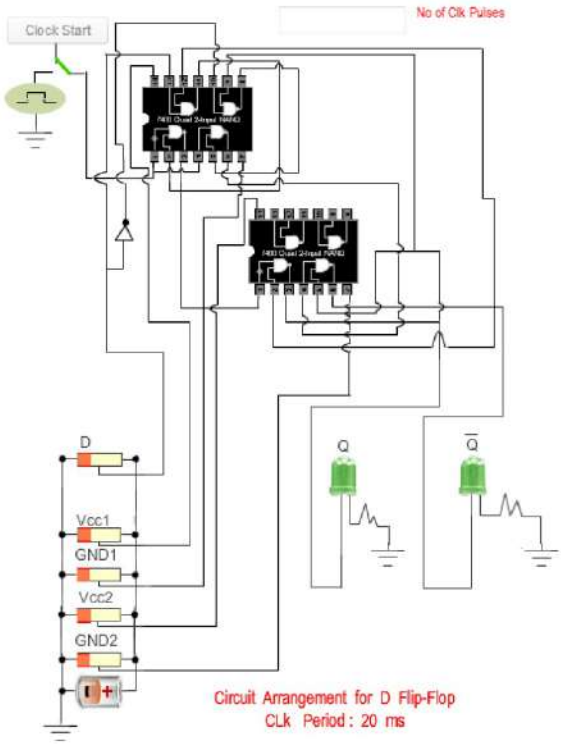

fig. 7.17: Circuit Diagram of D Flip FLop

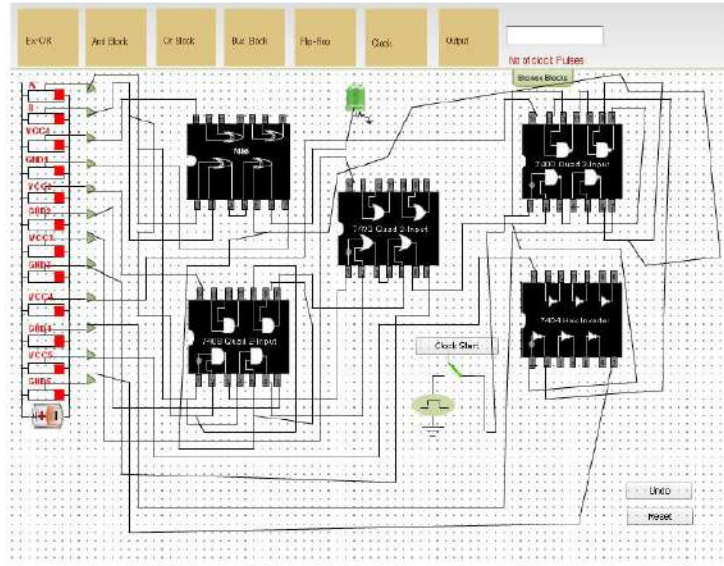

fig. 7.18: Circuit Diagram of 1-bit Full Adder using D FlipFlop

Observations

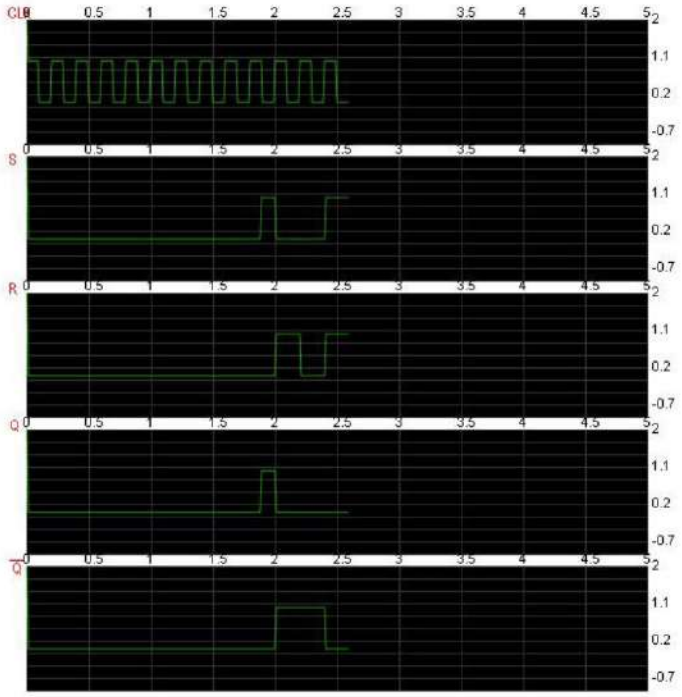

fig. 7.19: Timing Diagram of SR Flipflop

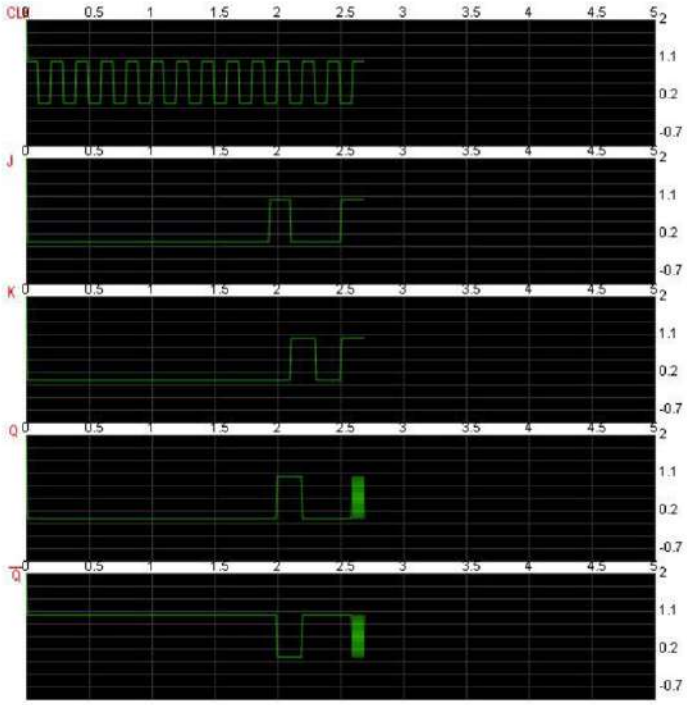

fig. 7.20: Timing Diagram of JK Flipflop

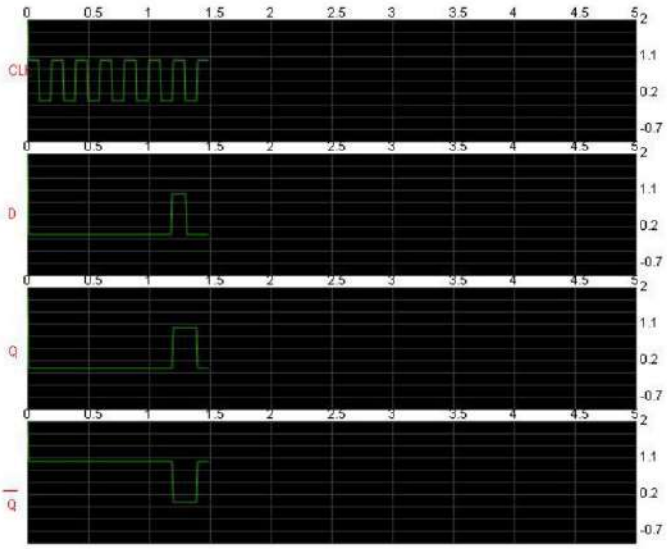

fig. 7.21: Timing Diagram of D Flipflop

RESULT:

The timing diagrams were obtained as shown in fig. 7.19, 7.20, 7.21 after inserting all inputs correctly in the circuits as shown in fig. 7.15, 7.16 and 7.17. In fig. 7.18, Serial 1 bit full adder was made using D flipflop. Hence, the sequential circuits were analysed and synthesised using the basic gates.