NATIONAL INSTITUTE OF TECHNOLOGY SILCHAR

CACHAR, ASSAM

DEC, 2020

B. TECH. IIIRD SEMESTER

SUBJECT: EC-221

PROJECT ON: DESIGN OF A THREE-STAGE SYNCHRONOUS COUNTER TO REPEAT THE NUMBER SEQUENCE: 0, 1, 3, 2, 6, 7, 5, 4 IN BINARY USING JK FLIPFLOPS AND K-MAPS.

SUBMITTED BY:

Name: Subhojit Ghimire

Branch: CSE - B

Sch. Id.: 1912160

UNDER THE GUIDANCE OF:

Dr. S.K. Tripathy

Assistant Professor

Department of ECE

NIT Silchar

Number Sequence : 0, 1, 3, 2, 6, 7, 5, 4

In binary : 000 → 001 → 011 → 010 → 110 → 111 → 101 → 100

Clearly, the synchronous counter we are dealing with counts the Gray code, hence, this project can also be named 3-bit Gray code counter.

STEP I : State Diagram:

The 3-bit Gray code counter has no inputs other than the clock and no outputs other than the outputs taken off each flip-flop in the counter.

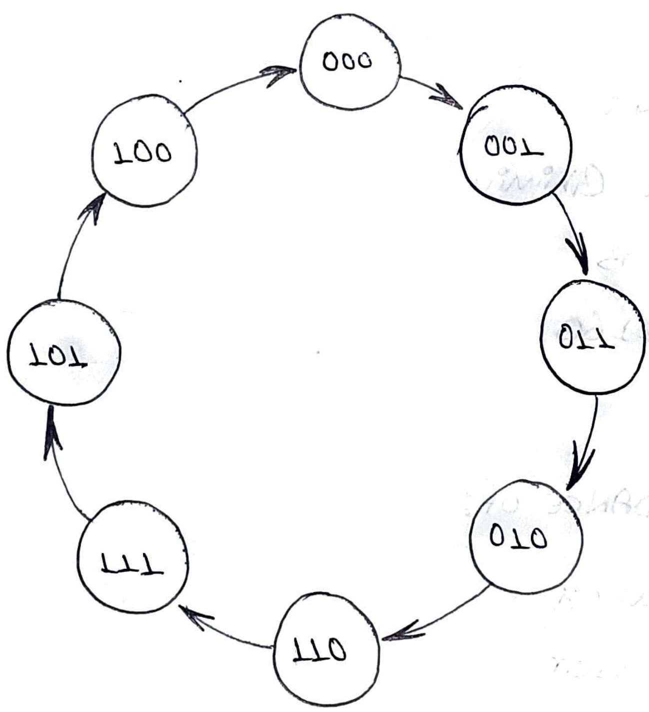

fig.: State diagram for 3-bit Graycode Converter

STEP II : Next-State Table:

The next state is the state that the counter guesses to from its present state upon application of a clock pulse. The next-state table is derived from the state diagram and for the 3-bit Gray code counter, the next-state table is as follows:

PRESENT STATE			NEXT STATE		
Q_2	Q_1	Q_0	Q_2	Q_1	Q_0
0	0	0	0	0	1
0	0	1	0	1	1
0	1	1	0	1	0
0	1	0	1	1	0
1	1	0	1	1	1
1	1	1	1	0	1
1	0	1	1	0	0
1	0	0	0	0	0

Table: Next-State table for 3-bit Gray Code Counter

STEP III : FLIP-FLOP Transition Table :

OUTPUT TRANSITIONS		FLIP-FLOP INPUTS	
Q_N	Q_{N+1}	J	K
0 $\longrightarrow$	0	0	X
0 $\longrightarrow$	1	1	X
1 $\longrightarrow$	0	X	1
1 $\longrightarrow$	1	X	0

Table: Transition table for a J-K flipflop

To design the counter, the transition table is applied to each of the flip-flops in the counter, based on the next-state table. For example, for the present state 000, Q_0 goes from a present state of 0 to a next state of 1. To make this happen, J_0 must be a 1 and K_0 is don't care ($J_0 = 1$, $K_0 = x$). Next, Q_1 is 0 in the present state and remains 0 in the next state. For this transition, $J_1 = 0$ and $K_1 = x$. Similarly, for Q_2, it is 0 in the present state and remains 0 in the next state, therefore, $J_2 = 0$ and $K_2 = x$.

STEP IV: Karnaugh Maps:

$Q_2Q_1 \backslash Q_0$	0	1
00	0	0
01	1	0
11	x	x
10	x	x

J_2

$Q_2Q_1 \backslash Q_0$	0	1
00	0	1
01	x	x
11	x	x
10	0	0

J_1

$Q_2Q_1 \backslash Q_0$	0	1
00	1	x
01	0	x
11	1	x
10	0	x

J_0

$Q_2Q_1 \backslash Q_0$	0	1
00	x	x
01	x	x
11	0	0
10	1	0

K_2

$Q_2Q_1 \backslash Q_0$	0	1
00	x	x
01	0	0
11	0	1
10	x	x

K_1

$Q_2Q_1 \backslash Q_0$	0	1
00	x	0
01	x	1
11	x	x
10	x	1

K_0

fig: Karnaugh Maps for present state J and K inputs

STEP V : Logic Expressions for Flipflop Inputs:

From the K-maps above, the following expressions for the J and K inpust of each flipflop are obtained:

$$J_0 = Q_2 Q_1 + \bar{Q}_2 \bar{Q}_1 = \overline{Q_2 \oplus Q_1}$$

$$K_0 = Q_2 Q_1 + Q_2 Q_1 = Q_2 \oplus Q_1$$

$$J_1 = \bar{Q}_2 Q_0$$

$$K_1 = Q_2 Q_0$$

$$J_2 = Q_1 \bar{Q}_0$$

$$K_2 = \bar{Q}_1 \bar{Q}_0$$

STEP VI : Counter Implementation:

This step is to implement the combinational logic from the expressions for the J and K inputs as obtained in Step-5 and to connect the flipflops to form the complete 3-bit Gray Code Counter as shown below.

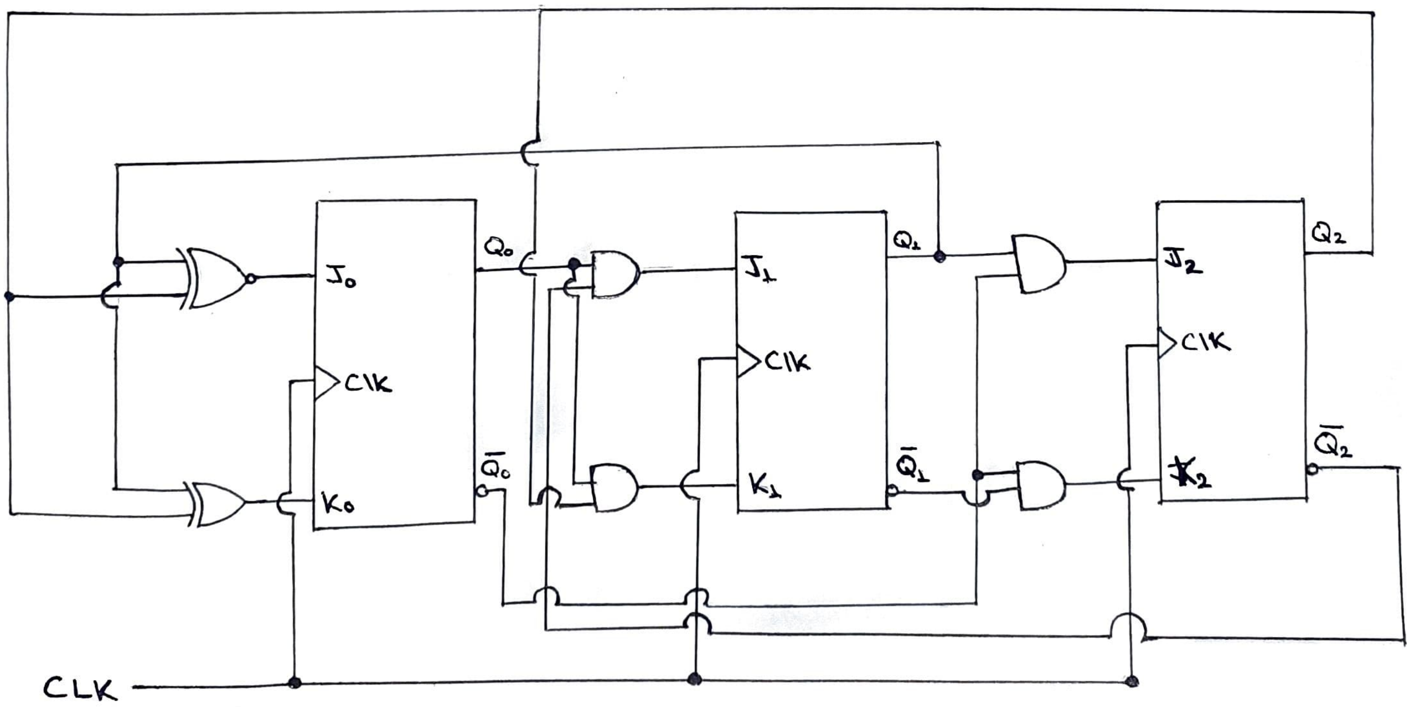

fig.: 3-bit Gray Code Counter Circuit