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NATIONAL INSTITUTE OF TECHNOLOGY SILCHAR

CACHAR, ASSAM

LABORATORY EXERCISE BOOK

B.TECH. IIIRD SEM.

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BRANCH: CSE - 'B'

SUBJECT: CIRCUIT AND SWITCHING LAB

CODE : EC-222

25/11/2020
Experiment-03

AIM: To verify the truth table and timing diagram of RS, JK, T and D flip-flops by using NAND and OR gates ICs and analyse the circuit of RS, JK, T and D flip-flops with the help of LEDs display.

THEORY:

A flip flop is an electronic circuit with two stable states that can be used to store binary data. The stored data can be changed by applying varying inputs. Flip-flops and latches are fundamental building blocks of digital electronics systems used in computers, communications and many more.

1. RS Flipflop: The basic NAND gate RS flipflop circuit is used to store the data and thus provides feedback from both of its outputs again back to its inputs. The RS flip flop has three inputs - SET, RESET and its current output Q relating to its current state.

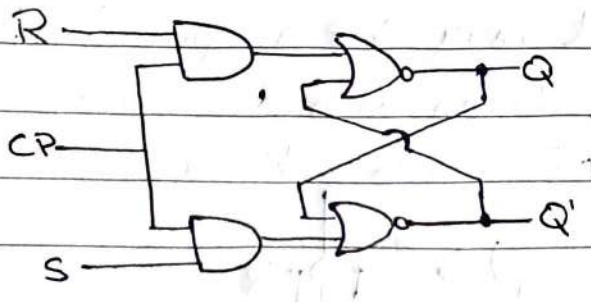

fig-3.1.: RS flipflop

CLK	S:	R	Q	STATE
×	0	0	No Change	Previous
↑	0	1	0	Reset
↑	1	0	1	Set
↑	1	1	-	forbidden

fig. 3.2: Characteristics table of RS flip flop.

2. D flipflop: A D flipflop has a single data input. This type of flipflop is obtained from the SR flipflop by connecting the R input through an inverter, and the S input is connected directly to data input. This modified clocked SR flipflop is known as D flipflop.

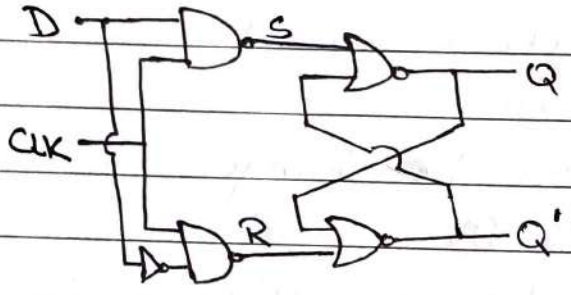

fig.: 3.3: D flipflop

D	reset	CLK	Q	Q'
0	0	0	0	1
0	0	1	0	1
0	1	0	0	1
0	1	1	0	1
1	0	0	0	1
1	0	1	1	0
1	1	0	0	1
1	1	1	0	1

fig.: 3.4: Characteristic table of D flipflop

3. JK flipflop: In a RS flipflop, the input R=S=1 leads to an indeterminate output. The RS flipflop circuit may be re-joined if both the inputs are 1 then also the outputs are complement of each other.

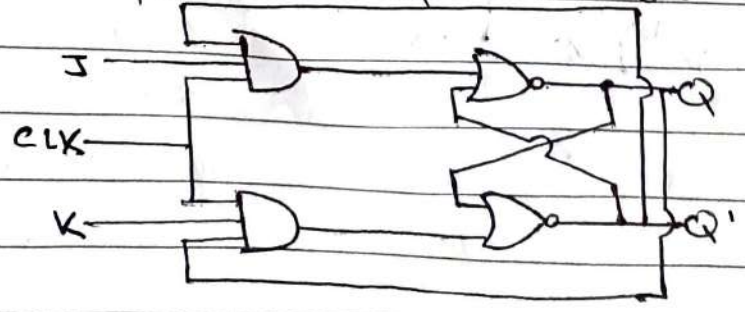

fig.: 3.5: JK flipflop

CLK	J	K	Q_n	Q_{n+1}	Inference
0	x	x	—	—	Latched
1	0	0	0	0	No Change
1	0	0	1	1	No Change
1	0	1	0	0	Reset
1	0	1	1	0	Reset
1	1	0	0	1	Set
1	1	0	1	1	Set
1	1	1	0	1	Toggle
1	1	1	1	0	Toggle

fig.: 3.6 : Characteristics table of JK flipflop

4. T FlipFlop : T flipflop is also known as toggle flipflop. The T flipflop is modification of the JK flipflop. Both the JK flipflop are held at logic 1 and the clock signal continuous to change.

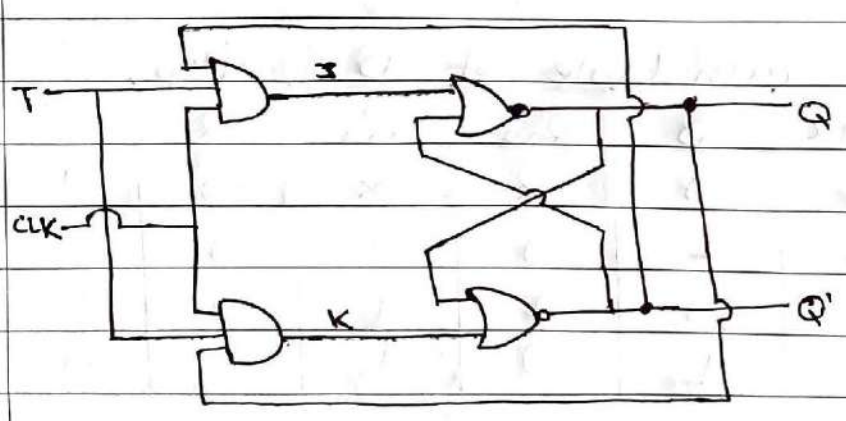

fig.: 3.7: T flipflop

CLK	T	Q	Q'
1	0	Q	Q'
1	1	Q'	Q
0	x	Q	Q'

fig. 3.8: Characteristics Table of T flipflop

Circuit Diagram

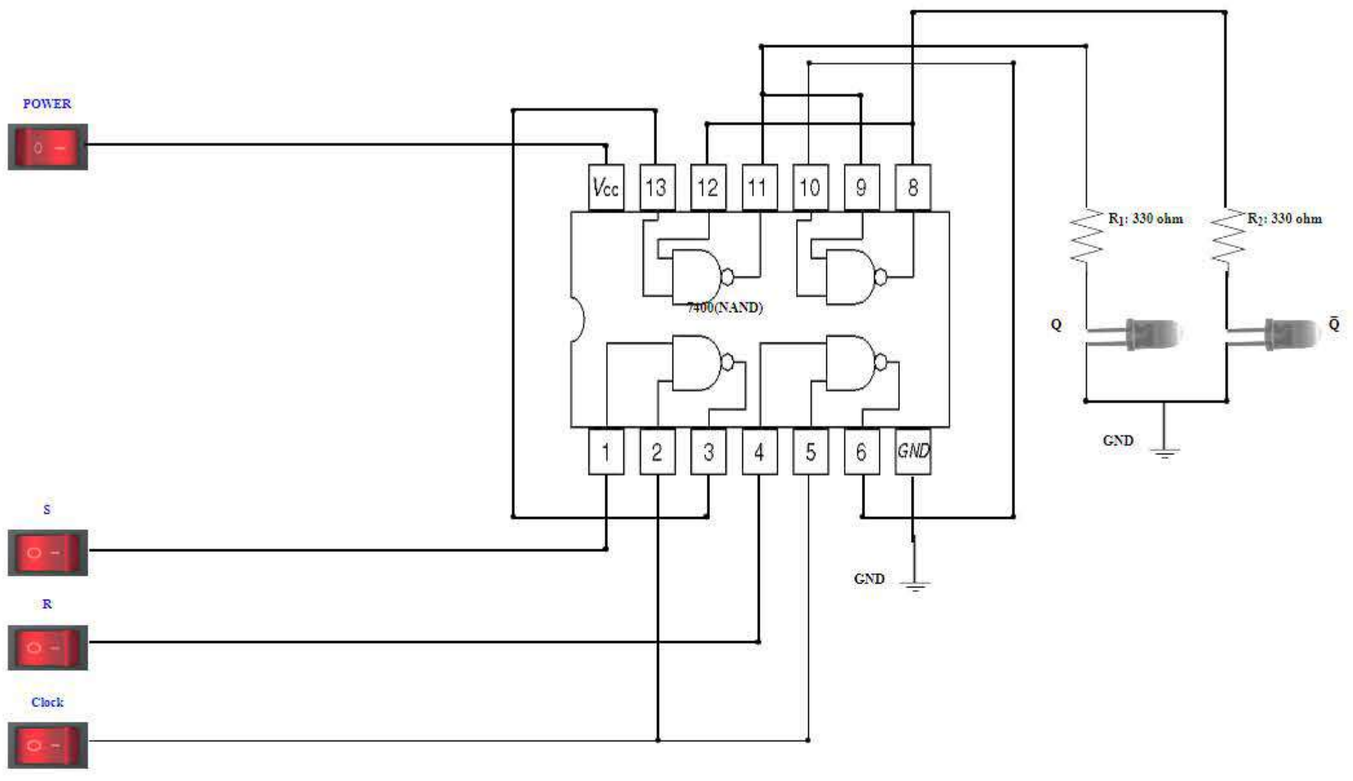

fig. 3.9: Circuit Diagram of SR FlipFlop

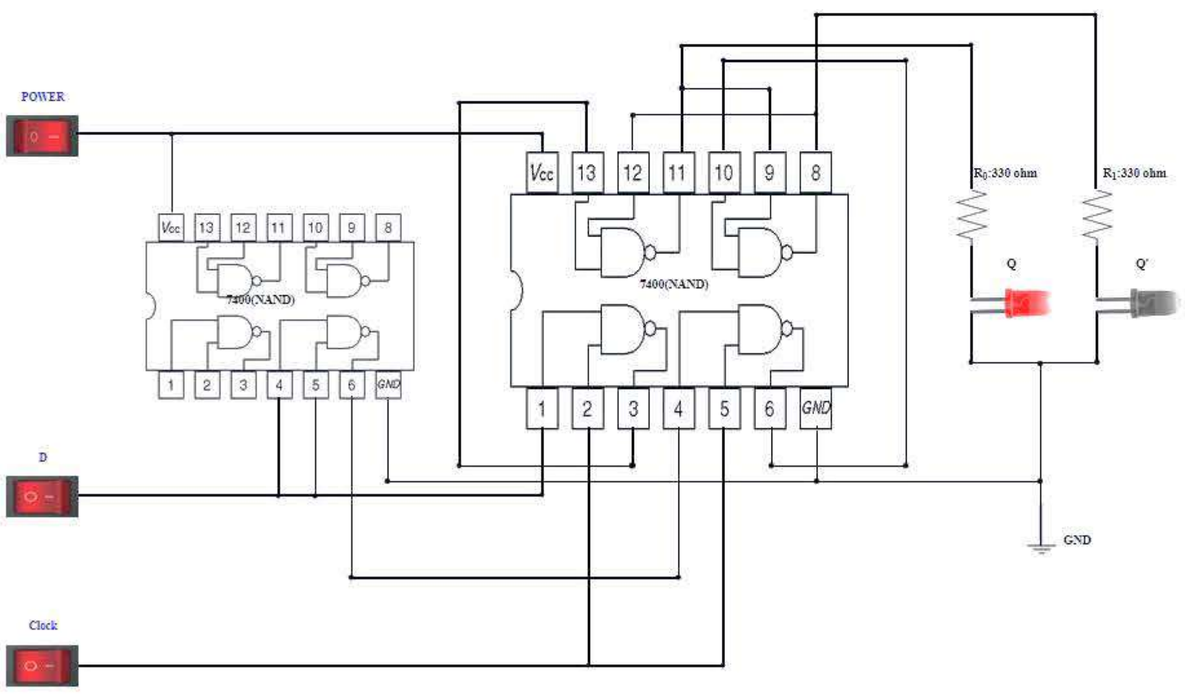

fig. 3.10: Circuit Diagram of D FlipFlop

Circuit Diagram

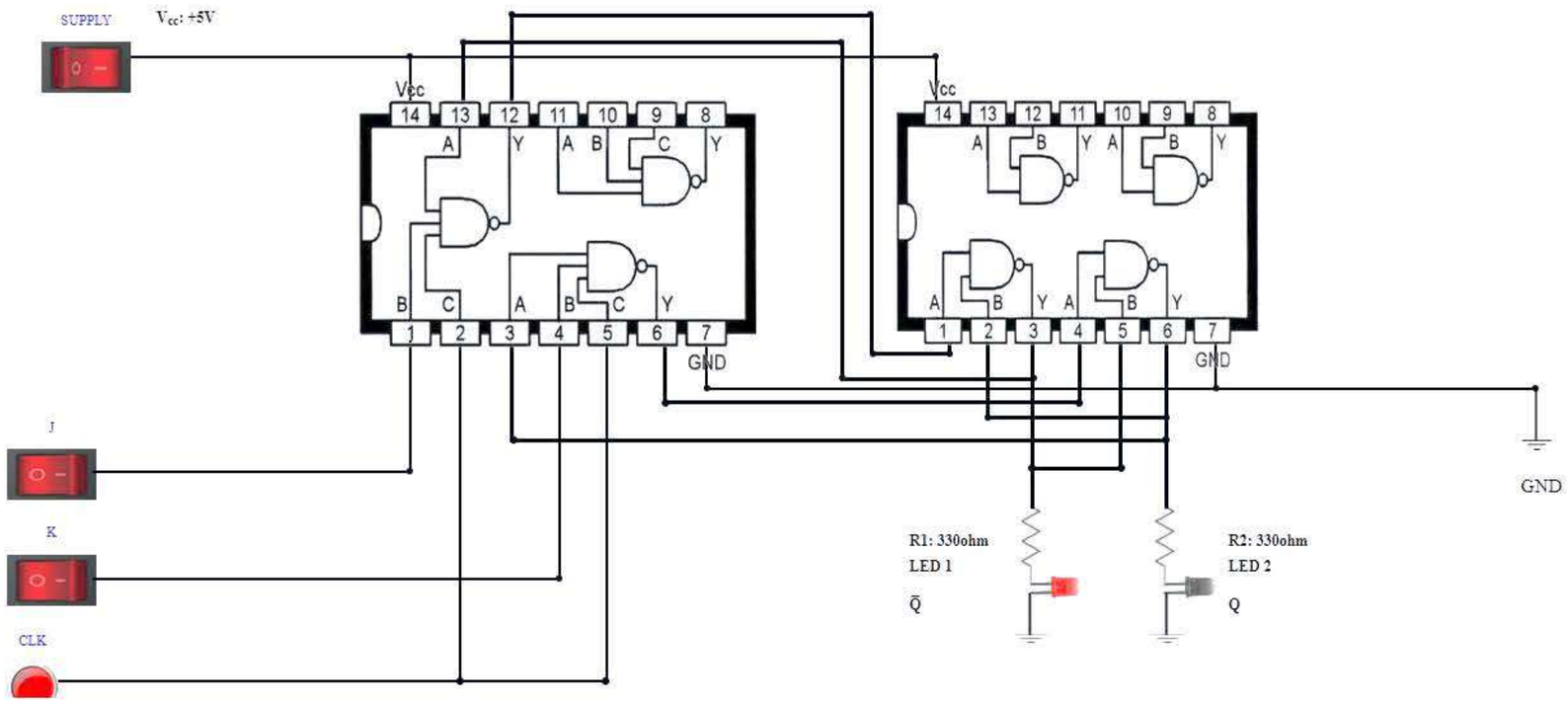

fig. 3.11: Circuit Diagram of JK FlipFlop

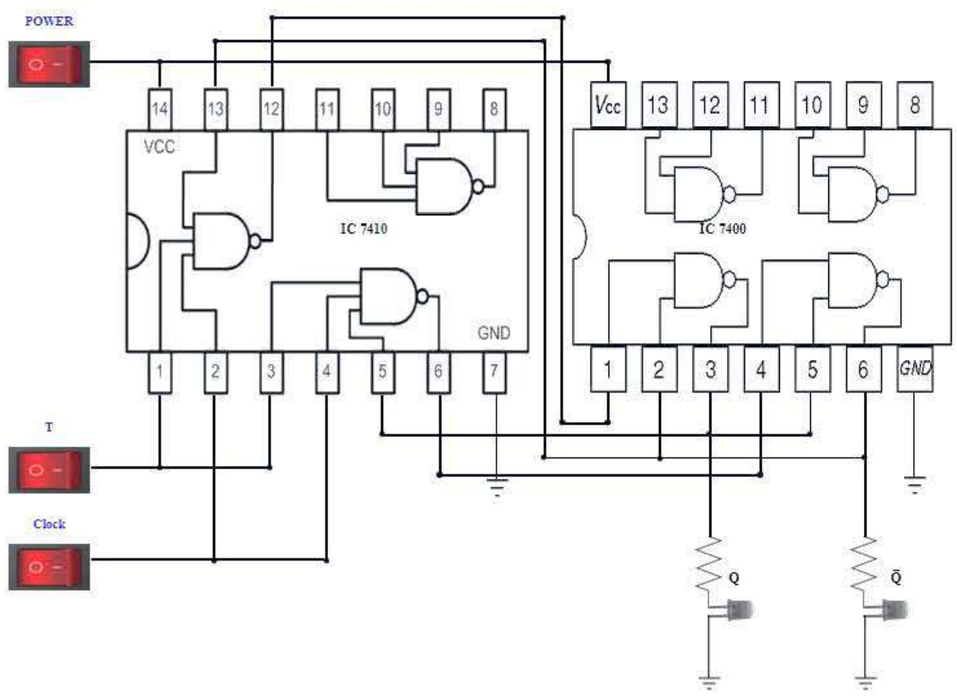

fig. 3.12: Circuit Diagram of T FlipFlop

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OBSERVATIONS:

Table 3.1: Truth table of SR flipflop

S.No.	Clock	S	R	Q_{n-1}	Q'_{n-1}	Q	Q'	Remark
1	0	0	0	x	x	0	1	No Change
2	1	0	1	0	1	0	1	Reset
3	1	1	0	0	1	1	0	Set
4	1	1	1	1	0	0	1	Invalid

Table 3.2: Truth table of JK flipflop

S.No.	Clock	J	K	Q_{n-1}	Q'_{n-1}	Q	Q'	Remark
1	0	0	0	x	x	0	1	No Change
2	1	0	0	0	1	0	1	No Change
3	1	0	1	0	1	0	1	Reset
4	1	1	0	0	1	1	0	Set
5	1	1	1	1	0	0	1	Toggle

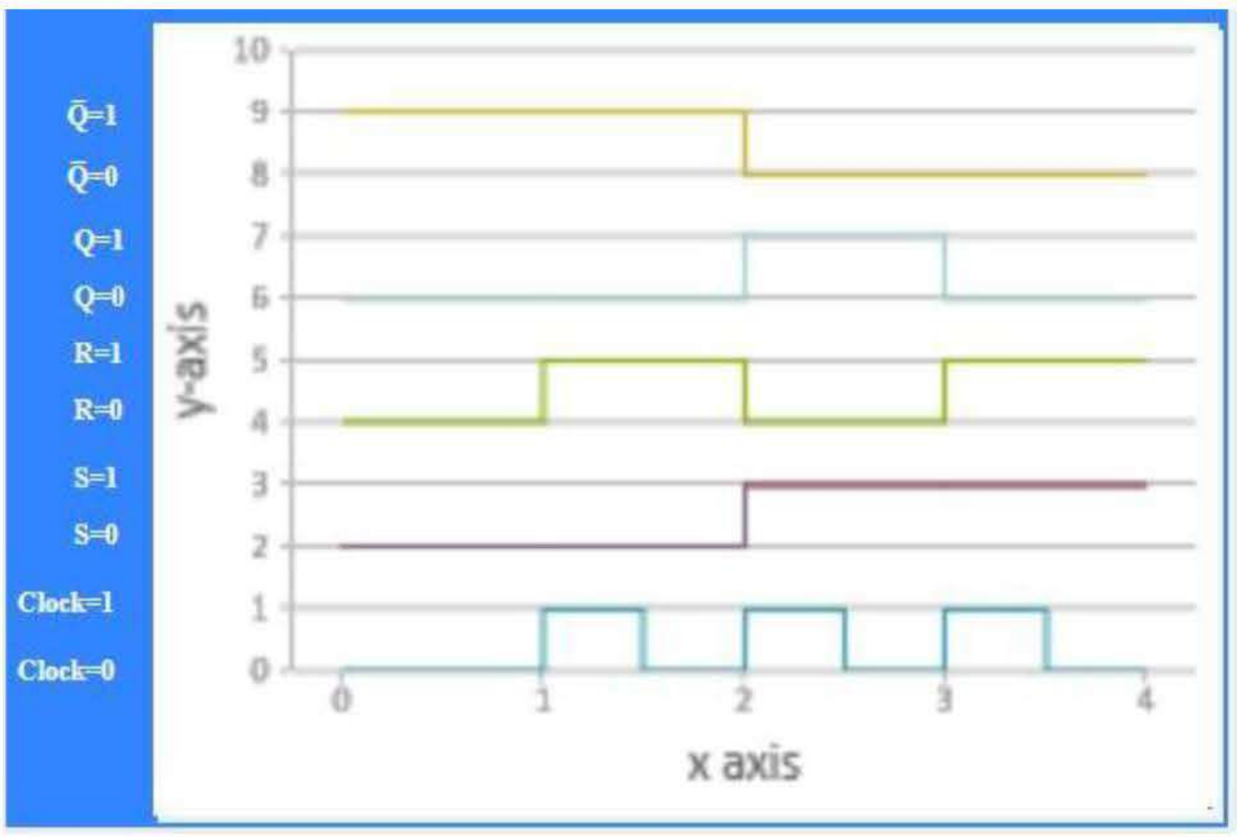

fig. 3.13: Clock Diagram of SR FlipFlop

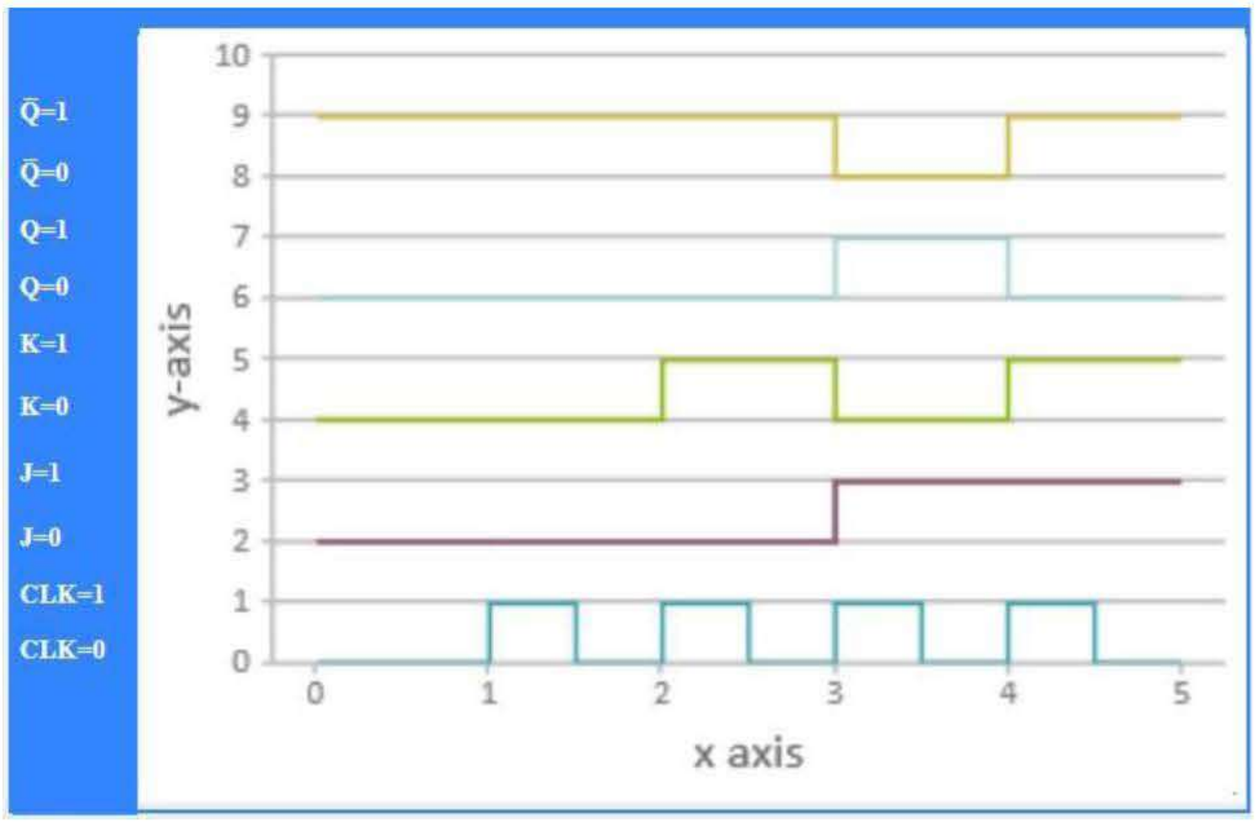

fig. 3.14: Clock Diagram of SR FlipFlop

Table 3.3: Truth table of D flipflop

S.No.	Clock	D	Q_{n-2}	Q_{n-1}	Q	Q'	Remark
1	0	0	x	x	0	1	No Change
2	0	1	0	1	0	1	No Change
3	1	0	0	1	0	1	Reset
4	1	1	0	1	1	0	Set.

Table 3.4.: Truth table of T flipflop

S.No.	Clock	T	Q_{n-1}	Q_{n-1}	Q	Q'	Remark
1.	0	0	x	x	0	1	No Change
2.	1	0	0	1	0	1	No Change
3.	1	1	0	1	1	0	Toggle.

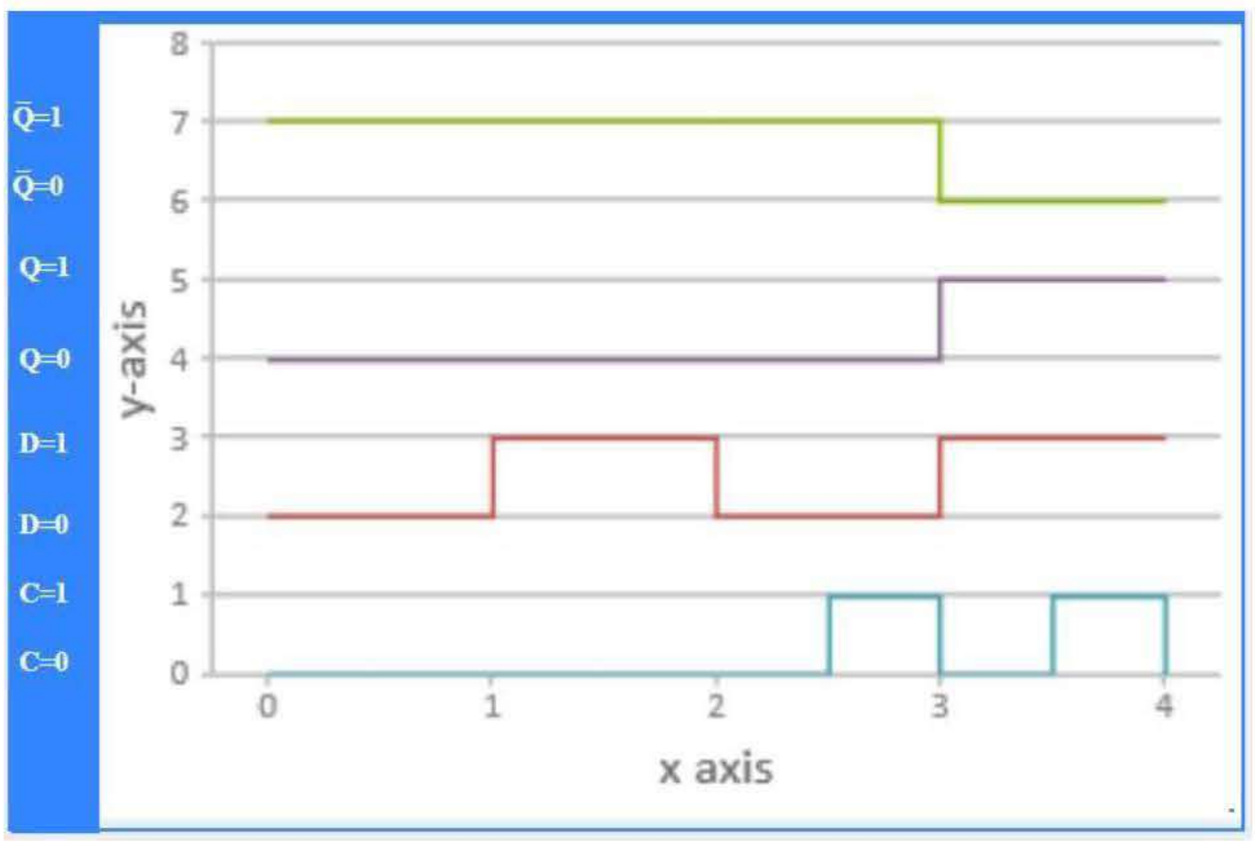

fig. 3.15: Clock Diagram of D FlipFlop

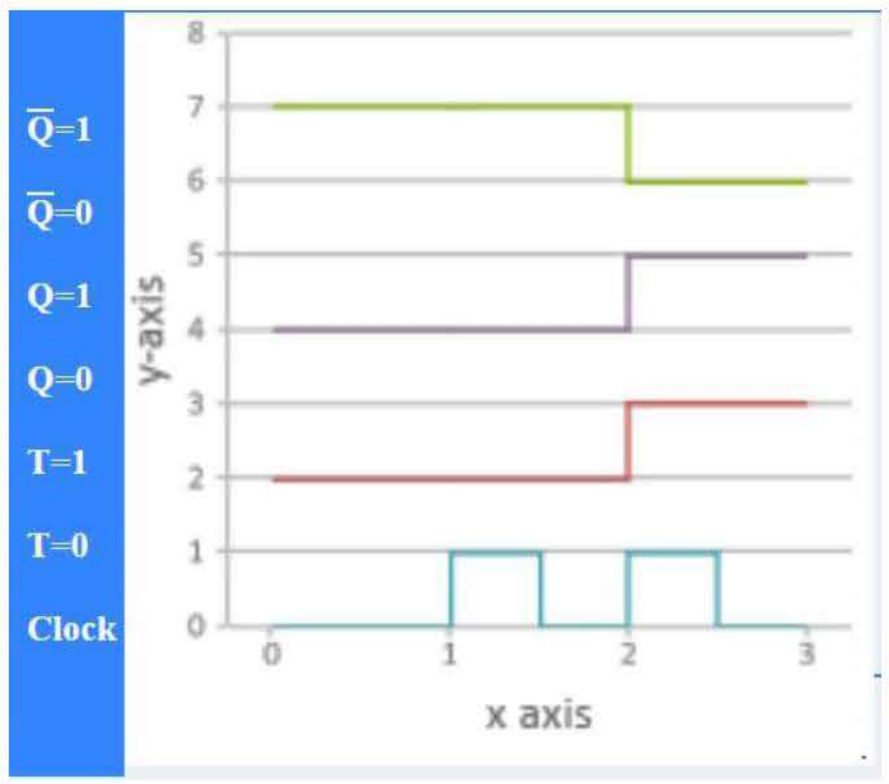

fig. 3.16: Clock Diagram of T FlipFlop

RESULT:

The truth table and clock diagram for SR, JK, D and T flipflops were obtained as shown in Table 3.1 - 3.4 and fig. 3.13 - 3.16, respectively.

25/11/2020
Experiment-04

AIM: To Analyse The Circuit and Truth Table of 4-Bit SIPO Shift Register By Using IC7474 (D Flipflop).

THEORY:

In SIPO (Serial In Parallel Out) shift registers, the data is stored into the register serially while it is retrieved from it in parallel-fashion. Figure 4.1. shows an n-bit synchronous SIPO shift register sensitive to positive edge of the clock pulse. Here the data word which is to be stored (Data IN) is fed serially at the input of the first flipflop (D1 of FF1). It is also seen that the inputs of all other flipflops (except the first flipflop FF1) are driven by the outputs of the preceding ones, like the input of FF2 is driven by the output of FF1. In this kind of shift register, the data stored within the register is obtained as a parallel output data word (Data out) at the individual output pins of the flip-flops (Q_1 to Q_n).

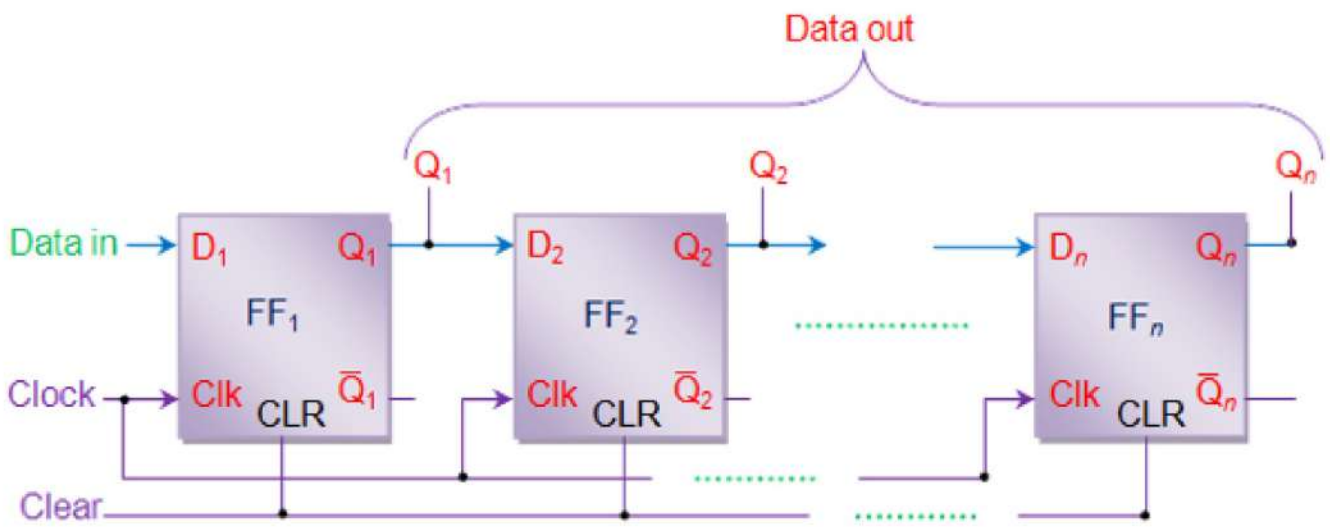

fig. 4.1: n-bit Serial-In Parallel-Out Shift Register

Analysing on the same grounds, one can note that the n-bit input data word is obtained as an n-bit output data word from the shift register at the rising edge of the n^{th} clock pulse. This working of the shift-register can be summarised as in Table 4.1 and the corresponding waveforms as given in figure 4.2.

Clock Cycle	Data in	Q_1	Q_2	...	Q_n
1	B_1 →	B_1	0	...	0
2	B_2 →	B_2	B_1	...	0
3	B_3 →	B_3	B_2	...	0
4	B_4 →	B_4	B_3	...	0
5	B_5 →	B_5	B_4	...	0
6	B_6 →	B_6	B_5	...	0
.	.	.	.	...	.
.	.	.	.	...	.
.	.	.	.	...	.
n	B_n →	B_n	B_{n-1}	...	B_1

Output of SIPO (right-shift) Shift Register

Table 4.1: Data movement in Right Shift SIPO Shift Register

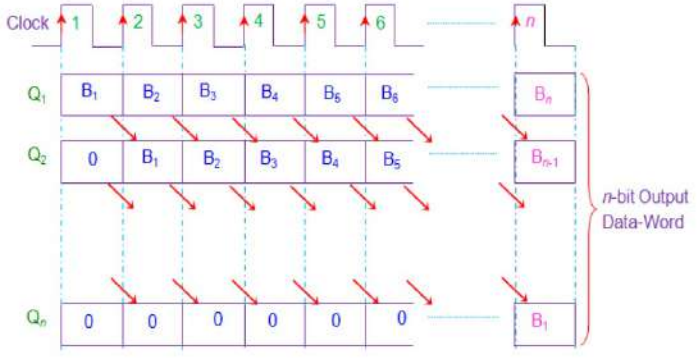

Fig. 4.2: Output Waveform of n-bit Right Shift SIPO Shift Register

In the right shift SIPO shift register, data bits shift from left to right for each clock pulse. However if the data bits are made to shift from right to left in the same design, one gets a left shift SIPO shift-register as shown in figure 4.3. Nevertheless, the basic working principle remains the same except the fact that now B_n down to B_1 is stored in Q_n down to Q_1 i.e, $Q_1 = B_1$, $Q_2 = B_2$, ... $Q_n = B_n$ at the n^{th} clock pulse.

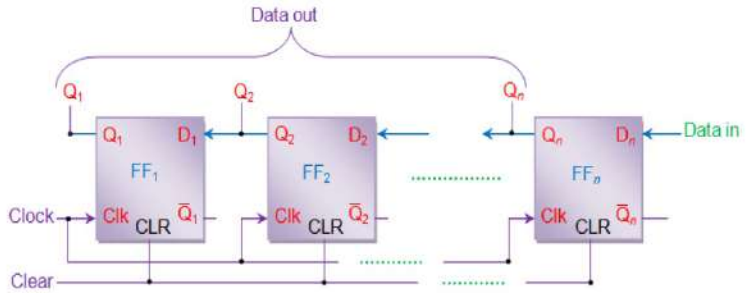

fig. 4.3: n-bit Left Shift SIPO Shift Register

Circuit Diagram

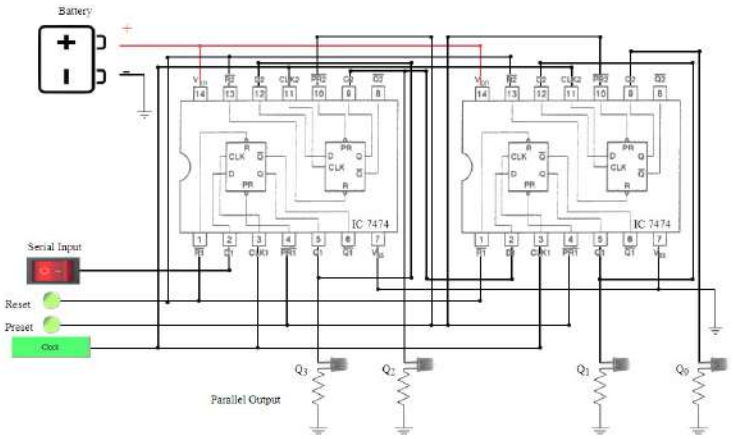

fig. 4.4: Circuit Diagram of 4-bit SIPO Shift Register

OBSERVATION TABLE:

Table 4.2.: Truth Table of 4-bit of SIPO Shift Register

S.No.	Clock	Input Data	Q_3	Q_2	Q_1	Q_0
1	0	0	0	0	0	0
2	1	1	1	0	0	0
3	2	0	0	1	0	0
4	3	0	0	0	1	0
5	4	0	0	0	0	1
6	5	0	0	0	0	0

RESULT:

The truth table for 4-Bit Serial-In Parallel-Out Shift Register was obtained as shown in the Table 4.2