Subject: Computer Architecture and Organisation.
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Q.1.

Soln:

(a) $xT: AR \leftarrow AR, \quad AR \leftarrow 0$

The value is stored as well at cleared at the same time, which is not possible.

(b) $yT: R1 \leftarrow R2, \quad R1 \leftarrow R3$

The values R2 and R3 are stored in R1 at the same time, which is not possible.

(c) $zT: AR, \quad PC \leftarrow PC+1$

The value of PC is incremented the same time (PC+1) is being stored in PC, i.e., two process at the same time, which can not be possible.

Q.2.

Soln:- (a) 245.625

Step I: Binary Conversion:

$(245.625)_{10} \longrightarrow (11110101.101)_2$

Step II: Normalisation:

$(-1) \times 1.1110101101 \times 2^7$

Step III: Biased-exponent:

$7 + 127 = 134$

$(134)_{10} = (10000110)_2$

Step IV: Single precision(IEEE):

0	10000110	11101011010
S (1)	E (8)	M (23)

(b) 1/16

$= 0.0625$

Step I: Binary Conversion:

$(0.0625)_{10} \longrightarrow (0.0001)_2$

Step II: Normalisation:

$(-1)^0 \times 1.0 \times 10^0 \times 2^{-4}$

Step III: Biased Exponent:

$-4 + 127 = 123$

$(123)_{10} \rightarrow (1111011)_2$

Step IV: Single precision (IEEE):

0	1111011	0
S	E	M

Q.3.

Soln:-

Normalisation:

Normalisation in IEEE floating point refers to the case where the fraction is at least 1/b, where b represents base.

Excess-exponent:

Excess-exponent in IEEE floating point refers to the representation of negative exponents, i.e., it defines the placement for decimal points.

Special Values:

Special values in IEEE floating point refers to the bit patterns whose exponent field is all zeros or all ones have special values or meanings.

Q.4.

Soln:- Assumptions:

Fetch routine starts at location 0.

BRM macroinstruction at location 10.

10: IF ($AC_0 = 1$) THEN CAR ← 12 ; ELSE CAR ← (CAR+1)

11: CAR ← 13 ; PC ← (PC) + 1

12: PC ← (IR (address))

13: CAR ← 0

Q.5.

Soln:- Three inputs: x, y, z.

Three output: A, B, C

when, Binary input : 0, 1, 2 or 3; Binary output : 1, 2, 3 or 4

when, Binary input: 4, 5, 6 or 7 ; Binary output: 3, 4, 5 or 6.

Making truth table:

x	y	z	A	B	C
0	0	0	0	0	1
0	0	1	0	1	0
0	1	0	0	1	1
0	1	1	1	0	0
1	0	0	0	1	1
1	0	1	1	0	0
1	1	0	1	0	1
1	1	1	1	1	0

K-map for respective outputs:

x \ yz	00	01	11	10
0	0	0	1	0
1	0	1	1	1

$A = xz + xy + yz$

x \ yz	00	01	11	10
0	0	1	0	1
1	1	0	1	0

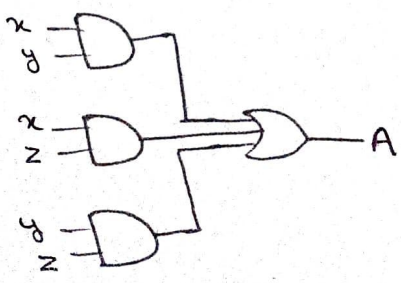
$B = x'y'z + x'yz' + xy'z' + xyz$

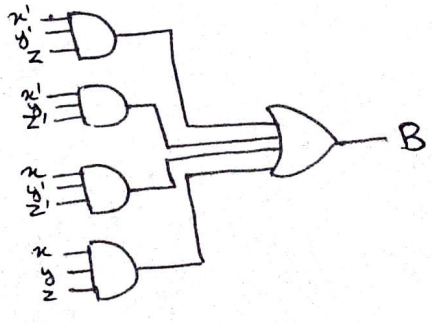
$= x \oplus y \oplus z$

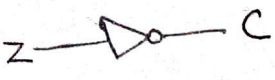
x \ yz	00	01	11	10
0	1	0	0	1
1	1	0	0	1

$C = z'$

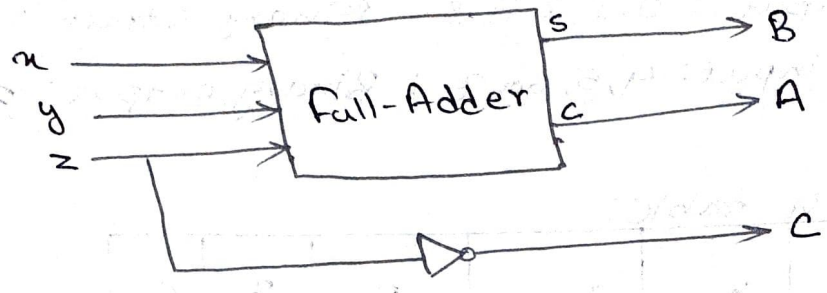
Logic - diagram for respective outputs:







The so-obtained Combinational Circuit:



Q.6.) Ans) (C) 10101010.... 1010

Q.7.) Ans) (B) Either S1 or S2

Q.8.) Ans) (D) I, II and III

Q.9.) Ans) (C) (i) and (iv)

Q.10. Ans) (A) C1640000H

Q.11. Ans) (D) Hardwired control, Horizontal micro-programming, Vertical micro-programming