National Institute of Technology, Silchar
MidSemester (UG) Examination, March '2021
Subject Code : CS-205 ,Subject: Computer Architecture
Semester: 4th.Branch: CSE
Total Marks: 20
(All questions are self explanatory and requires no clarification from the course coordinator).

1. What is wrong with the following register transfer statements? **2**
a. xT: AR ←AR, AR← 0
b. yT: R1← R2, R1 ←R3
zT: PC← AR, PC ←PC+1

2. Represent the following decimal numbers in IEEE 754 single precision format: **2**
245.625 ii) 1/16

3. Explain normalization, excess-exponent and special values with respect to IEEE floating point representation **3**

4. Assume a microinstruction set that includes a microinstruction with the following symbolic form: **3**
IF (AC_0 = 1) THEN CAR (C_{0-6}) ELSE CAR (CAR) + 1
AC_0 is the sign bit of the accumulator and C_{0-6} are the first seven bits of the microinstruction. Using this microinstruction, write a microprogram that implements a Branch Register Minus(BRM) machine instruction which branches if the AC is negative. Assume that bits C_1 through C_{11} of the microinstruction specify a parallel set of micro-operation. Express the program symbolically.

5. Design a combinational circuit with three inputs x,y,z and three outputs A,B,C. When the binary input is 0,1,2 or 3 the binary output is one greater than the input. When the binary input is 4,5,6 or 7, the binary output is one less than the input. **4**

6. Booth's algorithm for integer multiplication gives worst performance when the multiplier pattern is **1**

(A) 10000000....0001

(B) 111111111....1111

(C) 10101010.....1010

(D) 01111111.....1110

7. For computer based on three-address instruction formats, each address field can be used to specify which of the following: **1**
(S1) A memory operand
(S2) A processor register
(S3) An implied accumulator register

(A) Either S2 or S3

(B) Either S1 or S2

(C) Only S2 and S3

(D) All of S1, S2 and S3

8. Consider the following processor design characteristics. **1**

I. Hardwired control unit
II. Register-to-register arithmetic operations only
III. Fixed-length instruction format

Which of the characteristics above are used in the design of a RISC processor?

(A) I and II only

(B) II and III only

(C) I and III only

(D) I, II and III

9. For relocation of programs during execution time, the addressing modes suitable are? **1**

(i) Relative Addressing
(ii) Indirect Addressing
(iii) Absolute Addressing
(iv) Based Addressing

(A) (i) and (ii) (B) (ii) and (iii)
(C) (i) and (iv) (D) (i), (ii) and (iii)

10. The value of a *float* type variable is represented using the single-precision 32-bit floating point format of IEEE-754 standard that uses 1 bit for sign, 8 bits for biased exponent and 23 bits for mantissa. A *float* type variable *X*is assigned the decimal value of -14.25. The representation of *X*in hexadecimal notation is **1.**

(A) C1640000H

(B) 416C0000H

(C) 41640000H

(D) C16C0000H

11. Arrange the following configuration for CPU in decreasing order of operating speeds: Hardwired control, vertical micro- programming, horizontal micro-programming **1**

(A) Horizontal micro-programming, Hardwired control, Vertical micro-programming

(B) Vertical micro-programming, Horizontal micro-programming, Hardwired control

(C) Hardwired control, Vertical micro-programming, Horizontal micro-programming

(D) Hardwired control, Horizontal micro-programming, Vertical micro-programming