National Institute of Technology, Silchar

Cachar, Assam, India

MICROPROCESSOR ASSIGNMENT

EE 223

B.Tech. IIIrd Semester

Branch- Computer Science and Technology

Submitted To:

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Answers:

1. The four categories of 8085 are Data transfer, arithmetic, logic and branch.

2. The Task to be performed is called the opcode (operation code) and the data to be operated on is called the operand which may be specified as data register or address. Opcode: MOV and operand: H, L.

3. The machine code, 01 100 111=67H.

4. (a) 2647H OPCODE=MVI OPERANDS=H, 47H

   (b) C6F5H OPCODE=ADI OPERANDS=A (IMPLIED), F5H

   (c) 91H OPCODE=SUB OPERSNDS=A (IMPLIED), C

5. (a) HEX = 325020H OPCODE=STA OPERANDS=2050H
   (b) HEX = C27020H OPODE=JNZ OPERANDS=2070H

6. 064FH (2bytes); Load the first byte
   0E78H (2bytes); Load the Second byte
   79H (1byte); Get ready for addition
   80H (1byte); Add two bytes
   D307H (2bytes); Display the result at port 7
   76H (1byte); End of program

7.

INSTRUCTION	**ADDRESS**	**HEX**
MVI B, 4FH	2000	064F
MVI C, 78H	2002	0E78
MOV A,C	2004	79
ADD B	2005	80
OUT 07H	2006	D307
HLT	2008	76

8.

INSTRUCTION	ADDRESS	HEX
MVI A, 8FH	2020	3E8F
MVI B, 68H	2022	0668
SUB B	2024	90
ANI 0FH	2025	E60F
STA 2070H	2027	327020
HLT	202A	76

9.

INSTRUCTION	ADDRESS	HEX
IN F2H	2020	DBF2
CMA	2002	2F
ORA A	2003	B7
JZ START	2004	CA0020

10. **Logical Steps to add two HEX numbers:**
Load A2H in One register.
Load 18H in Second register.
Copy A2H in accumulator .
Add the contents of the second register to the contents of the accumulator.
End of Program.

11.
```
MVI B, A2H
MVI C, 18H
MOV A, B
ADD C
HLT
```

12. **Register contents:**
Initial:
B = 28H A = 97H
After the execution:
A = 28H B = 28H C = 28H

13. In Q6, if the code 07H(port address) is omitted, the processor assumes the opcode of the next instruction 76H(HLT) as the address of the output port, outputs the contents of the accumulator to the address 76H, and continues to the next code. After the next code, results are indeterminate.

14. In Q8, if the byte 0FH is omitted, the processor assumes the opcode 32H of the next instruction (STA) as the second byte of the ANI instruction. The processor is a sequential machine; it assumes the next code 20H (the lower order address of 2070H) as the opcode of the next instruction and continue.

15. Given following HEX-codes, identify the mnemonics:

(a)	
HEX-Code	Mnemonics
3E F2	MVI A, F2H
32 32 20	STA 2032H
76	HLT

(b)	
HEX-Code	Mnemonics
06 82	MVI B, 82H
78	MOV A,B
32 50 20	STA 2050H
FF	RST07

(c)	
HEX-Code	Mnemonics
06 4F	MVI B, 4FH
0E 37	MOV A,B
78	MOV A,B
81	ADD
00	NOP
32 35 20	STA 2035H
76	HLT

16. (a) Loads the 8 bit data i.e. F2H in the accumulator and stores the content of the accumulator in the memory address 2032H.
(b) Loads the 8 bit data i.e. 82H in the register B, and then copies the content of B to accumulator A. Finally stores the content of the accumulator in the address 2035H.

17. Opcode 00 represents NOP in mnemonics which indicates execute no operation.

18.

HEX-Code	Mnemonics
06 4F	Loads 4FH in the register B
0E 37	Loads 37H in the register B
78	Copies the content of register B to the accumulator
81	Adds the content of register C to the content of the accumulator
00	Performs no operation
32 35 20	Stores the content of the accumulator to the memory address 3025H
76	Halts the program

For sum:

Hex-Code	**Binary**
4F	01001111
37	00110111
Sum: 86	10000110

Therefore, the sum is stored at the address 2035H.