

UG END SEMESTER EXAMINATION, 2021

BRANCH : CSE

SCH ID : 1912160

SUBJECT : Computer Architecture and Organisation.

SUBJECT CODE : CS205

SEMESTER : IVth

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Q.10

1(a) Ans : The effective MIPS rate,

$$\begin{aligned}\text{MIPS rate} &= [n\alpha + (1-\alpha)]n \\ &= (n\alpha - \alpha + 1)n\end{aligned}$$

1(b) Ans : Given, $n = 32$

$$n = 8 \text{ MIPS}$$

$$\text{MIPS rate} = 80$$

Placing the values in the expression obtained in 1(a),

$$80 = (32\alpha - \alpha + 1) * 8$$

$$\text{or, } 80 = (32\alpha - \alpha + 1) * 8$$

$$\text{or, } 10 = 32\alpha - \alpha + 1$$

$$\text{or, } 10 = 31\alpha + 1$$

$$\text{or, } 9 = 31\alpha$$

$$\text{or, } \alpha = \frac{9}{31}$$

$$\therefore \alpha = 0.29$$

Q.2

<u>2. (a). Ans)</u>	Instructions	clock Cycle	Times	Loop	Total Sum
	Load	4	4	64	1024
	Multiply	8	1	64	512
	Add	2	1	64	128
	Store	4	0	64	0
	TOTAL				1664

∴ The total number of processor cycles needed to execute the given code segment, ignoring all other time delays is ¹⁶⁶⁴~~1664~~ cycles.

2. (b). Ans) $\frac{1664}{64} = 26$

∴ The total execution time on SIMD machine, ignoring instruction broadcast and other delays is 26 clock cycles.

2. (c). Ans) Speed up Gain = $\frac{\text{CPU cycles on SIMD machine}}{\text{CPU cycles on SISD machine}}$

$$= \frac{1664}{26}$$

$$= 64 \text{ times}$$

Q.30 A

3. (a) Ans: 2048 bytes / sector.
64 sectors per track
512 tracks per surface
10 surfaces

So, $2048 * 64 * 512 * 10$ bytes per surface

~~i.e., 671,088,640 bytes~~

i.e., 671,088,640

i.e., 640 MB

3. (b) Ans: Seek time + rotational delay + track to track

$$= 10 \text{ ms} + 8.3 + 1.5 \text{ ms}$$

$$= 19.8 \text{ ms}$$

3. (c) Ans: 6 MB = 6,291,456 bytes

$$\frac{6,291,456}{131,072} = 48 \text{ tracks}$$

$$48 * 64 = 3072 \text{ sectors.}$$

\therefore 48 tracks, 3072 sectors, 4.8 cylinders.

3. (d) Ans:

Q.40

40(i). Ans: Bus arbitration method:

It is a process by which the current bus master accesses and then leaves the control of the bus and passes it to another bus requesting processor unit.

40(ii). Ans: Direct Mapping:

It is a type of mapping where a particular block of main memory can map to only one particular line of the ~~code~~ cache.

40(iii). Ans: Set associative mapping:

It is a type of mapping where the drawbacks of direct mapping are removed. In this type, the problem of possible thrashing in direct mapping is addressed by grouping few lines together creating a set instead of a single line.

40(iv). Ans: Page replacement algorithm:

It decides which memory page is to be replaced. The process of replacement is sometimes called swap out or write to disk. It is done when requested page is not found in the main memory.

Qo5o Ans:

(a) \rightarrow Ans) $P - N + \log_2 K$

(b) \rightarrow Ans) 32

(c) \rightarrow Ans) interrupt register

(d) \rightarrow Ans) address space

(e) \rightarrow Ans) independent request

(f) \rightarrow Ans) instruction is not executed
exception is served immediately

(g) \rightarrow Ans) Bus arbitrator

(h) \rightarrow Ans) mapping process.