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NATIONAL INSTITUTE OF TECHNOLOGY SILCHAR

CACHAR, ASSAM

LABORATORY EXERCISE BOOK

B.TECH. IIIRD SEM.

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SCH. ID.: 1912160

BRANCH: CSE - 'B'

SUBJECT: CIRCUIT AND SWITCHING LAB

CODE : EC-222

02/12/2020
Experiment-05

AIM: ANALYSIS AND SYNTHESIS OF MULTI-BIT SEQUENTIAL CIRCUITS USING SHIFT REGISTERS.

THEORY:

A REGISTER capable of shifting information either to right or left is called a shift register. In a shift register, the flip-flops are connected in such a way that the binary bits are entered into the shift register, shifted from one location to another and finally shifted out. There are different types of shift registers, namely - Serial-In-Serial-Out (SISO), Serial-In-Parallel-Out (SIPO), Parallel-In-Parallel-Out (PIPO) and Parallel-In-Serial-Out (PISO).

4-Bit Shift Register:

The SN54/74LS95B is a 4-bit Shift Register with serial and parallel synchronous operating modes. These operating modes are controlled by a mode control input (S). The serial shift right and parallel load are activated by separate clock inputs which are selected by a mode control input (S). The data is transferred from the serial or parallel D inputs to the Q outputs synchronous with the HIGH to LOW transition of appropriate clock input.

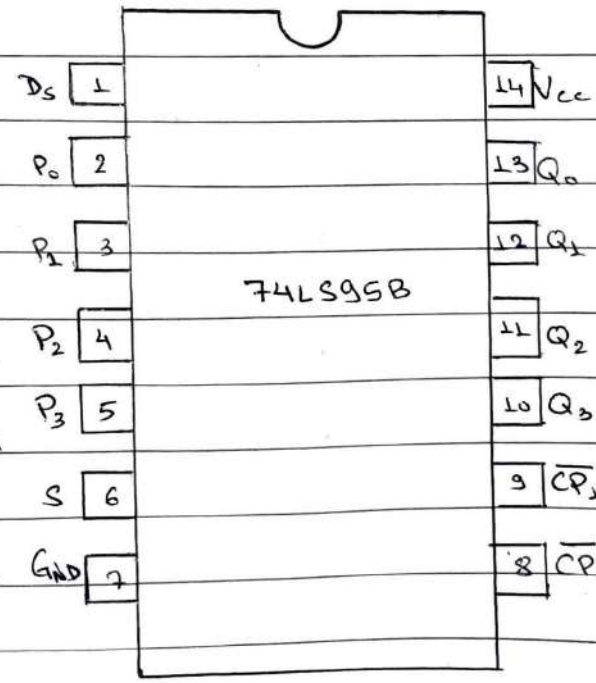

fig.: 5.1: 74LS95B, 4-bit Shift Register.

PIN NAMES: (as seen in fig 5.1)

D_S : Serial Data Input

P_0-P_3 : Parallel Data Inputs

S : Mode Control Input

GND : Ground

CP_1 : Serial Clock (Active LOW Going Edge) Input

CP_2 : Parallel Clock (Active LOW Going Edge) Input

Q_0 - Q_3 : Parallel Outputs

V_{CC} : Voltage Common Collector.

FUNCTIONAL DESCRIPTION:

The SN54/74LS95B is a 4-bit Shift Register with serial and parallel synchronous operating modes. It has a Serial (D_S) and four parallel (P_0-P_3) Data inputs, and four Parallel (Q_0-Q_3) Data Outputs. The serial or parallel mode of operation is controlled by a Mode Control Input (S) and two Clock Inputs, CP_1 and CP_2. When the Mode Control Input (S) is HIGH, CP_2 is enabled. A HIGH to LOW transition on enabled CP_2 directly loads parallel data from the P_0-P_3 inputs to the Q_0-Q_3 Outputs. When the mode Control Input is LOW, CP_1 is enabled. A HIGH to LOW transition on an enabled CP_1 transfers the data from Serial Input (D_S) to Q_0 and Shifts the data in Q_0 to Q_1; Q_1 to Q_2; Q_2 to Q_3 respectively (right-Shift). for normal operation, S should only change states when both Clock inputs are LOW. However, Changing S from LOW to HIGH while

CP_2 is HIGH, or changing S from HIGH to LOW while CP_1 is HIGH and CP_2 is LOW will not cause any changes on the register outputs.

OPERATING MODES	INPUTS					OUTPUTS			
	S	CP_1	CP_2	D_S	P_n	Q_0	Q_1	Q_2	Q_3
Shift	L	⊓	x	l	x	L	q_0	q_1	q_2
	L	⊓	x	h	x	H	q_0	q_1	q_2
Parallel load	H	x	⊓	x	P_n	P_0	P_1	P_2	P_3

figure 5.2: Truth Table

Here, (on the figure 5.2),

L: is low voltage level

H: is high voltage level

x: is don't care

l: is low voltage one set-up prior to the high to low clock transition

h: is high voltage one set-up prior to the high to low clock transition.

P_n: is the state of referenced input

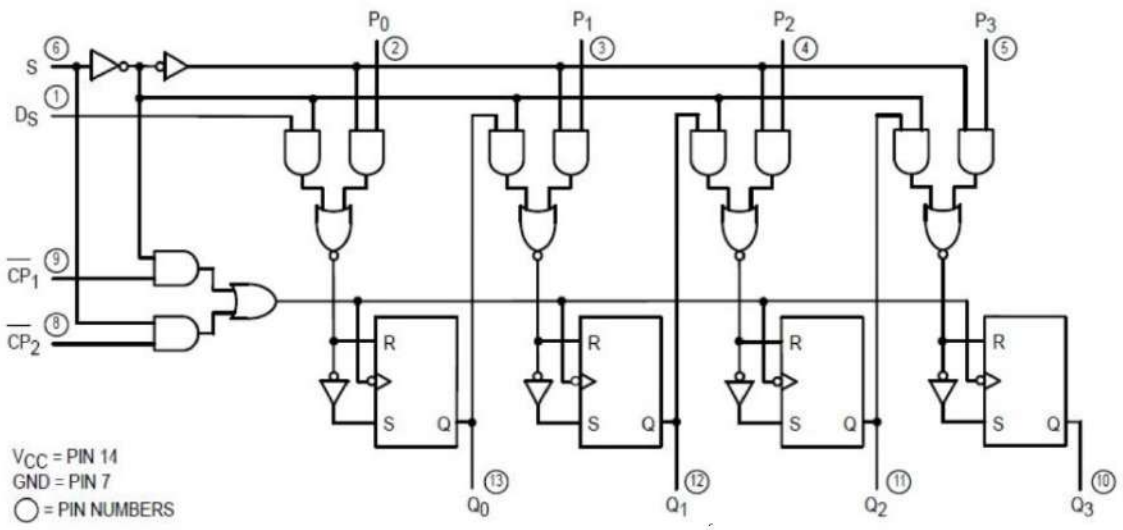

fig. 5.3: Logic Diagram of 74LS95B

Circuit Diagram

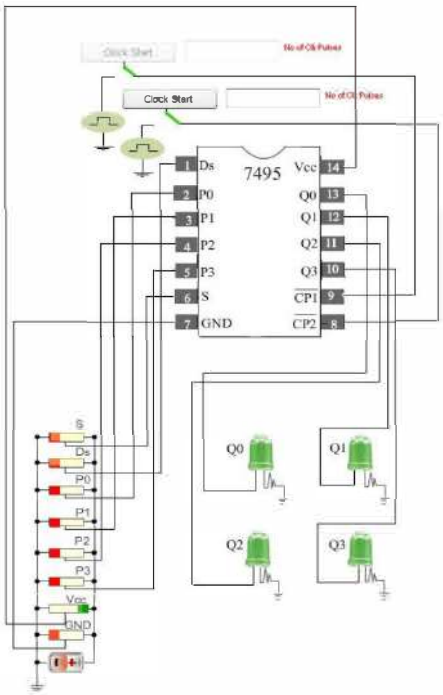

fig. 5.4.: Circuit Diagram of 74LS95B

Observation

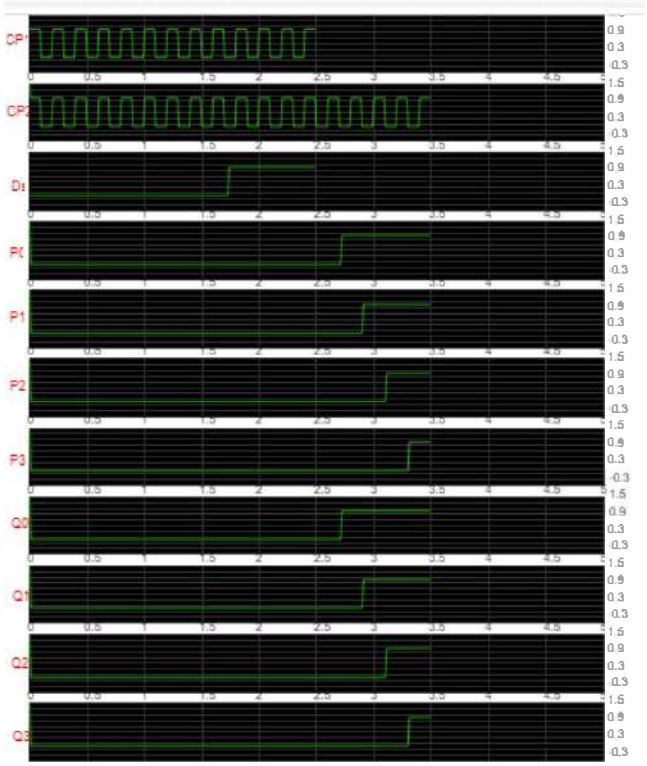

fig. 5.5: Timing Diagram of 74LS95B

RESULT:

The timing diagram was obtained as shown in figure 5.5 after inserting all the inputs. The multi bit sequential circuit was thus ~~successfully~~ successfully analysed and synthesised using shift registers.

02/12/2020
Experiment-06

AIM: To verify the Truth Table and Timing Diagram of 4-bit Synchronous Parallel Counter and 4-bit Asynchronous Parallel Counter by using JK flipflop ICs and analyse the circuit of 4-bit Synchronous Parallel Counter and 4-bit Asynchronous Parallel Counter with the help of LEDs Display.

THEORY:

A counter is a device which stores (and sometimes displays) the numer of time a particular event or process has occurred, often in relation to clock signal. Counters are used in digital electronics for counting purpose, they can count specific event happening in the circuit. For example, in UP counter, a counter increases count for every rising edge of clock. Counters are broadly categorised into two - (i) Asynchronous counter.
(ii) Synchronous Counter.

1. Asynchronous Counter:

In asynchronous counter, we don't use universal clock, only first flipflop is driven by main clock and the clock inputs of rest of the following counters is driven by output of previous flipflops.

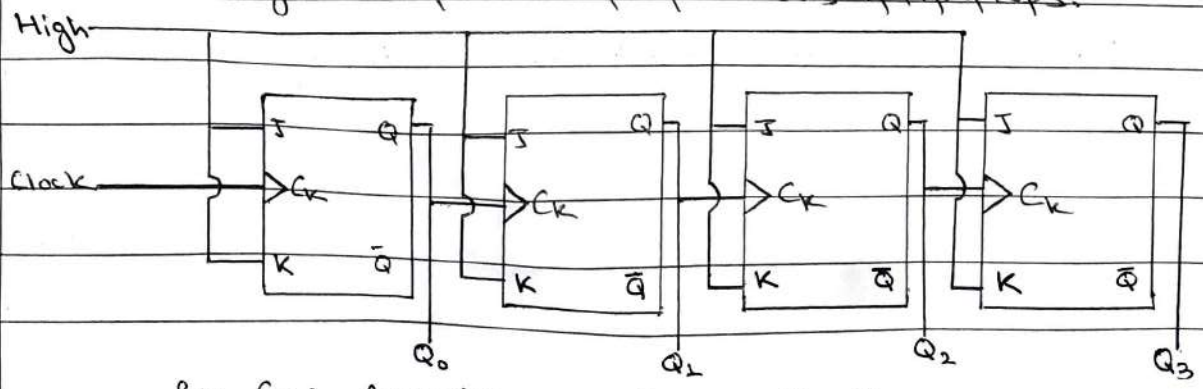

fig. 6.1: Asynchronous Counter Circuit

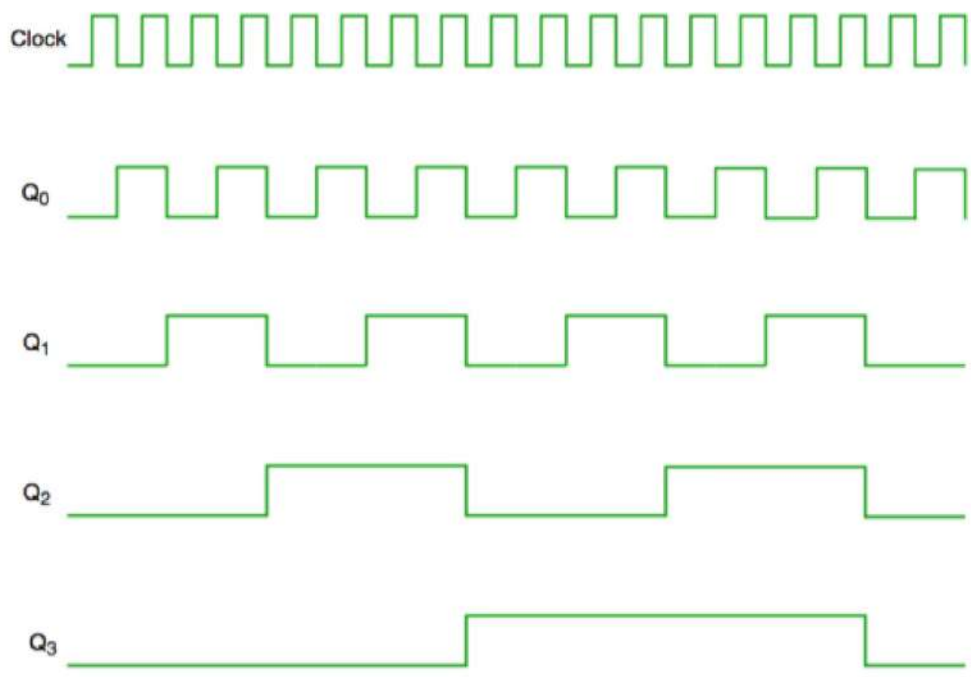

fig. 6.2: Timing Diagram of Asynchronous Counter

It is evident from the timing diagram that Q_0 is changing as soon as the rising edge of clock pulse is encountered; Q_1 is changing when rising edge of Q_0 is encountered (because Q_0 is like clock pulse for second flipflop) and so on. In this way, ripples are generated through Q_0, Q_1, Q_2 and Q_3, and hence this counter is also called RIPPLE counter.

2. Synchronous Counter:

Unlike the asynchronous counter, the synchronous counter has one global clock which drives each flipflop so output changes in parallel. The one advantage of synchronous over asynchronous counter is that it can operate on higher frequency than asynchronous counter as it does not have cumulative delay because of the same clock given to each flipflop.

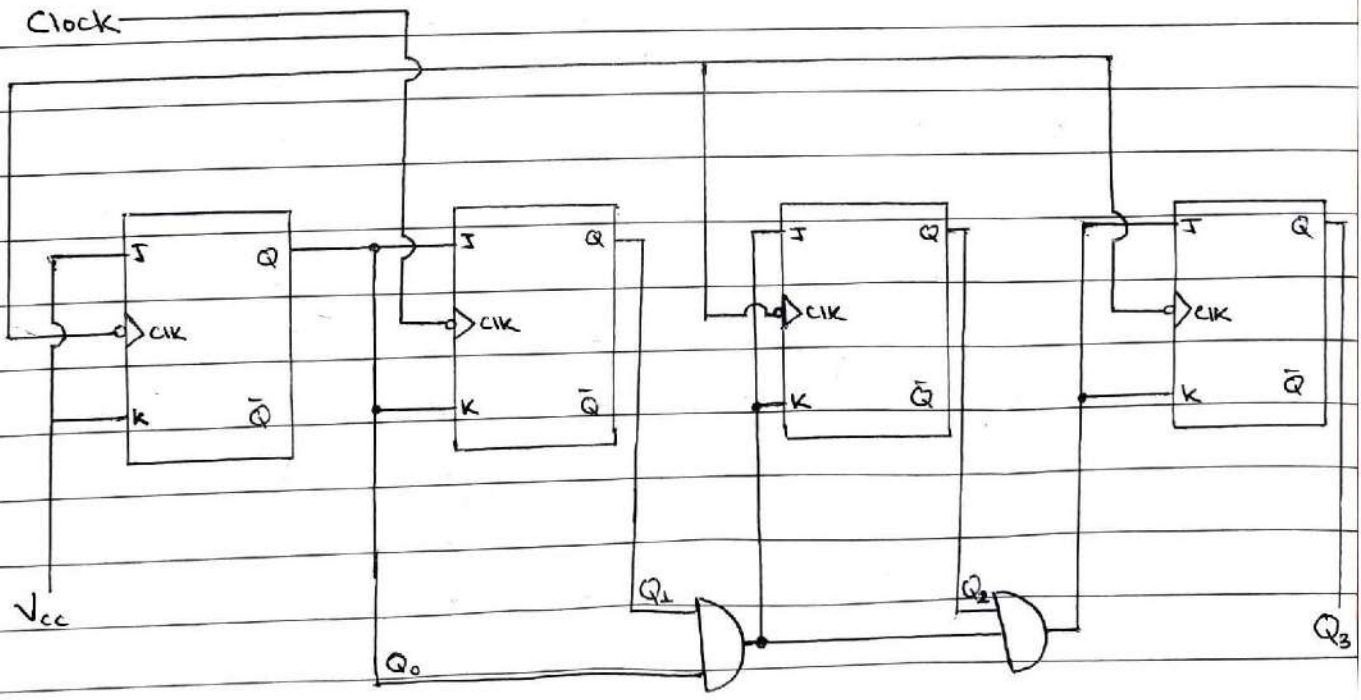

fig. 6.3: Synchronous Counter Circuit.

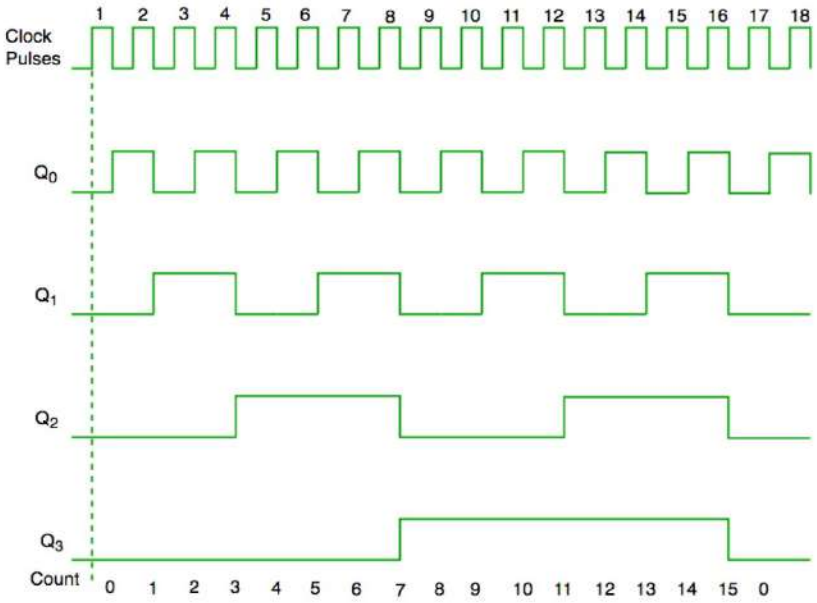

fig. 6.4: Timing Diagram of Synchronous Counter

From the timing diagrams above, we see that Q_0 bit gives response to each falling edge of clock while Q_1 is dependent on Q_0; Q_2 is dependent on Q_1 and Q_0, and finally Q_3 is dependent of Q_2, Q_1 and Q_0

Circuit Diagram

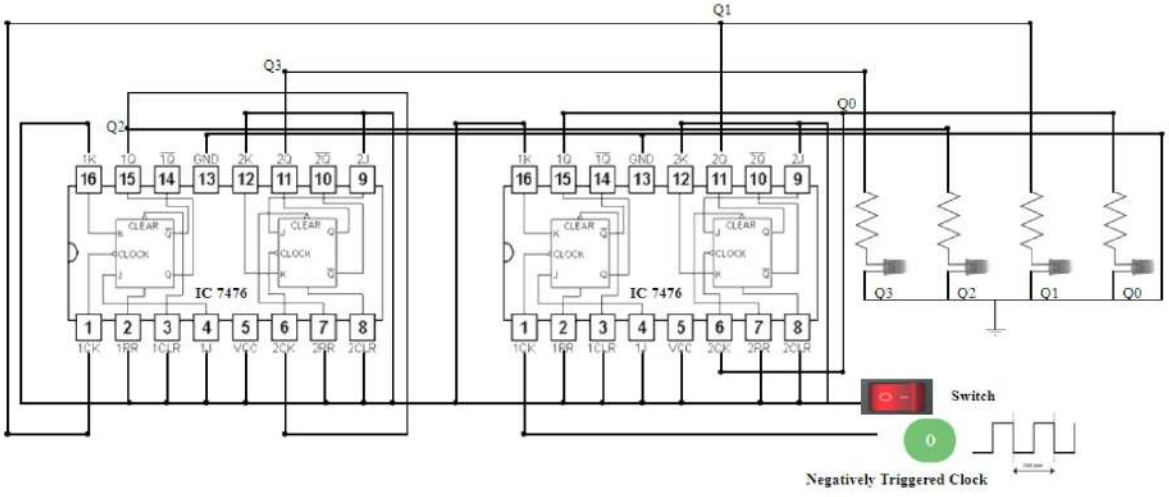

fig. 6.5: 4-Bit Asynchronous Parallel Counter using J-K Flip-Flop

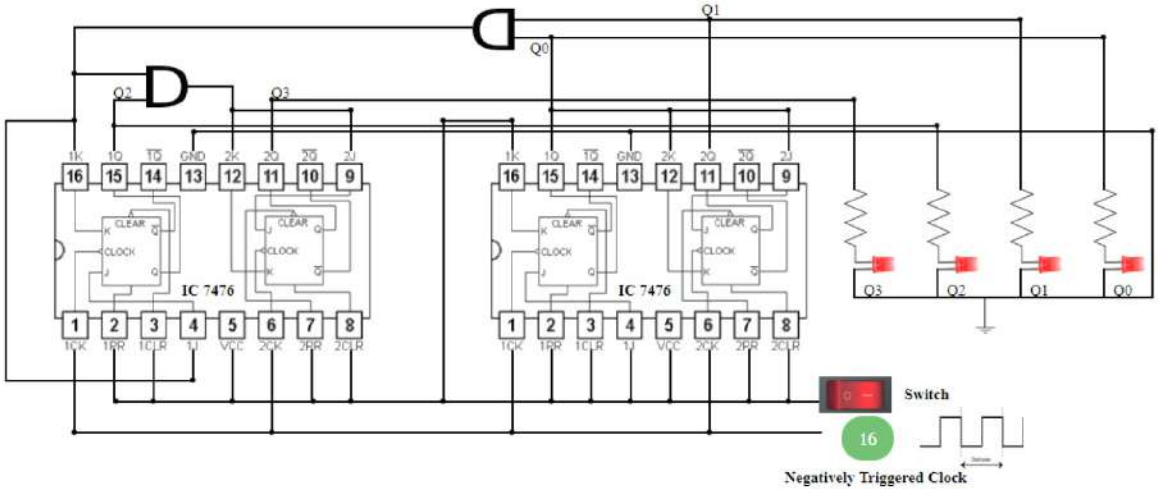

fig. 6.6: Bit Synchronous Parallel Counter using J-K Flip-Flop

OBSERVATIONS:

Serial No	Clock	Q_3	Q_2	Q_1	Q_0
1	0	x	x	x	x
2	1	0	0	0	0
3	2	0	0	0	1
4	3	0	0	1	0
5	4	0	0	1	1
6	5	0	1	0	0
7	6	0	1	0	1
8	7	0	1	1	0
9	8	0	1	1	1
10	9	1	0	0	0
11	10	1	0	0	1
12	11	1	0	1	0
13	12	1	0	1	1
14	13	1	1	0	0
15	14	1	1	0	1
16	15	1	1	1	0
17	16	1	1	1	1

Table: 6.1 : Asynchronous Parallel Counter Truth Table

OBSERVATIONS:

Serial No	Clock	Q_3	Q_2	Q_1	Q_0
1	0	x	x	x	x
2	1	0	0	0	0
3	2	0	0	0	1
4	3	0	0	1	0
5	4	0	0	1	1
6	5	0	1	0	0
7	6	0	1	0	1
8	7	0	1	1	0
9	8	0	1	1	1
10	9	1	0	0	0
11	10	1	0	0	1
12	11	1	0	1	0
13	12	1	0	1	1
14	13	1	1	0	0
15	14	1	1	0	1
16	15	1	1	1	0
17	16	1	1	1	1

Table 6.2: Synchronous Parallel Counter Truth Table

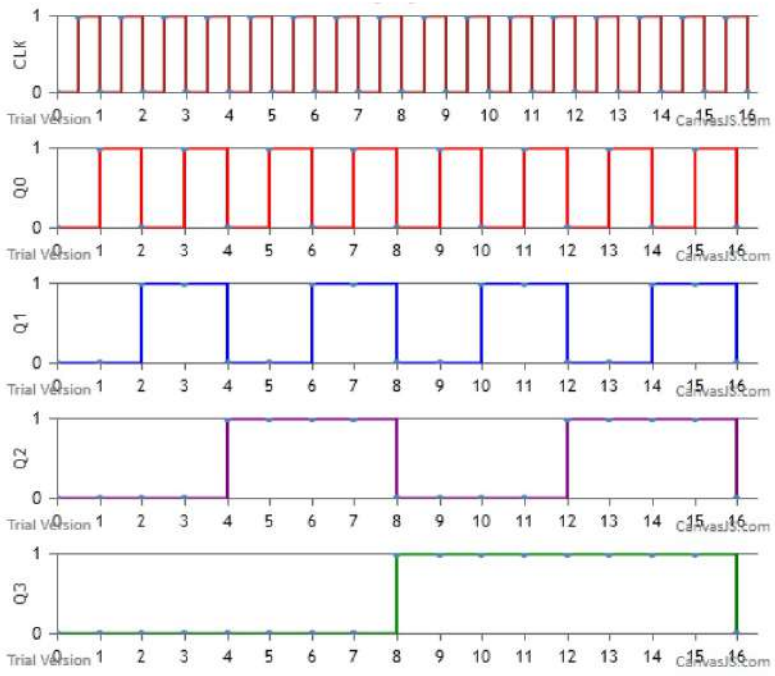

fig. 6.7: Time Diagram of Asynchronous Parallel Counter

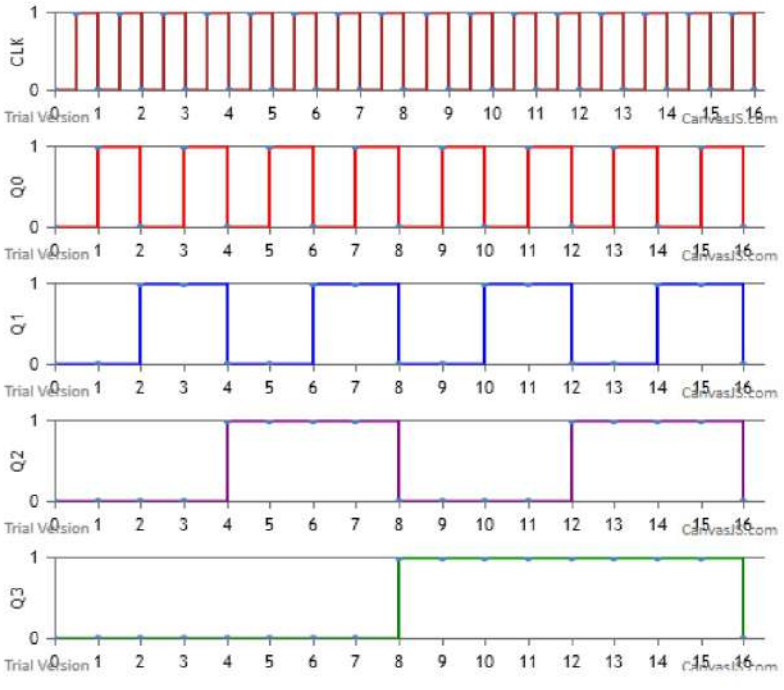

fig. 6.8: Time Diagram of Synchronous Parallel Counter

RESULT:

The truth table for Asynchronous Parallel Counter and its timing diagram were obtained as shown in the table 6.1 and fig. 6.7, respectively. And the truth table and the timing diagram for Synchronous Parallel Counter were obtained as shown in the table 6.2 and fig. 6.8, respectively.