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NATIONAL INSTITUTE OF TECHNOLOGY SILCHAR

CACHAR, ASSAM

LABORATORY EXCERCISE BOOK

B.TECH. IIIRD SEM.

NAME: SUBHOJIT GHIMIRE

SCH. ID.: 1912160

BRANCH: C.S.E. - B

SUBJECT: MICROPROCESSOR LAB

CODE : EE224

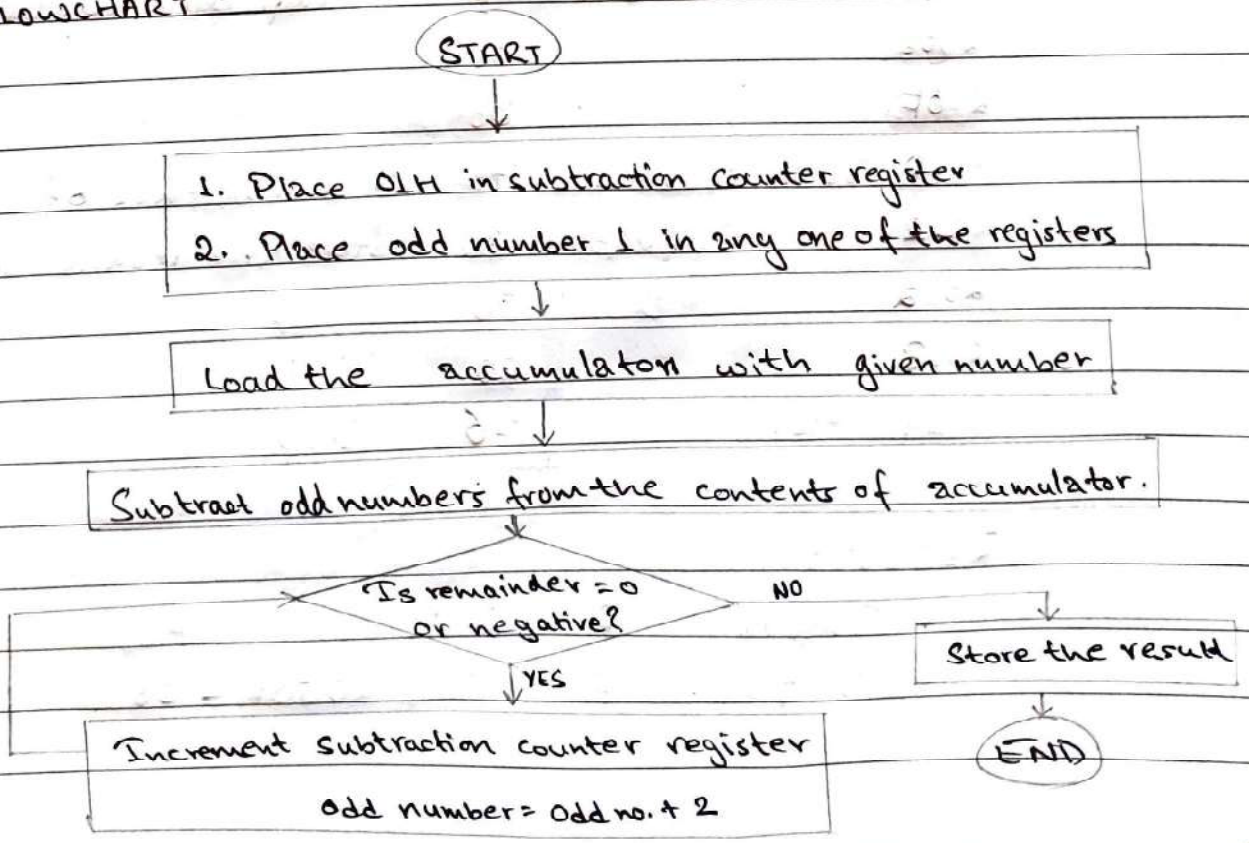
06/10/2020
Experiment-04

AIM: FINDING SQUARE ROOT OF A NUMBER

THEORY:

1. Assign the value of register B and C with 01H
2. Load Accumulator with the given number.
3. Subtract the content of accumulator with the content of register B.
4. Check if the value of accumulator is zero, if yes, then go to step 8.
5. Increase the content of register B by 02H
6. Increase the content of register C by 01H
7. Go to step 3.
8. Move the content of register C to accumulator.
9. Store the result to the memory 2050.
10. Terminate the program.

FLOWCHART:



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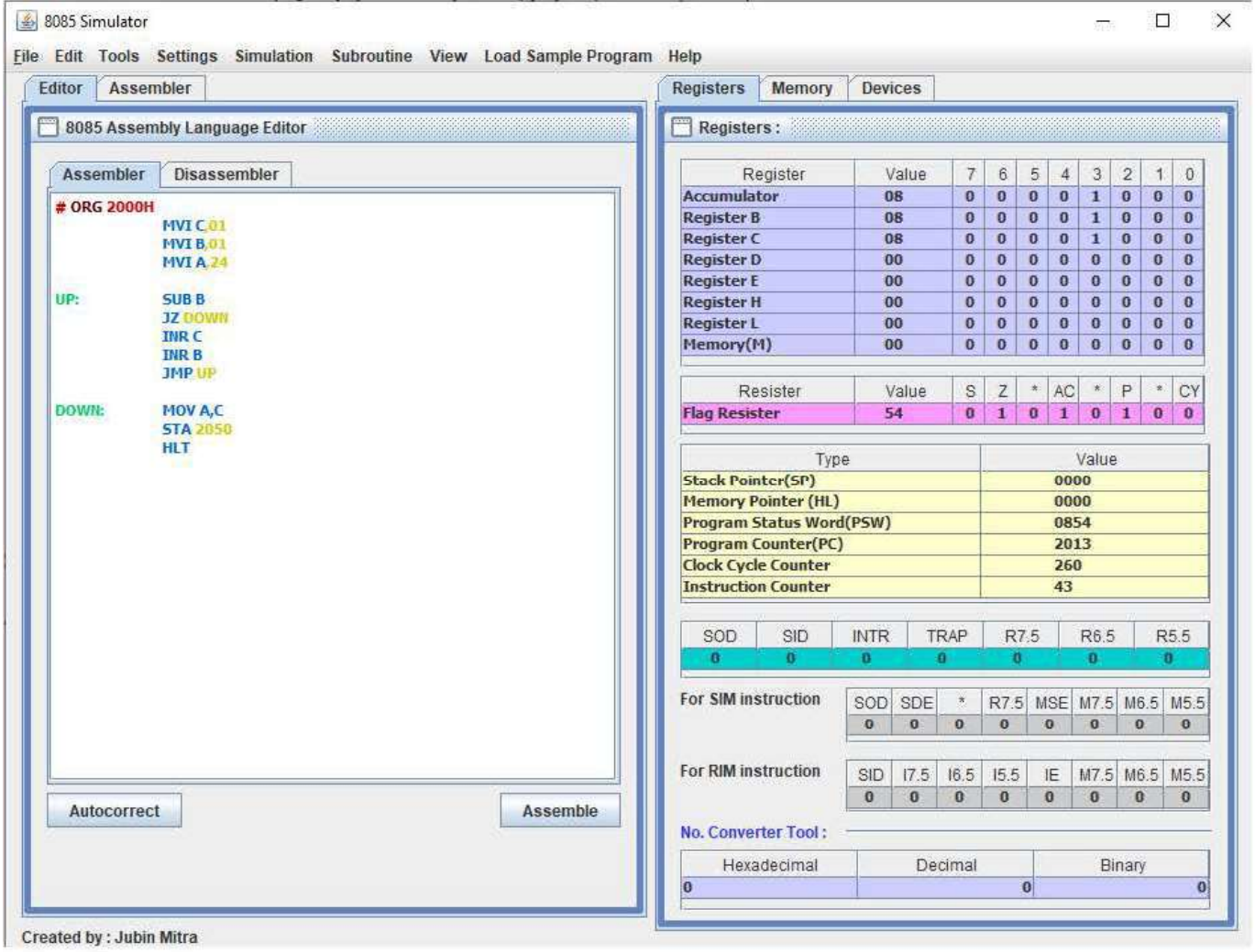
PROGRAM:

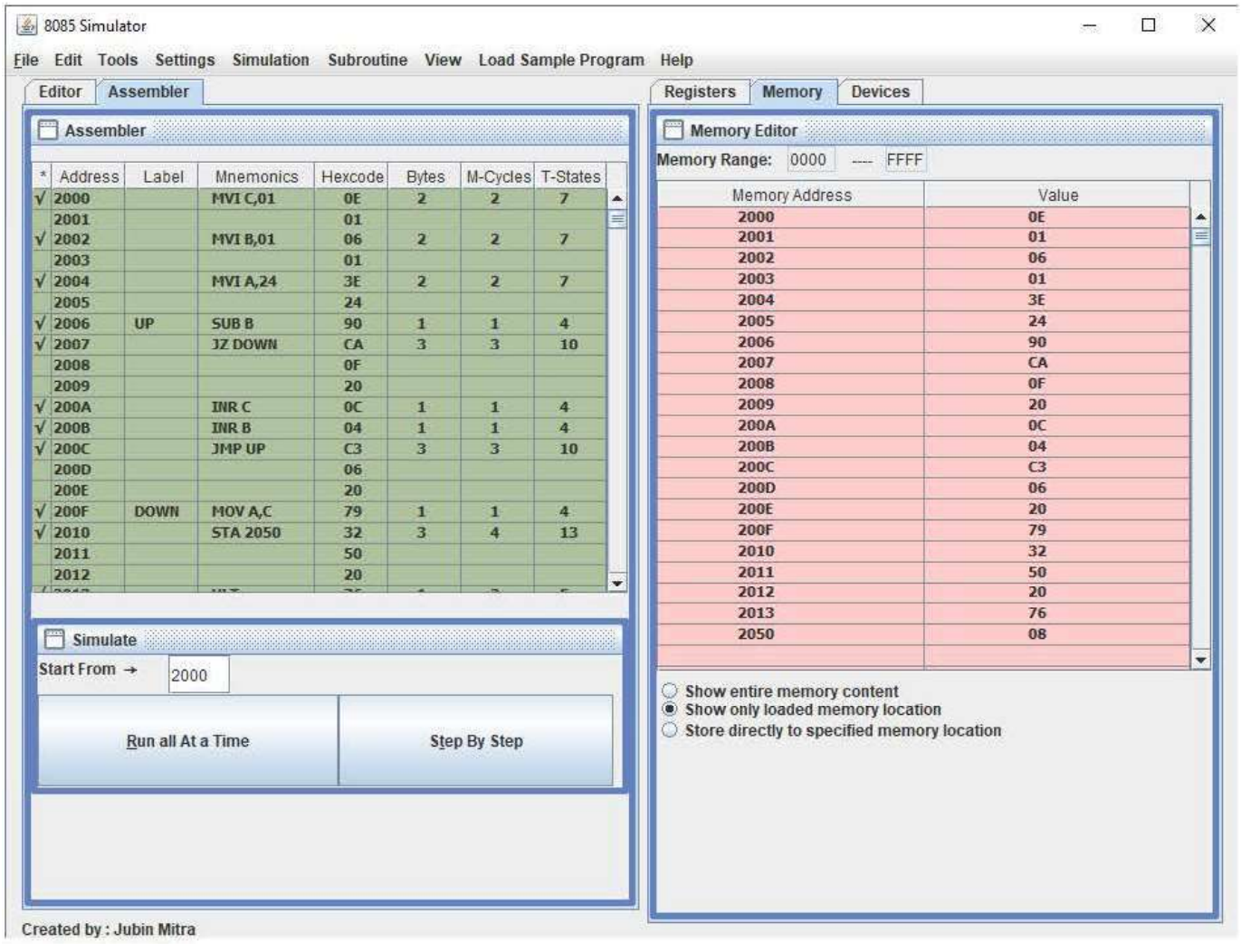
Address	Label	Mnemonics	Hexcode	Comment
2000		MVI C, 01H	0E	Place 01 in register C
2001			01	
2002		MVI, B, 01	06	Place odd number 1 in register B
2003			01	
2004		MVI A, 24	3E	Load acc. with given number 24.
2005			24	
2006	UP	SUB B	90	Subtract B from the accumulator
2007		JZ 2010	CA	If acc. content is 0, jump
2008			10	
2009			20	
200A		INR C	0C	Increment register C
200B		INR B	04	Increment odd number
200C		INR B	04	Increment odd number.
200D		JMP 2006	C3	Jump back to label UP
200E			06	
200F			20	
2010	DOWN	MOV A, C	79	Move contents of C to A
2011		STA 2050	32	Store the results in 2050 H
2012			50	
2013			20	
2014	HLT		76	Stop

RESULT:

Input: A - 24H

Output: A - 06 ; 2050H - 06H


8085 Simulator
File Edit Tools Settings Simulation Subroutine View Load Sample Program Help
Editor Assembler
8085 Assembly Language Editor
Assembler Disassembler
ORG 2000H
MVI C,01
MVI B,01
MVI A,24
UP: SUB B
JZ DOWN
INR C
INR B
JMP UP
DOWN: MOV A,C
STA 2050
HLT
Autocorrect
Assemble
Registers Memory Devices
Registers :
Register | Value | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0
Accumulator | 08 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0
Register B | 08 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0
Register C | 08 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0
Register D | 00 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0
Register E | 00 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0
Register H | 00 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0
Register L | 00 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0
Memory(M) | 00 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0
Resister | Value | S | Z | * | AC | * | P | * | CY
Flag Resister | 54 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0
Type | Value
Stack Pointer(SP) | 0000
Memory Pointer (HL) | 0000
Program Status Word(PSW) | 0854
Program Counter(PC) | 2013
Clock Cycle Counter | 260
Instruction Counter | 43
SOD | SID | INTR | TRAP | R7.5 | R6.5 | R5.5
0 | 0 | 0 | 0 | 0 | 0 | 0
For SIM instruction
SOD | SDE | * | R7.5 | MSE | M7.5 | M6.5 | M5.5
0 | 0 | 0 | 0 | 0 | 0 | 0 | 0
For RIM instruction
SID | I7.5 | I6.5 | I5.5 | IE | M7.5 | M6.5 | M5.5
0 | 0 | 0 | 0 | 0 | 0 | 0 | 0
No. Converter Tool :
Hexadecimal | Decimal | Binary
0 | 0 | 0
Created by : Jubin Mitra


8085 Simulator
File Edit Tools Settings Simulation Subroutine View Load Sample Program Help
Editor Assembler
Assembler
* | Address | Label | Mnemonics | Hexcode | Bytes | M-Cycles | T-States
√ 2000 | MVI C,01 | 0E | 2 | 2 | 7
2001 | 01
√ 2002 | MVI B,01 | 06 | 2 | 2 | 7
2003 | 01
√ 2004 | MVI A,24 | 3E | 2 | 2 | 7
2005 | 24
√ 2006 | UP | SUB B | 90 | 1 | 1 | 4
√ 2007 | JZ DOWN | CA | 3 | 3 | 10
2008 | 0F
2009 | 20
√ 200A | INR C | 0C | 1 | 1 | 4
√ 200B | INR B | 04 | 1 | 1 | 4
√ 200C | JMP UP | C3 | 3 | 3 | 10
200D | 06
200E | 20
√ 200F | DOWN | MOV A,C | 79 | 1 | 1 | 4
√ 2010 | STA 2050 | 32 | 3 | 4 | 13
2011 | 50
2012 | 20
Simulate
Start From → 2000
Run all At a Time
Step By Step
Registers Memory Devices
Memory Editor
Memory Range: 0000 ---- FFFF
Memory Address | Value
2000 | 0E
2001 | 01
2002 | 06
2003 | 01
2004 | 3E
2005 | 24
2006 | 90
2007 | CA
2008 | 0F
2009 | 20
200A | 0C
200B | 04
200C | C3
200D | 06
200E | 20
200F | 79
2010 | 32
2011 | 50
2012 | 20
2013 | 76
2050 | 08
Show entire memory content
Show only loaded memory location
Store directly to specified memory location
Created by : Jubin Mitra

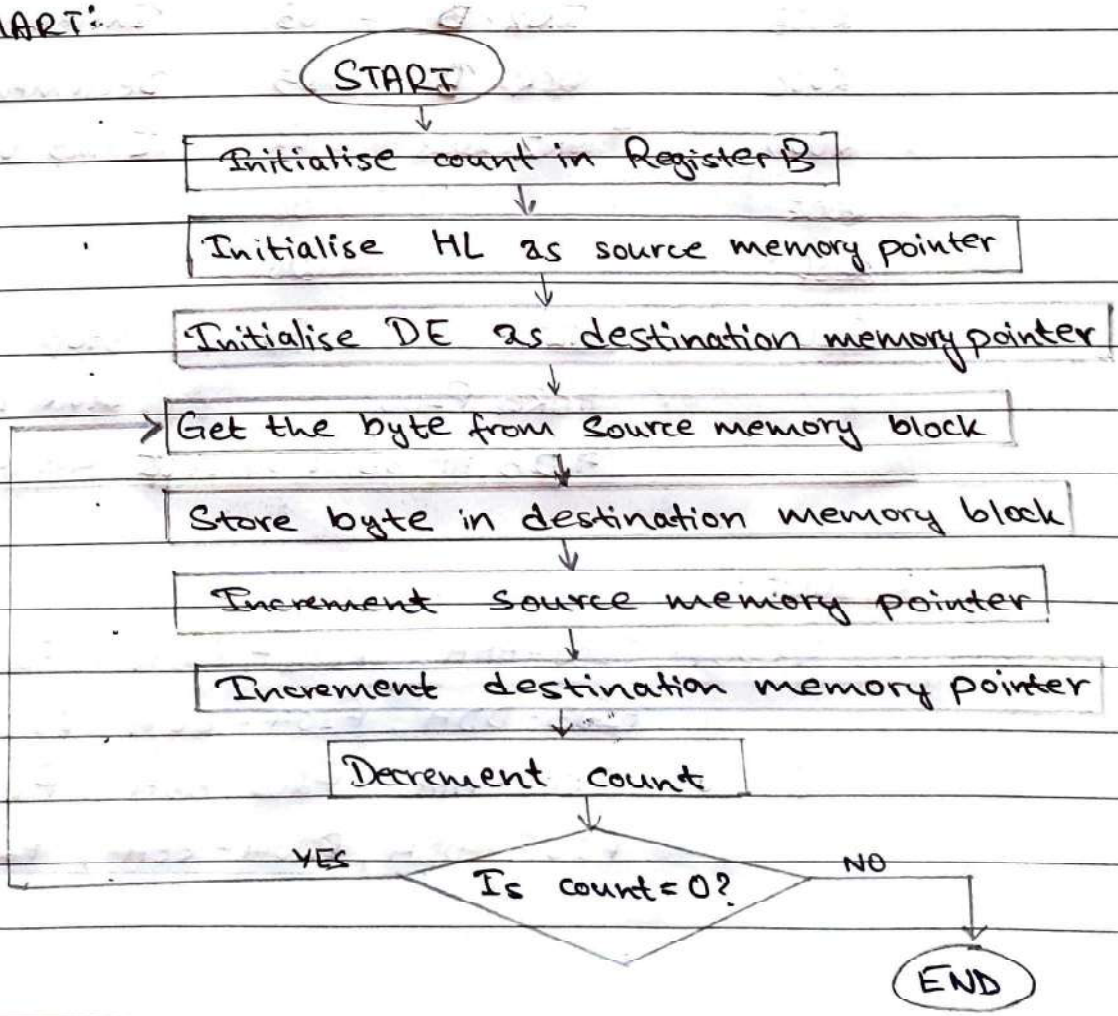
06 / 10 / 2020
Experiment-05

AIM : TO MOVE A BLOCK OF DATA

THEORY:

1. Place size of block in reg. B
2. Load register pair HL with address ~~F100H~~ F100H
3. Load register pair DE with address F200H
4. Move the content pointed by HL into accumulator
5. Store the content of acc. into memory pointed by DE
6. Increment address value of register pairs HL and DE by 1.
7. Decrement value of register B by 1
8. If zero flag is not equal to 0, go to step 4.
9. Stop

FLOWCHART:



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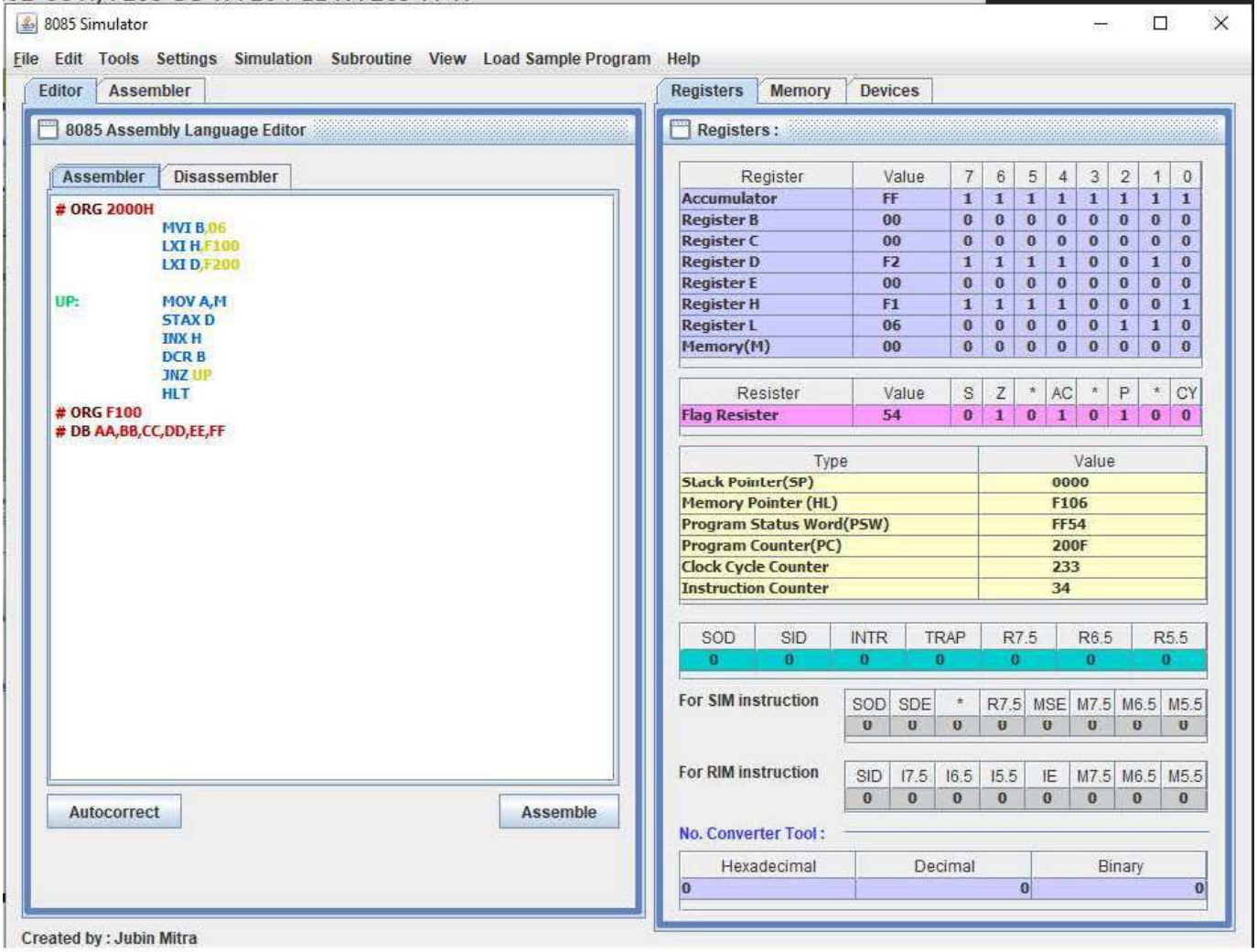
PROGRAM :

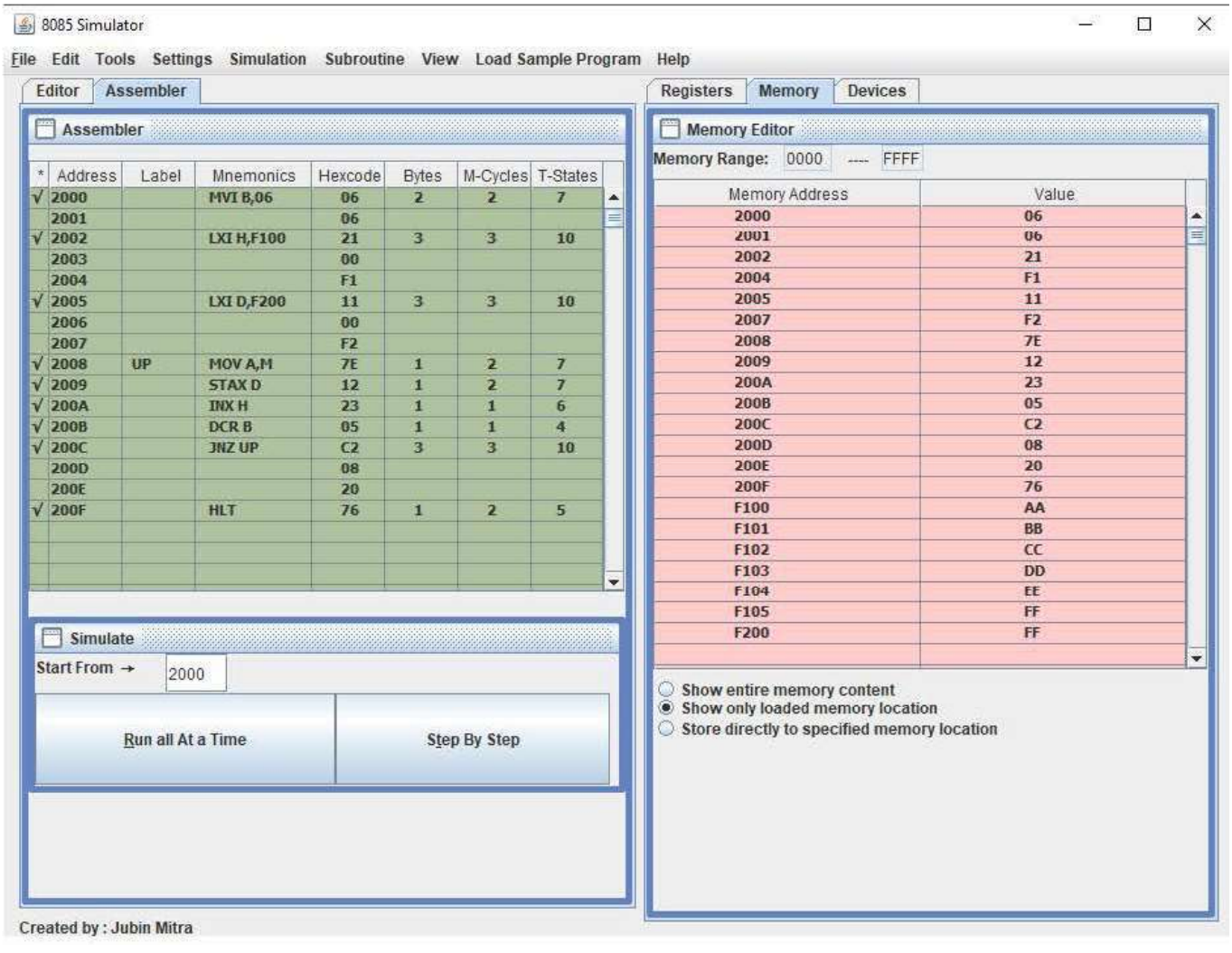
Address	Label	Mnemonics	Hexcode	Comments
		#ORG 2000H		
2000		MVI B, 06	16	Place 06 in register B
2001			06	
2002		LXI H, F100	21	LOAD starting address into HL
2003			00	
2004			F1	
2005		LXI B, F200	01	Load destination address into DE
2006			00	
2007			F2	
2008	UP	MOV A, M	7E	Move content of memory to acc.
2009		STAX B	02	Move content of acc. to DE
200A		INX H	23	Increment HL pair address
200B		INX B	03	Increment DE pair address
200C		DCR B	15	Decrement reg. B by 1
200D		JNZ 2008	C2	Jump until D=0
200E			08	
200F			20	
2010		HLT	76	Stop
		#ORG F100		Store block at address F100
		#DB AA, BB, CC, DD, EE, FF		Get data from successive location

RESULT :

INPUT: F100 - AAH, F101 - BBH, F102 - CCH
F103 - DDH, F104 - EEH, F105 - FFH

OUTPUT: F200 - AAH, F201 - BBH, F202 - CCH
F203 - DDH, F204 - EEH, F205 - FFH


8085 Simulator
File Edit Tools Settings Simulation Subroutine View Load Sample Program Help
Editor Assembler
8085 Assembly Language Editor
Assembler Disassembler
ORG 2000H
MVI B,06
LXI H,F100
LXI D,F200
UP: MOV A,M
STAX D
INX H
DCR B
JNZ UP
HLT
ORG F100
DB AA,BB,CC,DD,EE,FF
Autocorrect
Assemble
Created by : Jubin Mitra
Registers Memory Devices
Registers :
Register | Value | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0
Accumulator | FF | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1
Register B | 00 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0
Register C | 00 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0
Register D | F2 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 0
Register E | 00 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0
Register H | F1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 1
Register L | 06 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0
Memory(M) | 00 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0
Resister | Value | S | Z | * | AC | * | P | * | CY
Flag Resister | 54 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0
Type | Value
Stack Pointer(SP) | 0000
Memory Pointer (HL) | F106
Program Status Word(PSW) | FF54
Program Counter(PC) | 200F
Clock Cycle Counter | 233
Instruction Counter | 34
SOD | SID | INTR | TRAP | R7.5 | R6.5 | R5.5
0 | 0 | 0 | 0 | 0 | 0 | 0
For SIM instruction
SOD | SDE | * | R7.5 | MSE | M7.5 | M6.5 | M5.5
0 | 0 | 0 | 0 | 0 | 0 | 0 | 0
For RIM instruction
SID | I7.5 | I6.5 | I5.5 | IE | M7.5 | M6.5 | M5.5
0 | 0 | 0 | 0 | 0 | 0 | 0 | 0
No. Converter Tool :
Hexadecimal | Decimal | Binary
0 | 0 | 0


8085 Simulator
File Edit Tools Settings Simulation Subroutine View Load Sample Program Help
Editor Assembler
Assembler
* | Address | Label | Mnemonics | Hexcode | Bytes | M-Cycles | T-States
√ 2000 | MVI B,06 | 06 | 2 | 2 | 7
2001 | 06
√ 2002 | LXI H,F100 | 21 | 3 | 3 | 10
2003 | 00
2004 | F1
√ 2005 | LXI D,F200 | 11 | 3 | 3 | 10
2006 | 00
2007 | F2
√ 2008 | UP | MOV A,M | 7E | 1 | 2 | 7
√ 2009 | STAX D | 12 | 1 | 2 | 7
√ 200A | INX H | 23 | 1 | 1 | 6
√ 200B | DCR B | 05 | 1 | 1 | 4
√ 200C | JNZ UP | C2 | 3 | 3 | 10
200D | 08
200E | 20
√ 200F | HLT | 76 | 1 | 2 | 5
Simulate
Start From → 2000
Run all At a Time
Step By Step
Created by : Jubin Mitra
Registers Memory Devices
Memory Editor
Memory Range: 0000 ---- FFFF
Memory Address | Value
2000 | 06
2001 | 06
2002 | 21
2004 | F1
2005 | 11
2007 | F2
2008 | 7E
2009 | 12
200A | 23
200B | 05
200C | C2
200D | 08
200E | 20
200F | 76
F100 | AA
F101 | BB
F102 | CC
F103 | DD
F104 | EE
F105 | FF
F200 | FF
Show entire memory content
Show only loaded memory location
Store directly to specified memory location

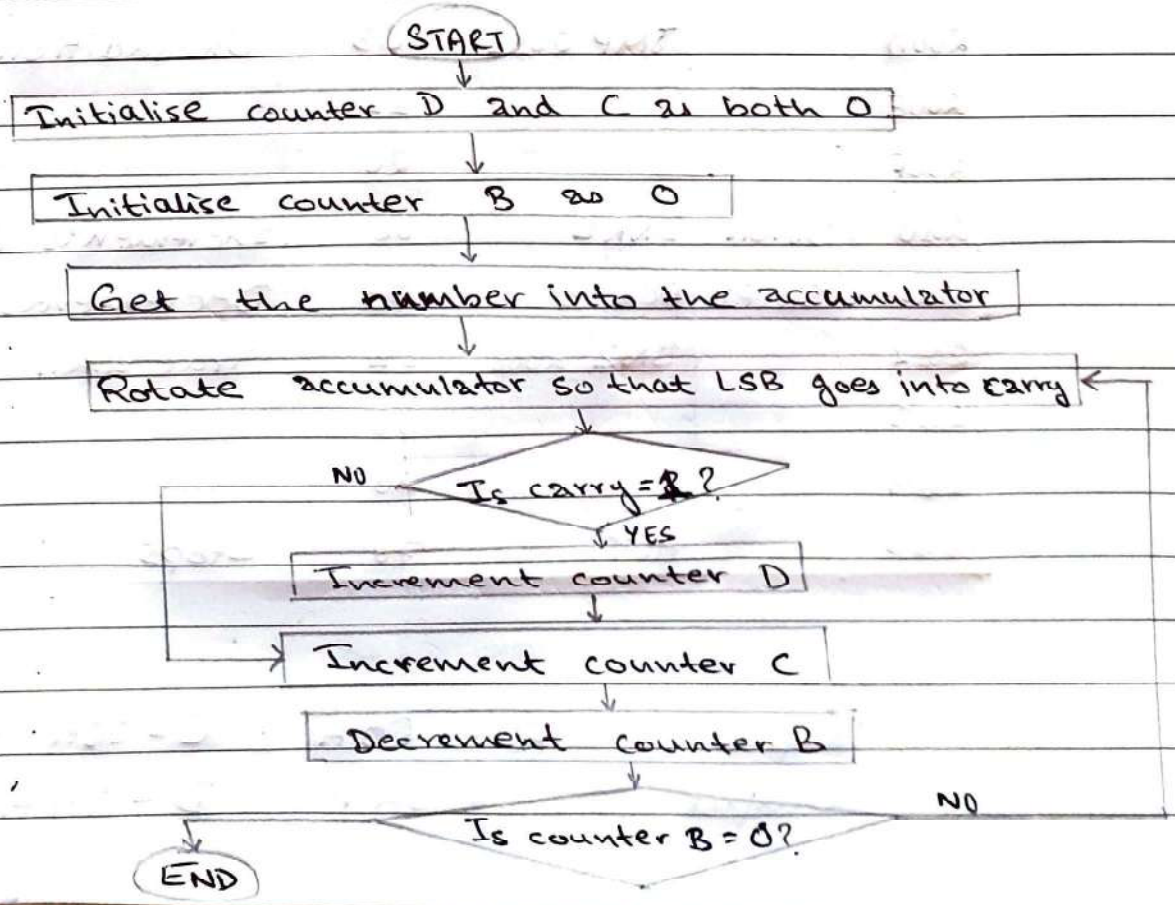
06/10/2020
Experiment-07

AIM: TO CHECK NUMBER OF 1's AND 0's IN GIVEN NUMBER

THEORY:

1. Clear registers C and D
2. Take number into Accumulator.
3. Counter 8 loaded in register B.
4. Rotate left through carry.
5. Jump to step 8 if CF=0
6. D+1 ⇒ D for 1's counter
7. Unconditional jump to step 9
8. C+1 ⇒ C for 0's counter
9. B-1 ⇒ B
10. Jump to Step 4 until B=0
11. Terminate.

FLOWCHART:



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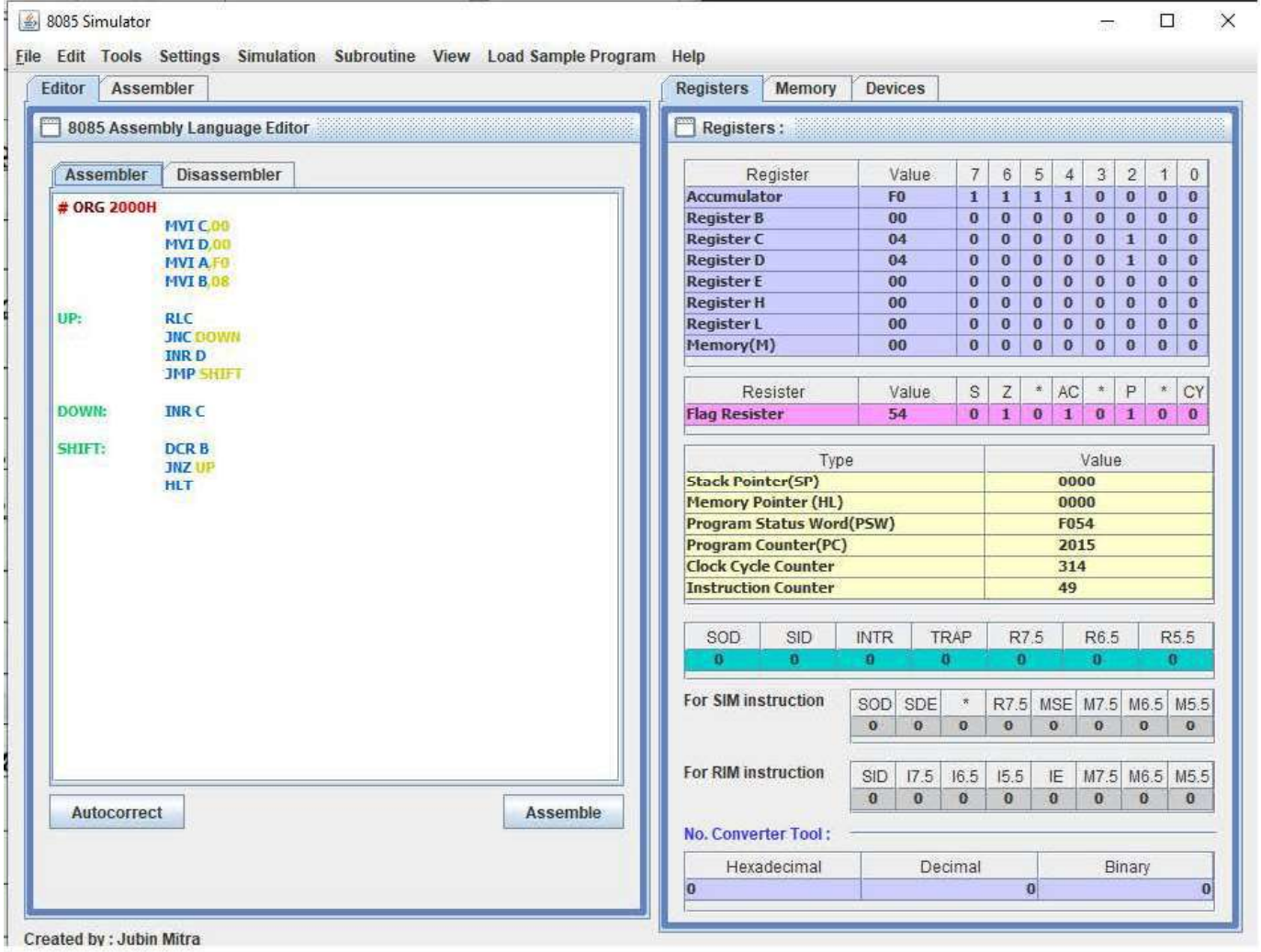
PROGRAM:

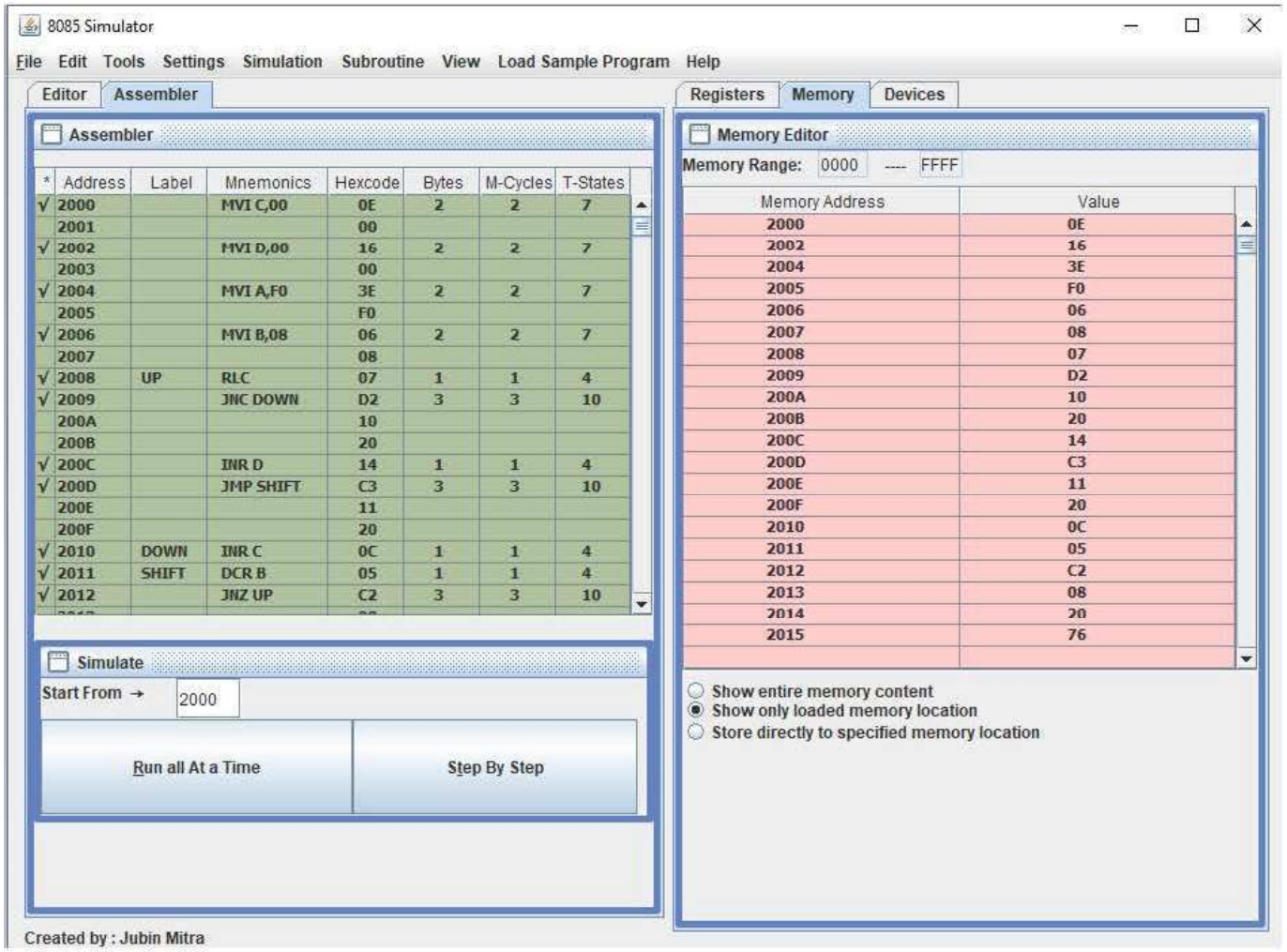
Address	Label	Mnemonics	Hexcode	Comments
		#ORG 2000H		
2000		MVI C,00	0E	Clears register C
2001			00	
2002		MVI D,00	16	Clears register D
2003			00	
2004		MVI A,F0	3E	Takes number into accumulator
2005			F0	
2006		MVI B,08	06	Counter 8 loaded in B reg.
2007			08	
2008	UP	RLC	07	Rotate left through carry
2009		JNC 2010	D2	Jump if CF=0
200A			10	
200B			20	
200C		INR D	14	Increments D for 1's counter
200D		JMP 2011	C3	Unconditional Jump
200E			11	
200F			20	
2010	DOWN	INR C	0C	Increments C for 0's counter
2011	SHIFT	DCR B	05	Decrements B
2012		JNZ 2008	C2	True until B=0
2013			08	
2014			20	
2015		HLT	76	Stops

RESULT:

Input : A - F0H ; C - 00H ; D - 00H

Output : C - 04H ; D - 04H


8085 Simulator
File Edit Tools Settings Simulation Subroutine View Load Sample Program Help
Editor Assembler
8085 Assembly Language Editor
Assembler Disassembler
ORG 2000H
MVI C,00
MVI D,00
MVI A,F0
MVI B,08
UP: RLC
JNC DOWN
INR D
JMP SHIFT
DOWN: INR C
SHIFT: DCR B
JNZ UP
HLT
Autocorrect
Assemble
Registers Memory Devices
Registers :
Register | Value | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0
Accumulator | F0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0
Register B | 00 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0
Register C | 04 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0
Register D | 04 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0
Register E | 00 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0
Register H | 00 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0
Register L | 00 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0
Memory(M) | 00 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0
Resister | Value | S | Z | * | AC | * | P | * | CY
Flag Resister | 54 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0
Type | Value
Stack Pointer(SP) | 0000
Memory Pointer (HL) | 0000
Program Status Word(PSW) | F054
Program Counter(PC) | 2015
Clock Cycle Counter | 314
Instruction Counter | 49
SOD | SID | INTR | TRAP | R7.5 | R6.5 | R5.5
0 | 0 | 0 | 0 | 0 | 0 | 0
For SIM instruction
SOD | SDE | * | R7.5 | MSE | M7.5 | M6.5 | M5.5
0 | 0 | 0 | 0 | 0 | 0 | 0 | 0
For RIM instruction
SID | I7.5 | I6.5 | I5.5 | IE | M7.5 | M6.5 | M5.5
0 | 0 | 0 | 0 | 0 | 0 | 0 | 0
No. Converter Tool :
Hexadecimal | Decimal | Binary
0 | 0 | 0
Created by : Jubin Mitra


8085 Simulator
File Edit Tools Settings Simulation Subroutine View Load Sample Program Help
Editor Assembler
Assembler
* | Address | Label | Mnemonics | Hexcode | Bytes | M-Cycles | T-States
√ 2000 | MVI C,00 | 0E | 2 | 2 | 7
2001 | 00
√ 2002 | MVI D,00 | 16 | 2 | 2 | 7
2003 | 00
√ 2004 | MVI A,F0 | 3E | 2 | 2 | 7
2005 | F0
√ 2006 | MVI B,08 | 06 | 2 | 2 | 7
2007 | 08
√ 2008 | UP | RLC | 07 | 1 | 1 | 4
√ 2009 | JNC DOWN | D2 | 3 | 3 | 10
200A | 10
200B | 20
√ 200C | INR D | 14 | 1 | 1 | 4
√ 200D | JMP SHIFT | C3 | 3 | 3 | 10
200E | 11
200F | 20
√ 2010 | DOWN | INR C | 0C | 1 | 1 | 4
√ 2011 | SHIFT | DCR B | 05 | 1 | 1 | 4
√ 2012 | JNZ UP | C2 | 3 | 3 | 10
Simulate
Start From → 2000
Run all At a Time
Step By Step
Registers Memory Devices
Memory Editor
Memory Range: 0000 ---- FFFF
Memory Address | Value
2000 | 0E
2002 | 16
2004 | 3E
2005 | F0
2006 | 06
2007 | 08
2008 | 07
2009 | D2
200A | 10
200B | 20
200C | 14
200D | C3
200E | 11
200F | 20
2010 | 0C
2011 | 05
2012 | C2
2013 | 08
2014 | 20
2015 | 76
Show entire memory content
Show only loaded memory location
Store directly to specified memory location
Created by : Jubin Mitra