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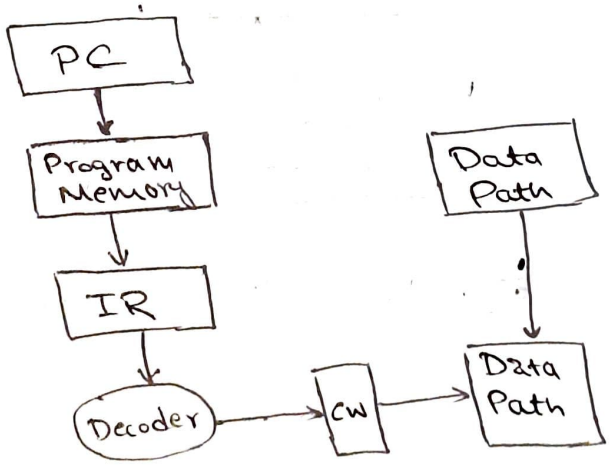
Q.1.

(a) Ans)

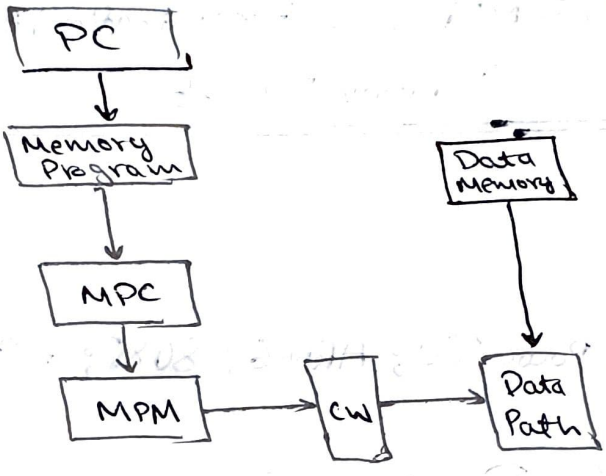
RISC :- IBM PowerPC; ARM6; 8085; Hitachi; SUNSPARC

CISC :- 8086; Pentium; 6800

(b) Ans) : RISC (Reduced Instruction Set Computer) is a CPU design plan based on simple orders and acts fast. This architecture can be represented as the diagram below.



CISC (Complex Instruction Set Computer) is a CPU design plan based on signal commands skilled in executing multi-step operations. This architecture can be represented as following diagram:



Q.1.b (c) Ans: Von-Neumann architecture:

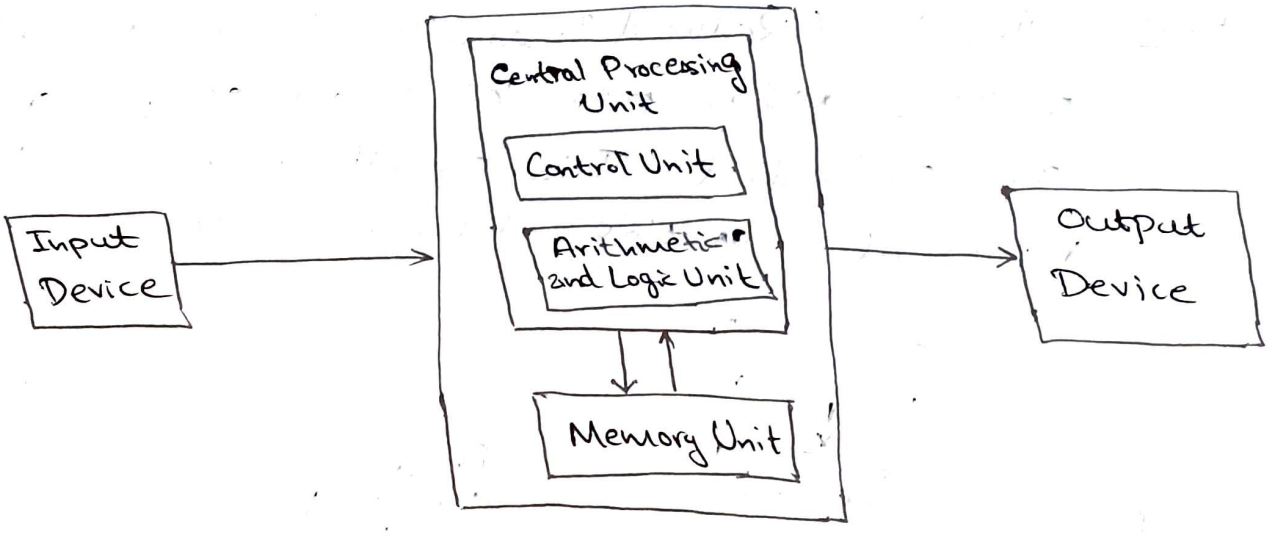


fig: Block Diagram.

Merits of VonNeumann Architecture:

(i) It takes less physical space.

(ii) It handles only one memory block which is simpler and easier to achieve.

(iii) It is comparitively cheaper.

Demerits of VonNeumann Architecture:

(i) A defective program can overwrite another in memory due to shared memory, which may cause it to crash.

(ii) The CPU often sits idle because it is faster than the data bus.

(iii) Given that data and instruction share same data bus, the rate of performance is slower.

Q.2.

(a) Ans) There are generally 5 types of addressing modes:

(i) Direct Addressing Mode: E.g.: LDA 2500H

(ii) Register Addressing Mode: E.g.: MOV A,B

(iii) Register Indirect Addressing Mode: E.g.: MOV A,M

(iv) Immediate Addressing Mode: E.g.: MVI A,05H

(v) Implicit Addressing Mode: E.g.: CMA

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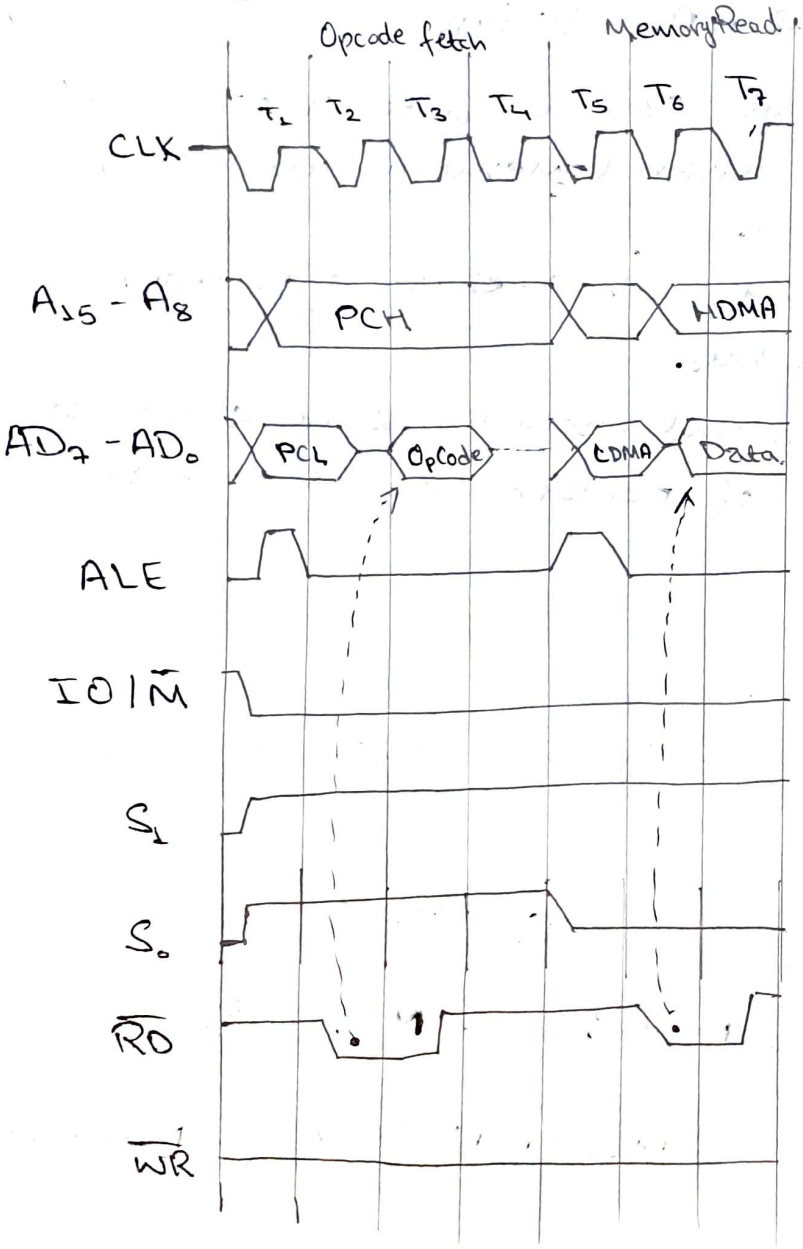
Q.3.(b)

Ans: Given, Instruction : MVI A, 42H

At location 4000H → 3EH is stored.
At location 4001H → 42H is stored.

Timing diagram for executing the instruction:



At 5 MHz clock frequency, the time needed to execute the instruction $= \frac{\text{No. of T states}}{\text{Clock frequency}} = \frac{7\,T}{5 \times 10^6} = 1.4\,\mu s$

Q.4°

Ans Program:

```
        LXI  H, XX70H
        LXI  B, XX90H

LOOP:   MOV  A, M
        CPI  0DH
        JZ   OUTPUT
        CPI  30H
        JC   SKIP
        CPI  39H
        JNC  SKIP
        STAX B
        INX  B

SKIP:   INX  H
        JMP  LOOP

OUTPUT: HLT
```

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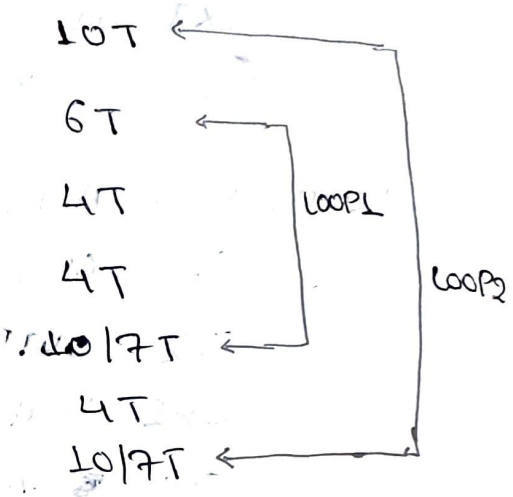
Q.5.)

Ans:

```
        MVI B, 14H          7T
LOOP2:  LXI D, 16-BIT       10T
LOOP1:  DCX D               6T
        MOV A, D            4T
        ORA E               4T
        JNZ LOOP1           10/7T
        DCR B               4T
        JNZ LOOP2           10/7T
```



Required time delay is 2 sec.

Time Required to run inner loop1 = (6+4+4+10) × Count − 3

= 24T × count − 3T

Time Required to run outer loop2 = 7T + 10T + (LOOP1)T + (4T+10T) × 20 − 3T

$\therefore T_L = 4T + (24T + 24 \times \text{count}\ T - 3T)\ 20$

Given, $T_L = 2$ sec

$T = 0.5 \times 10^{-6}$ sec

So, $$\frac{2 - 4\ (0.5 \times 10^{-6})}{20 \times 0.5 \times 10^{-6}} - 21 = 24\ \text{count}$$

$\therefore$ count $= (8332)_{10}$

$\therefore$ count $= (208C)_{16}$