National Institute of Technology, Silchar
End-Semester (UG) Examinations, May 2021

Subject Code: **CS-205** Subject: **Computer Architecture and Organization**

Semester: Four Department: CSE

Duration: One hour Total Marks: 30

Figure in the right hand margin indicates full marks for the question.

Answer all the questions.

1.	Let α be the percentage of program code that can be executed simultaneously by n processors in a computer system. Assume that the remaining code must be executed sequentially by a single processor. Each processor has an execution rate of x MIPS.	
1.(a)	Write the expression for the effective MIPS rate when using the system for exclusive execution of this program, in terms of n, α,and x.	[2]
1. (b)	If n = 32 and x = 8 MIPS, determine the value of α that will yield a system performance of 80 MIPS.	[1]
2.	The following code segment needs to be executed 64 times for the evaluation of the vector arithmetic expression: D(I) = A(I) + B(I) * C(I) for 0 <= I <= 63. Load R1, B(I) /R1 ← Memory(α + I)/ Load R2, C(I) /R2 ← Memory(β+ I)/ Multiply R1, R2 /R1 ← (R1) × (R2)/ Load R3, A(I) /R3 ← Memory(γ + I)/ Add R3, R1 /R3 ← (R3) + (R1)/ Load D1, R3 /Memory(θ+ I) ← (R3)/ where R1, R2, and R3 are processor registers, and α, β, γ, θ are the starting main memory addresses of arrays B(I), C(I), A(I), and D(I), respectively. Assume four clock cycles for each Load or Store, two cycles for the Add, and eight cycles for the Multiplier on either a uniprocessor or a single processor in an SIMD machine.	
2.(a)	Calculate the total number of processor cycles needed to execute this code segment repeatedly 64 times on a SISD uni-processor computer sequentially, ignoring all other time delays.	[1]
2.(b)	Consider the use of an SIMD computer with 64 processing elements to execute the vector operations in six synchronized vector instructions over 64-component vector data and both driven by the same-speed clock. Calculate the total execution time on the SIMD machine, ignoring instruction broadcast and other delays.	[1]
2.(c)	What is the speedup gain of the SIMD computer over the SISD computer?	[1]
3.	Consider a magnetic disk drive with 10 surfaces, 512 tracks per surface, and 64 sectors per track. Sector size is 2 KB. The average seek time is 10 ms, the track-to-track access time is 1.5 ms, and the drive rotates at 3600 rpm. Successive tracks in a cylinder can be read without head movement.	
3.(a)	What is the disk capacity?	[1]
3.(b)	What is the average access time? Assume this file is stored in successive sectors and tracks of successive cylinders, starting at sector 0, track 0, of cylinder i.	[1]
3.(c)	Estimate the time required to transfer a 6-MB file.	[2]
3.(d)	What is the burst transfer rate?	[1]
4.	Write short notes on any four of the following.	[10]
	i) Bus arbitration method. ii) Non-restoring division.	

	iii) Direct mapping iv) Set-associative mapping v) Page replacement algorithms vi) Data Transmission modes	
5	**Fill in the blanks.**	
5. (a)	The size of the physical address space of a processor is 2*P* bytes. The word length is 2*W* bytes. The capacity of cache memory is 2*N* bytes. The size of each cache block is 2*M* words. For a *K*-way set-associative cache memory, the length (in number of bits) of the tag field is_____.	[1]
5. (b)	A processor has 16 integer registers (R0, R1, .. , R15) and 64 floating point registers (F0, F1,… , F63). It uses a 2-byte instruction format. There are four categories of instructions: Type-1, Type-2, Type-3, and Type-4. Type-1 category consists of two instructions, each with 3 integer register operands (3Rs). Type-2 category consists of eight instructions, each with 2 floating point register operands (2Fs). Type-3 category consists of 16 instructions, each with one integer register operand and one floating point register operand (1R+1F). Type-4 category consists of N instructions, each with a floating point register operand (1F). The maximum value of N is _____.	[1]
5. (c)	A CPU generally handles an interrupt by executing an interrupt service routine by checking the _____ after finishing the execution of the current instruction.	[1]
5. (d)	In memory-mapped I/O, the I/O devices and the memory share the same _____	[1]
5. (e)	Bus arbitration methods are Daisy chaining method, Polling method and _____	[1]
5. (f)	If during the execution of an instruction an exceptionis raised then the instruction is _____and the exception is_____.	[2]
5. (g)	To overcome the conflict over the possession of the BUS we use _____.	[1
5. (h)	The transformation from the instruction code bits to an address in control memory where the routine is located is referred to as _____.	[1]