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NATIONAL INSTITUTE OF TECHNOLOGY SILCHAR

CACHAR, ASSAM

LABORATORY EXERCISE BOOK

B.TECH. IIIRD SEM.

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BRANCH: C.S.E. - B

SUBJECT: MICROPROCESSOR LAB

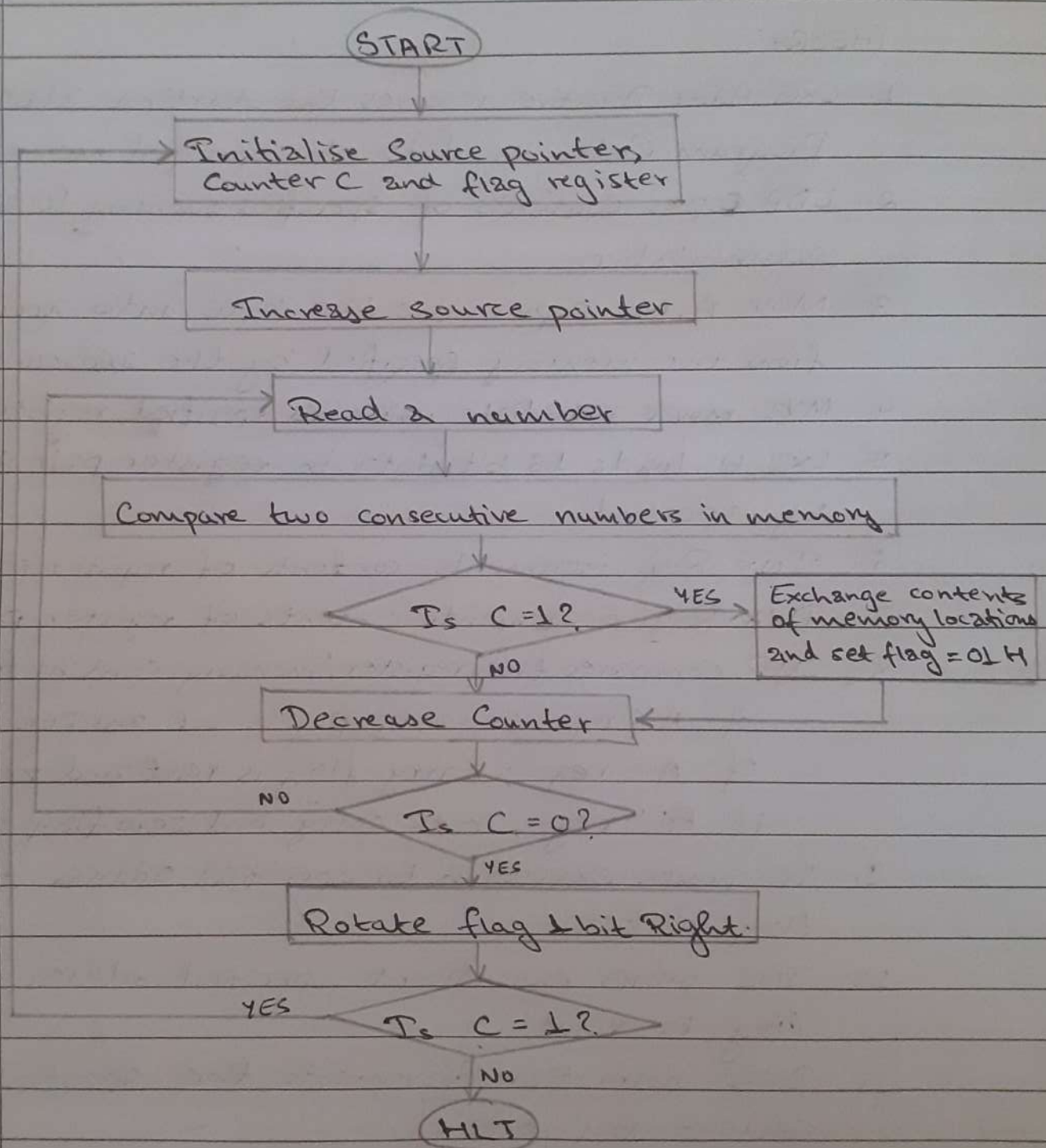
CODE: EE224

AIM: TO ARRANGE NUMBERS IN ASCENDING ORDER

THEORY:

1. ORG Addr. Directive reserves the starting address for Program Code or data in specified memory array.
2. LDA Copies contents of specified memory location to accumulator.
3. MOV A, M copies the data byte into accumulator from the memory specified by the address of HL pair.
4. MVI moves immediate value to specified register.
5. LXI H loads 16 bit data in register pair designated by operand.
6. INX Reg. increments contents of register pair by one.
7. DCX Reg. decrements contents of register pair by one.
8. CMP compares the register/memory content to accumulator.
if $A < \text{reg}$; carry flag is set and zero flag is reset
if $A = \text{reg}$; carry flag is reset and zero flag is set
if $A > \text{reg}$; both carry and zero flag are reset.
9. JC jumps execution to specified address if carry flag is set.
10. JNZ jumps execution to specified address if zero flag is reset.
11. DCR instruction decrements the specified register content by one.
12. HLT stops any further execution.

FLOWCHART:



PROGRAM:

Address	Label	Mnemonics	Opcode	Comment
		#ORG 2000H		
2000		LDA F100H	3A	Load Count from F100 to Acc.
2001			00	
2002			F1	
2003		DCR A	3D	Decrement A by 1
2004		MOV C, A	4F	Moves A contents to C
2005	FRONT	MOV B, C	41	Moves C contents to B
2006		LXI H, F200	21	Loads F200 content in HL
2007			00	
2008			F2	
2009	UP	MOV A, M	7E	Moves HL pointed content to Acc.
200A		INX H	23	Increases HL content by 1
200B		CMP M	BE	Compares reg. M to A
200C		JC DOWN	DA	If A < M, jumps to DOWN
200D			14	
200E			20	
200F		MOV D, M	56	Moves M content to D
2010		MOV M, A	77	Moves Acc. content to Memory
2011		DCX H	2B	Decreases HL content by 1
2012		MOV M, D	72	Moves D contents to Memory
2013		INX H	23	Increases HL content by 1
2014	DOWN	DCR B	05	Decreases B content by 1
2015		JNZ UP	C2	If B ≠ 0, jumps to UP
2016			09	
2017			20	
2018		DCR C	0D	Decrements C content by 1
2019		JNZ FRONT	C2	If C ≠ 0, jumps to FRONT

201A

201B

201C

HLT

76

Terminates further execution

#ORG F100H

Stores number count at address

#DB 04

Gets this number when called.

#ORG F200H

Stores numbers at address

#DB DD,CC,BB,AA

Gets these numbers when add called

RESULT:

Input: F100-04H; F200-DDH;
F201-CC H; F202-BB H;
F203-AA H;

Output: F200-AAH; F201-BB H;
F202-CC H; F203-DD H

8085 Simulator

File Edit Tools Settings Simulation Subroutine View Load Sample Program Help

Editor Assembler

8085 Assembly Language Editor

Assembler Disassembler

```
# ORG 2000H
LDA F100
DCR A
MOV C,A

FRONT:
MOV B,C
LXI H,F200

UP:
MOV A,M
INX H
CMP H
JC DOWN
MOV D,M
MOV M,A
DCX H
MOV M,D
INX H

DOWN:
DCR B
JNZ UP
DCR C
JNZ FRONT
HLT

# ORG F100H
# DB 04
# ORG F200H
# DB DD,CC,BB,AA
```

Autocorrect Assemble

Registers Memory Devices

Registers:

Register	Value	7	6	5	4	3	2	1	0
Accumulator	BB	1	0	1	1	1	0	1	1
Register B	00	0	0	0	0	0	0	0	0
Register C	00	0	0	0	0	0	0	0	0
Register D	AA	1	0	1	0	1	0	1	0
Register E	00	0	0	0	0	0	0	0	0
Register H	F2	1	1	1	1	0	0	1	0
Register L	01	0	0	0	0	0	0	0	1
Memory(M)	BB	1	0	1	1	1	0	1	1

Register	Value	S	Z	* AC	* P	* CY	
Flag Register	54	0	1	0	1	0	0

Type	Value
Stack Pointer(SP)	0000
Memory Pointer (HL)	F201
Program Status Word(PSW)	BB54
Program Counter(PC)	201C
Clock Cycle Counter	542
Instruction Counter	82

SOD	SID	INTR	TRAP	R7.5	R6.5	R5.5
0	0	0	0	0	0	0

For SIM instruction

SOD	SDE	*	R7.5	MSE	M7.5	M6.5	M5.5
0	0	0	0	0	0	0	0

For RIM instruction

SID	I7.5	I6.5	I5.5	IE	M7.5	M6.5	M5.5
0	0	0	0	0	0	0	0

No. Converter Tool:

Hexadecimal	Decimal	Binary
0		0

Created by : Jubin Mitra

8085 Simulator

File Edit Tools Settings Simulation Subroutine View Load Sample Program Help

Editor Assembler

Assembler

* Address	Label	Mnemonics	Hexcode	Bytes	M-Cycles	T-States
✓ 2000		LDA F100	3A	3	4	13
2001			00			
2002			F1			
✓ 2003		DCR A	3D	1	1	4
✓ 2004		MOV C,A	4F	1	1	4
✓ 2005	FRONT	MOV B,C	41	1	1	4
✓ 2006		LXI H,F200	21	3	3	10
2007			00			
2008			F2			
✓ 2009	UP	MOV A,M	7E	1	2	7
✓ 200A		INX H	23	1	1	6
✓ 200B		CMP M	BE	1	2	7
✓ 200C		JC DOWN	DA	3	3	10
200D			14			
200E			20			
✓ 200F		MOV D,M	56	1	2	7
✓ 2010		MOV M,A	77	1	2	7
✓ 2011		DCX H	2B	1	1	6
✓ 2012		MOV M,D	72	1	2	7

Simulate

Start From → 2000

Run all At a Time Step By Step

Registers Memory Devices

Memory Editor

Memory Range: 0000 ---- FFFF

Memory Address	Value
200D	14
200E	20
200F	56
2010	77
2011	2B
2012	72
2013	23
2014	05
2015	C2
2016	09
2017	20
2018	0D
2019	C2
201A	05
201B	20
201C	76
F100	04
F200	AA
F201	BB
F202	CC
F203	DD

☐ Show entire memory content
☒ Show only loaded memory location
☐ Store directly to specified memory location

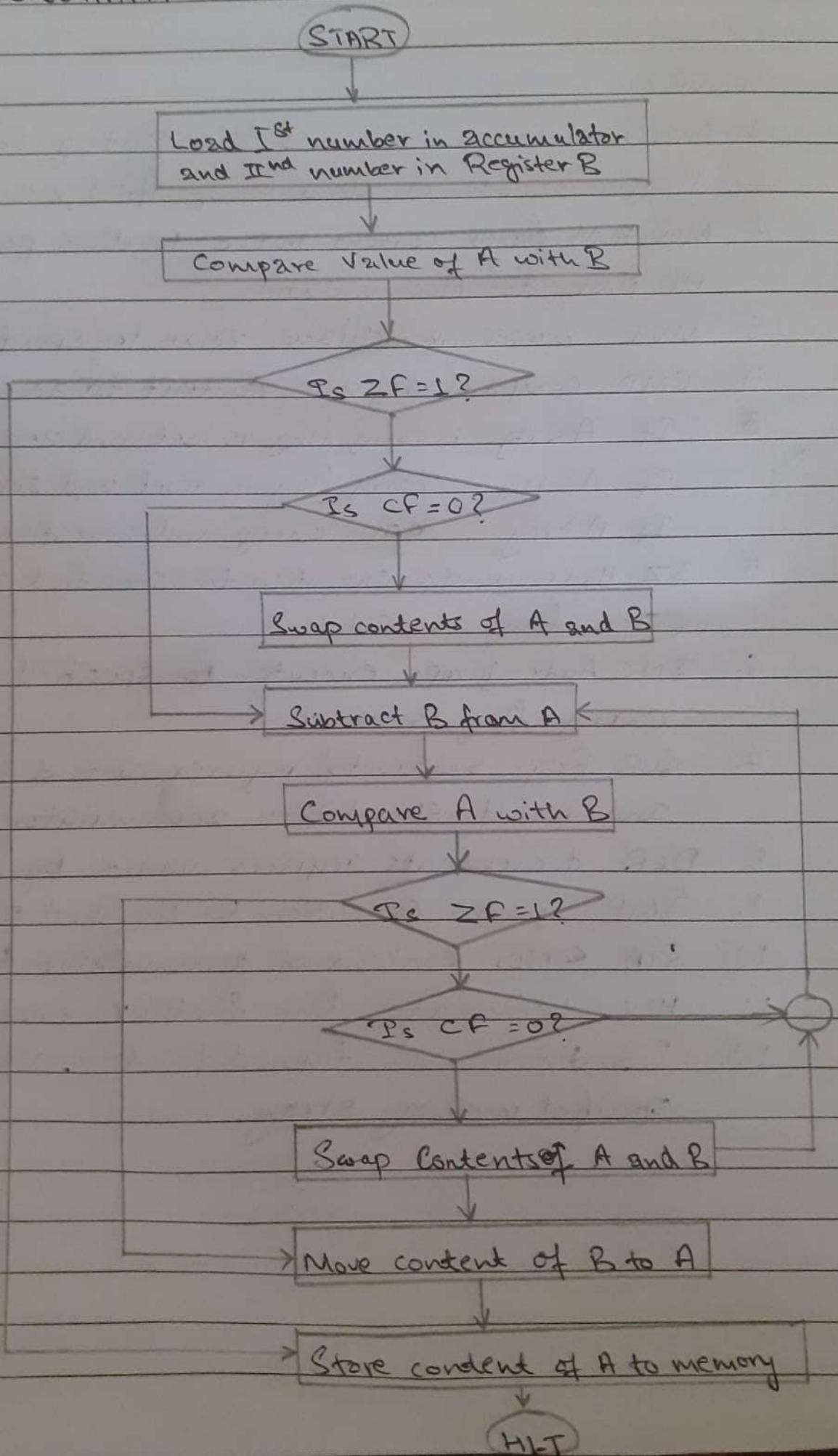
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AIM : TO FIND GCD OF TWO NUMBERS.

THEORY:

1. ORG Addr. Directive reserves the starting address for Program code or data in specified memory array.
2. MOV A,M copies content in the location pointed by HL pair to Accumulator.
3. MVI moves immediate value to specified register.
4. CMP compares register content to accumulator.
 - If $A < \text{reg.}$; carry flag is set and zero flag is reset.
 - If $A = \text{reg.}$; carry flag is reset and zero flag is set.
 - If $A > \text{reg.}$; both carry and zero flags are reset.
5. JZ Addr. jumps execution to specified address if zero flag is set.
6. JNC Addr. jumps execution to specified address if carry flag is reset.
7. SUB Reg. subtracts register content by accumulator and result stored into accumulator.
8. DCR decrements register value by 1.
9. JMP jumps execution to specified address.
10. STA copies content of accumulator to address.
11. HLT terminates the further execution.
12. DB directive is defined to store values in specified memory array.

FLOWCHART :



PROGRAM:

Address	Label	Mnemonics	Opcode	Comment
		#ORG 2000H		
2000		MVI A, 09	3E	Load first number in Accumulator
2001			09	
2002		MVI B, 07	06	Load second no. in reg. B
2003			07	
2004		CMP B	BB	Compare B to A
2005		JZ DOWN	CA	if A=B, jumps to DOWN
2006		J	1D	
2007			20	
2008		INC SHIFT	D2	if A>B, jump to SHIFT
2009			0E	
200A			20	
200B		MOV C, A	4F	Move A contents to C
200C		MOV A, B	78	Move B contents to A
200D		MOV B, C	41	Move C contents to B
200E	SHIFT	SUB B	90	Subtract B from A
200F		CMP B	88	Compare B to A
2010		JZ MOVE	CA	if A=B, move to MOVE
2011			1C	
2012			20	
2013		INC SHIFT	D2	If A>B, jump to SHIFT
2014			0E	
2015			20	
2016		MOV C, A	4F	Move A contents to C
2017		MOV A, B	78	Move B contents to A
2018		MOV B, C	41	Move C contents to B
2019		JMP SHIFT	C3	Jump to SHIFT

201A			0E	
201B			20	
201C	MOVE	MOV A,B	78	Move B content to Acc
201D	DOWN	STA F200	32	Store Acc.content in F200
201E			00	
201F			F2	
2020		HLT	76	Terminate

RESULT:

Input: A - 09H ; B - 07H

Output: A - 01H ; F200 - 01H

8085 Simulator

File

Edit

Tools

Settings

Simulation

Subroutine

View

Load Sample Program

Help

Editor

Assembler

8085 Assembly Language Editor

Assembler

Disassembler

```
# ORG 2000H
MVI A,09
MVI B,07
CMP B
JZ DOWN
JNC SHIFT
MOV C,A
MOV A,B
MOV B,C

SHIFT:
SUB B
CMP B
JZ MOVE
JNC SHIFT
MOV C,A
MOV A,B
MOV B,C
JMP SHIFT

MOVE:
MOV A,B

DOWN:
STA F200
HLT
```

Autocorrect

Assemble

Registers

Memory

Devices

Registers :

Register	Value	7	6	5	4	3	2	1	0
Accumulator	01	0	0	0	0	0	0	0	1
Register B	01	0	0	0	0	0	0	0	1
Register C	01	0	0	0	0	0	0	0	1
Register D	00	0	0	0	0	0	0	0	0
Register E	00	0	0	0	0	0	0	0	0
Register H	00	0	0	0	0	0	0	0	0
Register L	00	0	0	0	0	0	0	0	0
Memory(M)	00	0	0	0	0	0	0	0	0

Resister	Value	S	Z	*	AC	*	P	*	CY
Flag Resister	54	0	1	0	1	0	1	0	0

Type	Value
Stack Pointer(SP)	0000
Memory Pointer (HL)	0000
Program Status Word(PSW)	0154
Program Counter(PC)	2020
Clock Cycle Counter	213
Instruction Counter	35

SOD	SID	INTR	TRAP	R7.5	R6.5	R5.5
0	0	0	0	0	0	0

For SIM instruction

SOD	SDE	*	R7.5	MSE	M7.5	M6.5	M5.5
0	0	0	0	0	0	0	0

For RIM instruction

SID	I7.5	I6.5	I5.5	IE	M7.5	M6.5	M5.5
0	0	0	0	0	0	0	0

No. Converter Tool :

Hexadecimal	Decimal	Binary
0		0

8085 Simulator

File

Edit

Tools

Settings

Simulation

Subroutine

View

Load Sample Program

Help

Editor

Assembler

Assembler

*	Address	Label	Mnemonics	Hexcode	Bytes	M-Cycles	T-States
✓	2000		MVI A,09	3E	2	2	7
	2001			09			
✓	2002		MVI B,07	06	2	2	7
	2003			07			
✓	2004		CMP B	B8	1	1	4
✓	2005		JZ DOWN	CA	3	3	10
	2006			1D			
	2007			20			
✓	2008		JNC SHIFT	D2	3	3	10
	2009			0E			
	200A			20			
✓	200B		MOV C,A	4F	1	1	4
✓	200C		MOV A,B	78	1	1	4
✓	200D		MOV B,C	41	1	1	4
✓	200E	SHIFT	SUB B	90	1	1	4
✓	200F		CMP B	B8	1	1	4
✓	2010		JZ MOVE	CA	3	3	10
	2011			1C			
	2012			20			

Simulate

StartFrom → 2000

Run all At a Time

Step By Step

Registers

Memory

Devices

Memory Editor

Memory Range: 0000 ---- FFFF

Memory Address	Value
200C	78
200D	41
200E	90
200F	B8
2010	CA
2011	1C
2012	20
2013	D2
2014	0E
2015	20
2016	4F
2017	78
2018	41
2019	C3
201A	0E
201B	20
201C	78
201D	32
201F	F2
2020	76
F200	01

☐ Show entire memory content
☒ Show only loaded memory location
☐ Store directly to specified memory location

Created by : Jubin Mitra