# An electronic Van der Pol/Duffing oscillator

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## 1 General schematics of the electronic Van der Pol/Duffing oscillator

Figure 1 presents the (simplified) schematics of the electronic circuit used to implement a Van der Pol/Duffing oscillator in [1], inspired by [2–4]. The goal of this design was to create an oscillator with precisely tunable damping parameters. As shall be shown in Section 2, the relation between the input and output voltages, $V_{\text{in}}$ and $V_{\text{out}}$, respectively, is a Van der Pol/Duffing equation. An additional output $V_1$ is proportional to the time derivative of $V_{\text{out}}$. The circuit contains three operational amplifiers that make up two integrators and an inverting amplifier, two buffers, and five analog multipliers. Two potentiometers ($p_2$ and $p_3$) are used to tune some of the parameters of the circuit (the linear and cubic stiffness coefficients), while the remaining parameters (damping coefficients) are given by input signals to the circuit.

The practical realization in [1] also uses three additional switches and three additional buffers. The latter are needed to ensure low-impedance output and high-impedance input signals. As for the switches, two of them are used to enable the measurement of the division ratios of the potentiometers, and the third one can be used to obtain either a single- or double-well oscillator. Two additional potentiometers are also used to trim the offsets in the output signals. The circuit requires an external power source with symmetric supplies. The input and output signals can be imposed/measured with BNC connectors.

## 2 Governing equations

The following section assumes ideal operational amplifier behavior, i.e., no current flows into the input pins, and the voltage of these input pins is identical (due to the feedback action of the amplifier) [5]. It is also assumed that the buffers are perfect. Their output voltage is thus, from left to right, $p_i V_i$ $(0 \leq p_i \leq 1)$ for $i = 2, 3$, where $p_2$ and $p_3$ are the division ratios of the potentiometers.

Since the inverting input of the leftmost operational amplifier is (virtually) grounded, the currents going into $R_1$, $R_2$, $R_3$, $R_4$ and $R_8$ all go into $C_1$, summing up to $I_1$. This realizes a summing integrator governed by

$$\dot{V}_1 = -\frac{1}{C_1} I_1 = -\frac{1}{C_1}\left(\frac{p_2 V_2}{R_2} + \frac{p_3 V_3}{R_3} + \frac{V_4}{R_8} + \frac{V_5}{R_1} + \frac{V_{\text{in}}}{R_4}\right). \tag{1}$$

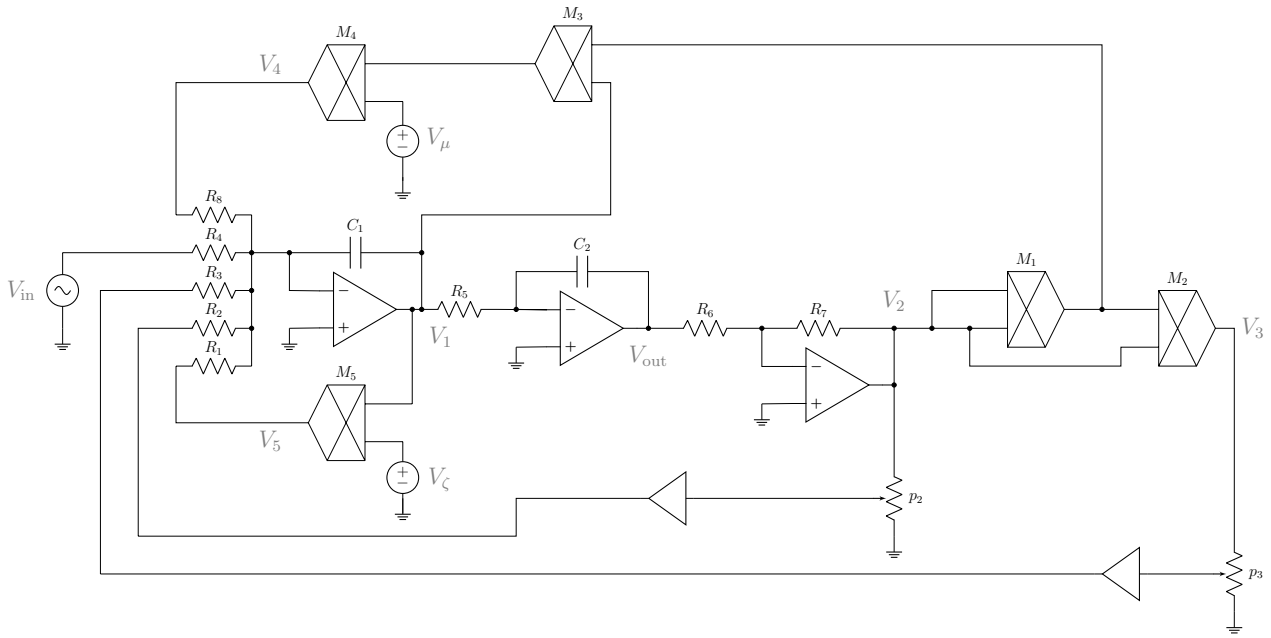


Figure 1: Schematics of the electronic Van der Pol/Duffing oscillator.

The inverting input of the middle operational amplifier is also (virtually) grounded, and since the current going into $R_5$ also goes into $C_2$, this circuit implements an integrator governed by

$$\dot{V}_{\text{out}} = -\frac{V_1}{C_2 R_5}. \tag{2}$$

Finally, since the inverting input of the rightmost amplifier is (virtually) grounded and the current going through $R_6$ also goes into $R_7$, the circuit implements an inverting amplifier, i.e.,

$$V_2 = -\frac{R_7 V_{\text{out}}}{R_6}. \tag{3}$$

The output of the first multiplier $M_1$ is $g_{\text{m}} V_2^2$, and that of $M_2$ is

$$V_3 = g_{\text{m}}^2 V_2^3, \tag{4}$$

where $g_{\text{m}}$ is the gain of the electronic multiplier. The output of $M_3$ is $g_{\text{m}}^2 V_1 V_2^2$, and that of $M_4$ is

$$V_4 = V_\mu g_{\text{m}}^3 V_1 V_2^2. \tag{5}$$

Finally, the output of $M_5$ is

$$V_5 = V_\zeta g_{\text{m}} V_1. \tag{6}$$

Assembling Equations (1)-(6), one obtains a second-order differential equation for $V_{\text{out}}$:

$$C_1 C_2 R_4 R_5 \ddot{V}_{\text{out}} + V_\zeta \frac{g_m C_2 R_4 R_5}{R_1} \dot{V}_{\text{out}} + p_2 \frac{R_4 R_7}{R_2 R_6} V_{\text{out}} + V_\mu \frac{g_m^3 C_2 R_4 R_5 R_7^2}{R_6^2 R_8} V_{\text{out}}^2 \dot{V}_{\text{out}} + p_3 \frac{g_{\text{m}}^2 R_4 R_7^3}{R_3 R_6^3} V_{\text{out}}^3 = V_{\text{in}}, \tag{7}$$

which is a Van der Pol/Duffing equation of type

$$m\ddot{V}_{\text{out}} + c\dot{V}_{\text{out}} + kV_{\text{out}} + \mu V_{\text{out}}^2 \dot{V}_{\text{out}} + k_3 V_{\text{out}}^3 = V_{\text{in}}. \tag{8}$$

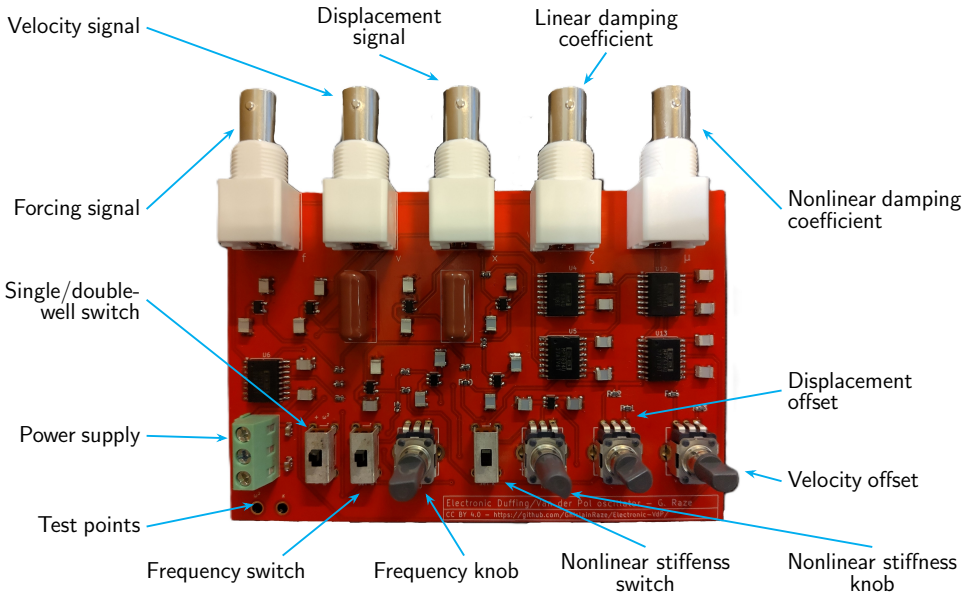


Figure 2: Picture of the electronic van der Pol/Duffing oscillator.

Figure 2 shows a photograph of the realization of the circuit in Figure 1 using Texas Instrument OPA210 operational amplifiers [6] and MPY634 multipliers [7].

## 3 Design choices

The electronic Van der Pol/Duffing oscillator was designed to be interfaced with a MicroLabBox from dSPACE, hence had to be able to work with voltages in the $\pm 10\ V$ range. These requirements guided the choice of the electrical parameters and integrated circuits, and are discussed in [4].

### 3.1 Integrated circuits choice

OPA210 are precision operational amplifiers with very low offset voltage ($\leq 5\ \mu V$), which was the main motivation for their selection, together with their supply voltage range ($V_{\text{s}} = \pm 18\ V$). In addition, they feature a large bandwidth for this application (GBW = 18 MHz) for a relatively low quiescent current [6]. For simplicity, buffers were realized with the same operational amplifiers in an input follower configuration.

The MPY634 analog multipliers were chosen for their availability, for their wide bandwidth (10 MHz) and for their adequate voltage range [7].

### 3.2 Other elements

Bipolar capacitors with high capacitances were needed to allow for relatively low resonance frequencies (in order to require reasonable resistances). Most dielectric materials with a high dielectric constant generally also feature high dissipation, which entails parasitic damping in the oscillator that can be complicated to model. Polypropylene (PP) film capacitors were thus selected for $C_1$ and $C_2$ due to their low dissipation, since their relatively large volume is not a problem in this application.

Lossy integrators can be used instead of the integrators implemented with the first and second operational amplifiers by placing a resistor with large resistance in parallel to $C_1$ and/or $C_2$. Since there was no saturation issue with the integrators, and since the offsets are quite small in the tested version of the circuit, this was not deemed necessary. In addition, this circuit contains potentiometers to trim the offsets.

Following the application note, bypass capacitors of $0.1\mu$F were used for all integrated circuits [6], and bulk capacitors of $10\mu$F were used for the power supply.

### 3.3 Parameter values

The design considerations outlined herein led to the parameters gathered in Table 1. Note that the potentiometers allow for a flexible range of parameters $k$ and $k_3$, but if the extreme values of these ranges are not satisfactory, other resistances and/or capacitances should be selected. The same goes for parameters $c$ and $\mu$.

| **Parameter** | **Value** |
|---|---|
| $R_1$ (k$\Omega$) | 100 |
| $R_2$ (k$\Omega$) | 10 |
| $R_3$ (k$\Omega$) | 1 |
| $R_4$ (k$\Omega$) | 100 |
| $R_5$ (k$\Omega$) | 1 |
| $R_6$ (k$\Omega$) | 10 |
| $R_7$ (k$\Omega$) | 10 |
| $R_8$ (k$\Omega$) | 1 |
| $C_1$ ($\mu$F) | 1 |
| $C_2$ ($\mu$F) | 1 |
| $g_\mathrm{m}$ (V$^{-1}$) | 0.1 |

Table 1: Electrical parameters of the electronic Van der Pol/Duffing oscillator.

## 4 Circuit implementation

### 4.1 Use of the circuit

The electrical Van der Pol/Duffing oscillator can be used in an experimental setup. This section briefly describes how to use the printed circuit board (PCB) in [1]. The reader can refer to Figure 2

to identify the different elements on the PCB.

BNC connectors are used to drive the circuit via the forcing signal port (symbol `f` on the PCB for $V_{\text{in}}$) and to measure its output (symbols `x` and `v` on the PCB for $V_{\text{out}}$ and for $V_1$, respectively). Additionally, the voltages $V_\zeta$ and $V_\mu$ are set with BNC connectors (with symbols $\zeta$ and $\mu$ on the PCB, respectively), which allows for a precise tuning of the damping parameters. The circuit requires an external DC power source with symmetric supplies connected to the terminal block in the bottom left corner of the PCB. The supply voltage can range from $\pm 8\ V$ to $\pm 18\ V$ to comply with the maximum ratings of the integrated circuits [6, 7].

The parameters $m$, $c$, $\mu$, $k$ and $k_3$ in Equation (8) can be computed by a simple comparison with Equation (7). The value of $p_2$ and $p_3$ can be adjusted by turning the knobs of the potentiometers. The switches `Set` $\omega^2$ and `Set` $\kappa$ on the PCB need to be up when the circuit is in operation, but can be down to make the determination of the value of these parameters easy when the circuit is not in operation. When they are down, they connect the potentiometers $p_2$ and $p_3$ (respectively) to the positive power supply. The output of the buffer connected to the potentiometer is also connected to a test point (vias) in the bottom left of the PCB ($\omega^2$ and $\kappa$ on the PCB, respectively). If the positive supply voltage is $V_{\text{s}}$ and the switches are down, the voltage measured at these test points should be equal to $p_i V_{\text{s}}$, allowing the user to deduce the value of $p_i$.

The last switch ($\pm\omega^2$ on the PCB) is used to implement a single- or double-well oscillator, when the switch is up or down, respectively. In the latter case, $p_2$ is connected to $V_{\text{out}}$ instead of $V_2$ (cf. Figure 1).

Finally, two potentiometers (`x offset` and `v offset`) can be adjusted to negate the DC voltage offsets of the `x` and `v` channels when there are no external forcing and limit cycles.

### 4.2 Non-ideal behavior

Although the circuit does replicate the dynamics of a Van der Pol/Duffing oscillator quite faithfully, this replication is not perfect due to several non-idealities. The ones suspected to be the most impactful are listed hereafter:

1. **Voltage offsets:** there exists voltage offsets at the input and output of the different integrated circuits, preventing a perfect symmetry in the oscillator. This can be partially fought with the trimming potentiometers. It is recommended to adjust them so as to have a zero output displacement and velocity when the input force is zero and there are no limit cycles.

2. **Imperfect integrators:** due to its finite open-loop gain, an operational amplifier used in an integrator will not perform an exact integration [6]. As also mentioned earlier, dissipation in the capacitors may also be the cause for an imperfect integrator behavior.

3. **Imperfect nonlinearity:** analog multipliers can also feature a small error (the output will not exactly be the product of the input voltages) [7].

## References


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