Maseeh College of Engineering
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ECE 560: FALL 2023 - PROJECT
ASSERTION BASED VERIFICATION

ASSERTION-BASED VERIFICATION OF AN AHB2APB BRIDGE

VERIFICATION PLAN

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AHB2APB Bridge Assertion-Based Verification

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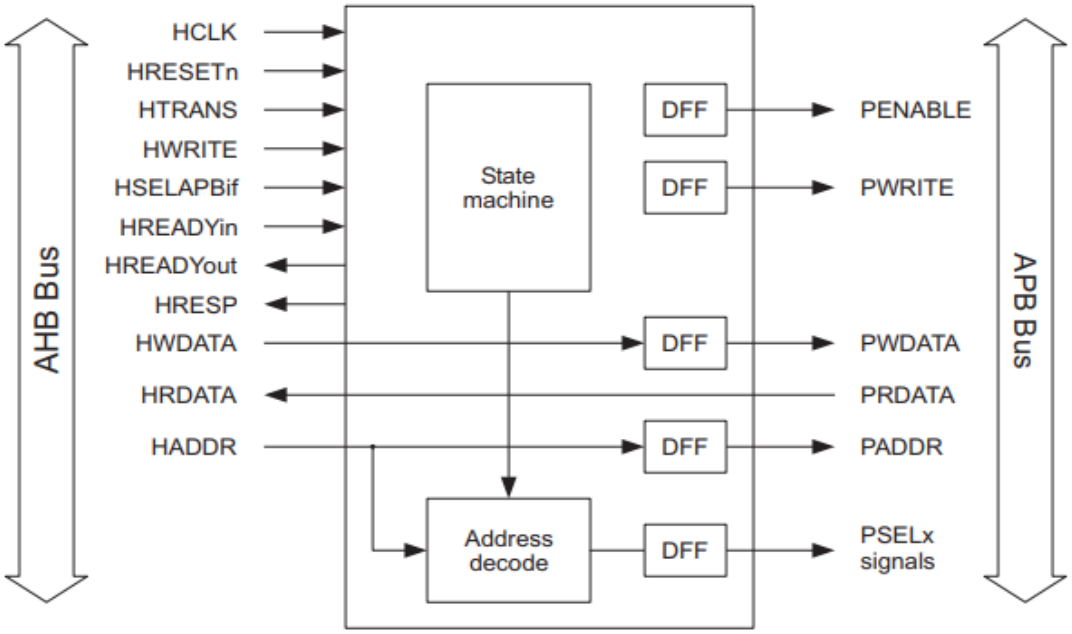
Introduction:

The purpose of this Verification Plan is to outline the approach and methodology we will use to verify the functionality and performance of the AHB-APB bridge design. The AHB-APB bridge is a critical component that is responsible for facilitating communication between the high-performance system bus (AHB) and the low-power peripheral bus (APB).

Project Proposal:

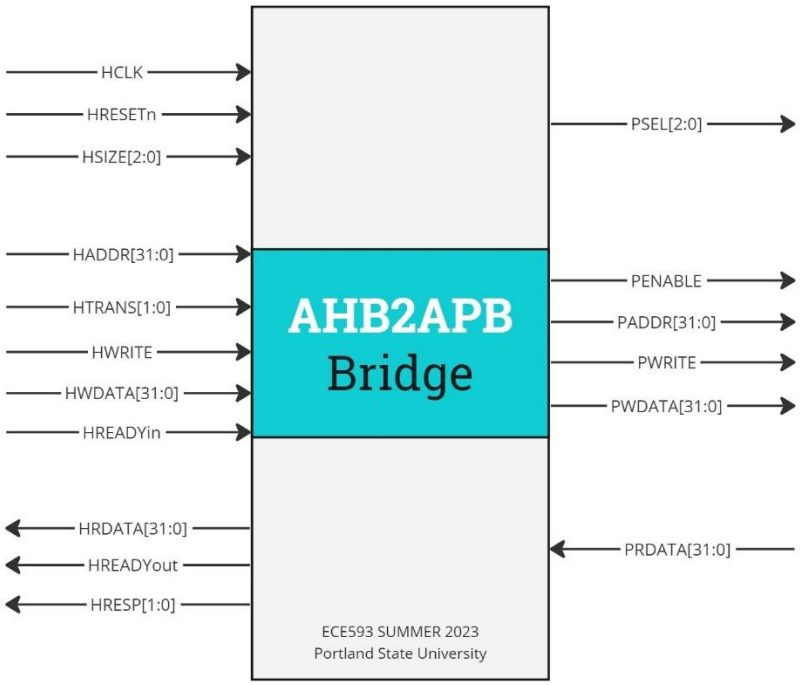
We are taking an assertion-based formal verification approach to functionally verify the AHB2APB design. We will write properties capturing the design specifications of the bridge given the official ARM AMBA specifications of the AHB and APB Protocols as well as the bridge itself. We will write assumptions to set the expected input of the different signals, and write the assertions to verify the expected behavior of the outputs, we also plan to write a few cover properties to make sure we thoroughly verified the design. We selected an RTL code for the AHB2APB bridge design, which is included as an attachment to this submission. The chosen RTL code can also be found here: https://github.com/prajwalgekkouga/AHB-to-APB-Bridge.

Design Description:



Basic Description:

- AHB to APB bridge provides an interface between the high speed AHB and the low power APB.
- Read and write transfers on the AHB are converted into equivalent transfers on the APB.
- It has AHB slave bus interface, APB transfer state machine, which is independent of the device memory map, and APB output signal generation.
- It buffers address, controls, and data from the AHB, drives the APB peripherals and returns data along with a response signal to the AHB.
- APB data bus is divided into read (PRDATA), where data travels from the peripherals to the bridge and write (PWDATA), where data travels from the bridge to the peripherals.
- Data transfers can have 3 different sizes (HSIZE) Byte, halfword or full word.
- Data transfers are either sent as a single transfer or can be sent in a burst (HBURST). Bursts can be incremental or wrapping bursts with 4 or 8-beats.



Input Port:

AHB:

- HCLK: Clock signal for the AHB interface.
- HRESETn: Active-low reset signal for the AHB interface.
- HSIZE[2:0]: Size of the transfer on the AHB interface.
- HADDR[31:0]: Address for the AHB transfer.
- HTRANS[1:0]: Transfer type on the AHB interface.
- HWRITE: Write enable signal for the AHB interface.
- HWDATA[31:0]: Write data on the AHB interface.
- HREADYin: Ready signal indicating the availability of the AHB interface.

APB:

- PRDATA[31:0]: Read data on the APB interface.

Output Port:

AHB:

- HRDATA[31:0]: Read data from the AHB interface.
- HREADYout: Ready signal indicating the readiness of the AHB interface.
- HRESP[1:0]: Response indicating the status of the AHB transfer.

APB:

- PSEL[2:0]: Slave select signal on the APB interface.
- PENABLE: Enable signal for the APB interface.
- PADDR[31:0]: Address for the APB transfer.
- PWRITE: Write enable signal for the APB interface.
- PWDATA[31:0]: Write data on the APB interface.

Timing Diagrams

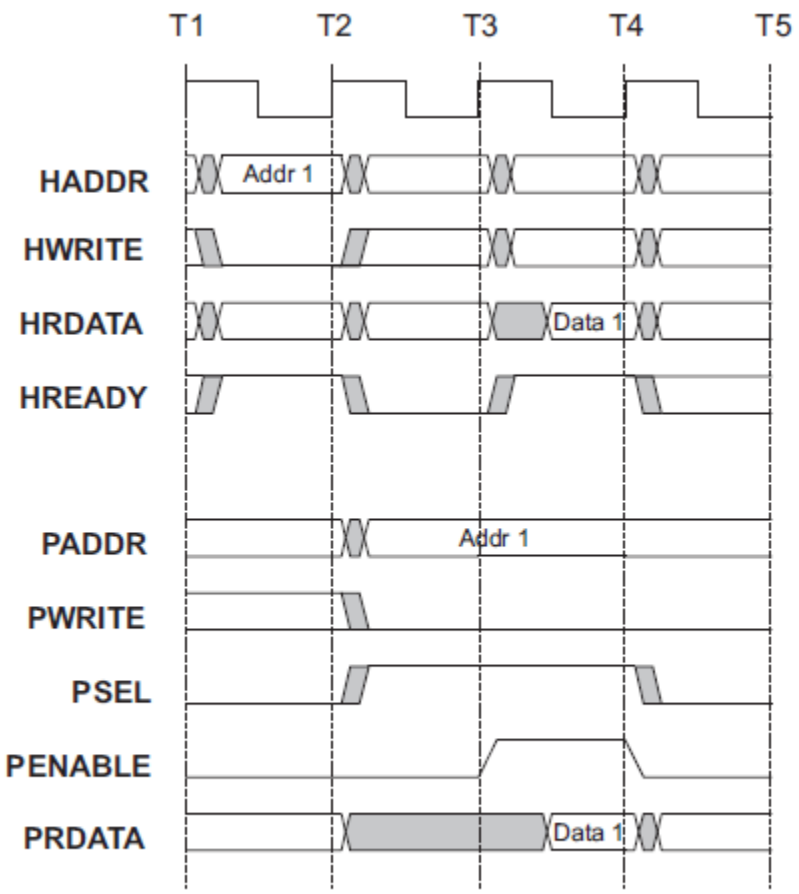


Figure 5-9 Read transfer to AHB

HADDR is sampled by APB at T2 which can be seen with the PADDR signal displaying “addr 1” at T2. At T2 PWRITE is pulled low and PSEL is asserted high. PSEL must also be high during the PENABLE signal, which must also be asserted high during the transfer for Data1 to be valid. HREADY Must also be high when DATA1 is on the HRDATA line. Each read requires a wait state for the transfer to occur.

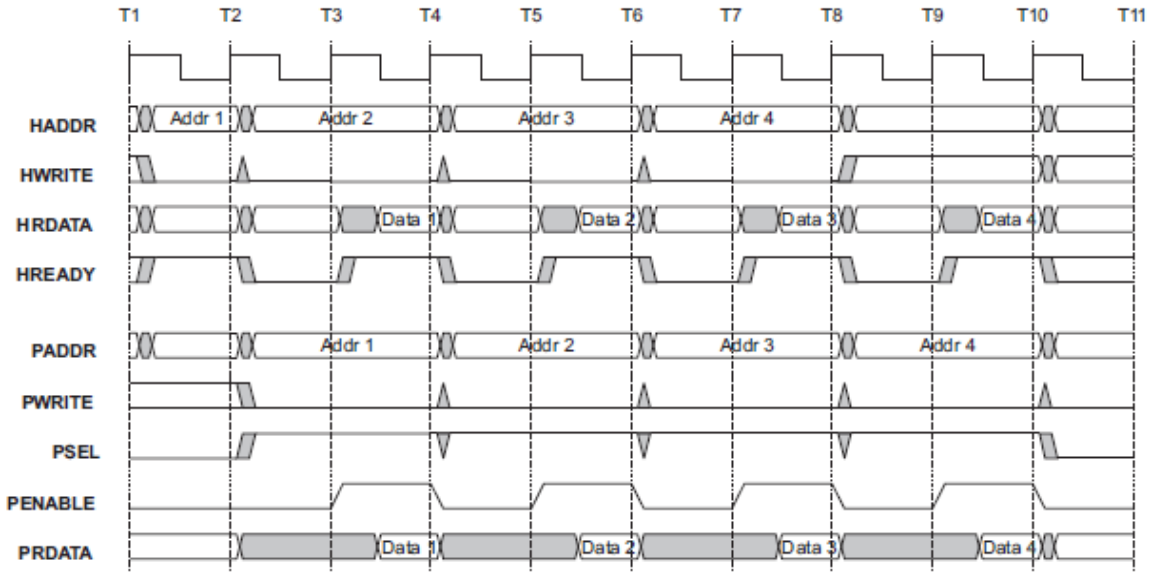


Figure 5-10 Burst of read transfers

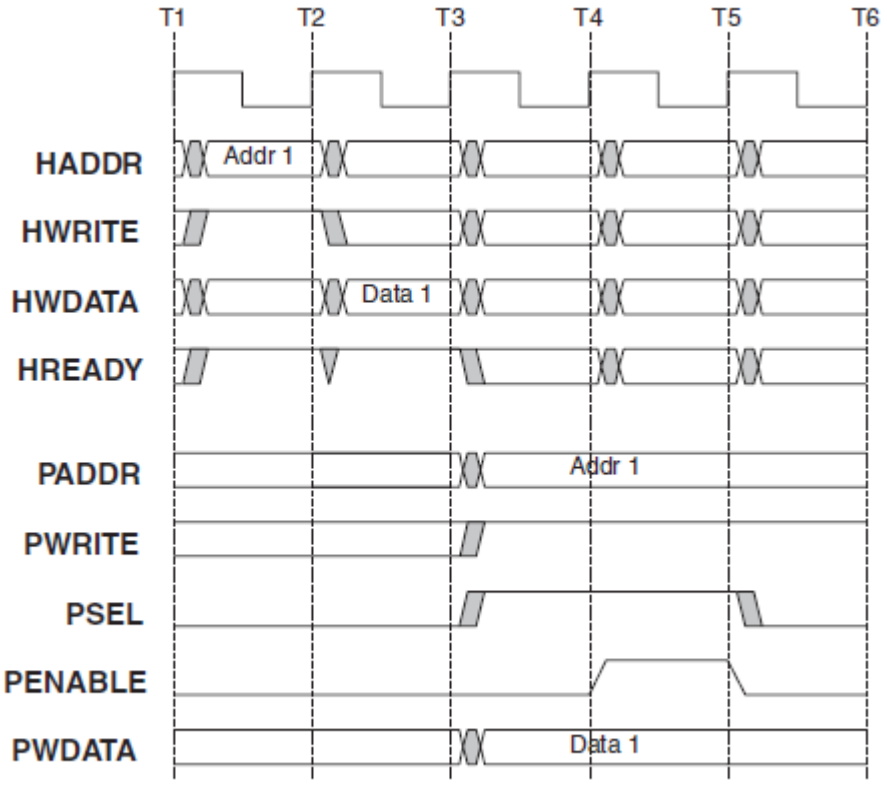


Figure 5-11 Write transfer from AHB

Write transfers can occur with zero transfers. The bridge must sample the address and data of the transfer and must hold these values for the duration of the write transfer.

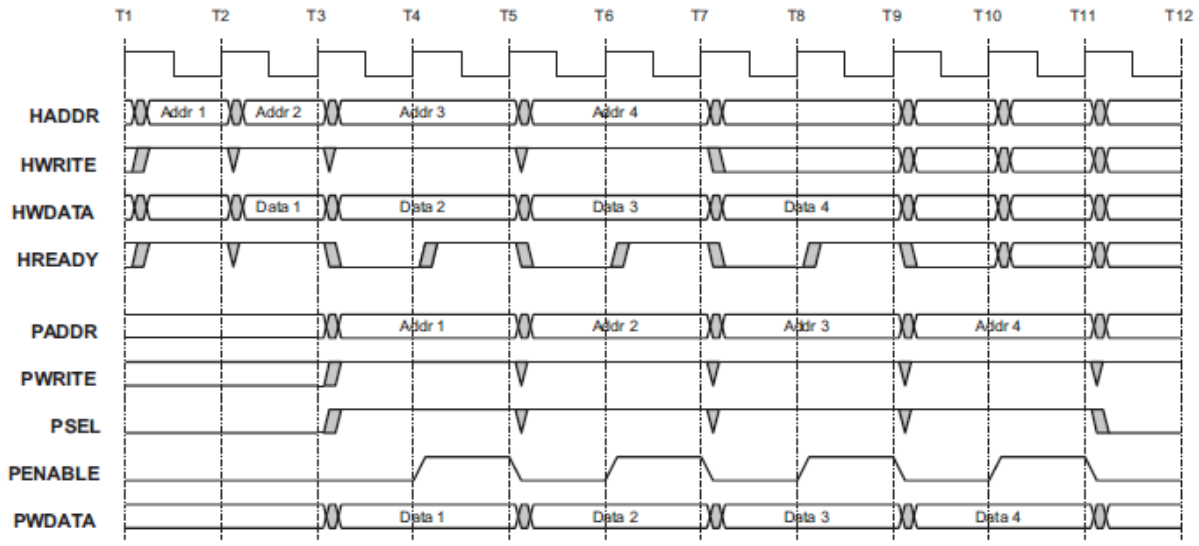


Figure 5-12 Burst of write transfers

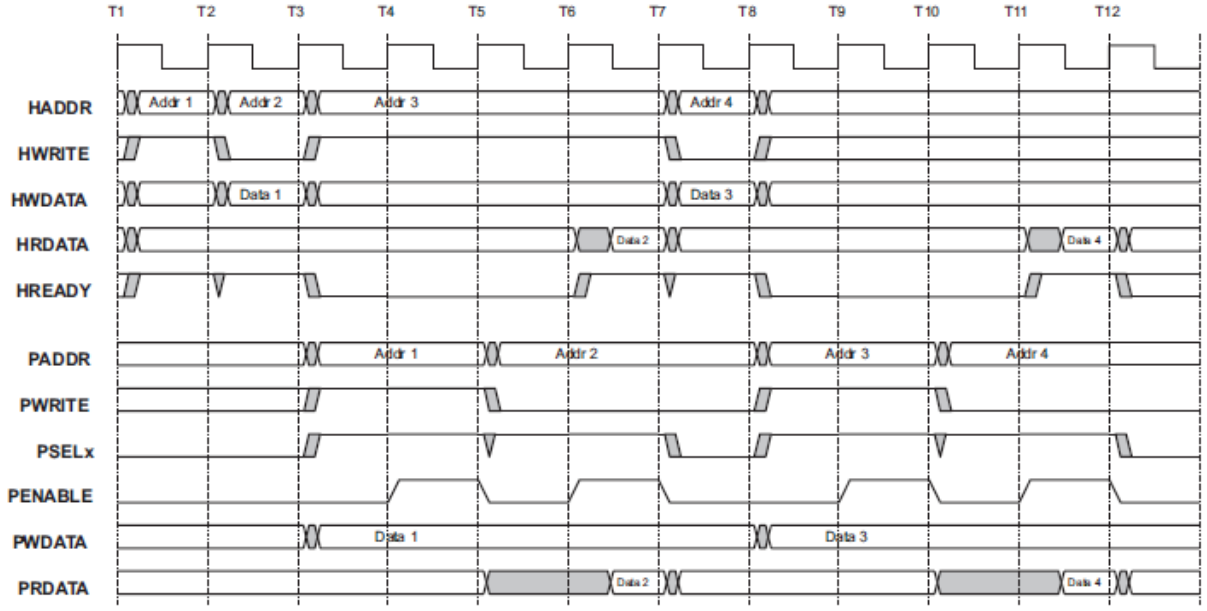


Figure 5-13 Back to back transfers

When a read follows a write, there must be 3 wait states to complete the read. The three wait states can be seen on HREADY and PWRITE.

Verification Plan Spreadsheet

Please refer to our attached xlsx spreadsheet for our verification methodology of each function to be validated, methodology used, description, interface of design, etc.

Summary

We have an excel Validation plan which specifies the functions, and interfaces we are verifying as well as the methodologies we are using. We plan to mostly use FPV (Formal Property Verification) to verify the FSM implementations, a