

# N-Channel Enhancement Mode Field Effect Transistor

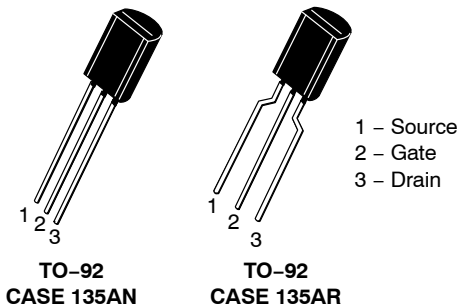
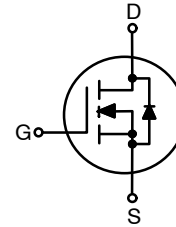
## 2N7000, 2N7002, NDS7002A

### Description

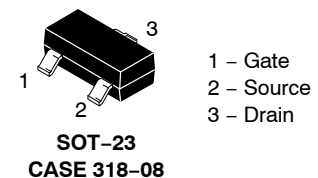
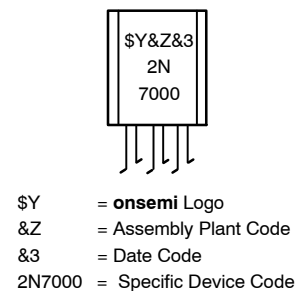
These N-channel enhancement mode field effect transistors are produced using onsemi's proprietary, high cell density, DMOS technology. These products have been designed to minimize on-state resistance while providing rugged, reliable, and fast switching performance. They can be used in most applications requiring up to 400 mAdc and can deliver pulsed currents up to 2 A. These products are particularly suited for low-voltage, low-current applications, such as small servo motor control, power MOSFET gate drivers, and other switching applications.

### Features

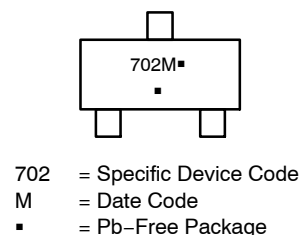
- High Density Cell Design for Low  $R_{DS(on)}$
- Voltage Controlled Small Signal Switch
- Rugged and Reliable
- High Saturation Current Capability
- This Device is Pb-Free and Halogen Free



### MARKING DIAGRAM



### MARKING DIAGRAM



(Note: Microdot may be in either location)

### ORDERING INFORMATION

See detailed ordering and shipping information on page 7 of this data sheet.

## 2N7000, 2N7002, NDS7002A

**ABSOLUTE MAXIMUM RATINGS** Values are at  $T_C = 25^\circ\text{C}$  unless otherwise noted.

Symbol	Parameter	Value			Unit
		2N7000	2N7002	NDS7002A	
V <sub>DSS</sub>	Drain-to-Source Voltage	60			V
V <sub>DGR</sub>	Drain-Gate Voltage (R <sub>GS</sub> ≤ 1 MW)	60			V
V <sub>GSS</sub>	Gate-Source Voltage – Continuous	±20			V
	Gate-Source Voltage – Non Repetitive (tp < 50 ms)	±40			
I <sub>D</sub>	Maximum Drain Current – Continuous	200	115	280	mA
	Maximum Drain Current – Pulsed	500	800	1500	
P <sub>D</sub>	Maximum Power Dissipation Derated above 25°C	400	200	300	mW
		3.2	1.6	2.4	mW/°C
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Temperature Range	-55 to 150		-65 to 150	°C
T <sub>L</sub>	Maximum Lead Temperature for Soldering Purposes, 1/16-inch from Case for 10 s	300			°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

**THERMAL CHARACTERISTICS** Values are at  $T_C = 25^\circ\text{C}$  unless otherwise noted.

Symbol	Parameter	Value			Unit
		2N7000	2N7002	NDS7002A	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	312.5	625	417	$^\circ\text{C/W}$

### ELECTRICAL CHARACTERISTICS

Values are at  $T_C = 25^\circ\text{C}$  unless otherwise noted.

Symbol	Parameter	Conditions	Type	Min	Typ	Max	Unit
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#### OFF CHARACTERISTICS

$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, I_D = 10 \mu\text{A}$	All	60	–	–	V
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 48 \text{ V}, V_{GS} = 0 \text{ V}$	2N7000	–	–	1	$\mu\text{A}$
		$V_{DS} = 48 \text{ V}, V_{GS} = 0 \text{ V}, T_C = 125^\circ\text{C}$		–	–	1	mA
		$V_{DS} = 60 \text{ V}, V_{GS} = 0 \text{ V}$	2N7002	–	–	1	$\mu\text{A}$
		$V_{DS} = 60 \text{ V}, V_{GS} = 0 \text{ V}, T_C = 125^\circ\text{C}$	NDS7002A	–	–	0.5	mA
$I_{GSSF}$	Gate – Body Leakage, Forward	$V_{GS} = 15 \text{ V}, V_{DS} = 0 \text{ V}$	2N7000	–	–	10	nA
		$V_{GS} = 20 \text{ V}, V_{DS} = 0 \text{ V}$	2N7002 NDS7002A	–	–	100	
$I_{GSSR}$	Gate – Body Leakage, Reverse	$V_{GS} = -15 \text{ V}, V_{DS} = 0 \text{ V}$	2N7000	–	–	-10	nA
		$V_{GS} = -20 \text{ V}, V_{DS} = 0 \text{ V}$	2N7002 NDS7002A	–	–	-100	

#### ON CHARACTERISTICS

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 1 \text{ mA}$	2N7000	0.8	2.1	3	V
		$V_{DS} = V_{GS}, I_D = 250 \mu\text{A}$	2N7002 NDS7002A	1	2.1	2.5	

# 2N7000, 2N7002, NDS7002A

## ELECTRICAL CHARACTERISTICS (continued)

Values are at  $T_C = 25^\circ\text{C}$  unless otherwise noted.

Symbol	Parameter	Conditions	Type	Min	Typ	Max	Unit
<b>ON CHARACTERISTICS</b>							
$R_{DS(on)}$	Static Drain–Source On–Resistance	$V_{GS} = 10\text{ V}, I_D = 500\text{ mA}$	2N7000	–	1.2	5	$\Omega$
		$V_{GS} = 10\text{ V}, I_D = 500\text{ mA}, T_C = 125^\circ\text{C}$		–	1.9	9	
		$V_{GS} = 4.5\text{ V}, I_D = 75\text{ mA}$		–	1.8	5.3	
		$V_{GS} = 10\text{ V}, I_D = 500\text{ mA}$	2N7002	–	1.2	7.5	
		$V_{GS} = 10\text{ V}, I_D = 500\text{ mA}, T_C = 100^\circ\text{C}$		–	1.7	13.5	
		$V_{GS} = 5\text{ V}, I_D = 50\text{ mA}$		–	1.7	7.5	
		$V_{GS} = 5\text{ V}, I_D = 50\text{ mA}, T_C = 100^\circ\text{C}$		–	2.4	13.5	
		$V_{GS} = 10\text{ V}, I_D = 500\text{ mA}$	NDS7002A	–	1.2	2	
		$V_{GS} = 10\text{ V}, I_D = 500\text{ mA}, T_C = 125^\circ\text{C}$		–	2	3.5	
		$V_{GS} = 5\text{ V}, I_D = 50\text{ mA}$		–	1.7	3	
		$V_{GS} = 5\text{ V}, I_D = 50\text{ mA}, T_C = 125^\circ\text{C}$		–	2.8	5	
$V_{DS(on)}$	Drain–Source On–Voltage	$V_{GS} = 10\text{ V}, I_D = 500\text{ mA}$	2N7000	–	0.6	2.5	V
		$V_{GS} = 4.5\text{ V}, I_D = 75\text{ mA}$		–	0.14	0.4	
		$V_{GS} = 10\text{ V}, I_D = 500\text{ mA}$	2N7002	–	0.6	3.75	
		$V_{GS} = 5.0\text{ V}, I_D = 50\text{ mA}$		–	0.09	1.5	
		$V_{GS} = 10\text{ V}, I_D = 500\text{ mA}$	NDS7002A	–	0.6	1	
		$V_{GS} = 5.0\text{ V}, I_D = 50\text{ mA}$		–	0.09	0.15	
$I_{D(on)}$	On–State Drain Current	$V_{GS} = 4.5\text{ V}, V_{DS} = 10\text{ V}$	2N7000	75	600	–	mA
		$V_{GS} = 10\text{ V}, V_{DS} \geq 2 V_{DS(on)}$	2N7002	500	2700	–	
		$V_{GS} = 10\text{ V}, V_{DS} \geq 2 V_{DS(on)}$	NDS7002A	500	2700	–	
$g_{FS}$	Forward Transconductance	$V_{DS} = 10\text{ V}, I_D = 200\text{ mA}$	2N7000	100	320	–	mS
		$V_{DS} \geq 2 V_{DS(on)}, I_D = 200\text{ mA}$	2N7002	80	320	–	
		$V_{DS} \geq 2 V_{DS(on)}, I_D = 200\text{ mA}$	NDS7002A	80	320	–	

## DYNAMIC CHARACTERISTICS

$C_{iss}$	Input Capacitance	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}$	All	–	20	50	pF
$C_{oss}$	Output Capacitance		All	–	11	25	
$C_{rss}$	Reverse Transfer Capacitance		All	–	4	5	
$t_{on}$	Turn–On Time	$V_{DD} = 15\text{ V}, R_L = 25\ \Omega, I_D = 500\text{ mA}, V_{GS} = 10\text{ V}, R_{GEN} = 25\ \Omega$	2N7000	–	–	10	ns
		$V_{DD} = 30\text{ V}, R_L = 150\ \Omega, I_D = 200\text{ mA}, V_{GS} = 10\text{ V}, R_{GEN} = 25\ \Omega$	2N7002 NDS7002A	–	–	20	
$t_{off}$	Turn–Off Time	$V_{DD} = 15\text{ V}, R_L = 25\ \Omega, I_D = 500\text{ mA}, V_{GS} = 10\text{ V}, R_{GEN} = 25\ \Omega$	2N7000	–	–	10	ns
		$V_{DD} = 30\text{ V}, R_L = 150\ \Omega, I_D = 200\text{ mA}, V_{GS} = 10\text{ V}, R_{GEN} = 25\ \Omega$	2N7002 NDS7002A	–	–	20	

# 2N7000, 2N7002, NDS7002A

## ELECTRICAL CHARACTERISTICS (continued)

Values are at  $T_C = 25^\circ\text{C}$  unless otherwise noted.

Symbol	Parameter	Conditions	Type	Min	Typ	Max	Unit
<b>DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS</b>							
$I_S$	Maximum Continuous Drain-Source Diode Forward Current	2N7002	–	–	–	115	mA
		NDS7002A	–	–	–	280	
$I_{SM}$	Maximum Pulsed Drain-Source Diode Forward Current	2N7002	–	–	–	0.8	A
		NDS7002A	–	–	–	1.5	
$V_{SD}$	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 115\text{ mA}$ (Note 1)	2N7002	–	0.88	1.5	V
		$V_{GS} = 0\text{ V}, I_S = 400\text{ mA}$ (Note 1)	NDS7002A	–	0.88	1.2	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. Pulse test: Pulse Width  $\leq 300\text{ }\mu\text{s}$ , Duty Cycle  $\leq 2\%$

## TYPICAL PERFORMANCE CHARACTERISTICS

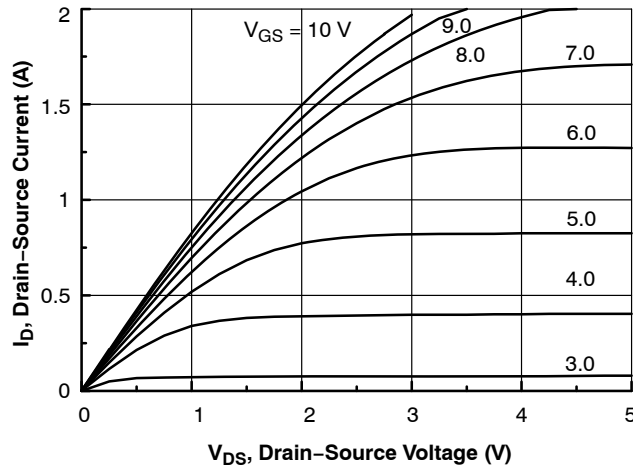


Figure 1. On-Region Characteristics

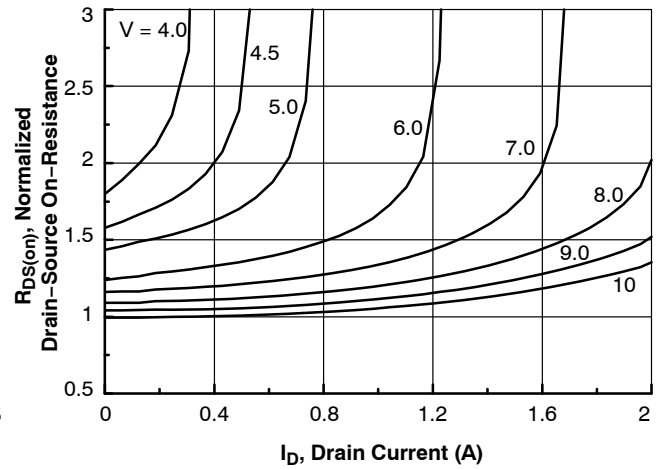


Figure 2. On-Resistance Variation with Gate Voltage and Drain Current

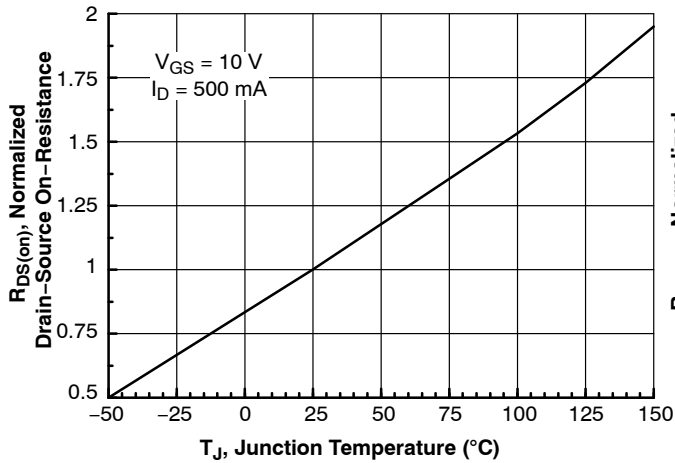


Figure 3. On-Resistance Variation with Temperature

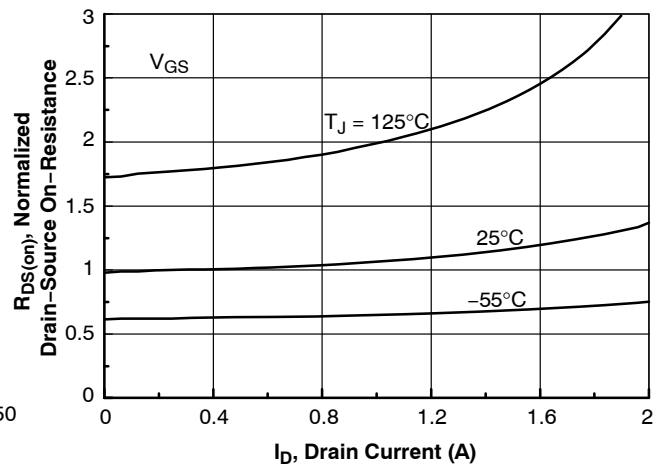


Figure 4. On-Resistance Variation with Drain Current and Temperature

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

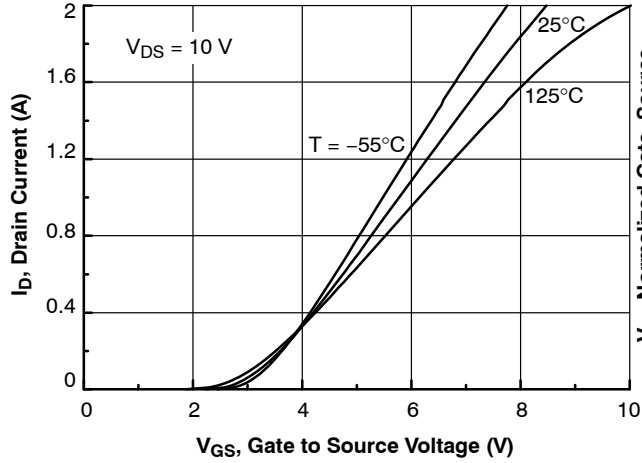


Figure 5. Transfer Characteristics

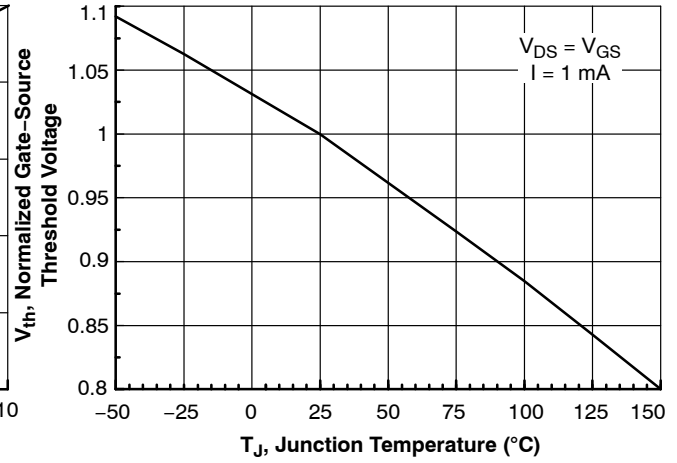


Figure 6. Gate Threshold Variation with Temperature

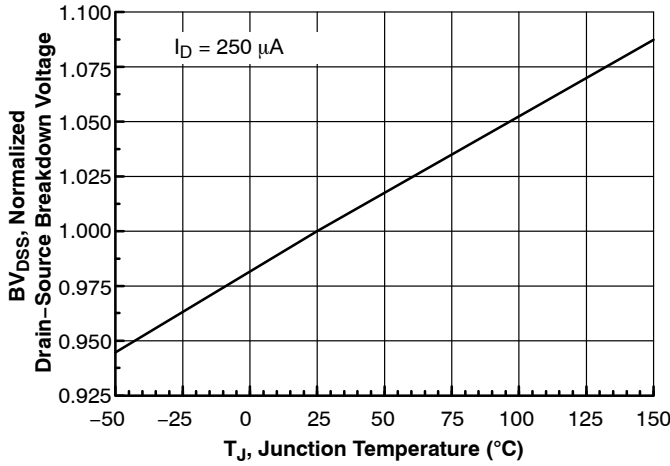


Figure 7. Breakdown Voltage Variation with Temperature

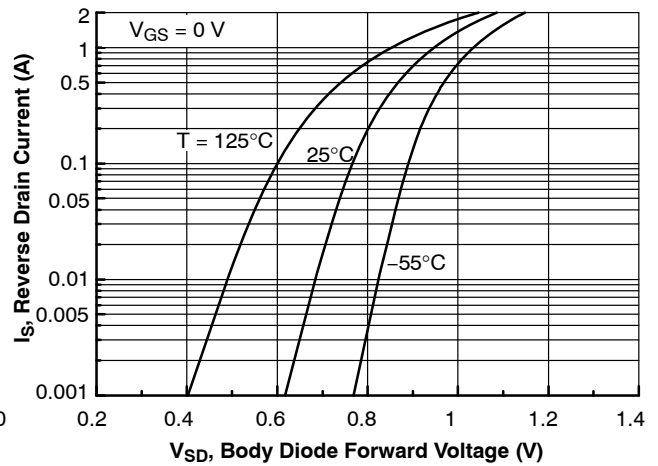


Figure 8. Body Diode Forward Voltage Variation with Temperature

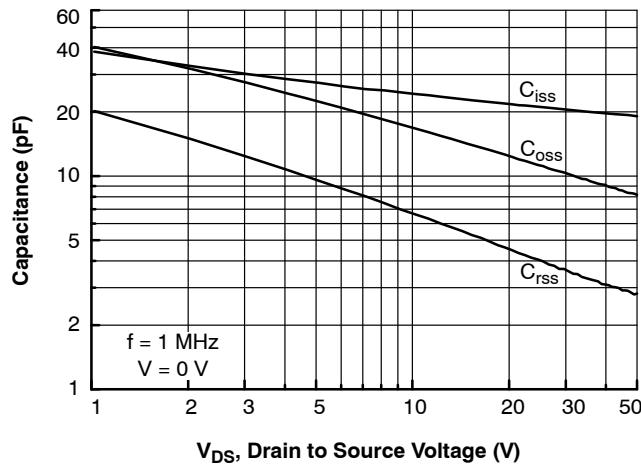


Figure 9. Capacitance Characteristics

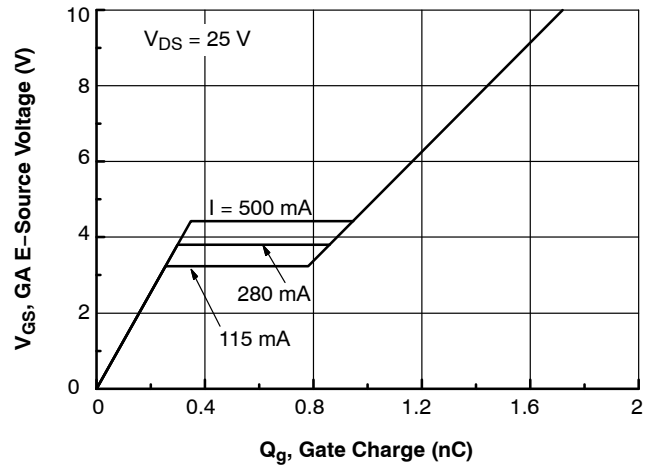


Figure 10. Gate Charge Characteristics

# 2N7000, 2N7002, NDS7002A

## TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

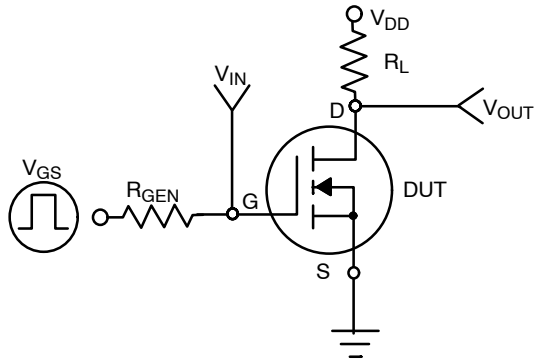


Figure 11. Switching Test Circuit

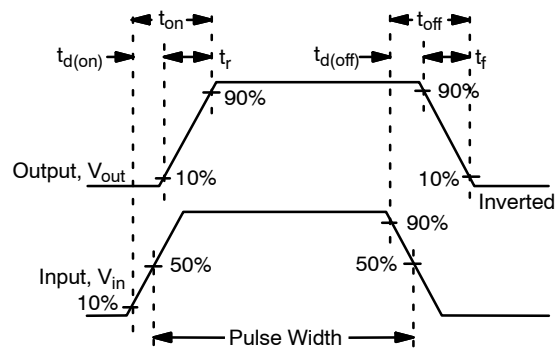


Figure 12. Switching Waveforms

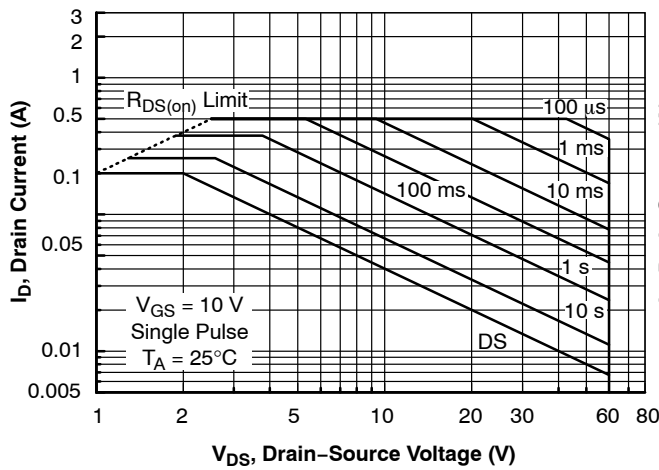


Figure 13. 2N7000 Maximum Safe Operating Area

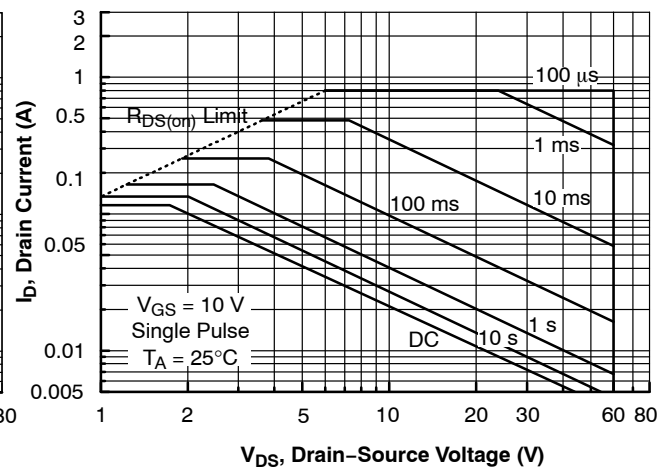


Figure 14. 2N7002 Maximum Safe Operating Area

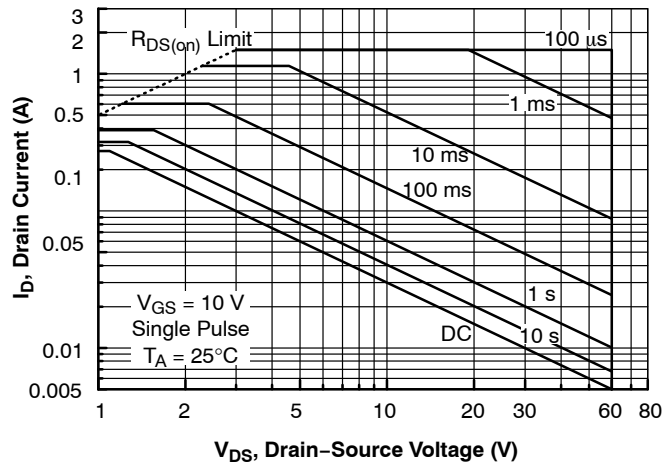


Figure 15. NDS7000A Maximum Safe Operating Area

# 2N7000, 2N7002, NDS7002A

## TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

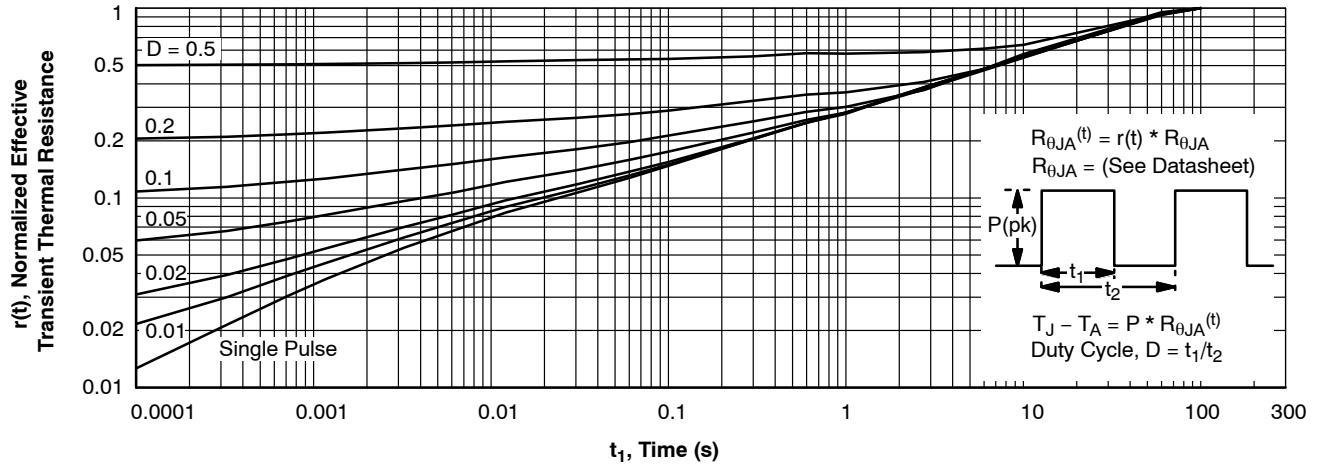


Figure 16. TO-92, 2N7000 Transient Thermal Response Curve

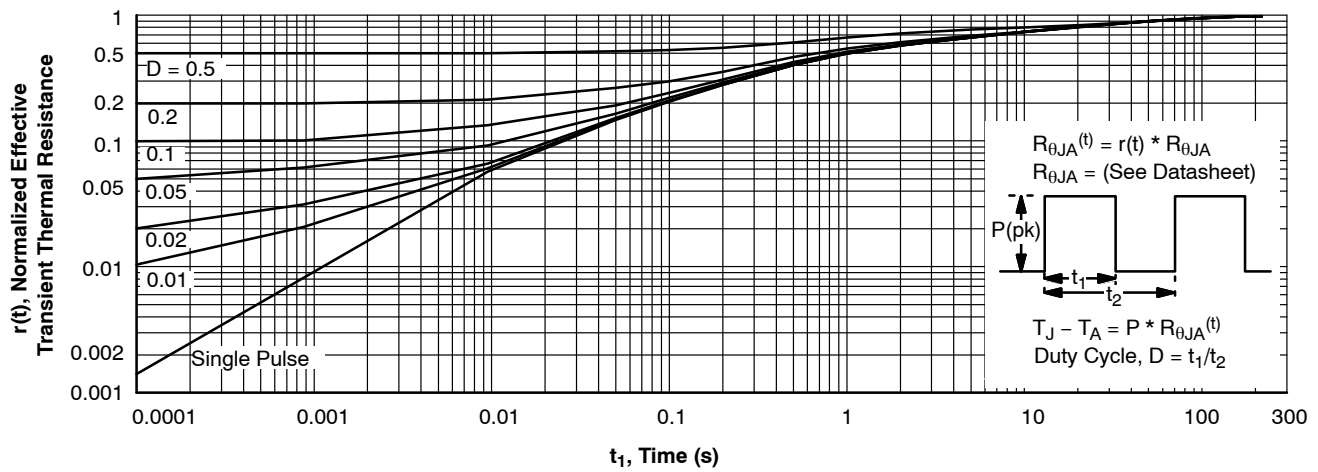


Figure 17. SOT-23, 2N7002 / NDS7002A Transient Thermal Response Curve

### ORDERING INFORMATION

Part Number	Marking	Package	Packing Method†	Min Order Qty / Immediate Pack Qty
2N7000	2N7000	TO-92 3L (Pb-Free)	Bulk	10000 / 1000
2N7000-D74Z			Ammo	2000 / 2000
2N7000-D75Z			Tape and Reel	2000 / 2000
2N7000-D26Z				2000 / 2000
2N7002	702	SOT-23 3L (Pb-Free)	Tape and Reel	3000 / 3000
NDS7002A	712			3000 / 3000

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# MECHANICAL CASE OUTLINE

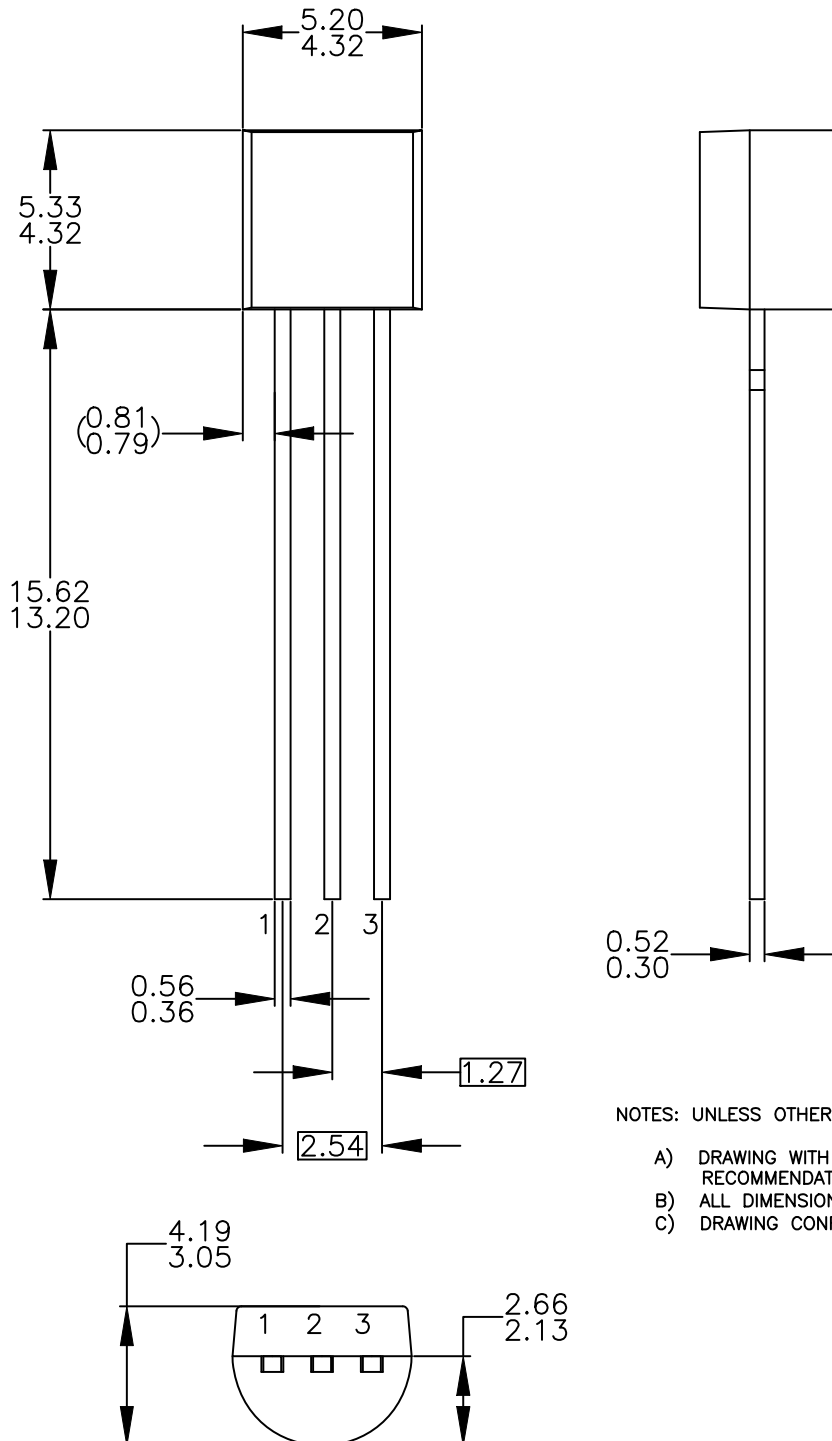
## PACKAGE DIMENSIONS

ON Semiconductor®

ON

TO-92 3 4.825x4.76  
CASE 135AN  
ISSUE O


DATE 31 JUL 2016



NOTES: UNLESS OTHERWISE SPECIFIED

- A) DRAWING WITH REFERENCE TO JEDEC TO-92 RECOMMENDATIONS.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DRAWING CONFORMS TO ASME Y14.5M-2009.

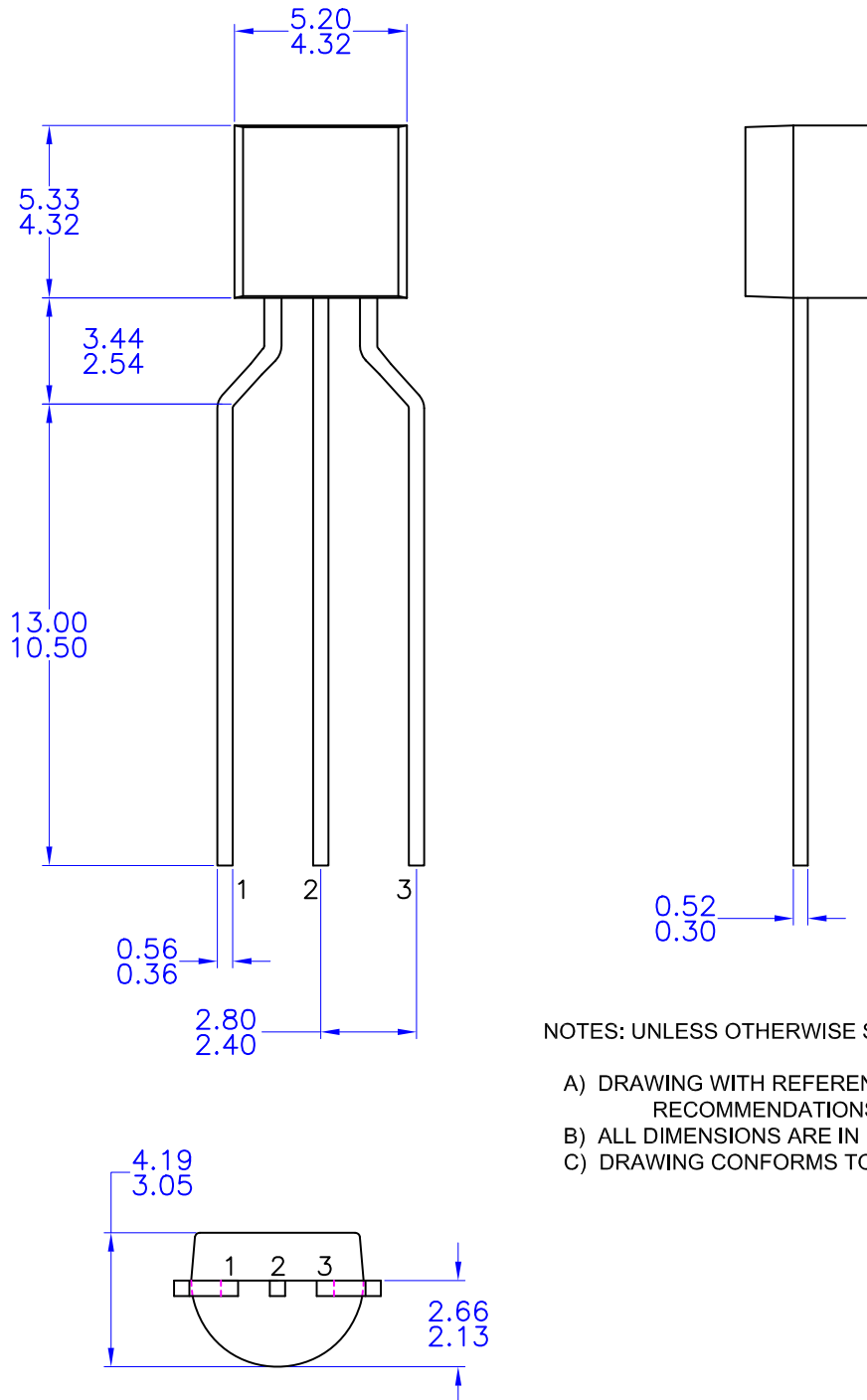
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**TO-92 3 4.83x4.76 LEADFORMED**  
**CASE 135AR**  
**ISSUE O**

DATE 30 SEP 2016



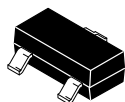
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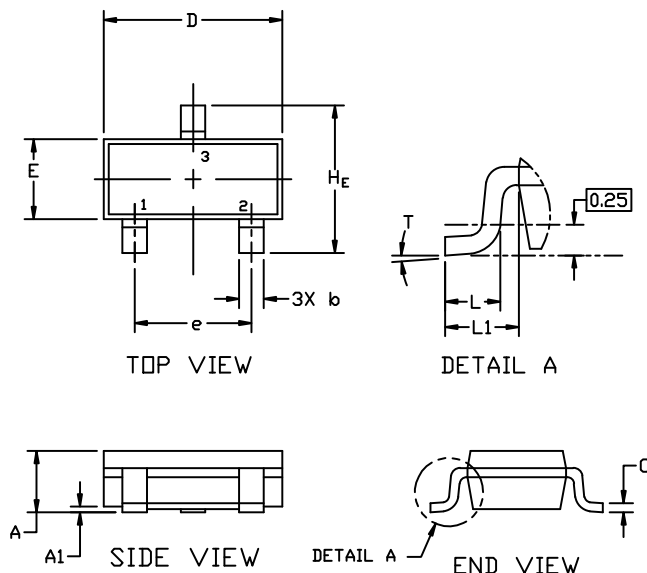
# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



SCALE 4:1

**SOT-23 (TO-236)**  
**CASE 318**  
**ISSUE AT**

DATE 01 MAR 2023

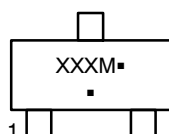


## NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M,1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF THE BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

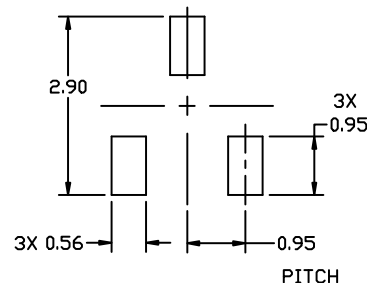
DIM	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.89	1.00	1.11	0.035	0.039	0.044
A1	0.01	0.06	0.10	0.000	0.002	0.004
b	0.37	0.44	0.50	0.015	0.017	0.020
c	0.08	0.14	0.20	0.003	0.006	0.008
D	2.80	2.90	3.04	0.110	0.114	0.120
E	1.20	1.30	1.40	0.047	0.051	0.055
e	1.78	1.90	2.04	0.070	0.075	0.080
L	0.30	0.43	0.55	0.012	0.017	0.022
L1	0.35	0.54	0.69	0.014	0.021	0.027
H <sub>E</sub>	2.10	2.40	2.64	0.083	0.094	0.104
T	0°	---	10°	0°	---	10°

## GENERIC MARKING DIAGRAM\*



XXX = Specific Device Code  
M = Date Code  
▪ = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.



## RECOMMENDED MOUNTING FOOTPRINT

\* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

## STYLES ON PAGE 2

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# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS



### SOT-23 (TO-236) CASE 318 ISSUE AT

DATE 01 MAR 2023

STYLE 1 THRU 5: CANCELLED	STYLE 6: PIN 1. BASE 2. EMITTER 3. COLLECTOR	STYLE 7: PIN 1. EMITTER 2. BASE 3. COLLECTOR	STYLE 8: PIN 1. ANODE 2. NO CONNECTION 3. CATHODE		
STYLE 9: PIN 1. ANODE 2. ANODE 3. CATHODE	STYLE 10: PIN 1. DRAIN 2. SOURCE 3. GATE	STYLE 11: PIN 1. ANODE 2. CATHODE 3. CATHODE-ANODE	STYLE 12: PIN 1. CATHODE 2. CATHODE 3. ANODE	STYLE 13: PIN 1. SOURCE 2. DRAIN 3. GATE	STYLE 14: PIN 1. CATHODE 2. GATE 3. ANODE
STYLE 15: PIN 1. GATE 2. CATHODE 3. ANODE	STYLE 16: PIN 1. ANODE 2. CATHODE 3. CATHODE	STYLE 17: PIN 1. NO CONNECTION 2. ANODE 3. CATHODE	STYLE 18: PIN 1. NO CONNECTION 2. CATHODE 3. ANODE	STYLE 19: PIN 1. CATHODE 2. ANODE 3. CATHODE-ANODE	STYLE 20: PIN 1. CATHODE 2. ANODE 3. GATE
STYLE 21: PIN 1. GATE 2. SOURCE 3. DRAIN	STYLE 22: PIN 1. RETURN 2. OUTPUT 3. INPUT	STYLE 23: PIN 1. ANODE 2. ANODE 3. CATHODE	STYLE 24: PIN 1. GATE 2. DRAIN 3. SOURCE	STYLE 25: PIN 1. ANODE 2. CATHODE 3. GATE	STYLE 26: PIN 1. CATHODE 2. ANODE 3. NO CONNECTION
STYLE 27: PIN 1. CATHODE 2. CATHODE 3. CATHODE	STYLE 28: PIN 1. ANODE 2. ANODE 3. ANODE				

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