Process for the course:

1. Read Course PM (as soon as possible)
2. Fill in self-estimation to be assigned to a group.
3. Perform labs (starts 2/11).
4. Download the software from Xilinx Vivado ML Standard.
   (NOTE 123GB harddisk required for installation and 71GB will be used,
   2019.2, are used in the lab)
   and/or Download Modelsim (4.5 GB)
5. Check RS-online: https://se.rs-online.com/web/
6. Choose a project (by 9/11)
7. Create a block diagram (Begin by 9/11, done 15/11).
8. Select components and order (Begin by 9/11, done 15/11).
9. Read data sheet , https://se.rs-online.com/web/ (Always during the course)
10. Test the circuits with logic analyzer / signal generator
11. Begin design and testing. (No later than 15/11)
12. Start the documentation. (By 24/11)
13. Read data sheet (Always during the course)
14. Book time for the exam. (earliest 12/12)
15. Complete the documentation and align it with the checklist.
    (Completed 2 days before the exam)
16. Create presentation material (slides) and prepare for your presentation.

Digital project laboratory, Project

Digital Project Laboratory, EDA234

Examiner

Arne Linde, tel 772 1683,
Rom: 4464
e-mail:arne@chalmers.se

Supervisor

Sven Knutsson, tel 772 5727
e-mail: sven.knutsson@chalmers.se

TA

Erik van Bennekum bennekum@chalmers.se

Course purpose:

- Give practical knowledge about digital integrated devices.
  - Learn to work whit hierarchical design.
  - Learn to deal whit limited recourses
- Go from a specification to a fully operating prototype.
- Training in presenting results in a written report and an oral presentation.

The project:

- Choose one in a list of suggested or propose one of your own.

Learning outcomes

- Understand the principles for a structured and **hierarchical description** of smaller digital systems [P, R].
- Understand the function, use and limitations of the **programmable logic circuits** [L, R, P].
- Understand the **function, use and limitations** of modern design **tools for electronic design** (EDA) [L, R, P].
- Know the requirements for power supply for digital circuits in environments with **multiple voltages** [R, P].
- Know how to **search for documentation** of commercial electronic components [R, B].

Skills and abilities

Based on a **vague requests**, develop a technical specification for a small digital system [R, P].

Realize a small digital system in programmable logic and other components in a structured manner using modern CAD tools [L, R, P].

Understand and use relevant parts of the **documentation** of existing **electronic components**, to be able to **interconnect them** [R].

Perform **engineering tradeoffs** and **debugging the design**.

Complete and document a prototype of a smaller digital system [P, R].

Produce technical documentation of their design so that it is understandable and useful for people at different levels in a company [R].

Debugging the design, using computer-based simulators and measuring instruments as logic analyzers and oscilloscope [W, B]

Complete and **document** a prototype of a smaller digital system [P, R].

Produce technical documentation of their design so that it is understandable and useful for people at different levels in a company [R].

Oral presentation of work in an engineering and professional manner [O].

Working in a **project form**, and continuously document the progress of the project [W,B].

VHDL - is important in the course.
So, choose a simple project concerning VHDL!
If the VHDL knowledge is low in the group!

Repet VHDL, se **Prerequisites EDA322** in Canvas
(extra importen Part 6 Testbenches)
Next lecture is a crash-course in VHDL)

the example is sufficient for grade three

Monday 31/10 13:15 EL43	Lecture 1: Introduction
Tuesday 1/11 10:00 EL43	Lecture 2: Programmable logic and VHDL. Crash-course in VHDL
Wednesday 2/11 10:00, 13:15 ED4220	Laboration 1: Introduction to the development tools
Thursday 3/11 10:00 EL43	Lecture 3: Report writing, etc. Frist hour: report and timing Second hour: more VHDL
Thursday 3/11 10:00 and 13:15 Project rooms ED4209-15	Laboration 1 and 2
Friday 4/11 08:00 Project rooms ED4209-15	Laboration 2 :Measuring equipment and troubleshooting

Install Modelsim on your Computer and if possible, install Vivado.

Three labs:1: Intro Vivado,
submission of a second counter
+ requirements for resource utilization.
2: Measurement technology with USB logic analyzer
- submission short report / reflection.

Both are performed in pairs or individually.
3: Design of a controller for an LCD, submission in groups.

Then some working code every week. (decided the week before)

Week 3 - 9

Logic design, building, testing, modifying and documenting. Room: Course laboratories

Supervisors give supervision in the Course lab (Zoom)
(from reading week (Lv) 2):

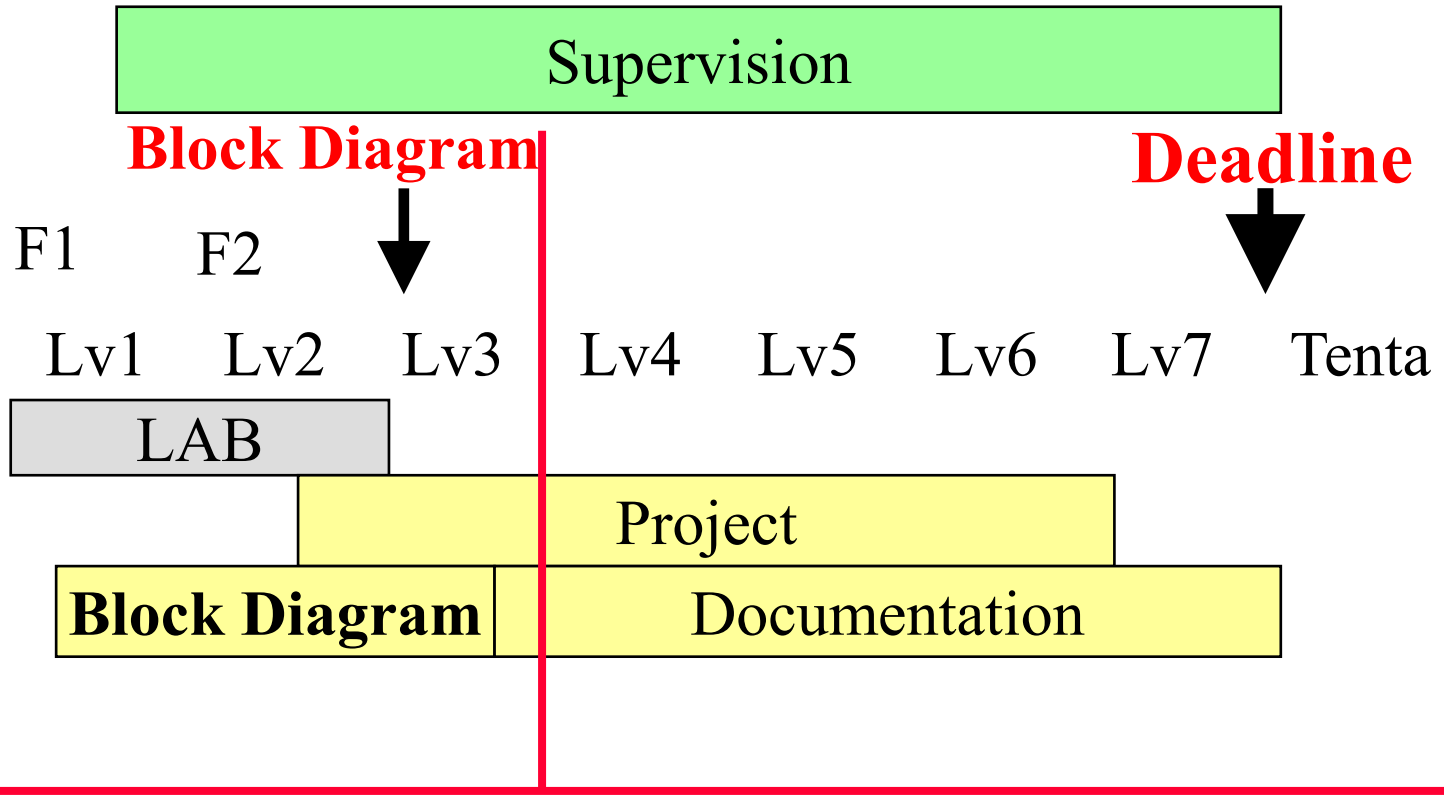
Use us when you runs into trouble!

(respect the timeslots fore supervision)

Monday13.15, Wednesday 10.00 and Friday 10.00 (my office 4464)

(Week 2 Monday15.15, Thursday 9.00 and Friday 10.00, not 29/11)

Other times after agreement. The Supervisor allocate space in the lab and the student must sign out keys and tools, measuring equipment and so on.



Friday, RV 3, the block diagram must be approved!
So that you can continue with the course.

Project *demands*:

- Size at least 22 points.
- Control unit – Data path

Some project can be allowed to use a microprocessor if the group gets permission from the Examiner.

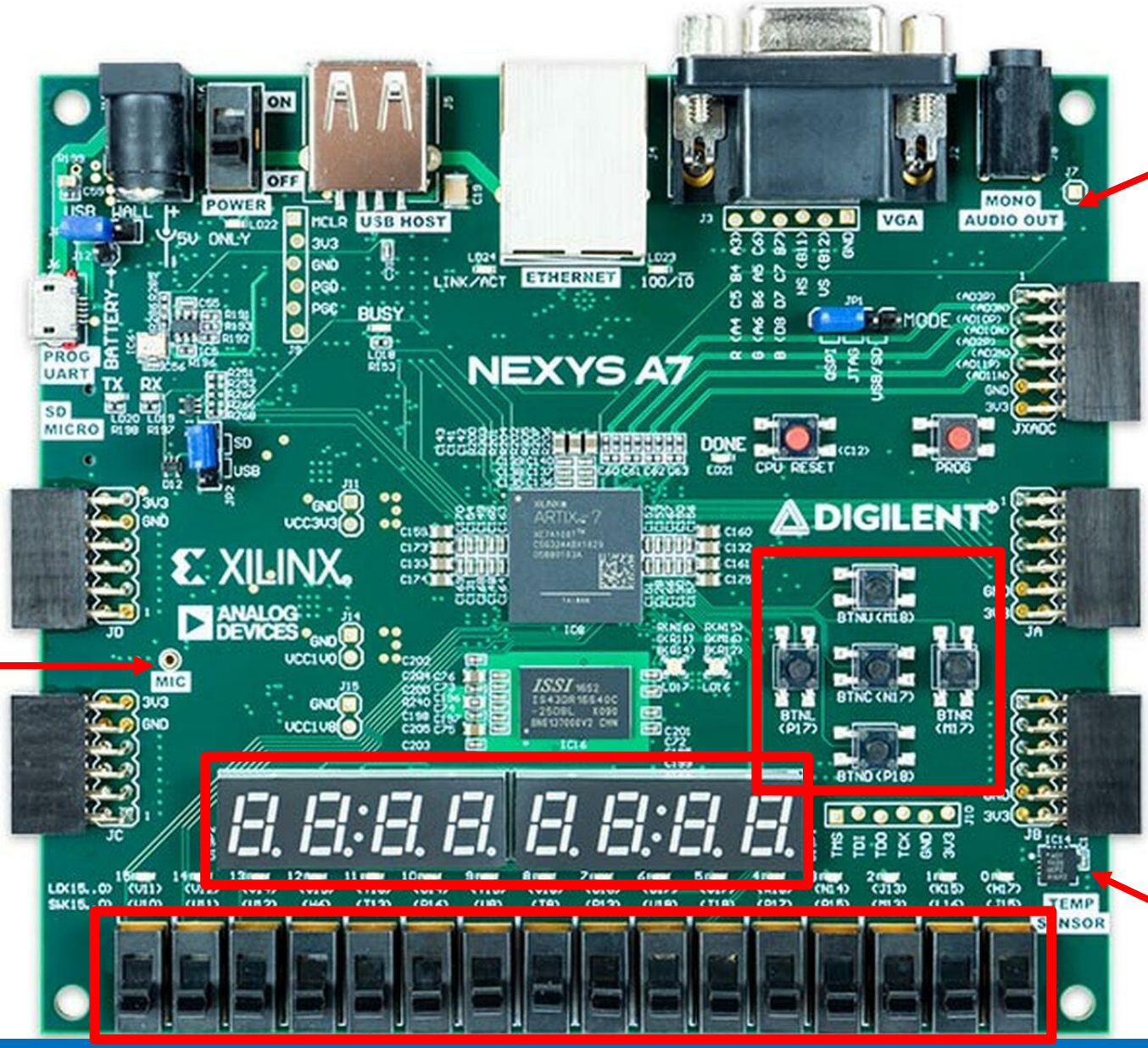
The group has presented a block diagram of its design to the Supervisor. This must be done 1x of November.

	development board	Pmod	Extern
LCD	-	9	12
Real-time clock	3	6	9
7-seg	3	3	3
RS-232, ½-way	6/9	6/9	6/9
Temp	6	6	9
Accelerometer	6	6	9
Radio 433, ½-way	-	6/12	6/12
IR, ½-way	-	6/9	9/12
A/D	9	9	12
Minne			
Ram	3	6	9
SDRAM	12	12	15
SD-kort	12		
sound / speech	3/9	-	3/15
BT	-	9	12
Keybord 4x4	-	6	6
Ultrasound		3	6

Demonstration of working Function 2/3 point (weekly task)

Working in final design Full point.

(only one score per function, not full score for multiple use of same interface)


Audio out
Mic
Temp sensor
NEXYS A7
DIGILENT
XILINX
ANALOG DEVICES
MIC
MONO AUDIO OUT
VGA
ETHERNET
USB HOST
POWER
PROG UART
SD MICRO
CPU RESET
PROG
BTNU (M18)
BTNC (N17)
BTNL (P17)
BTNR (M17)
BTND (P18)
TEMP SENSOR

Group size : 3 to 4 students *(maybe 5).*

Exam

- **written report** (10 - 20 pages)
  (included a part: who done what.)
- oral presentation – *about half an hour, all group members should participate, presentation should be directed to the thought of person that has requested the project*
- Exam questions
- demonstration
- meetings with supervisor once a week

– *student is not allowed to miss more than two meetings (Starting reading week 2)*

– Weekly VHDL hand ins

Self estimation Quiz

Estimation of own knowledge (1 low / non-existent, 5 excellent)
This is a form to estimate your ability.
I use this to form to group students with the same ambition.
There is a possibility to register in pairs.

Question 1 — 1 pts

Programming (Java, C, C++, C# or similar) [Select]

VHDL (Construction and simulation) [Select]

Analogue electronics (transistors, amplifiers etc.) [Select]

Measurements (Oscilloscope, Labview etc.) [Select]

Build your own electronics, repair electronic equipment [Select]

Grade:

* Project (3-5).

Group

• Report 1-5p (if approved)

* Prototype 1-5p

* **Project management 1-10p** *(weekly meeting + hand in)*

Group – grade (Summa 3-20p)

Project	3-9p	10-12p	13-14p	15-17p	18-20
3	U	U	3	3	4
4	U	3	3	4	5
5	U	3	4	5	5

Student Grade:

Project (3-5) from previous.

Student

Attend project meeting 1-3p (from week 3)
Oral presentation 1-3p
Project diary 1-3p
Personal report 1-3p (one page)

Group – grade (Summa 4-12p)

Group grade	<6p	6-7p	8-9p	10-11p	12
3	U	U	3	3	4
4	U	3	3	4	5
5	U	3	4	5	5

The report.

effective technical documentation

- Contents
- Abstract
- Report structured according the top-down-principles.
- Introduction and system specification.
- Overall system description
  in a well-structured diagram of functional blocks
- Divide those blocks into sub blocks and so on.
- Draw state-machines or ASM-diagrams when necessary for understanding.
- Draw time-diagrams for time critical signals.

In Appendix submit complete:

Circuit schematics, component list, layout of circuit boards, program code *(not from synthesize)* , list of all signals and so on.

Checklist for report approval

(It is not certain that you will be approved even if everything on this list is fulfilled, but if something is missing from the list, the report will be returned automatically.)

Summary

Table of Contents

System specification

Briefly describe what the system can do.

Overview with block diagram

The block diagram must have the appropriate complexity.

The text should support the understanding of the block diagram.

This section should give the reader a good overview of your design.

Description of the sub-blocks

Easy to understand and clear.

Describe the FPGA circuit (s) in general.
(If this is not done in the overview)

Design methodology:

Work according to top-down principles.

Start with system specification.

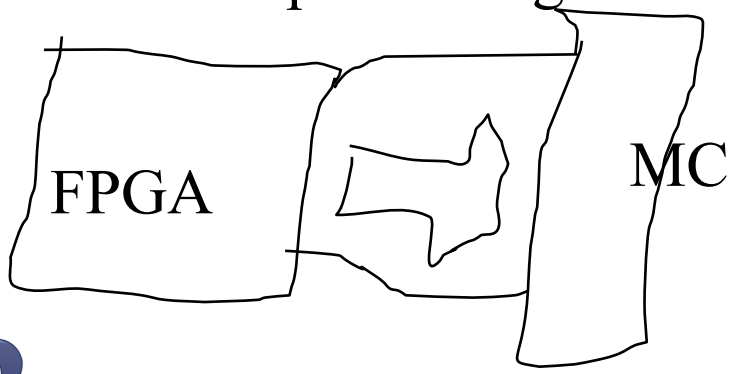
Divide the project in control unit and data path.

Divide those block in sub functions.

Write the Documentations continuesly.

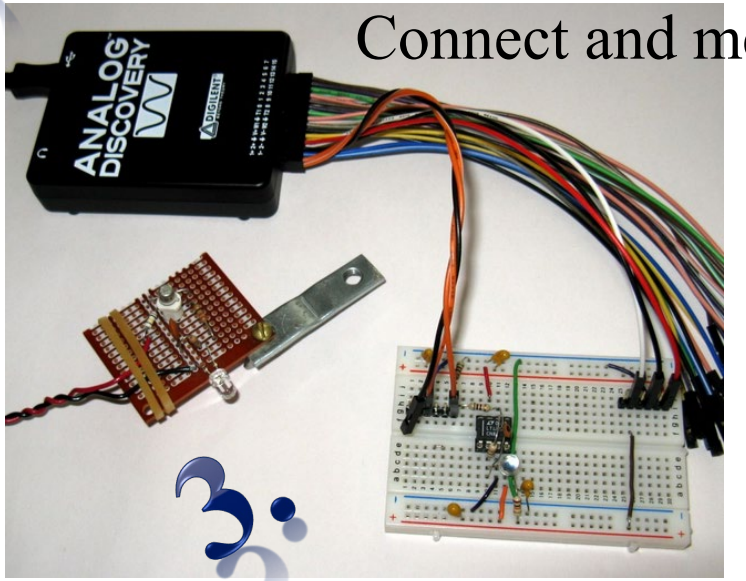
Procedure

1. Sketch up the design



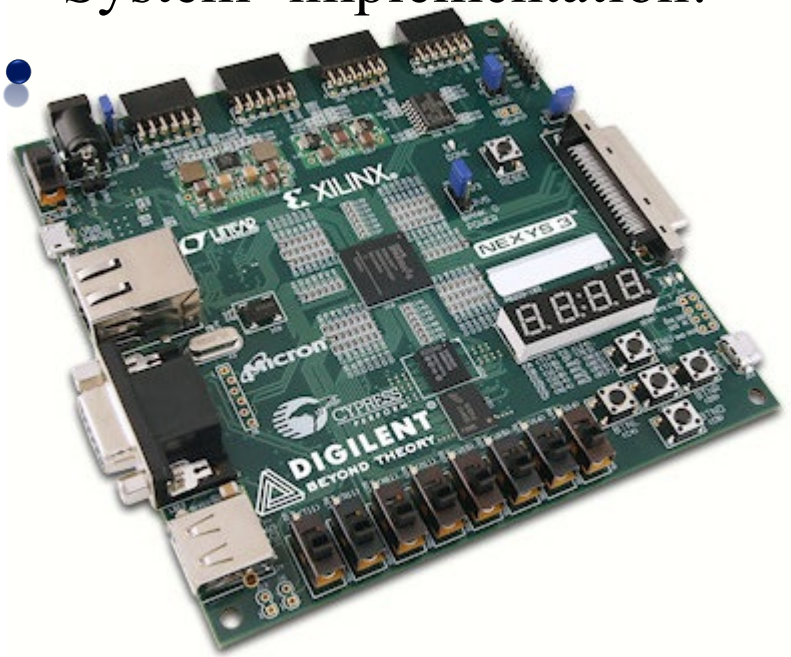
2. Read data sheet and **order**

3. Connect and measure!



What did I miss in the datasheet?

4. System- implementation!



Components:

Components that in the component list *may* be in stock. Other components, discuss with the supervisor first.

https://se.rs-online.com/

(http://se.farnell.com/)

Deadline

A design block diagram must be shown before Wednesday 9 of November. *(Approved before 15 of November)*
Realization of the design must be finished before Friday 16 of December.

Entrance cards, responsibility and security

You have access to the lab with entrance cards.

(Thursday if answered the questionnaire)

Group members are responsible fore the tools used by the group.

Turn off power whenever you leave the lab.

No work are permitted on parts **with net power** (240 V).

Repair of tools and instruments are **not allowed**.

Equipment that not work should be delivered to me as quickly as possibly.

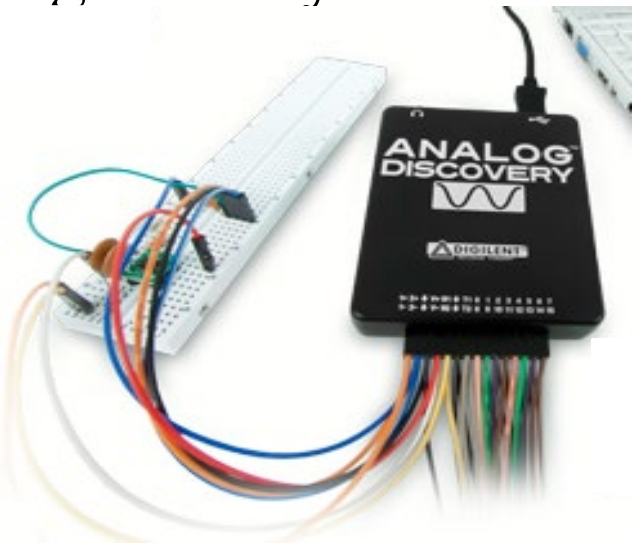
Usual problems

Lack of time: *(Each student should spend 140h)*

Late project start. *(not possibly during week 8)*

Too short time for building and debugging.

Start using the Logic Analyzer to late!



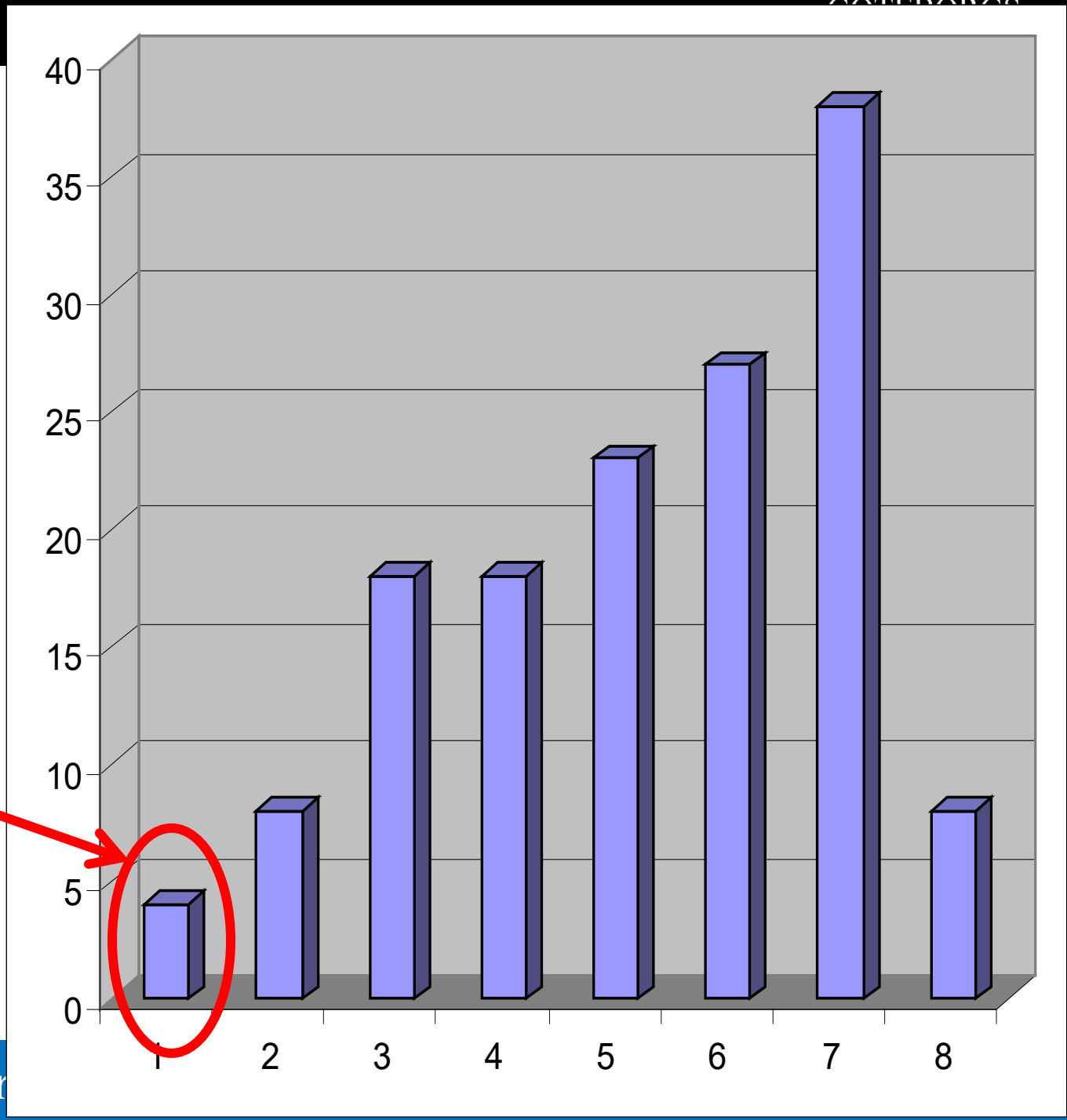
Electrical problems:

Decoupling, power distribution, wrong load, shortcut

Complexity

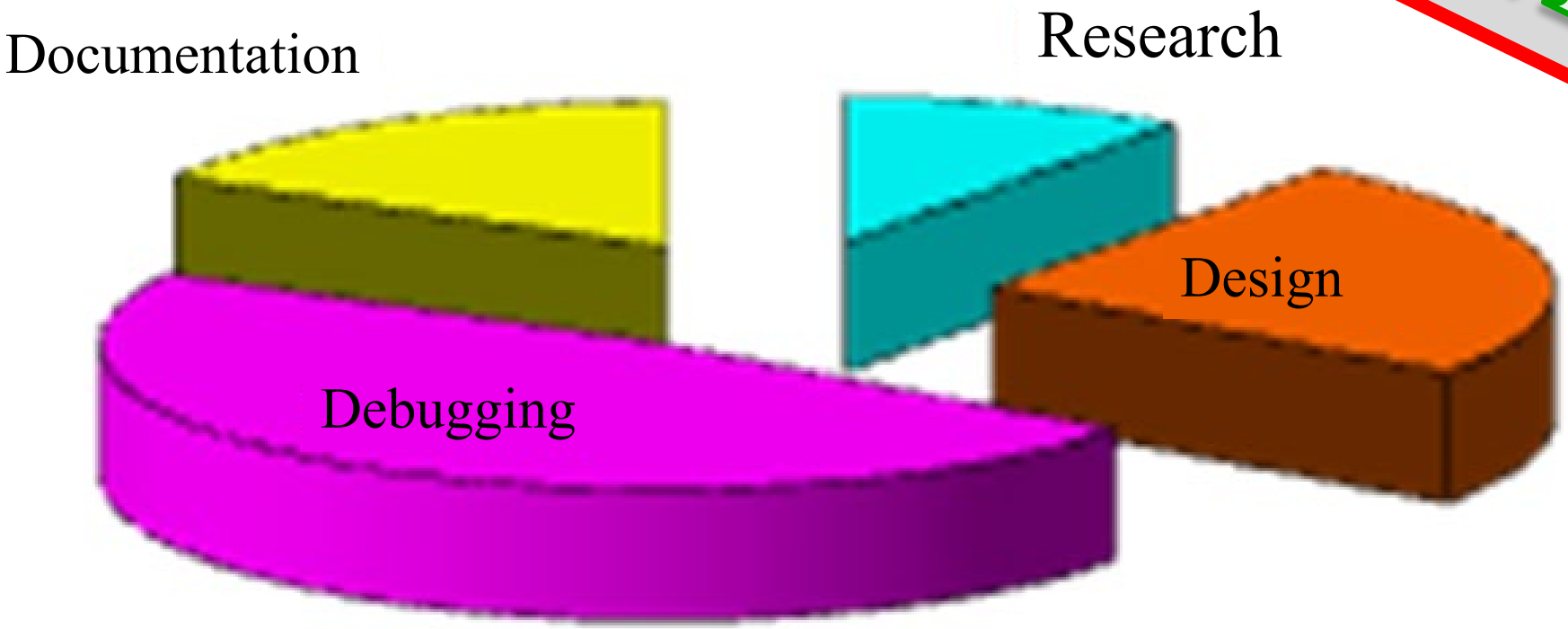
Average working hours per person per week, example.

Expected:
4 h Lecture
4 h Labb
12 h Own work



Time Consumption

RDFM



Problems in the group.

Members don't work towards the same goal.

Members don't do what they are supposed to do.

Week meeting
Exam questions

Problems with report

None or bad overview

Too many details! But no structure.

Try to make a design and realization, that is easy to explain.

Poor design strikes back three times

Difficult to design

Impossible to debug → huge time consumption on troubleshooting

Impossible to describe → bad report.

Project suggestion :

	Difficulty (5-3)
RANGE-FINDER	3
Digital Spirit Level	3
Laser-doom vest with weapon	3 to 4+
Project time meter	3 to 4
Motion detector	3 to -4

for unauthorized persons

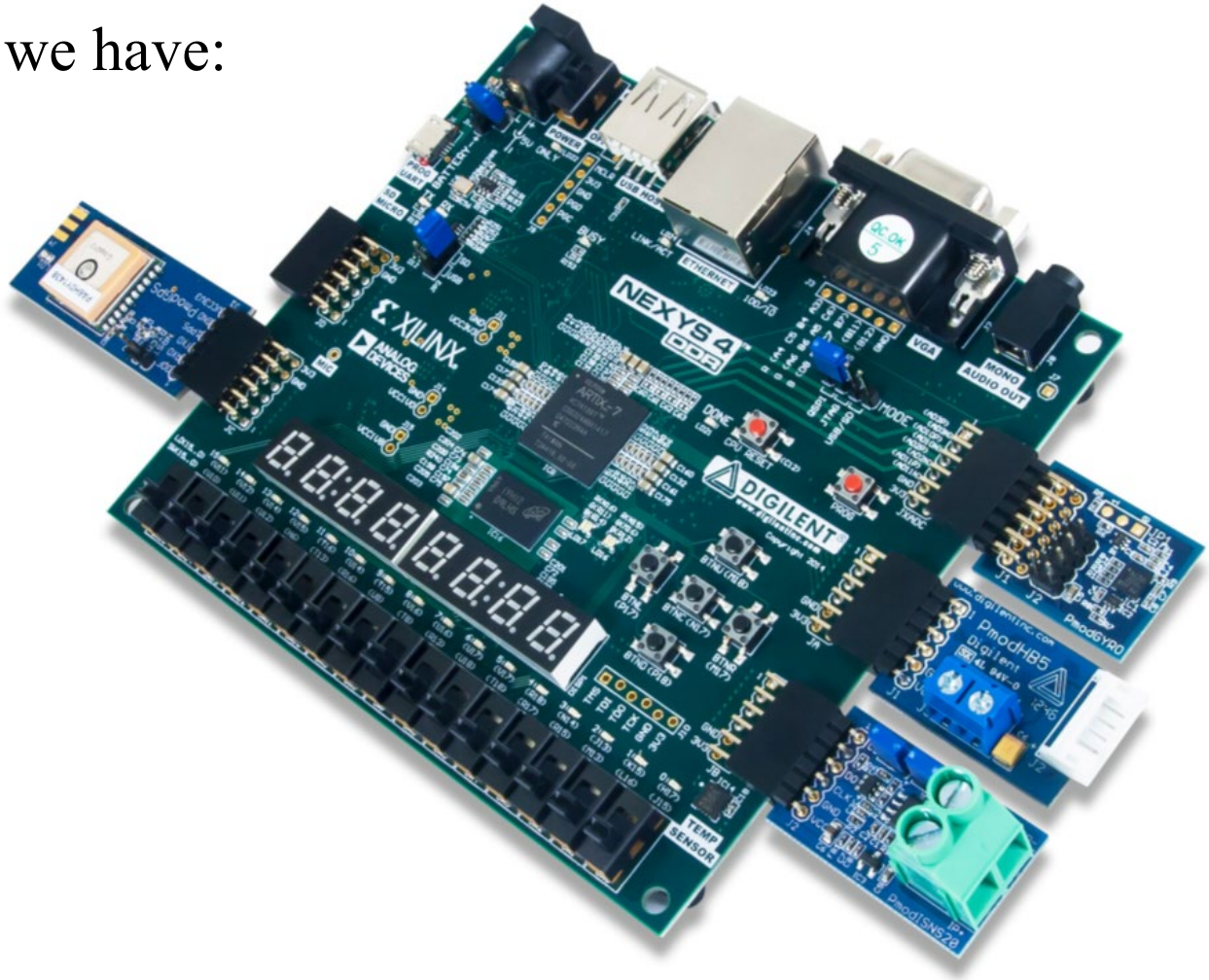
Talking clock	4
Alarm clock	4
Termometer	4

In Points 3 → 25p, 4 → 40p and 5 → 55p
(require some external component)

	development board	Pmod	Ext
LCD	-	9	12
Real-time clock	3	6	9
7-seg	3	3	3
RS-232, ½-way	6/9	6/9	6/9
Temp	6	6	9
Accelerometer	6	6	9
Radio 433, ½-way	-	6/12	6/12
IR, ½-way	-	6/9	9/12
A/D	9	9	12
Minne			
Ram	3	6	9
SDRAM	12	12	15
SD-kort	12		
sound / speech	3/9	-	3/15
BT	-	9	12
Keybord 4x4	-	6	6
Ultrasound		3	6

FPGA projects:
We have NEXSYS 4.
For Basys 3 systems we have:

Accelerometer / Gyro
A/D – D/A Converters
Mic/ Speaker
Bluetooth Moduler
RC-Servo driver
H-Bridge
Joystick
Radio 433MHz
SD-Card
Thermometer
Calendar
WiFi



What happens next?

- Choose a project *(look in the list or invent on your own)*

Its a good idea to use the FPGA-cards functions at the first iteration!

- Start with the labs.
- Book time for weekly meetings, with the supervisor.
- Course evaluation.

Course representatives for EDA234

TIDAL	oscar.ingagarden@hotmail.com	Oscar Larsson
TKELT	felixle@student.chalmers.se	Felix Lehmann
MPCSN	yanfengl@student.chalmers.se	Yanfeng Li
MPEES	jmunozbautista@gmail.com	Jorge Munoz Bautista

Block diagram

Project description
Speaking thermometer.
Design and implement a device that tell you the temperature outdoors and indoor when the corresponding button are press.

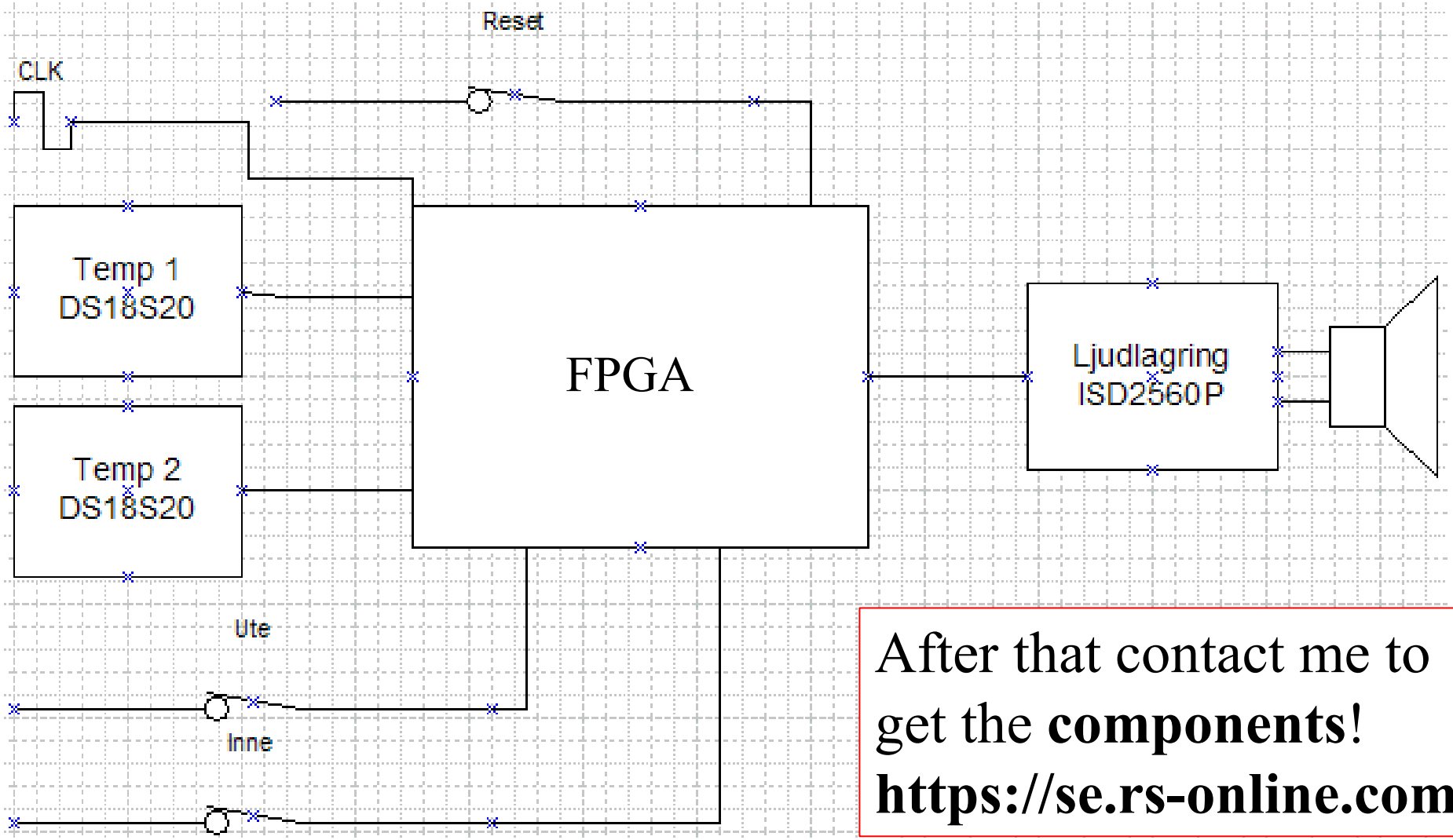
The temperature are told by speech.
For reading of temperature use: **DS18S20**.

What components do we need?

Obvious a DS18S20 and a FPGA.

Telefon- och ljudkretsar			
MT 8870	DTMF-mottagare	9*17	73-036-21
MT 8880	DTMF-mottagare/sändare	9*18	73-036-88
ISD2560P	60 sekunders ljudlagring	9*26	73-106-00

Firs try - This Week



After that contact me to get the **components**!
https://se.rs-online.com

Data sheets

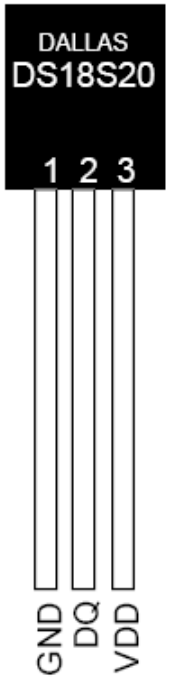
PRELIMINARY

DS18S20
High Precision
1-Wire® Digital Thermometer

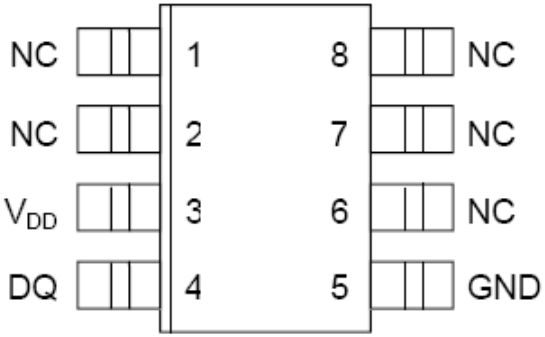
PIN DESCRIPTION

GND - Ground
DQ - Data In/Out
V_{DD} - Power Supply Voltage
NC - No Connect

PIN ASSIGNMENT

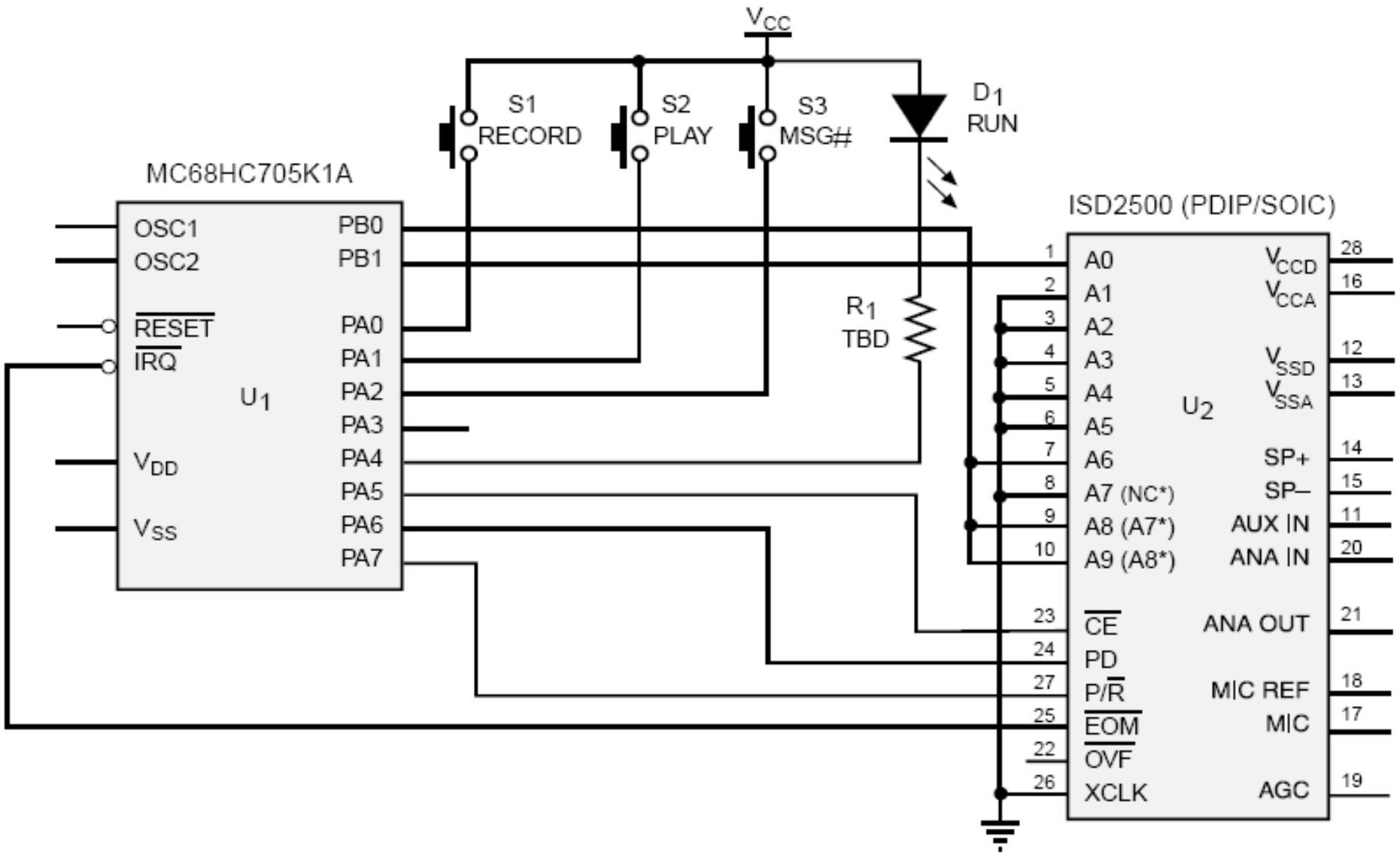


DS18S20 To-92 Package

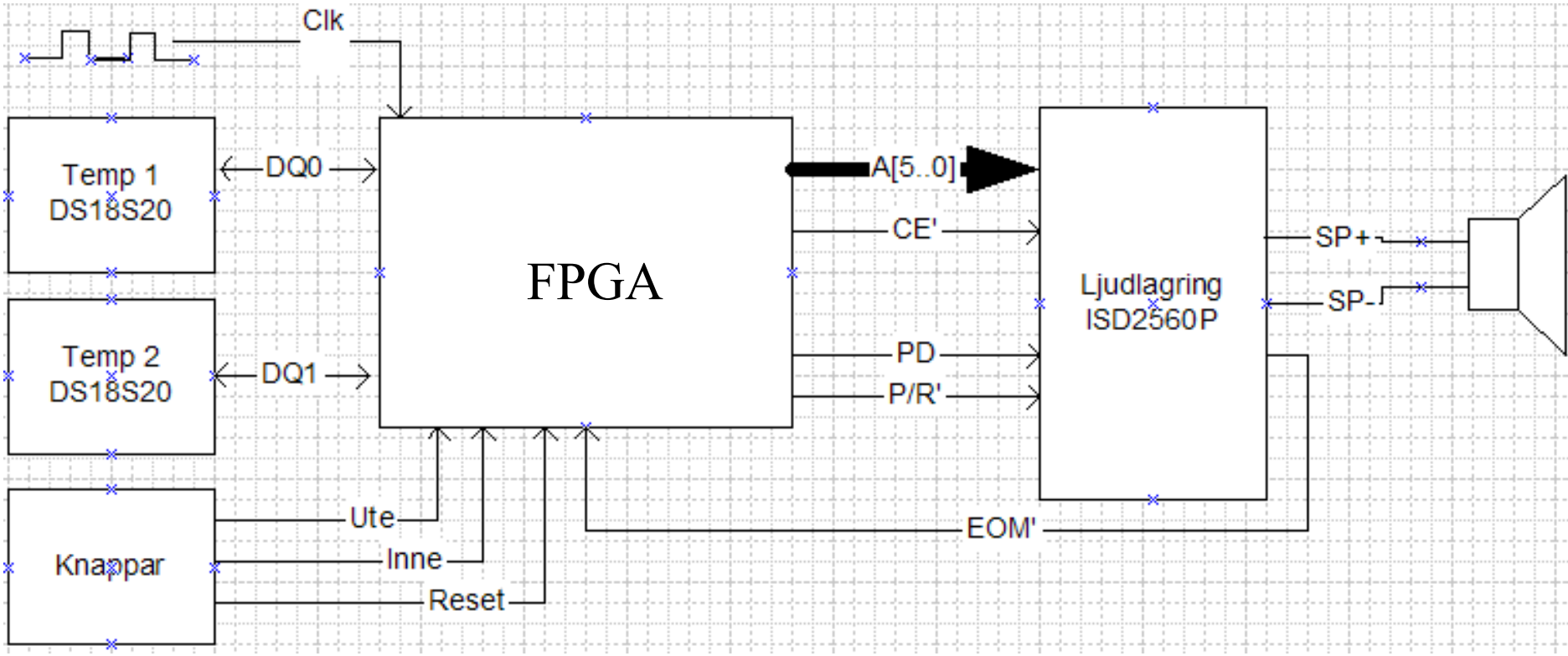


DS18S20Z
8-Pin SOIC (150 mil)

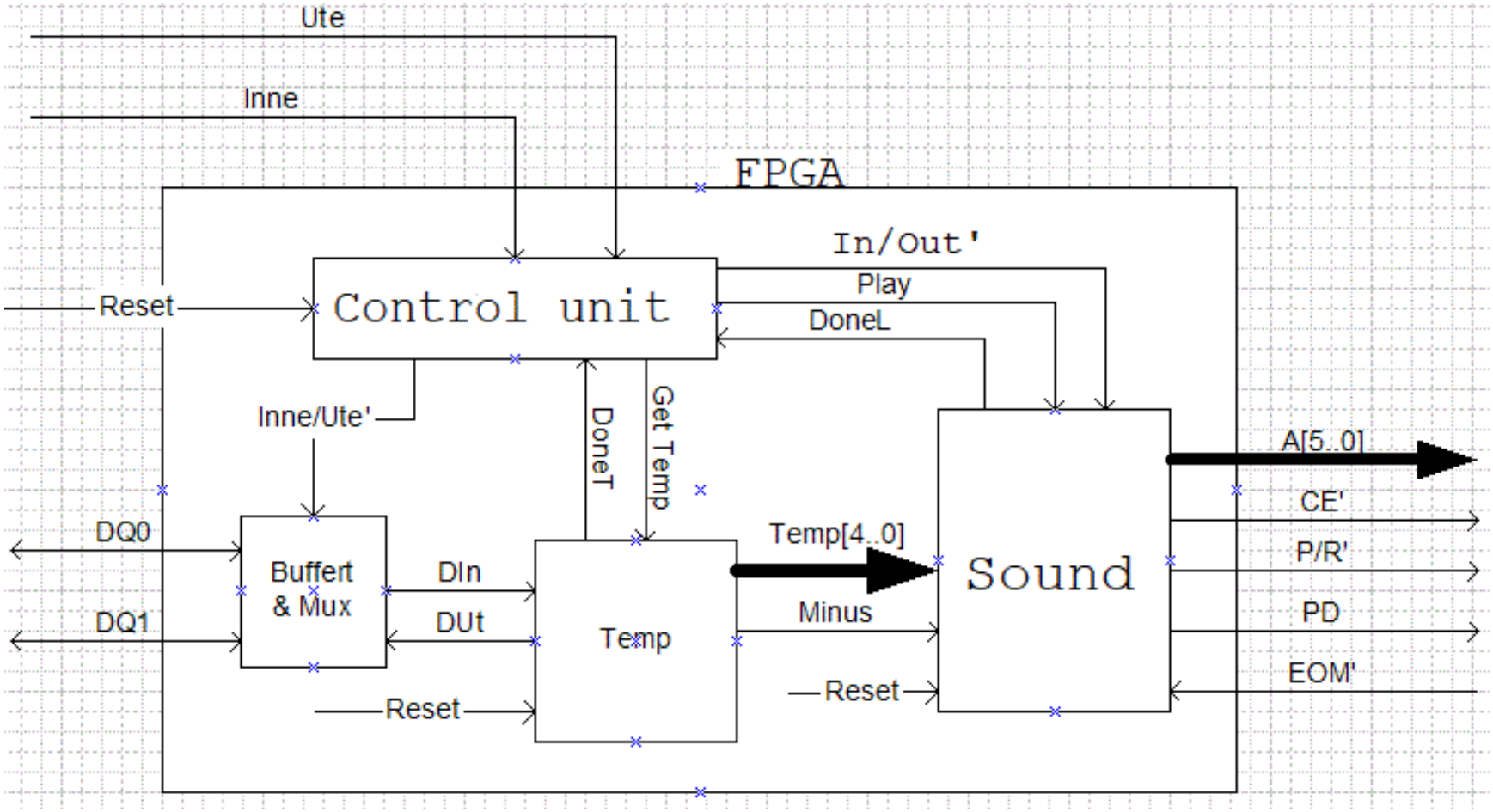
ISD2500 APPLICATION EXAMPLE –MICROCONTROLLER/ISD2500 INTERFACE



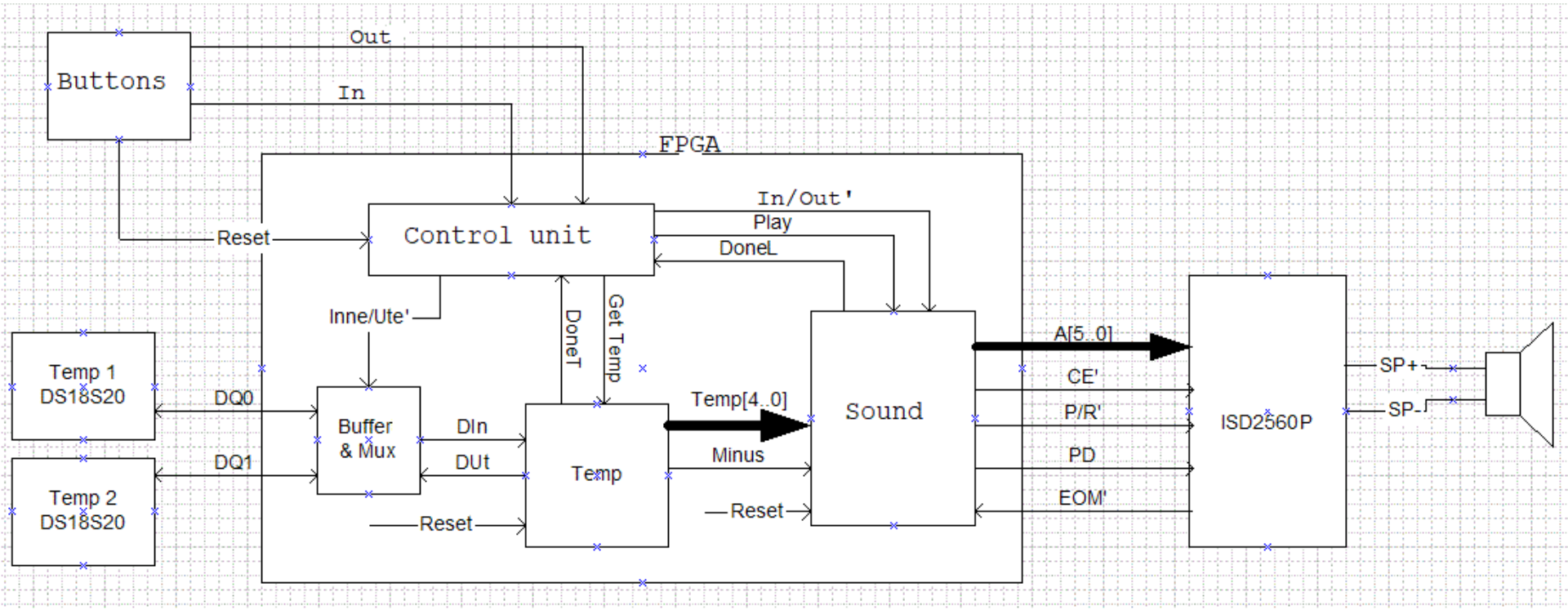
Block diagram – second try.



Block diagram – third try. (FPGA)



Final


Buttons
Out
In
FPGA
Reset
Control unit
In/Out'
Play
DoneL
Inne/Ute'
DoneT
Get Temp
Temp 1
DS18S20
Temp 2
DS18S20
DQ0
DQ1
Buffer
& Mux
DIn
DUt
Reset
Temp
Temp[4..0]
Minus
Reset
Sound
A[5..0]
CE'
P/R'
PD
EOM'
ISD2560P
SP+
SP-

Summary

- Submit your self evaluation – NOW (in Canvas)!
  if you have not done it!
- Look at the LabPM. - Simple lab? *(will be an update)*
- Look at the project proposals, select project.
- **Gather the project group.**
- **Repeat VHDL**
- Book tutorials.

- Lab Wednesday 10-12.

(Project room at the end of the week)