21EES101T-ELECTRICAL AND ELECTRONICSENGINEERING

EEE-UNIT 2

Unit-2-Electronics

Overview of Semiconductors, Diodes and Transistors, Introduction to JFET and MOSFET. Construction and working of power devices-SCR, BJT, MOSFET, IGBT -Switching Characteristics of SCR- Types of power converters- Natural and force commutation, Linear voltage Regulator, SMPS

Realize the logic expression using basic logic gates, Combinational logic design-Sum of Product form (SOP) and Product of Sum (POS) form, Minterm and Maxterm, Karnaugh Map (K-Map) representation of logical functions, Two variables K-Map, Three variables K-Map, Four variables K-Map. Introduction to FPGA.

Practice on realization of logical expression, combinational circuits, PCB design, soldering and testing

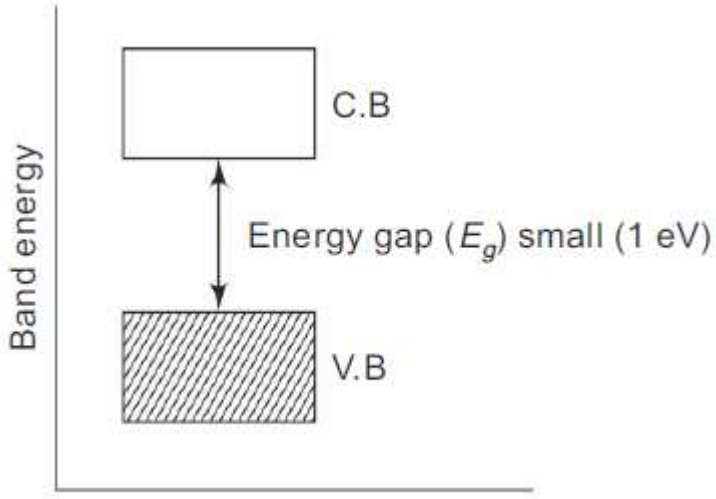
OVERVIEW OF SEMICONDUCTORS

- Depending on their conductivity, materials can be classified into three types as
- conductors,
- semiconductors and
- insulators.

Conductor is a good conductor of electricity. Insulator is a poor conductor of electricity. Semiconductor has its conductivity lying between these two extremes.

Energy Band of Semiconductor

In terms of energy band shown in Fig., the valence band is almost filled (partially filled) and conduction band is almost empty.



A comparatively smaller electric field (smaller than required for insulator) is required to push the electrons from the valence band to conduction band. At low temperatures, the valence band is completely filled and the conduction band is completely empty. Therefore a semiconductor virtually behaves as an insulator at low temperature. However even at room temperature some electrons crossover to the conduction band giving conductivity to the semiconductor. As temperature increases, the number of electrons crossing over to the conduction band increases and hence electrical conductivity increases. Hence a semiconductor has negative temperature coefficient of resistance.

Classifications of Semiconductors

Intrinsic Semiconductor: A pure semiconductor is called intrinsic semiconductor.

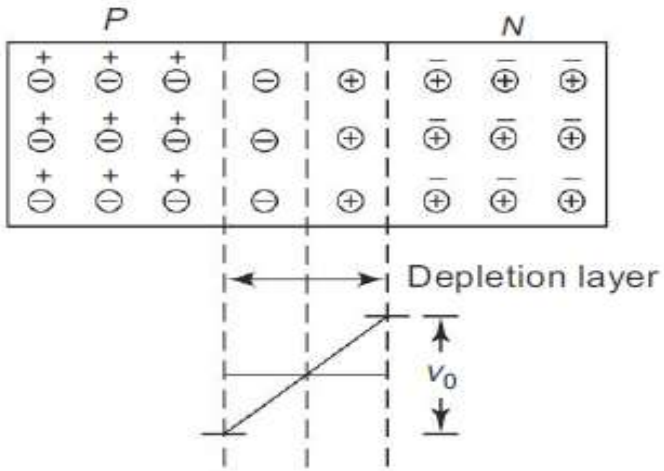
Extrinsic Semiconductor: Due to the poor conduction at room temperature, the intrinsic semiconductor, as such, is not useful in the electronic devices. Hence the current conduction capability of the intrinsic semiconductor should be increased. This can be achieved by adding a small amount of impurity to the intrinsic semiconductor, so that it becomes impurity semiconductor or extrinsic semiconductor. This process of adding impurity is known as **doping**.

N-type Semiconductor: A small amount of **pentavalent** impurities such as arsenic, antimony or phosphorus is added to the pure semiconductor (germanium or silicon crystal) to get N-type semiconductor. Thus, the addition of pentavalent impurity increases the number of electrons in the conduction band thereby increasing the conductivity of N-type semiconductor. As a result of doping, the number of free electrons far exceeds the number of holes in an N-type semiconductor. So electrons are called majority carriers and holes are called minority carriers

P-type Semiconductor: A small amount of trivalent impurities such as aluminum, Gallium or boron is added to the pure semiconductor to get the P-type semiconductor. The number of holes is very much greater than the number of free electrons in a P-type material, holes are termed as majority carriers and electrons as minority carriers.

THEORY OF PN JUNCTION DIODE

In a piece of semiconductor material, if one half is doped by P-type impurity and the other half is doped by N-type impurity, a PN junction is formed. The plane dividing the two halves or zones is called PN junction. As shown in Fig., the N-type material has high concentration of free electrons while P-type material has high concentration of holes. Therefore at the junction there is a tendency for the free electrons to diffuse over to the P-side and holes to the N-side. This process is called diffusion.



Formation of PN Junction

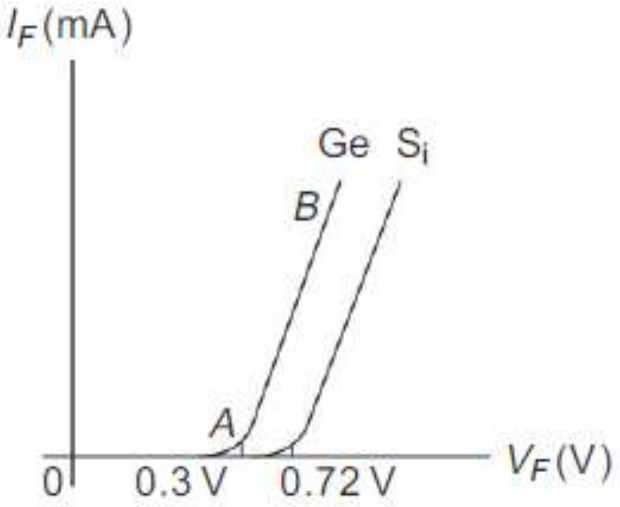
As the free electrons move across the junction from N-type to P-type, the donor ions become positively charged. Hence a positive charge is built. on the N-side of the junction. The free electrons that cross the junction uncover the negative acceptor ions by filling in the holes. Therefore a net negative charge is established on the P-side of the junction. This net negative charge on the P-side prevents further diffusion of electrons into the P-side. Similarly, the net positive charge on the N-side repels the holes crossing from P-side to N-side. Thus a barrier is set up near the junction which prevents further movement of charge carriers, i.e. electrons and holes. This is called potential barrier or junction barrier V_0. V_0 is 0.3 V for germanium and 0.72 V for silicon. The electrostatic field across the junction caused by the positively charged N-type region tends to drive the holes away from the junction and negatively charged P-type region tends to drive the electrons away from the junction. Thus the junction region is depleted to mobile charge carriers. Hence it is called **depletion layer.**

Under Forward Bias Condition

When positive terminal of the battery is connected to the P-type and negative terminal to the N-type of the PN junction diode, the bias applied is known as forward bias. Under the forward bias condition, the applied positive potential repels the holes in P-type region so that the holes move towards the junction and the applied negative potential repels the electrons in the N-type region and the electrons move towards the junction. Eventually when the applied potential is more than the internal barrier potential, the depletion region and internal potential barrier disappear.

V–I Characteristics of a Diode under Forward Bias

For $V_F > V_0$, the potential barrier at the junction completely disappears and hence, the holes cross the junction from P-type to N-type and the electrons cross the junction in the opposite direction, resulting in relatively large current flow in the external circuit.

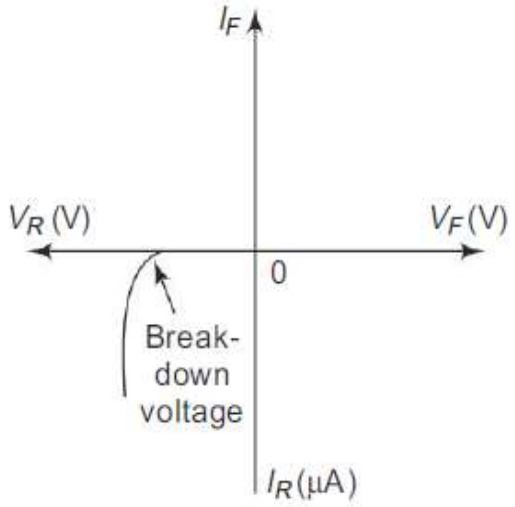


Under Reverse Bias Condition

When the negative terminal of the battery is connected to the P-type and positive terminal of the battery is connected to the N-type of the PN junction, the bias applied is known as reverse bias. Under applied reverse bias, holes which form the majority carriers of the P-side move towards the negative terminal of the battery and electrons which form the majority carrier of the N-side are attracted towards the positive terminal of the battery. Hence the width of the depletion region which is depleted of mobile charge carriers increases. Thus the electric field produced by applied reverse bias, is in the same direction as the electric field of the potential barrier. Hence, the resultant potential barrier is increased, which prevents the flow of majority carriers in both directions. Therefore, theoretically no current should flow in the external circuit. But in practice, a very small current of the order of a few microamperes flows under reverse bias.

V–I Characteristics of a Diode under Reverse Bias

For large applied reverse bias, the free electrons from the N-type moving towards the positive terminal of the battery acquire sufficient energy to move with high velocity to dislodge valence electrons from semiconductor atoms in the crystal. These newly liberated electrons, in turn, acquire sufficient energy to dislodge other parent electrons. Thus, a large number of free electrons are formed which is commonly called as an avalanche of free electrons. This leads to the breakdown of the junction leading to very large reverse current. The reverse voltage at which the junction breakdown occurs is known as **breakdown voltage**.



PN DIODE APPLICATIONS

An ideal PN junction diode is a two terminal polarity sensitive device that has zero resistance (diode conducts) when it is forward biased and infinite resistance (diode does not conduct) when reverse biased. Due to this characteristic the diode finds a number of applications as follows.

(i) rectifiers in dc power supplies
(ii) switch in digital logic circuits used in computers
(iii) clamping network used as dc restorer in TV receivers and voltage multipliers
(iv) clipping circuits used as wave shaping circuits used in computers, radars, radio and TV receivers
(v) demodulation (detector) circuits.

The same PN junction with different doping concentration finds special applications as follows:

(i) detectors (APD, PIN photo diode) in optical communication circuits
(ii) Zener diodes in voltage regulators
(iii) varactor diodes in tuning sections of radio and TV receivers
(iv) light emitting diodes in digital displays
(v) LASER diodes in optical communications
(vi) Tunnel diodes as a relaxation oscillator at microwave frequencies.

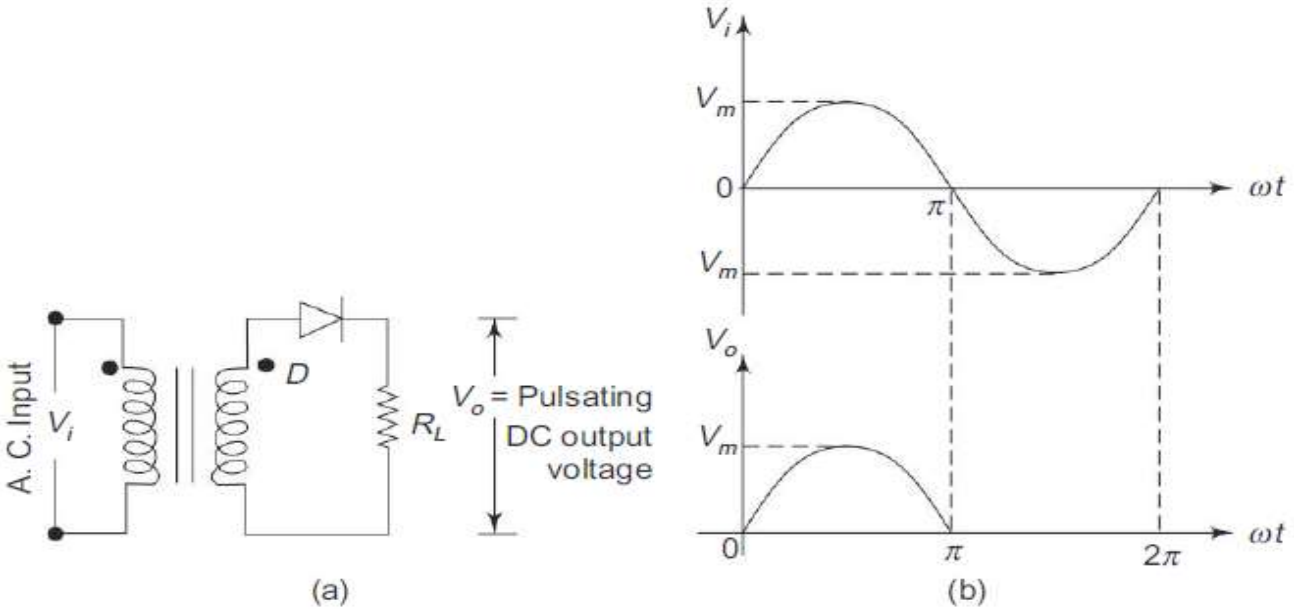
APPLICATIONS OF PN JUNCTION DIODE

RECTIFIERS, CLIPPERS, CLAMPERS ect..

RECTIFIERS-Rectifier is defined as an electronic device used for converting ac voltage into dc voltage

Half-wave Rectifier

It converts an ac voltage into a pulsating dc voltage using only one half of the applied ac voltage. The rectifying diode conducts during one half of the ac cycle only. Figure shows the basic circuit and waveforms of a half wave rectifier.



(a) Basic circuit of a Half-wave Rectifier and (b) Input and Output Waveforms of Half-wave Rectifier

Let V_i be the voltage to the primary of the transformer and given by the equation

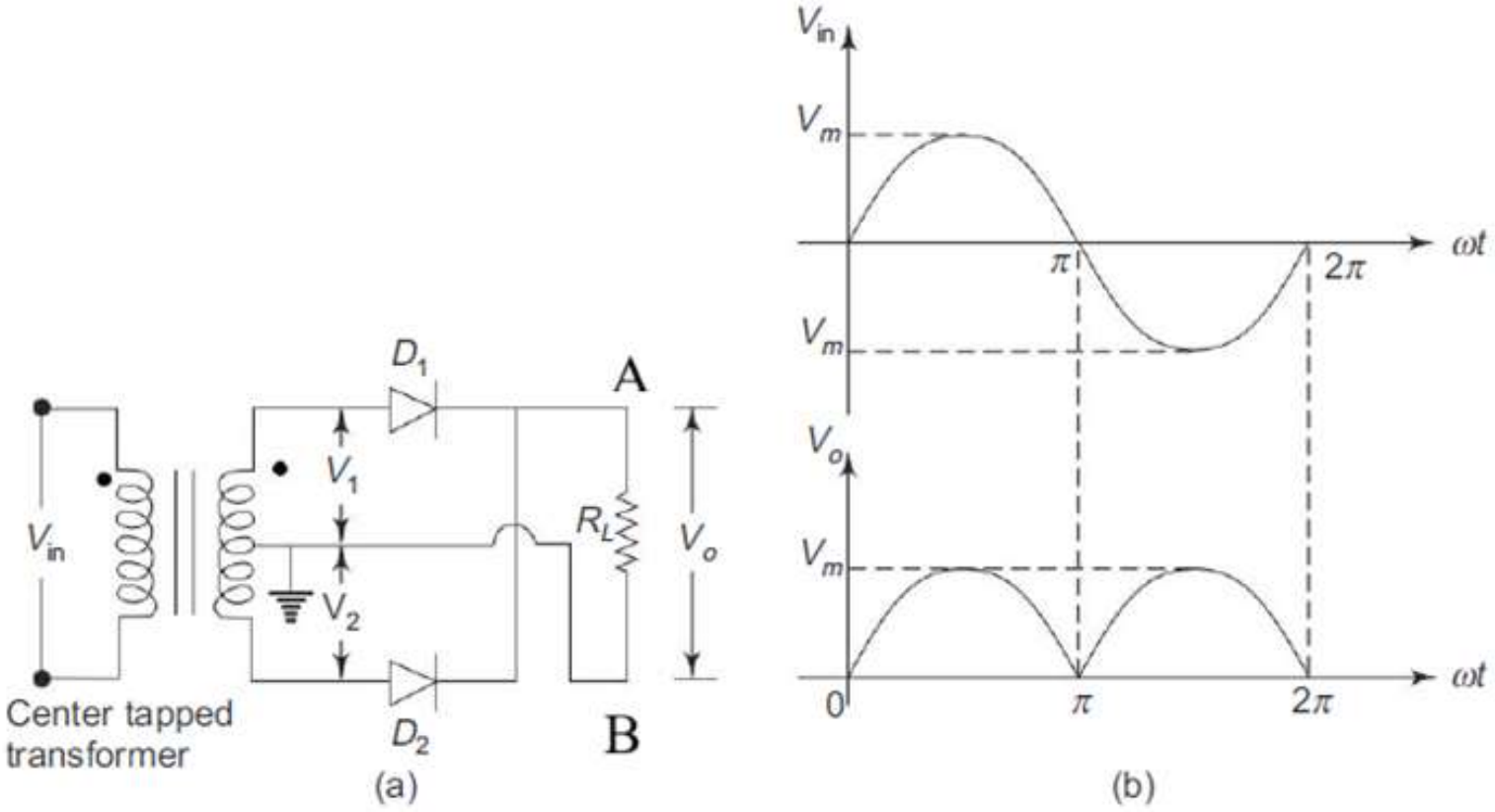
$$V_i = V_m \sin \omega t;\ V_m >> V_r$$

where V_r is the cut-in voltage of the diode. During the positive half-cycle of the input signal, the anode of the diode becomes more positive with respect to the cathode and hence, diode D conducts. For an ideal diode, the forward voltage drop is zero. So the whole input voltage will appear across the load resistance, R_L.

During negative half-cycle of the input signal, the anode of the diode becomes negative with respect to the cathode and hence, diode D does not conduct. For an ideal diode, the impedance offered by the diode is infinity. So the whole input voltage appears across diode D. Hence, the voltage drop across R_L is zero.

Full-wave Rectifier -Center Tapped

It converts an ac voltage into a pulsating dc voltage using both half cycles of the applied ac voltage. It uses two diodes of which one conducts during one half-cycle while the other diode conducts during the other half-cycle of the applied ac voltage. Figure shows the basic circuit and waveforms of full-wave rectifier.

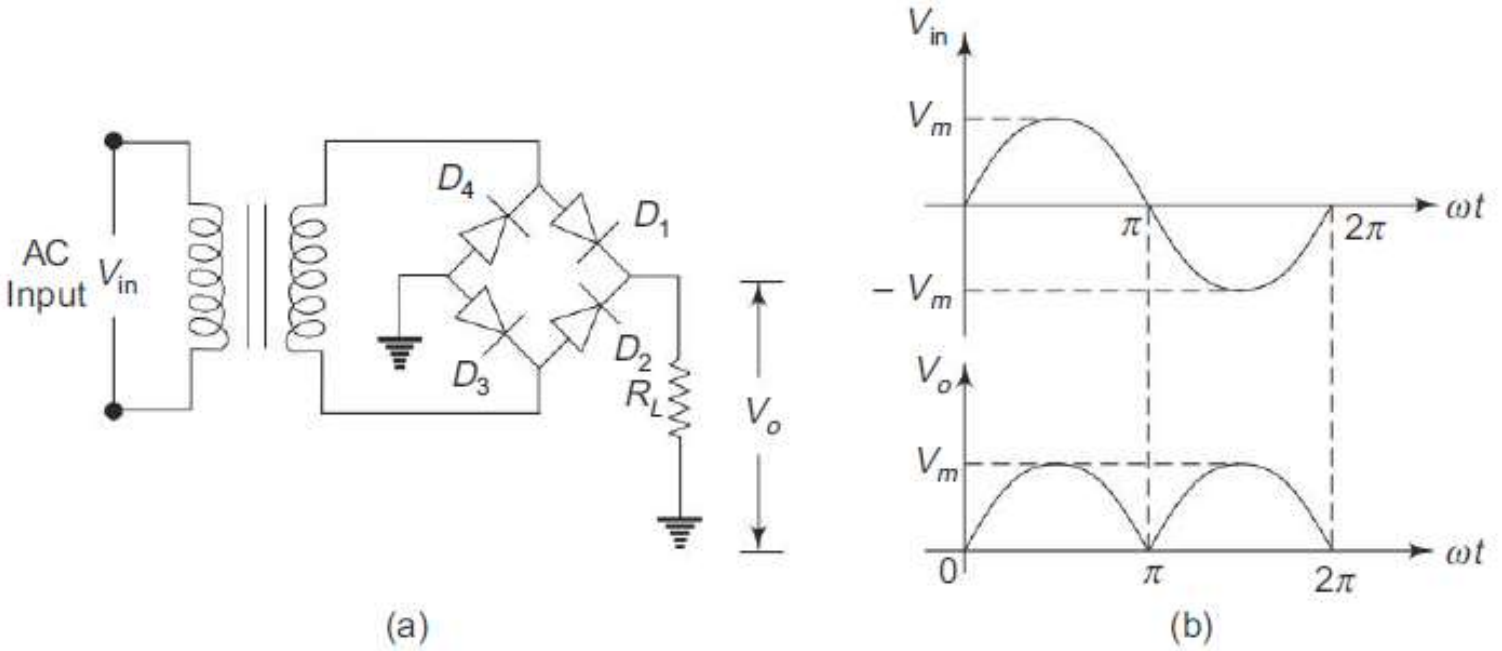


During positive half of the input signal, anode of diode D_1 becomes positive and at the same time the anode of diode D_2 becomes negative. Hence D_1 conducts and D_2 does not conduct. The load current flows through D_1 and the voltage drop across R_L will be equal to the input voltage.

During the negative half-cycle of the input, the anode of D_1 becomes negative and the anode of D_2 becomes positive. Hence, D_1 does not conduct and D_2 conducts. The load current flows through D_2 and the voltage drop across R_L will be equal to the input voltage.

Full-wave Rectifier - Bridge Rectifier

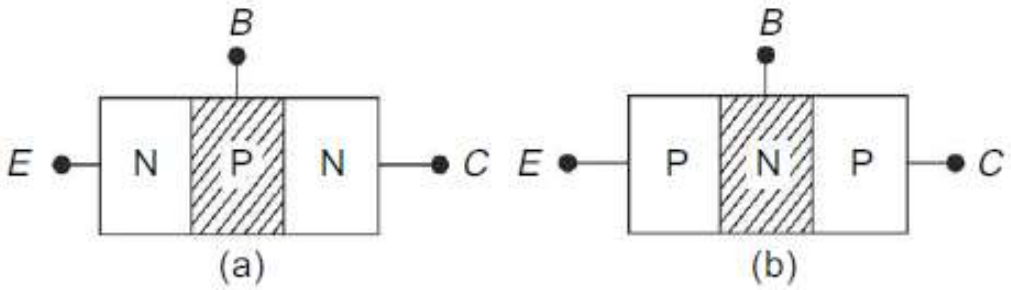
The need for a center tapped transformer in a full-wave rectifier is eliminated in the bridge rectifier. As shown in Fig. the bridge rectifier has four diodes connected to form a bridge. The ac input voltage is applied to diagonally opposite ends of the bridge. The load resistance is connected between the other two ends of the bridge.



BIPOLAR JUNCTION TRANSISTOR [BJT]

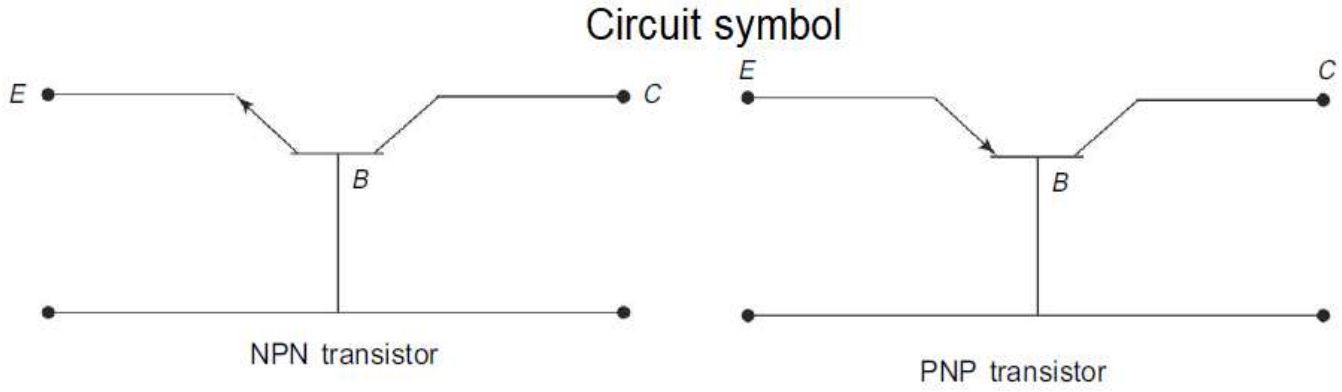
A Bipolar Junction Transistor (BJT) is a three terminal semiconductor device in which the operation depends on the interaction of both majority and minority carriers and hence the name Bipolar. It is used in amplifier and oscillator circuits, and as a switch in digital circuits. It has wide applications in computers, satellites and other modern communication systems.

The BJT consists of a silicon (or germanium) crystal in which a thin layer of N-type Silicon is sandwiched between two layers of P-type silicon. This transistor is referred to as PNP. Alternatively, in a NPN transistor, a layer of P-type material is sandwiched between two layers of N-type material. The two types of the BJT are represented in Fig.



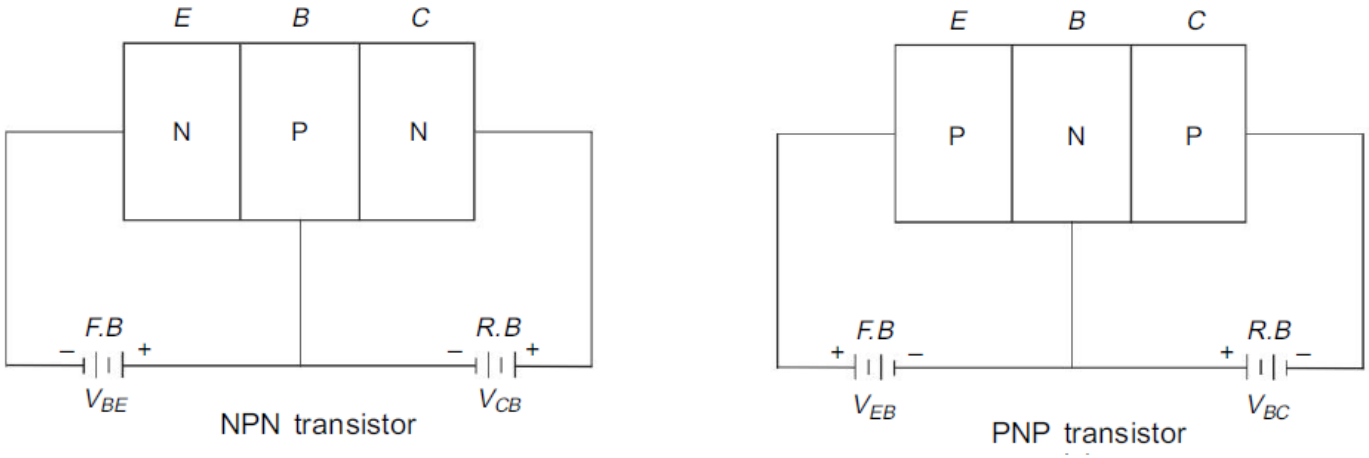
E- Emitter
B-Base
C-Collector

Transistor (a) NPN and (b) PNP



TRANSISTOR BIASING

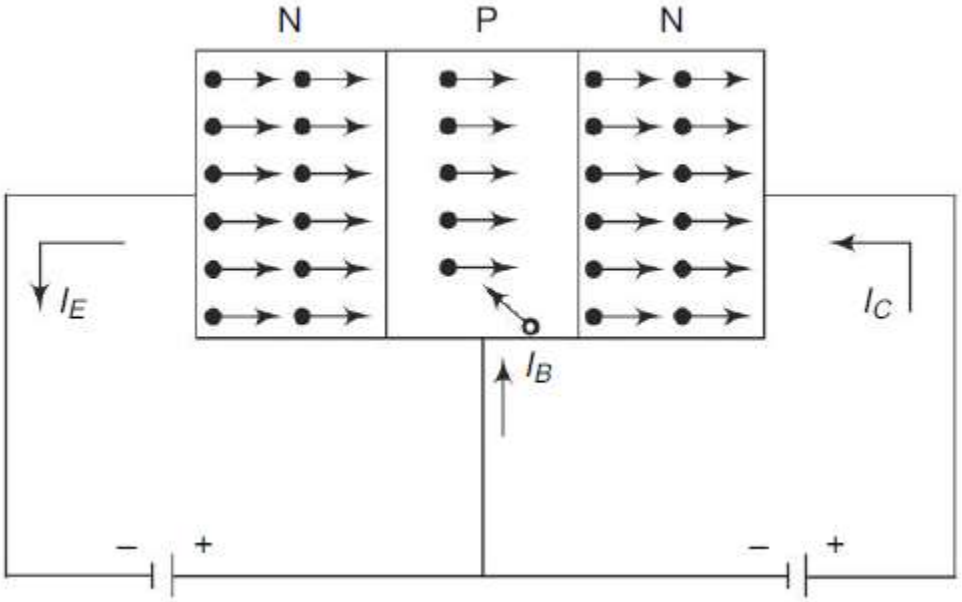
Usually the emitter-base junction is forward biased and collector-base junction is reverse biased. Due to the forward bias on the emitter-base junction an emitter current flows through the base into the collector. Though, the collector-base junction is reverse biased, almost the entire emitter current flows through the collector circuit.



OPERATION OF NPN TRANSISTOR

As shown in Fig. 13.4, the forward bias applied to the emitter base junction of an NPN transistor causes a lot of electrons from the emitter region to crossover to the base region. As the base is lightly doped with P-type impurity, the number of holes in the base region is very small and hence the number of electrons that combine with holes in the P-type base region is also very small. Hence a few electrons combine with holes to constitute a base current I_B. The remaining electrons (more than 95%) crossover into the collector region to constitute a collector current I_C. Thus the base and collector current summed up gives the emitter current, i.e. $I_E = -(I_C + I_B)$.

In the external circuit of the NPN bipolar junction transistor, the magnitudes of the emitter current I_E, the base current I_B and the collector current I_C are related by $I_E = I_C + I_B$.



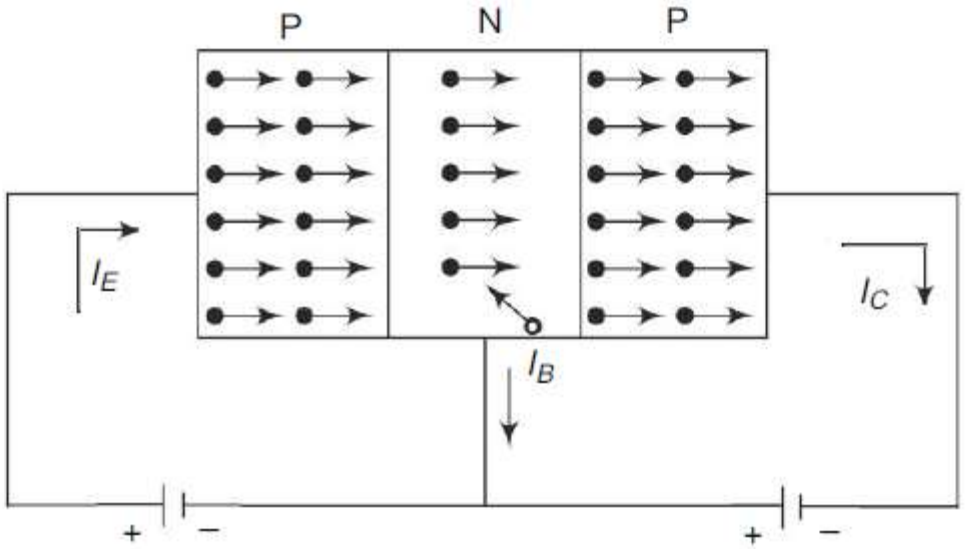
OPERATION OF PNP TRANSISTOR

As shown in Fig. 13.5, the forward bias applied to the emitter-base junction of a PNP transistor causes a lot of holes from the emitter region to crossover to the base region as the base is lightly doped with N-types impurity. The number of electrons in the base region is very small and hence the number of holes combined with electrons in the N-type base region is also very small. Hence a few holes combined with electrons to constitute a base current I_B. The remaining holes (more than 95%) crossover into the collector region to constitute a collector current I_C. Thus the collector and base current when summed up gives the emitter current, i.e. $I_E = -(I_C + I_B)$.

In the external circuit of the PNP bipolar junction transistor, the magnitudes of the emitter current I_E, the base current I_B and the collector current I_C are related by

$$I_E = I_C + I_B$$

This equation gives the fundamental relationship between the currents in a bipolar transistor circuit.

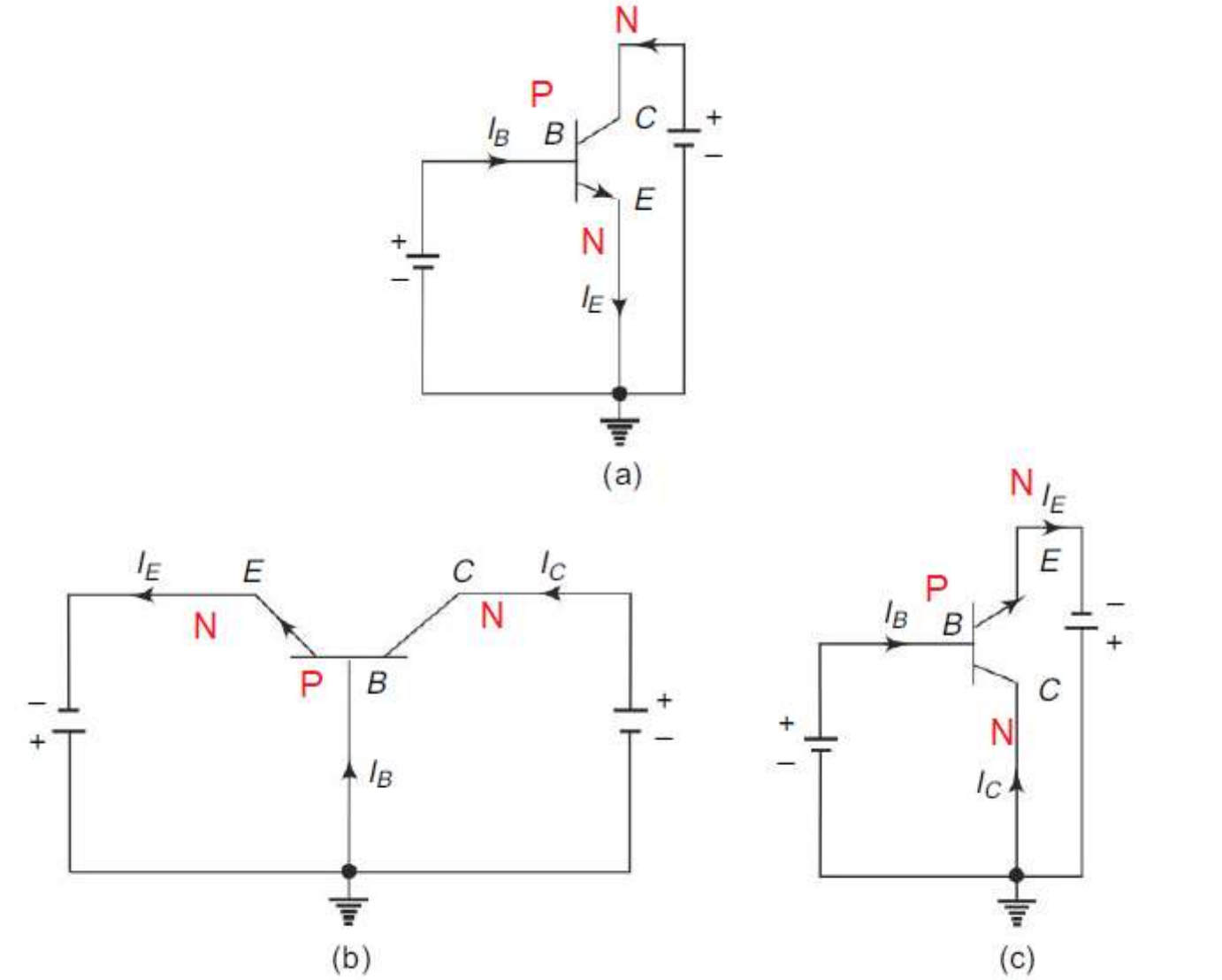


TYPES OF TRANSISTOR AMPLIFIER CONFIGURATION

(i) CB configuration This is also called grounded base configuration. In this configuration, emitter is the input terminal, collector is the output terminal and base is the common terminal.

(ii) CE configuration This is also called grounded emitter configuration. In this configuration, base is the input terminal, collector is the output terminal and emitter is the common terminal.

(iii) CC configuration This is also called grounded collector configuration. In this configuration, base is the input terminal, emitter is the output terminal and collector is the common terminal.



NPN Transistor configuration: (a) common emitter (b)common base and (c) common collector

CB Configuration

The circuit diagram for determining the static characteristics curves of an NPN transistor in the common base configuration is shown in Fig. 13.7.

Input characteristics To determine the input characteristics, the collector-base voltage V_{CB} is kept constant at zero volt and the emitter current I_E is increased from zero in suitable equal steps by increasing V_{EB}. This is repeated for higher fixed values of V_{CB}. A curve is drawn between emitter current I_E and emitter-base voltage V_{EB} at constant collector-base voltage V_{CB}. The input characteristics thus obtained are shown in Fig. 13.8.

When V_{CB} is equal to zero and the emitter-base junction is forward biased as shown in the characteristics, the junction behaves as a forward biased diode so that emitter current I_E increases rapidly with small increase in emitter-base voltage V_{EB}. When V_{CB} is increased keeping V_{EB} constant, the width of the base region will decrease. This effect results in an increase of I_E. Therefore, the curves shift towards the left as V_{CB} is increased.

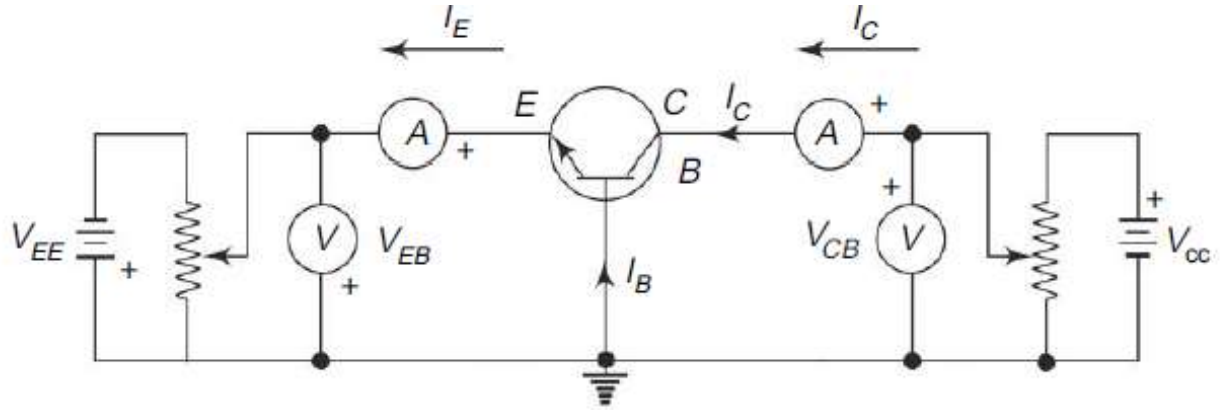


Fig. 13.7 Circuit to determine CB static characteristics

Output characteristics To determine the output characteristics, the emitter current I_E is kept constant at a suitable value by adjusting the emitter-base voltage V_{EB}. Then V_{CB} is increased in suitable equal steps and the collector current I_C is noted for each value of I_E. This is repeated for different fixed values of I_E. Now the curves of I_C versus V_{CB} are plotted for constant values of I_E and the output characteristics thus obtained is shown in Fig. 13.9.

From the characteristics, it is seen that for a constant value of I_E, I_C is independent of V_{CB} and the curves are parallel to the axis of V_{CB}. Further, I_C flows even when V_{CB} is equal to zero. As the emitter-base junction is forward biased, the majority carriers, i.e. electrons, from the emitter are injected into the base region. Due to the action of the internal potential barrier at the reverse biased collector-base junction, they flow to the collector region and give rise to I_C even when V_{CB} is equal to zero.

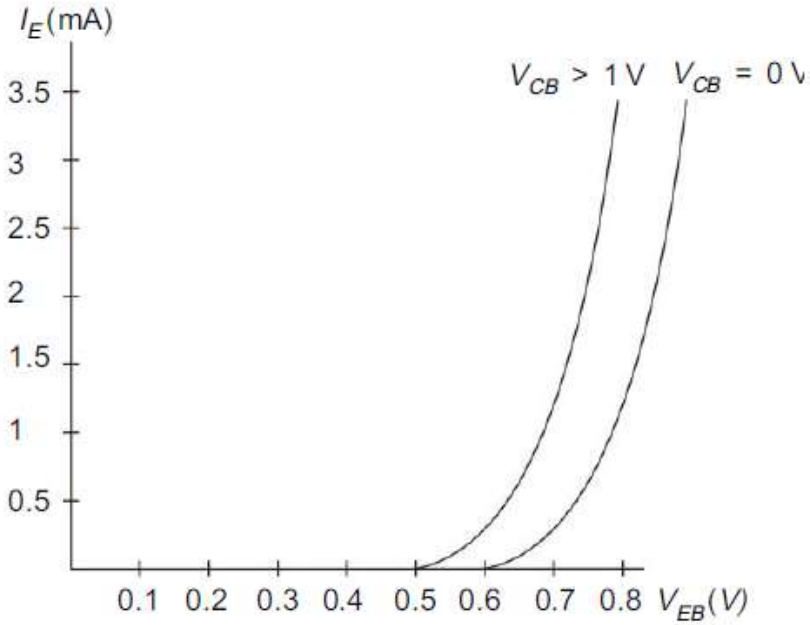


Fig. 13.8 CB Input characteristics

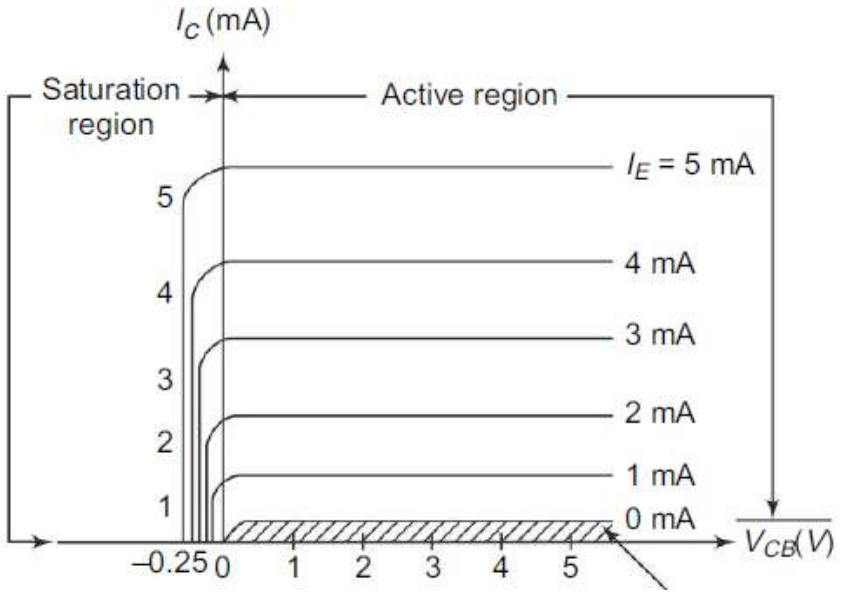


Fig. 13.9 CB Output Characteristics

CE Configuration

Input characteristics To determine the input characteristics, the collector to emitter voltage is kept constant at zero volt and base current is increased from zero in equal steps by increasing V_{BE} in the circuit shown in Fig. 13.10.

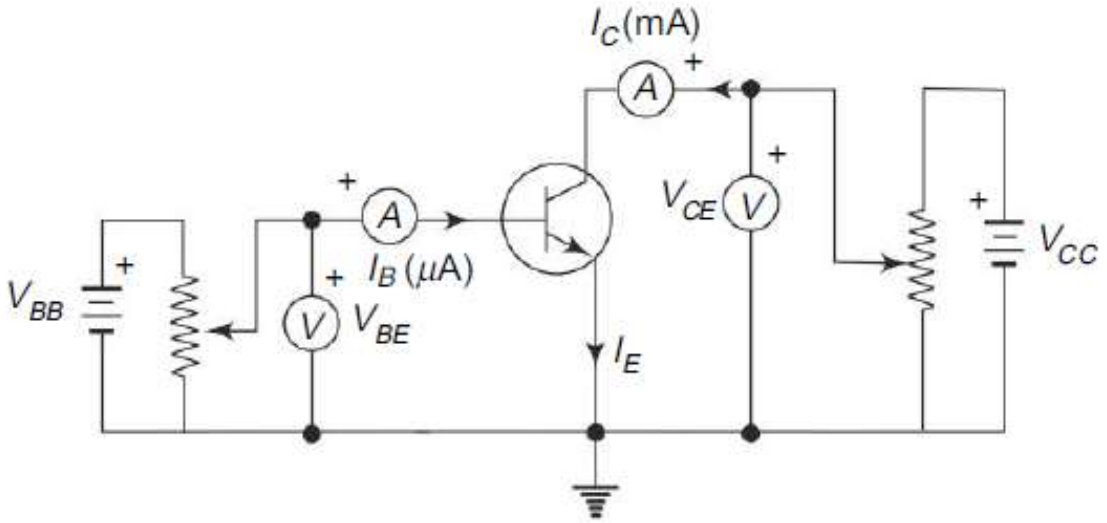


Fig. 13.10 Circuit to determine CE static characterisics

The value of V_{BE} is noted for each setting of I_B. This procedure is repeated for higher fixed values of V_{CE}, and the curves of I_B V_s V_{BE} are drawn. The input characteristics thus obtained are shown in Fig. 13.11.

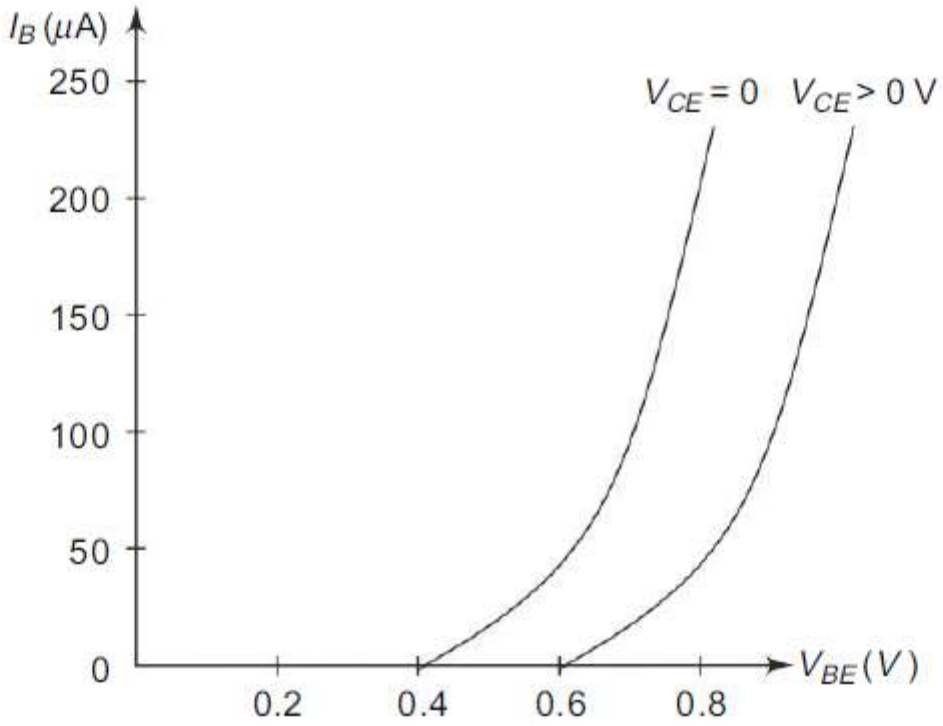


Fig. 13.11 CE input characteristics

When $V_{CE} = 0$, the emitter-base junction is forward biased and the junction behaves as a forward biased diode. Hence the input characteristic for $V_{CE} = 0$ is similar to that of a forward-biased diode. When V_{CE} is increased, the width of the depletion region at the reverse biased collector-base junction will increase. Hence the effective width of the base will decrease. This effect causes a decrease in the base current I_B. Hence, to get the same value of I_b as that for $V_{CE} = 0$, V_{BE} should be increased. Therefore, the curve shifts to the right as V_{CE} increases.

Output characteristics To determine the output characteristics, the base current I_B is kept constant at a suitable value by adjusting base-emitter voltage, V_{BE}. The magnitude of collector-emitter voltage V_{CE} is increased in suitable equal steps from zero and the collector current I_C is noted for each setting of V_{CE}. Now the curves of I_C versus V_{CE} are plotted for different constant values of I_B. The output characteristics thus obtained are shown in Fig. 13.12.

The output characteristics have three regions, namely, saturation region, cutoff region and active region. The region of curves to the left of the line OA is called the *saturation region* (hatched), and the line OA is called the saturation line. In this region, both junctions are forward biased and an increase in the base current does not cause a corresponding large change in I_C. The ratio of $V_{CE(sat)}$ to I_C in this region is called saturation resistance.

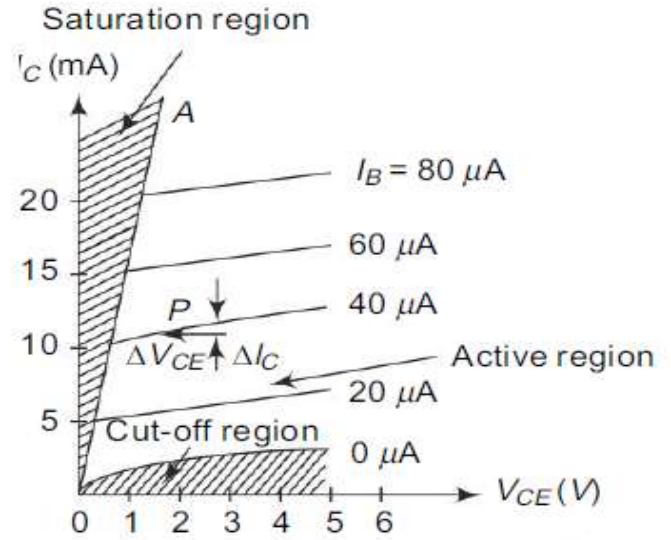


Fig. 13.12 CE output characteristics

The region below the curve for $I_B = 0$ is called the *cut-off region* (hatched). In this region, both junctions are reverse biased. When the operating point for the transistor enters the cut-off region, the transistor is OFF. Hence, the collector current becomes almost zero and the collector voltage almost equals V_{CC}, the collector supply voltage. The transistor is virtually an open circuit between collector and emitter.

The central region where the curves are uniform in spacing and slope is called the *active region* (unhatched). In this region, emitter-base junction is forward biased and the collector-base junction is reverse biased. If the transistor is to be used as a linear amplifier, it should be operated in the active region.

FIELD EFFECT TRANSISTOR

FET is a device in which the flow of current through the conducting region is controlled by an electric field. Hence the name Field Effect Transistor (FET). As current conduction is only by majority carries, FET is said to be a unipolar device.

Based on the construction, the FET can be classified into two types as Junction FET (JFET) and Metal Oxide Semiconductor FET (MOSFET).

Depending upon the majority carriers, JFET has been classified into two types named as (1) N-channel JFET with electrons as the majority carriers and (2) P-channel JFET with holes as the majority carriers.

Construction of N-Channel JFET

It consists of an N-type bar which is made of silicon. Ohmic contacts, (terminals) made at the two ends of the bar, are called Source and Drain.

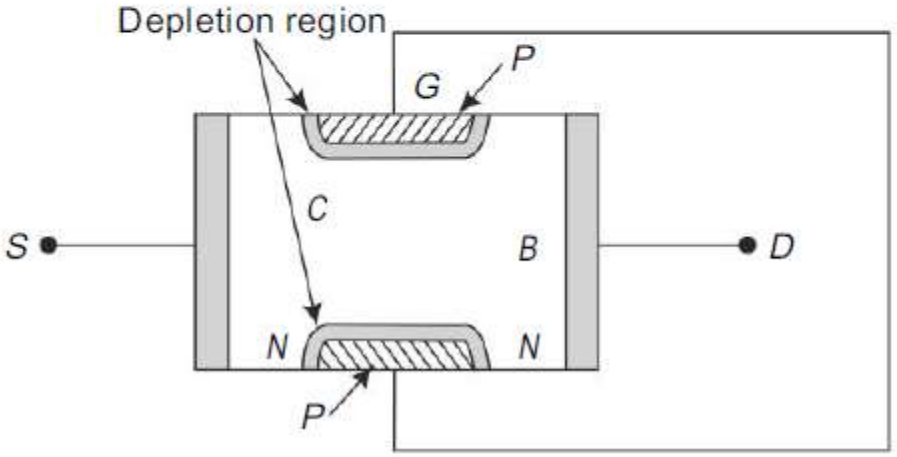
Source (S) This terminal is connected to the negative pole of the battery. Electrons which are the majority carriers in the N-type bar enter the bar through this terminal.

Drain (D) This terminal is connected to the positive pole of the battery. The majority carriers leave the bar through this terminal.

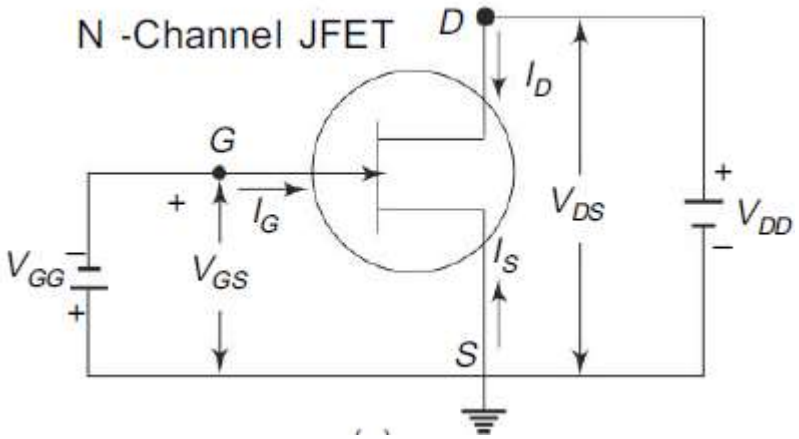
Gate (G) Heavily doped P-Type silicon is diffused on both sides of the N-type silicon bar by which PN junctions are formed. These layers are joined together and the called Gate *G*.

Operation of N-channel JFET

1. *When $V_{GS} = 0$ and $V_{DS} = 0$* When no voltage is applied between drain and source, and gate and source, the thickness of the depletion regions around the PN junction is uniform as shown in Fig.



JFET construction



2. *When $V_{DS} = 0$ and V_{GS} is decreased from zero* In this case PN junctions are reverse biased and hence the thickness of the depletion region increases. As V_{GS} is decreased from zero, the reverse bias voltage across the PN junction is increased and hence the thickness of the depletion region in the channel increases until the two depletion regions make contact with each other. In this condition, the channel is said to be cutoff. The value of V_{GS} which is required to cutoff the channel is called the cutoff voltage V_C.

3. *When $V_{GS} = 0$ and V_{DS} is increased from zero* Drain is positive with respect to the source with $V_{GS} = 0$. Now the majority carriers (electrons) flow through the N-channel from source to drain. Therefore the conventional current I_D flows from drain to source.

Because the resistance of the channel and the applied voltage V_{DS}, there is a gradual increase of positive potential along the channel from source to drain. Thus the reverse voltage across the PN junctions increases and hence the thickness of the depletion regions also increases. Therefore the channel is wedge shaped, as shown in Fig. 13.20.

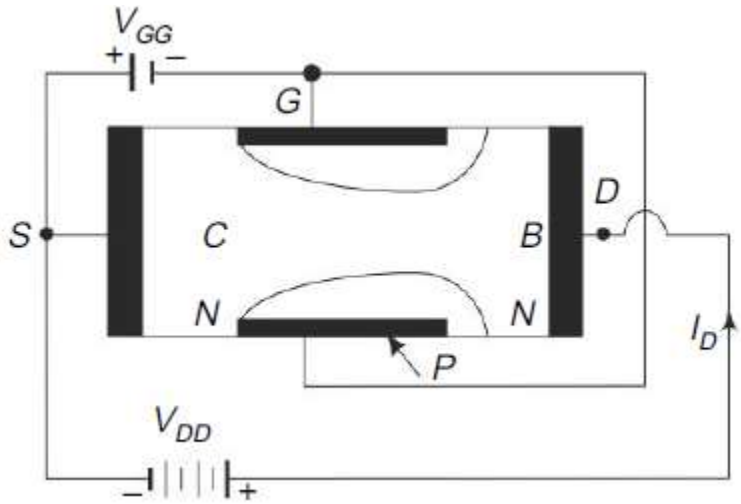


Fig. 13.20 JEFT Under Applied Bias

As V_{DS} is increased, the cross-sectional area of the channel will be reduced. At a certain value V_P of V_{DS}, the cross-sectional area at B becomes minimum. At this voltage, the channel is said to be pinched off and the drain voltage V_P is called the pinch-off voltage.

4.*When V_{GS} is negative and V_{DS} is increased* When the gate is maintained at a negative voltage less than the negative cutoff voltage, the reverse voltage across the junction is further increased. Hence for a negative value of V_{GS}, the curve of I_D versus V_{DS} is similar to that for $V_{GS} = 0$, but the values of V_P and BV_{DGO} are lower, as shown in Fig. 13.21.

From the curves, it is seen that above the pinch-off voltage, at a constant value of V_{DS}, I_D increases with an increase of V_{GS}. Hence a JFET is suitable for use as a voltage amplifier, similar to a transistor amplifier.

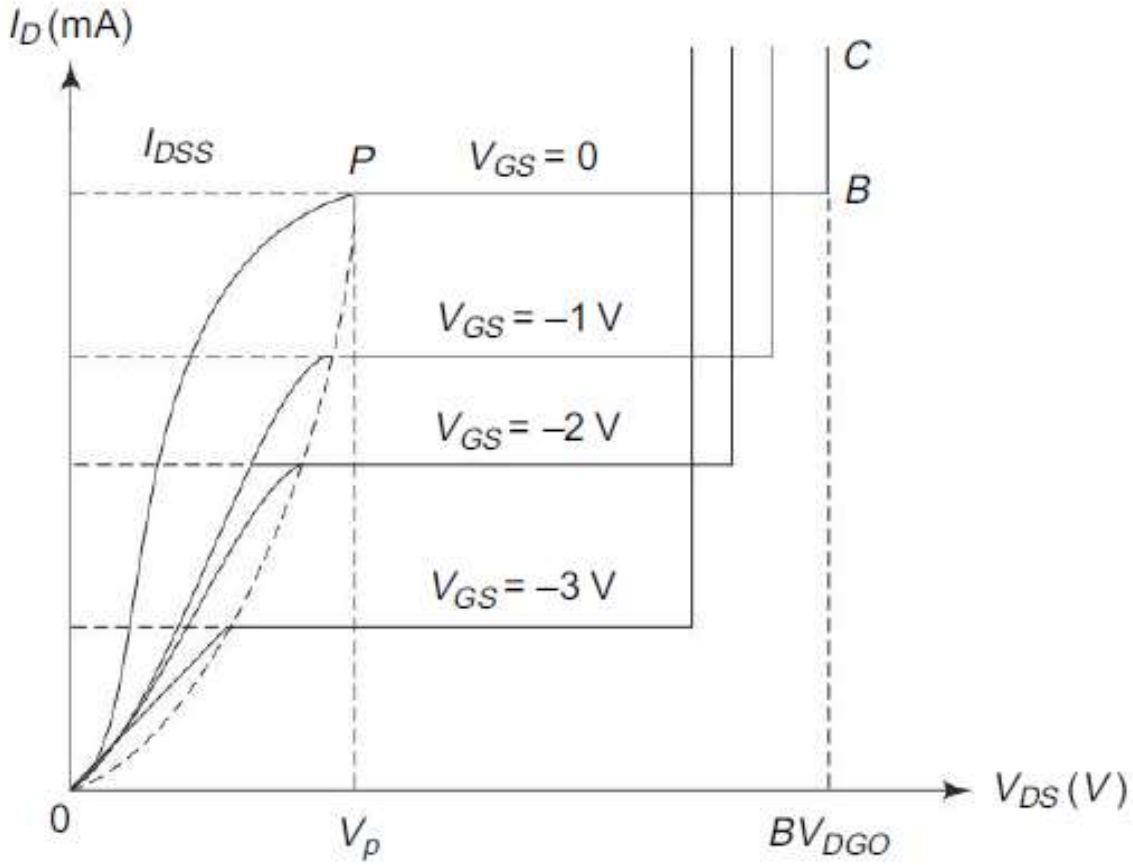


Fig. 13.21 Drain Characteristics

Comparison of JFET and BJT

1. FET operation depends only on the flow of majority carriers—holes for P-channel FETs and electrons for N-channel FETs. Therefore they are called Unipolar devices. Bipolar transitor (BJT) operation depends on both minority and majority current carriers.
2. FETs are less noisy than BJTs.
3. FETs exhibit a much higher input impedance ($> 100\ M\Omega$) than BJTs.
4. FETs are much easier to fabricate and are particularly suitable for ICs because they occupy less space than BJTs.
5. FET is normally less sensitive to temperature.
6. FET amplifiers have less voltage gain and produce more signal distortion except for small signal operation.
7. FET is a voltage controlled device whereas BJT is a current controlled device

Metal Oxide Semiconductor Field Effect Transistor (MOSFET)

MOSFET is the common term of the Insulated Gate Field Effect Transistor (IGFET). There are two forms of MOSFET: (i) Enhancement MOSFET and (ii) Depletion MOSFET.

Principle By applying a transverse electric field across an insulator, deposited on the semiconducting material, the thickness and hence the resistance of a conducting channel of a semiconducting material can be controlled.

Enhancement MOSFET

Construction The construction of an N-channel Enhancement MOSFET is shown in Fig. 13.23. Two highly doped N^+ regions are diffused in a lightly doped substrate of P-type silicon substrate. One N^+ region is called the source *S* and the other one is called the drain *D*. They are separated by 1 mil (10^{-3} inch). A thin insulating layer of SiO_2 is grown over the surface of the structure and holes are cut into the oxide layer, allowing contact with source and drain. Then a thin layer of metal aluminum is formed over the layer of SiO_2. This metal layer covers the entire channel region and it forms the gate *G*.

The metal area of the gate, in conjunction with the insulating oxide layer of SiO_2 and the semiconductor channel forms a parallel plate capacitor. This device is called the insulated gate FET because of the insulating layer of SiO_2. This layer gives an extremely high input resistance for the MOSFET.

Operation If the substrate is grounded and a positive voltage is applied at the gate, the positive charge on G induces an equal negative charge on the substrate side between the source and drain regions. Thus an electric field is produced between the source and drain regions. The direction of the electric field is perpendicular to the plates of the capacitor through the oxide. The negative charge of electrons which are minority carriers in the P-type substrate forms an inversion layer. As the positive voltage on the gate increases, the induced negative charge in the semiconductor

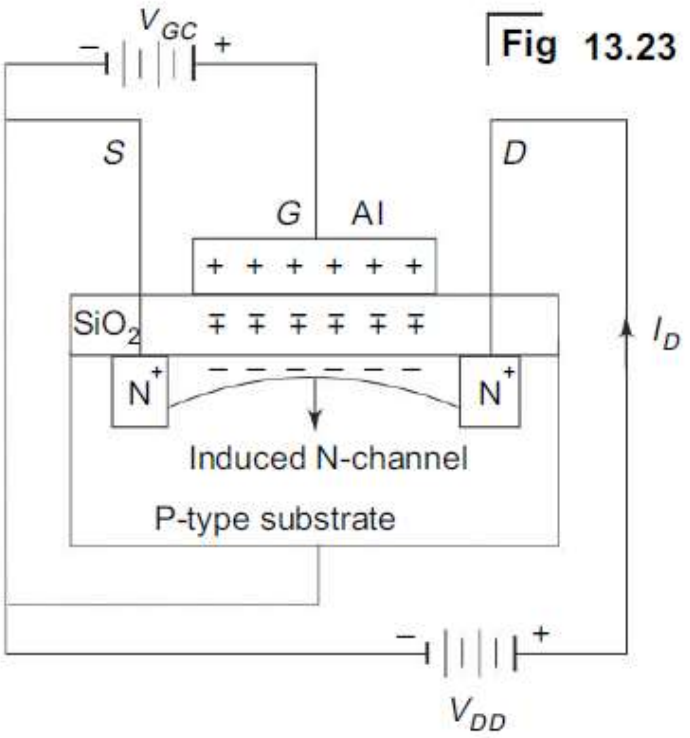


Fig 13.23 N-Channel Enhancement MOSFET

increases. Hence the conductivity increases and current flows from source to drain through the induced channel. Thus the drain current is enhanced by the positive gate voltage as shown in Fig. 13.25.

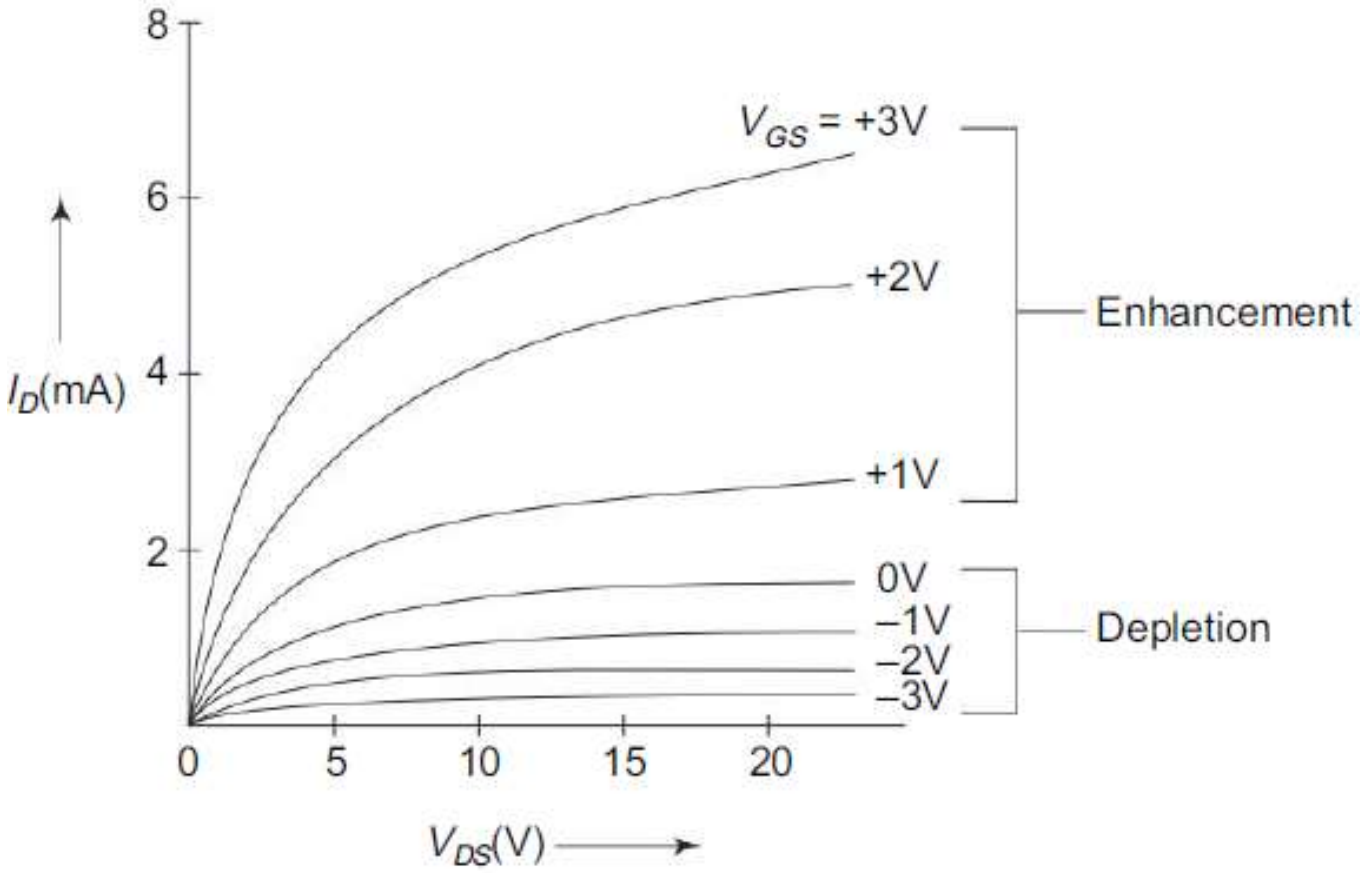


Fig. 13.25 Volt-Ampere Characteristics of MOSFET

2.5. INSULATED GATE BIPOLAR TRANSISTOR (IGBT)

IGBT is a new development in the area of power MOSFET technology. This device combines into it the advantages of both MOSFET and BJT. So an IGBT has high input impedance like a MOSFET and low-on-state power loss as in a BJT. Further, IGBT is free from second breakdown problem present in BJT.

2.5.1. Basic Structure and Working

Fig. 2.16 illustrates the basic structure of an IGBT. It is constructed virtually in the same manner as a power MOSFET. There is, however ; a major difference in the substrate. The n^+ layer substrate at the drain in a power MOSFET is now substituted in the IGBT by a p^+ layer substrate called collector. Like a power MOSFET, an IGBT has also thousands of basic structure cells connected appropriately on a single chip of silicon.

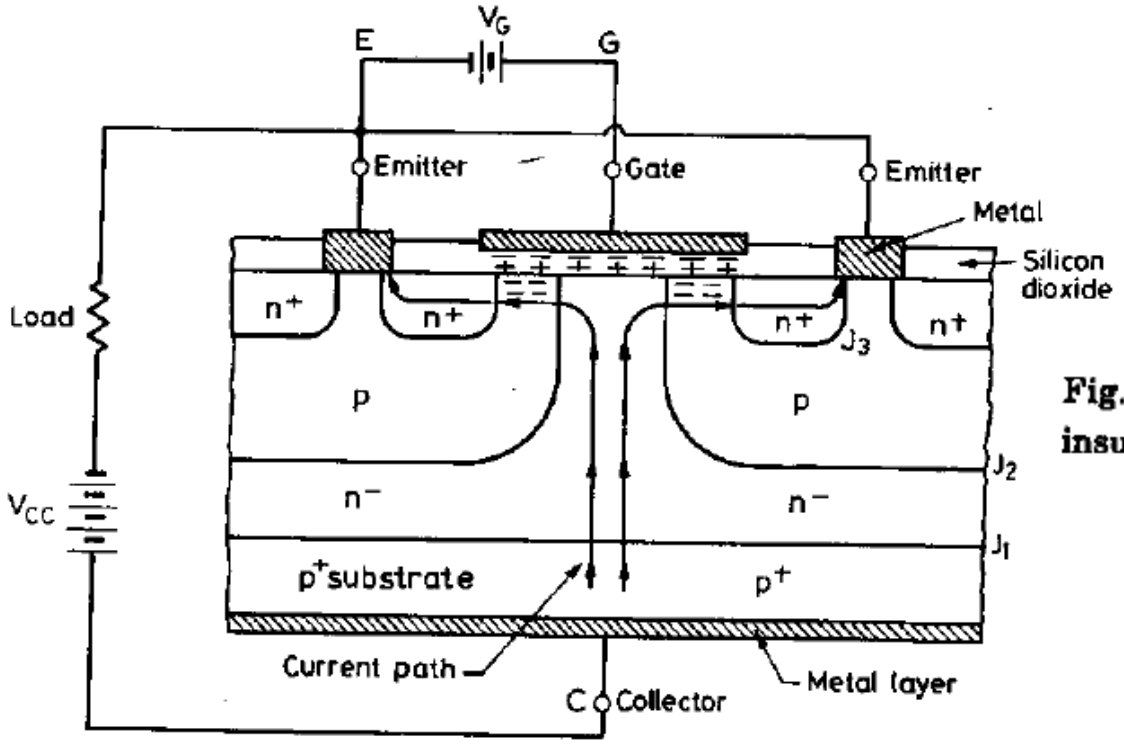


Fig. 2.16. Basic structure of an insulated gate bipolar transistor (IGBT).

When gate is positive with respect to emitter and with gate-emitter voltage more than the threshold voltage of IGBT, an n-channel is formed in the p-regions as in a power MOSFET, Fig. 2.16. This n-channel short circuits the n^- region with n^+ emitter regions. An electron movement in the n-channel, in turn, causes substantial hole injection from p^+ substrate layer into the epitaxial n^- layer. Eventually, a forward current is established as shown in Fig. 2.16.

The three layers p^+, n^- and p constitute a *pnp* transistor with p^+ as emitter, n^- as base and p as collector. Also n^-, p and n^+ layers constitute *npn* transistor as shown in Fig. 2.17 (a). Here n^- serves as base for *pnp* transistor and also as collector for *npn* transistor. Further,

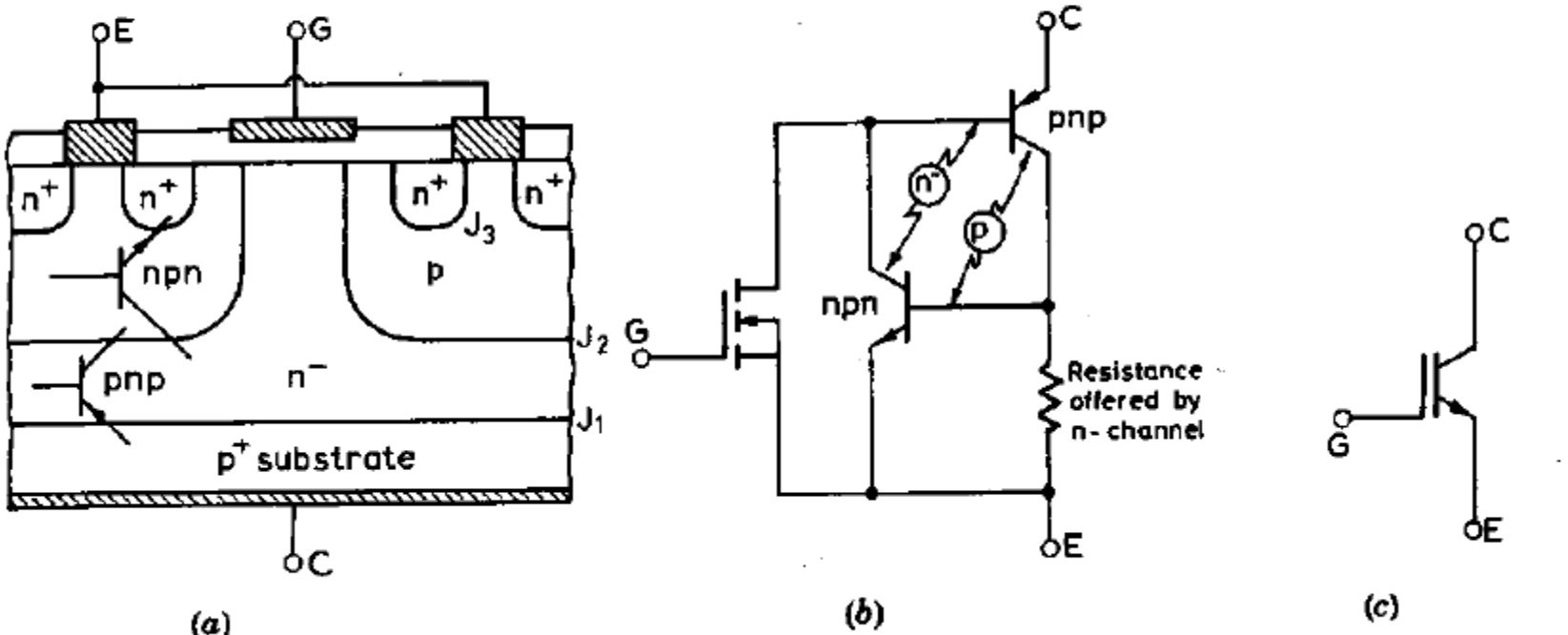


Fig. 2.17. IGBT (a) Basic structure, (b) its equivalent circuit and (c) its circuit symbol.

2.5.2. IGBT Characteristics

The circuit of Fig. 2.18 (*a*) shows the various parameters pertaining to IGBT characteristics.

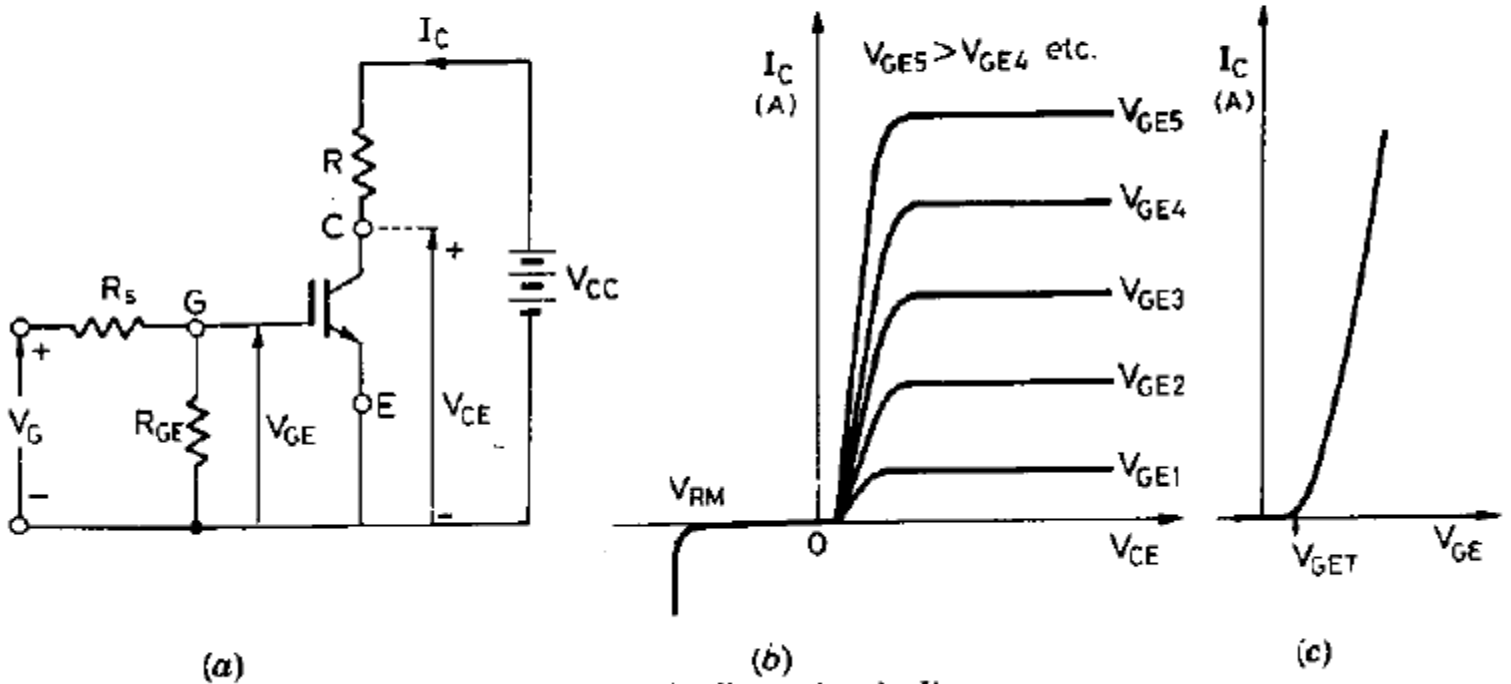


Fig. 2.18. IGBT (*a*) circuit diagram,
(*b*) static *V-I* characteristics and (*c*) transfer characteristics.

Static *V-I* or output characteristics of an IGBT (*n*-channel type) show the plot of collector current I_C versus collector-emitter voltage V_{CE} for various values of gate-emitter voltages. These characteristics are shown in Fig. 2.18 (*b*). In the forward direction, the shape of the output characteristics is similar to that of BJT. But here the controlling parameter is gate-emitter voltage V_{GE} because IGBT is a voltage-controlled device.

The transfer characteristic of an IGBT is a plot of collector current I_C versus gate-emitter voltage V_{GE} as shown in Fig. 2.18 (*c*). This characteristic is identical to that of power MOSFET. When V_{GE} is less than the threshold voltage V_{GET}, IGBT is in the off-state.

When the device is off, junction J_2 blocks forward voltage and in case reverse voltage appears across collector and emitter, junction J_1 blocks it.

2.5.4. Applications of IGBT

IGBTs are widely used in medium power applications such as dc and ac motor drives, UPS systems, power supplies and drives for solenoids, relays and contactors. Though IGBTs are somewhat more expensive than BJTs, yet they are becoming popular because of lower gate-drive requirements, lower switching losses and smaller snubber circuit requirements. IGBT converters are more efficient with less size as well as cost, as compared to converters based on BJTs. Recently, IGBT inverter induction-motor drives using 15-20 kHz switching frequency are finding favour where audio-noise is objectionable. In most applications, IGBTs will eventually push out BJTs. At present, the state of the art IGBTs are available upto 1200 V, 500 A.

SCR (Silicon Controlled Rectifier)

The basic structure and circuit symbol of SCR is shown in Fig. 13.28. It is a four-layer, three-terminal device in which the end P-layer acts as anode, the end N-layer acts as cathode and P-layer nearer to cathode acts as gate.

Characteristics of SCR The characteristics of SCR are shown in Fig. 13.29. SCR acts as a switch when it is forward biased. When the gate current $I_G = 0$, operation of SCR is similar to PNPN diode. When $I_G < 0$, the amount of reverse bias

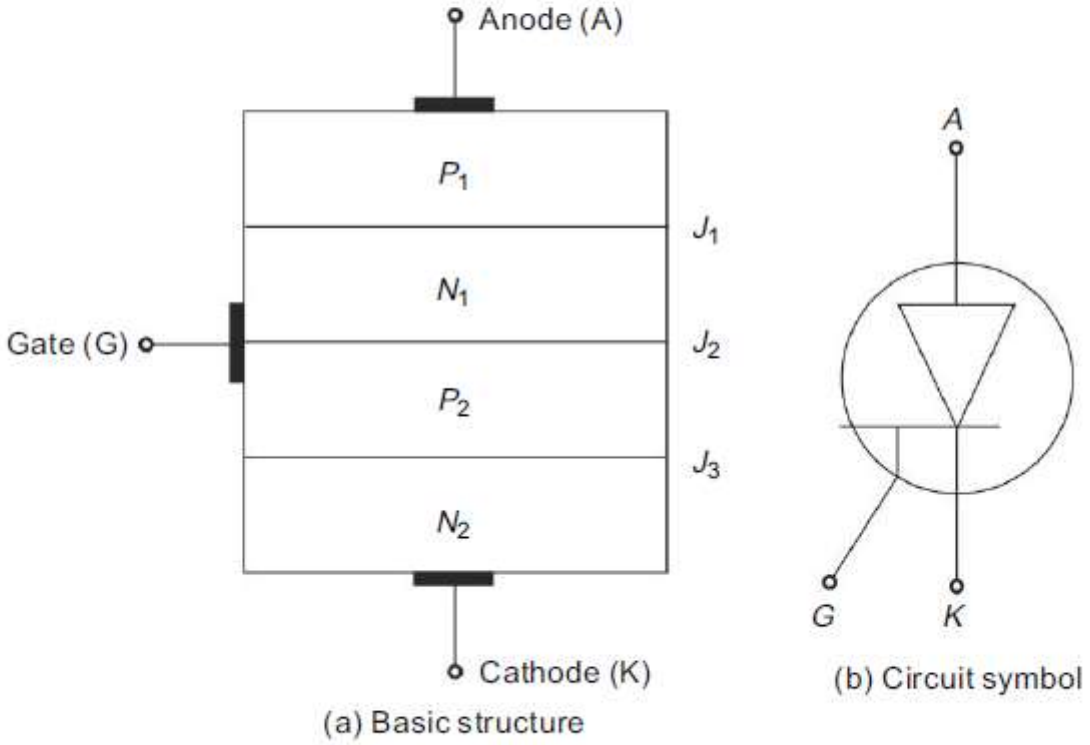


Fig. 13.28 Basic Structure and Circuit Symbol of SCR

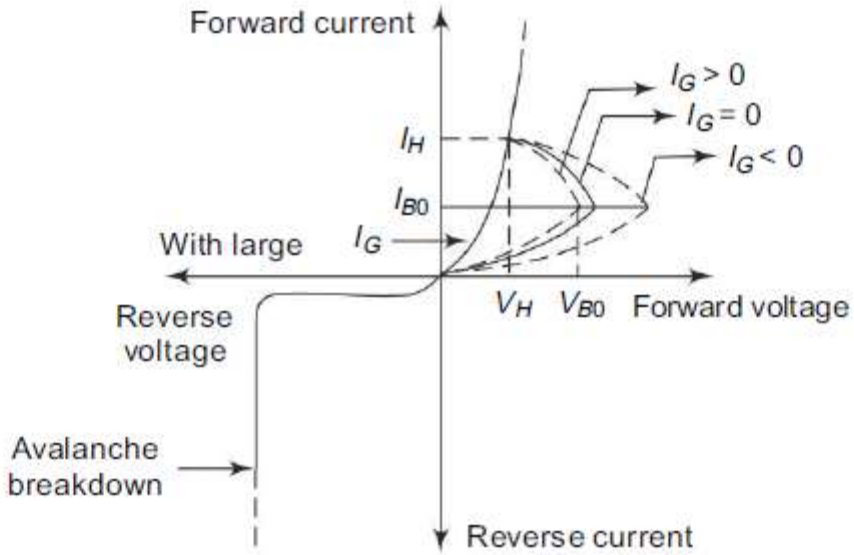


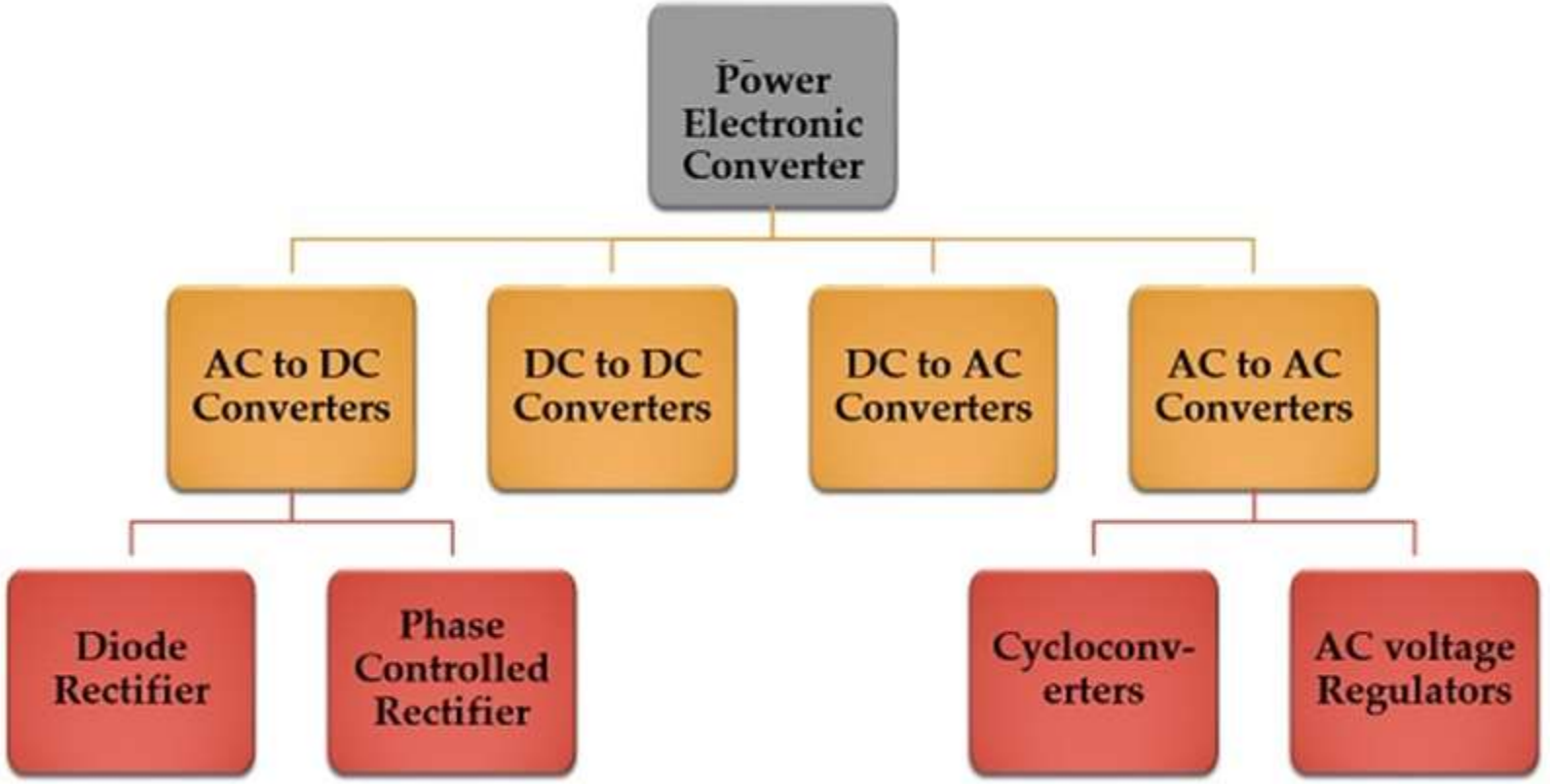
Fig. 13.29 Characteristics of SCR

applied to J_2 is increased. So the breakover voltage V_{BO} is increased. When $I_G > 0$, the amount of reverse bias applied to J_2 is decreased thereby decreasing the breakover voltage. With very large positive gate current, breakover may occur at a very low voltage such that the characteristic of SCR is similar to that of ordinary PN diode. As the voltage at which SCR is switched 'ON' can be controlled by varying the gate current I_G, it is commonly called as controlled switch. Once SCR is turned ON, the gate loses control, i.e. the gate cannot be used to switch the device OFF. One way to turn the device OFF is that the anode current is lowered below I_H by reducing the supply voltage below V_H, keeping the gate open.

SCR is used in relay control, motor control, phase control, heater control, battery chargers, inverters, regulated power supplies and as static switches.

Types of power converters

The classification of power converters are as follows:



1-AC to DC Converters

1A-Diode Rectifiers: This rectifier circuit changes applied ac input voltage into a fixed dc voltage. Either a single-phase or three-phase ac signal is applied at the input. These are mainly used in electric traction and in electrochemical processes like electroplating along with in battery charging and power supply. These are also used in welding and UPS related services.

1B-Phase Controlled Rectifiers: Unlike diode rectifiers, phase-controlled rectifiers are designed to convert a fixed value of ac signal voltage into a variable dc voltage. Here line voltage operates the rectifier hence these are sometimes known as line commutated ac to dc converters. Similar to diode rectifiers, here also the applied ac signal can be a single-phase or three-phase ac signal. Its major applications are in dc drives, HVDC systems, compensators, metallurgical and chemical industries as well as in excitation systems for synchronous machines.

2-DC to DC Converters

The converters that convert the dc signal of fixed frequency present at the input into a variable dc signal at the output are also known as **choppers**. Here the achieved output dc voltage may have a different amplitude than the source voltage. Generally, power transistors, MOSFETs, and thyristors are the semiconductor devices used for their fabrication. The output is controlled by a low power signal that controls these semiconductor devices from a control unit.

Here forced commutation is required to turn off the semiconductor device. Generally, in low power circuits power transistors are used while in high power circuits thyristors are used.
Choppers are classified on the basis of the type of commutation applied to them and on the basis of the direction of power flow. Some major uses of choppers are in dc drives, SMPS, subway cars, electric traction, trolley trucks, vehicles powered by battery, etc.

3-DC to AC Converters

The devices that are designed to convert the dc signal into ac signal are known as **inverters**. The applied input is a fixed dc voltage that can be obtained from batteries but the output obtained is variable ac voltage. The voltage and frequency of the signal obtained are of variable nature. Here the semiconductor device i.e., the thyristor is turned off by using either line, load, or forced commutation.
Thus, it can be said that by the use of inverters, a fixed dc voltage is changed into an ac voltage of variable frequency. Generally, the semiconductor devices used for its fabrication are power transistors, MOSFETs, IGBT, GTO, thyristors, ect
Inverters mainly find applications in induction motor and synchronous motor drives along with UPS, aircraft, and space power supplies. In high voltage dc transmission system, induction heating supplies as well as low power systems of mobile nature like flashlight discharge system in photography camera to very high power industrial system.
Like choppers, in inverters also conventional thyristors are used in high power applications and power transistors are used in low power applications

4-AC to AC Converters

An ac to ac converter is designed to change the ac signal of fixed frequency into a variable ac output voltage.

There are two classifications of ac to ac converters which are as follows:

4A-Cycloconverters: A cycloconverter is a device used for changing ac supply of fixed voltage and single frequency into an ac output voltage of variable voltage as well as different frequency. However, here the obtained variable ac signal frequency is lower than the frequency of the applied ac input signal. It adopts single-stage conversion. Generally, line commutation is mostly used in cycloconverters however forced or load commutated cycloconverters are also used in various applications.

These mainly find applications in slow-speed large AC traction drives such as a rotary kiln, multi MW ac motor drives, etc.

4B-AC Voltage Controllers (AC voltage regulators): The converters designed to change the applied ac signal of fixed voltage into a variable ac voltage signal of the same frequency as that of input. For the operation of these controllers, two thyristors in an antiparallel arrangement are used. Line commutation is used for turning off both the devices. It offers the controlling of the output voltage by changing the firing angle delay.

The major applications of ac voltage controllers are in lighting control, electronic tap changers, speed control of large fans and pumps as well.

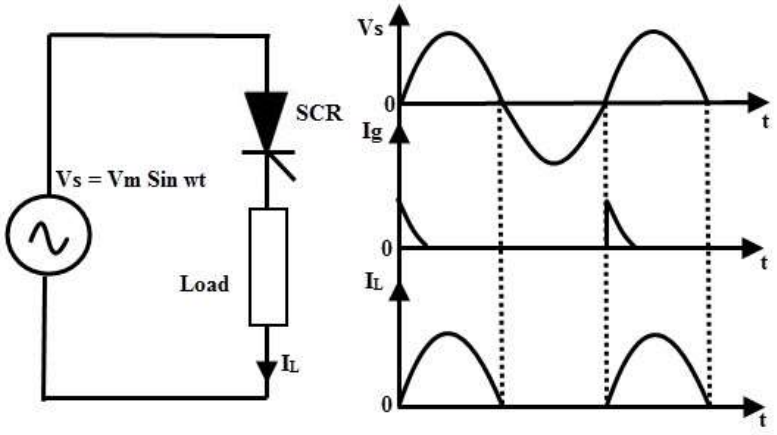
Commutation

Commutation is the process of turning off a conducting thyristor. There are two methods for commutation viz. natural commutation and forced commutation.

Natural Commutation

In natural commutation, the source of commutation voltage is the supply source itself. If the SCR is connected to an AC supply, at every end of the positive half cycle, the anode current naturally becomes zero (due to the alternating nature of the AC Supply). As the current in the circuit goes through the natural zero, a reverse voltage is applied immediately across the SCR (due to the negative half cycle). These conditions turn OFF the SCR.

This method of commutation is also called as Source Commutation or AC Line Commutation or Class F Commutation. This commutation is possible with line commutated inverters, controlled rectifiers, cyclo converters and AC voltage regulators because the supply is the AC source in all these converters.



Forced Commutation

In case of DC circuits, there is no natural current zero to turn OFF the SCR. In such circuits, forward current must be forced to zero with an external circuit (known as Commutating Circuit) to commutate the SCR. Hence the name, Forced Commutation.

This commutating circuit consist of components like inductors and capacitors and they are called Commutating Components. These commutating components cause to apply a reverse voltage across the SCR that immediately bring the current in the SCR to zero.

Depending on the process for achieving zero current in the SCR and the arrangement of the commutating components, Forced Commutation is classified into different types. They are:

Class A – Self Commutation by Resonating the Load

Class B – Self Commutation by Resonating the Load

Class C – Complementary Commutation

Class D – Auxiliary Commutation

Class E – Pulse Commutation

This commutation is mainly used in chopper and inverter circuits.

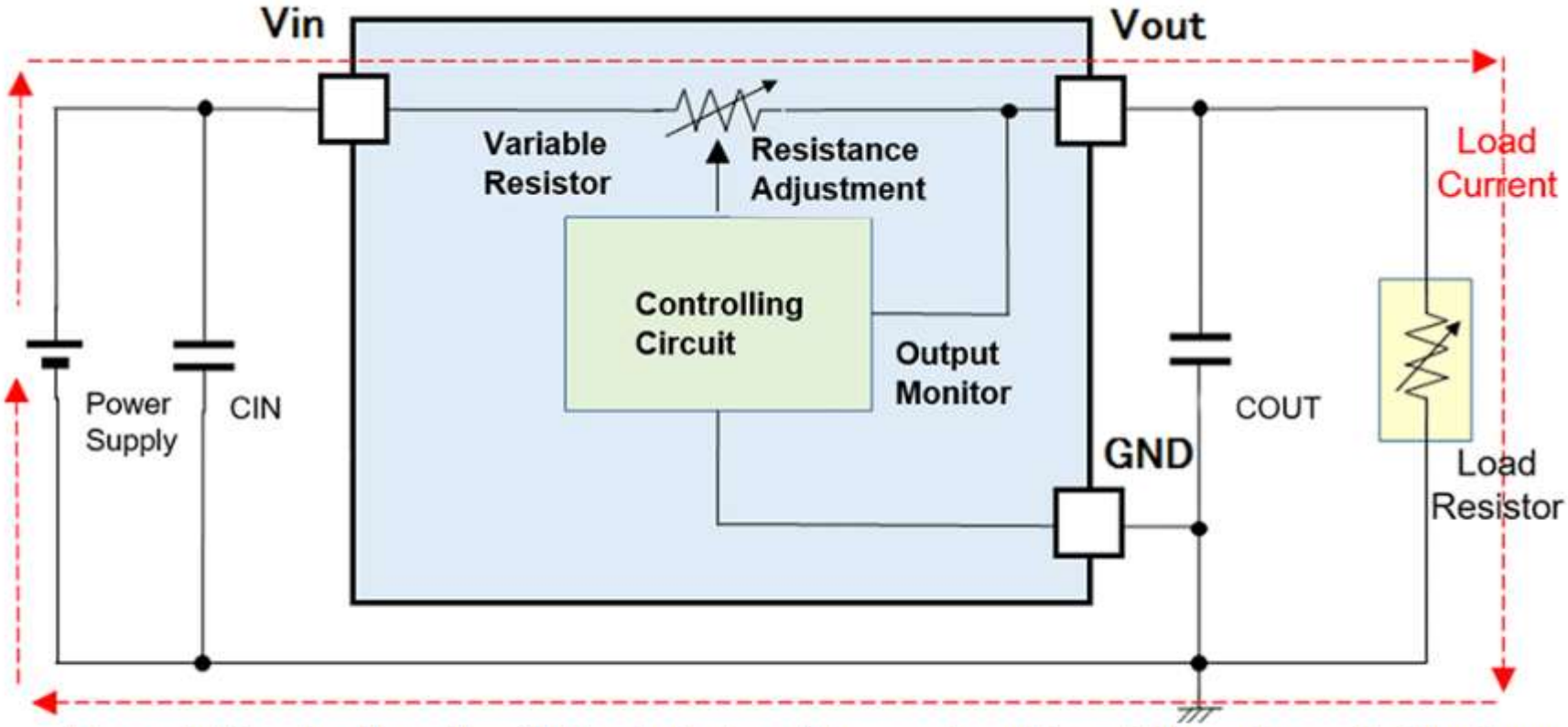
Linear Voltage Regulator

Electronic systems usually receive a power-supply voltage that is higher than the voltage required by the system's circuitry. For example, a 9 V battery might be used to power an amplifier that needs an input range of 0 to 5 V, In such case, we need to regulate the input power using a component that accepts a higher voltage and produces a lower voltage. One very common way to achieve this type of regulation is to incorporate a **linear voltage regulator**.

The simplest regulators are called 3-pin regulators, which output a stable fixed voltage just by inserting an input capacitor (CIN) between the VIN and the GND pins, and an output capacitor (COUT) between the VOUT and the GND pins.

The figure below illustrates that the controlling circuit supervises the output voltage and regulates the resistance value of the variable resistor so that the IC can output the set fixed voltage. For instance, if the input voltage (VIN) is fixed, a linear regulator can maintain a stable output voltage by keeping the ratio between the variable resistance value and the load resistance value fixed according to the changing rate of the load resistance value. The input voltage is divided by the two resistors, so linear regulators generate a lower output voltage than their input voltage.

The difference between the higher input voltage and lower output voltage will generate heat which is called waste heat. The current flowing inside the load resistor goes on to flow to the variable resistor, where the electricity is consumed with some heat generated.



The controlling circuit monitors Vout and adjusts resistance value of the variable resistor so that the linear regulator can generate a fixed output voltage.

SMPS-Switched Mode Power Supply [SMPS]

Various electrical and electronic loads are provided power using batteries. But batteries do not provide regulated power as they offer voltages of value either very high or very low. So, to obtain regulated dc output, SMPS is used.

Unlike linear power supply, which uses the standard linear method of voltage regulation, a switch mode power supply is a device that performs voltage regulation of unregulated signal by using **semiconductor switching methods**. It is considered to be highly efficient because it lessens power consumption thereby showing a decrease in the amount of heat dissipated. Thus, has replaced traditional linear power supply units.

SMPS includes a switching transistor (power MOSFET) for the purpose of voltage regulation. During operation, the transistor switches between on state and off state in a way that when it is on, it fully conducts current with the negligible voltage drop across it. While when it is off, it tries to completely block the flow of current. Thus, switching between on state (saturated) and off state (cut-off) occurs at high frequency, and in this way, the device acts as an ideal switch.

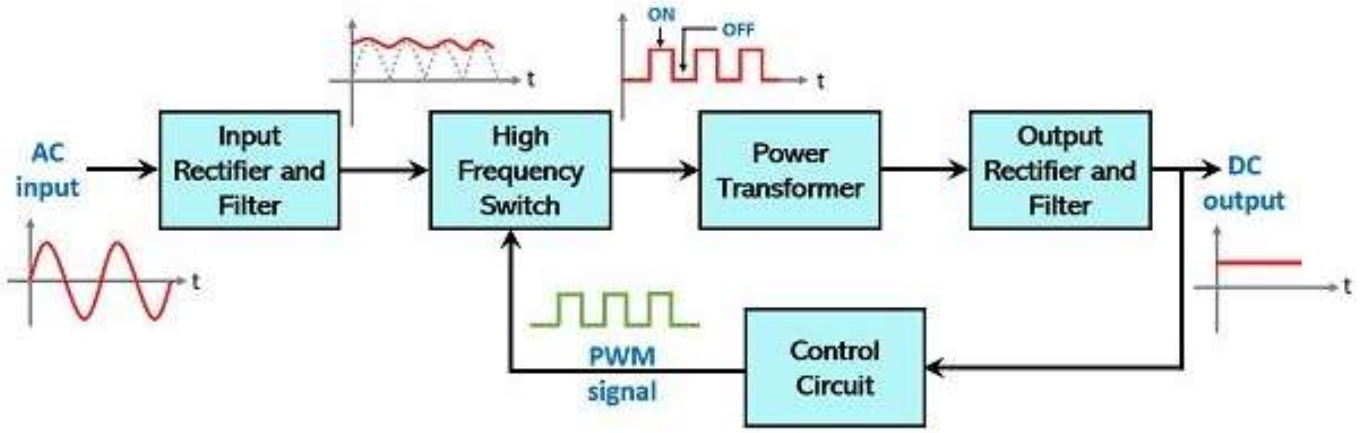
It is to be noted here that if the transformer operates at high frequency, so the device size is reduced. Hence, the overall size of the SMPS is small with less weight which is another advantage over linear power supplies.

Block Diagram and Working of SMPS

The major components that constitute SMPS are as follows:

1. Input rectifier and Filter (Diode rectifier and capacitor filter)
2. High-frequency switch (Power transistor or MOSFET)
3. Power transformer
4. Output rectifier and Filter (Diode rectifier and capacitor filter)
5. Control circuit (comparator and pulse width modulator)

Initially, the unregulated ac input signal from the source is provided to the input rectifier and filter circuit. Here the ac input signal is rectified to generate a dc signal and further smoothened to remove high-frequency noise component from it. The dc output (still in unregulated form) is fed to the power transistor that acts as a high-frequency switch.



Block diagram of Switch Mode Power Supply

Here the dc signal undergoes **chopping** (switching). This circuit acts as an ideal switch i.e., when the power transistor (chopper circuit) is in on state, current passes through it with negligible voltage drop, and dc signal is obtained at the output terminal of the transistor. However, under the off state of the power transistor, no current passes through it and leading to cause maximal voltage drop within it. Thus, at the output side, no voltage will be present.

Hence, according to the switching action of the power transistor dc voltage will be obtained at its output side. **The chopping frequency plays a crucial role in maintaining the desired dc voltage level**.

The obtained dc signal at the output of the chopper circuit is then fed to the primary winding of the high-frequency power transformer. Here the step-down transformer converts the high voltage signal into a low voltage level which is further provided as input to the output rectifier and filter unit. This simply filters out the unwanted residuals from the signal in order to provide a regulated dc signal as the output.

The control circuitry present here acts as the feedback circuit for the complete unit. This involves a comparator along with a pulse width modulator (PWM). The dc output from the rectifier and filter is fed to the control circuit where the error amplifier which acts as a comparator, compares the obtained dc voltage with the reference value.

If the dc output is greater than the reference value then the chopping frequency is to be decreased. The decrease in chopping frequency will reduce the output power and so the dc output voltage. However, if the dc output is less than the reference value then the chopping frequency is increased. When chopping frequency is raised then the dc output voltage will get increased.

The pulse width modulator in the above circuit is responsible for generating a fixed frequency pulse width modulated waveform whose duty cycle controls the chopping frequency.

Basically, the **duty ratio** is the ratio of on-time to the overall cycle time (i.e., on + off) time. Hence, by making necessary adjustments in the width of the pulses, the chopping frequency gets adjusted hence, regulated dc output can be obtained.

Advantages

1. It is highly efficient than linear power supplies. Typically, the efficiency of SMPS lies between 60% – 95%.
2. Due to the high-frequency operation of the device, the overall size is small and less bulky. Thus, is compact.
3. It is inexpensive because heat dissipation is less.
4. The obtained output voltage can be more or less than the supply input.

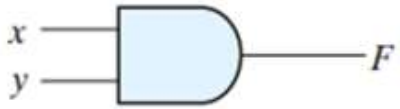
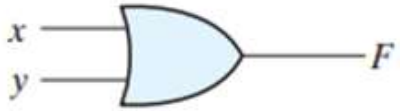
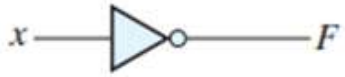
Disadvantages

1. The transient spike generation due to switching action is one of the major issues. This may lead to cause RF interference thus, isolation is mandatory.
2. The circuit is complex. Also, voltage regulation (controlling) is tricky.
3. Proper filtration is necessary to deal with noise and spikes.

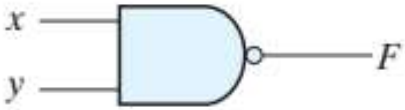
Applications of SMPS

The devices invented under the latest technologies require a highly efficient power supply which is offered by SMPS. Thus, it finds applications in various power amplifiers, personal computers, security and railway systems, television sets, motor drives, etc.

LOGIC GATES

Name	Graphic symbol	Algebraic function	Truth table
AND		$F = x \cdot y$	x y | F 0 0 | 0 0 1 | 0 1 0 | 0 1 1 | 1
OR		$F = x + y$	x y | F 0 0 | 0 0 1 | 1 1 0 | 1 1 1 | 1
Inverter / NOT		$F = x'$	x | F 0 | 1 1 | 0
Buffer		$F = x$	x | F 0 | 0 1 | 1

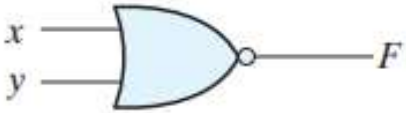
NAND



$F = (xy)'$

x	y	F
0	0	1
0	1	1
1	0	1
1	1	0

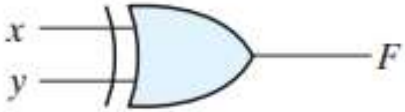
NOR



$F = (x + y)'$

x	y	F
0	0	1
0	1	0
1	0	0
1	1	0

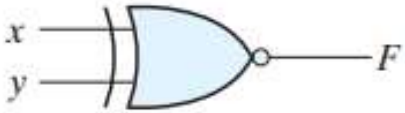
Exclusive-OR (XOR)



$F = xy' + x'y$
$= x \oplus y$

x	y	F
0	0	0
0	1	1
1	0	1
1	1	0

Exclusive-NOR or equivalence

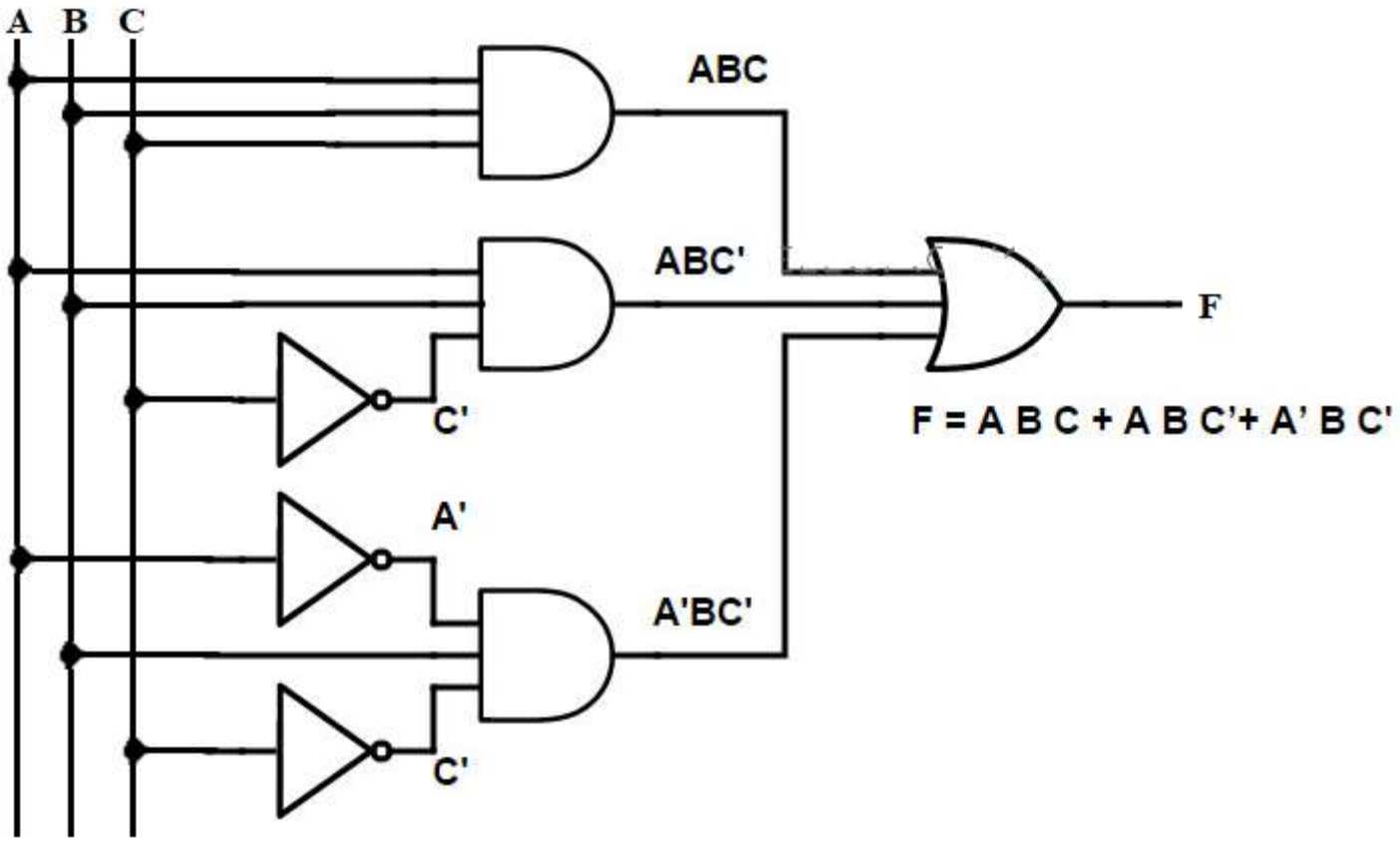


$F = xy + x'y'$
$= (x \oplus y)'$

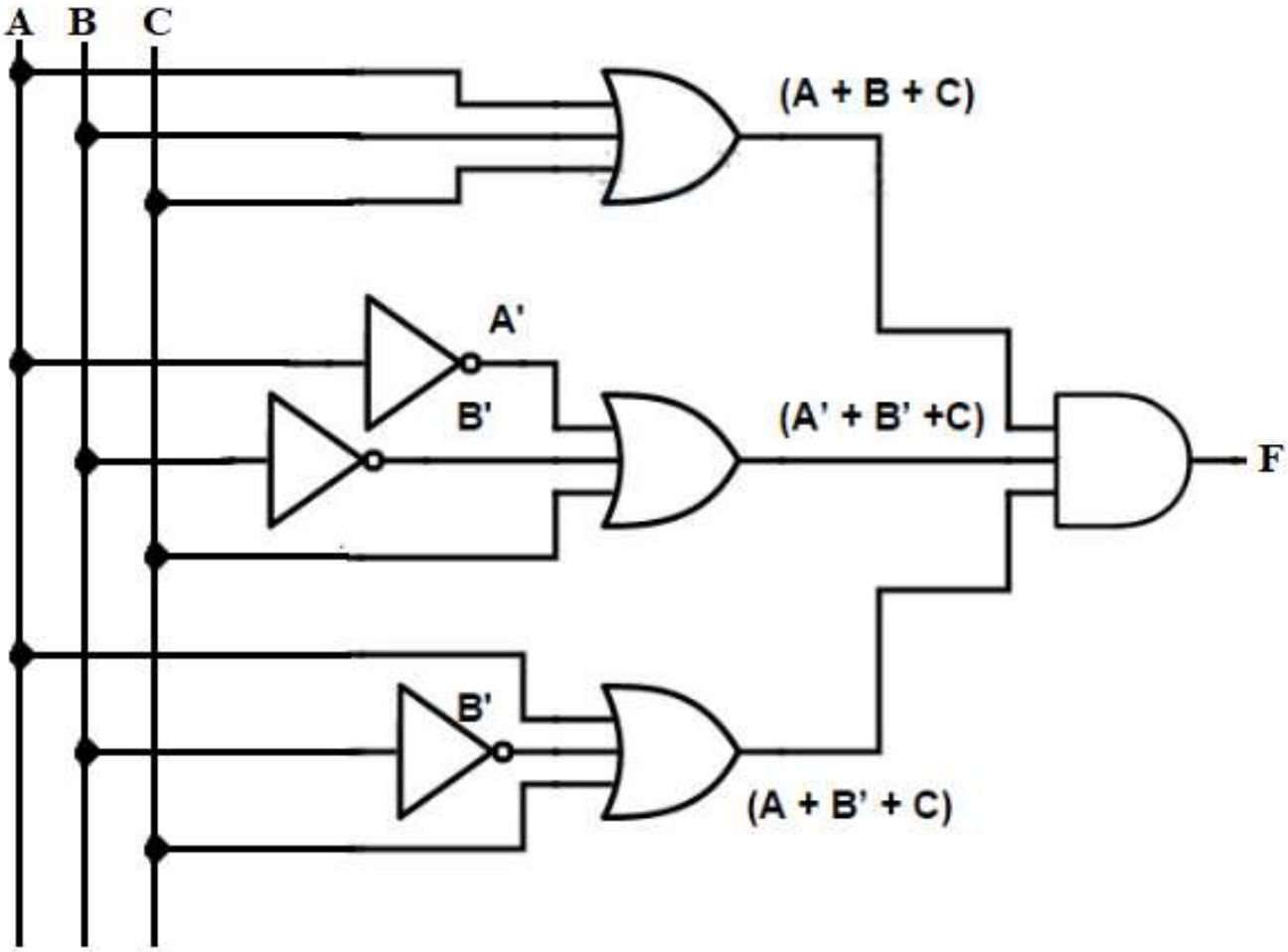
x	y	F
0	0	1
0	1	0
1	0	0
1	1	1

Realization [Implementation] of logic expression [Boolean Function] using basic logic gates

F = A B C + A B C'+ A' B C'



F = (A + B + C) (A' + B' +C) (A + B' + C)



SUM OF PRODUCTS [SOP] AND PRODUCT OF SUMS [POS]

Logical functions (Boolean expression) are generally expressed in terms of logical variables (inputs) in following forms. (Each input variable can have the value, either 0 or 1 only)

- **SUM OF PRODUCTS [SOP] Ex: AB'+ BC+C'D**
- **PRODUCT OF SUMS [POS] Ex: (A'+B') (B'+C) (C'+D)**

MINTERMS

A product term containing all the inputs of the functions in either complemented or uncomplemented form is called ***MINTERMS.***

Let us consider 3 variable (input) function. It has 2^3 all possible combinations. [A 'n' variable (input) function has 2^n all possible combinations]. Let the inputs are A, B, C and output is Y.

TRUTH TABLE-Example

	Inputs				Output
	A	B	C	MINTERMS	Y
0	0	0	0	A'B'C'	0
1	0	0	1	A'B'C	0
2	0	1	0	A'BC'	1
3	0	1	1	A'BC	1
4	1	0	0	AB'C'	1
5	1	0	1	AB'C	0
6	1	1	0	ABC'	1
7	1	1	1	ABC	0

- In minterms, 0 are assigned with bar letter and 1 are assigned with unbar letter.
- Within the row, all are multiplied (Product)
- Choose only the output 1.
- Add the minterms which having 1 output.
- In this example, we get Y= A'BC' + A'BC+ AB'C'+ ABC'. This expression is called canonical SOP form. [Standard SOP form]
- Each input is assigned with it equivalent decimal value. In the truth table, only the output Y= 1 is chosen, it corresponding input's decimal values are stated as below.

$$\mathbf{Y= \sum m\ (2,3,4,6)}$$

MAXTERMS

A sum term containing all the inputs of the functions in either complemented or uncomplemented form is called ***MAXTERMS.*** Let us consider the same truth table.

	Inputs				Output
	A	B	C	MAXTERMS	Y
0	0	0	0	(A+B+C)	0
1	0	0	1	(A+B+C')	0
2	0	1	0	(A+B'+C)	1
3	0	1	1	(A+B'+C')	1
4	1	0	0	(A'+B+C)	1
5	1	0	1	(A'+B+C')	0
6	1	1	0	(A'+B'+C)	1
7	1	1	1	(A'+B'+C')	0

- In maxterms, 1 are assigned with bar letter and 0 are assigned with unbar letter.
- Within the row, all are summed (Added)
- Choose only the output 0.
- Product the maxterms which having 0 output.
- In this example, we get Y= (A+B+C) (A+B+C') (A'+B+C') (A'+B'+C'). This expression is called canonical POS form. [Standard POS form]
- Each input is assigned with it equivalent decimal value. In the truth table, only the output Y= 0 is chosen, it corresponding input's decimal values are stated as below.

$$\mathbf{Y= \prod M\ (0,1,5,7)}$$

Note: Minterms and Maxterms are complement with each other.

1. For the Boolean function given below, obtain the (i) canonical SOP form (ii) canonical POS form.

Y(A,B,C)= A+B'C

= AXX+ XB'C

= AB'C'+ AB'C+ ABC'+ ABC+A'B'C+ AB'C

[Remove the common term; Since A+A=A]

Y= AB'C'+ AB'C+ ABC'+ ABC+A'B'C [Canonical SOP form]

100 101 110 111 001

(m_4 m_5 m_6 m_7 m_1)

Y= $\sum$m (1,4,5,6,7)

Y= $\prod$M (0,2,3) **[** Minterms and Maxterms are complement with each other**]**

M_0 M_2 M_3

000 010 011

Y= (A+B+C) (A+B'+C) (A+B'+C') [Canonical POS form]

Karnaugh maps/ K-map

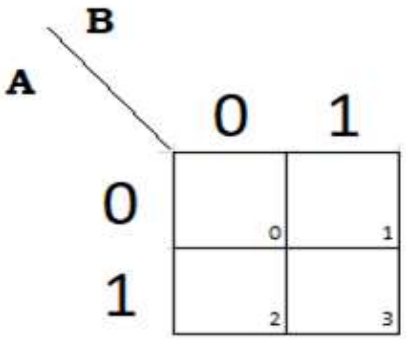
If the number of input variables is more than 2, its very difficult to minimize the Boolean function by Boolean algebra. Karnaugh maps/ K map overcomes this difficulty.

Karnaugh maps/ K map

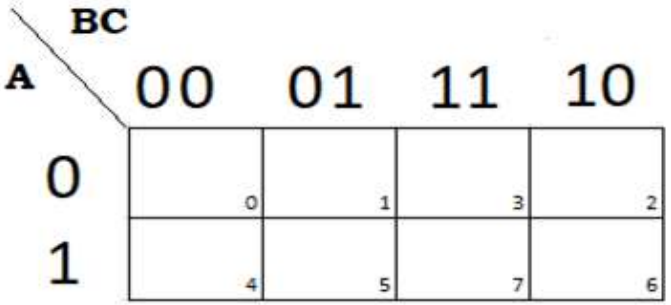
- A visual way to simplify logic expressions
- It gives the most simplified form of the expression
- K-Maps are a graphical technique used to simplify a logic equation.
- K-Maps can be used for any number of input variables, BUT are only practical for **two, three, and four variables**

General Structure of K-Map

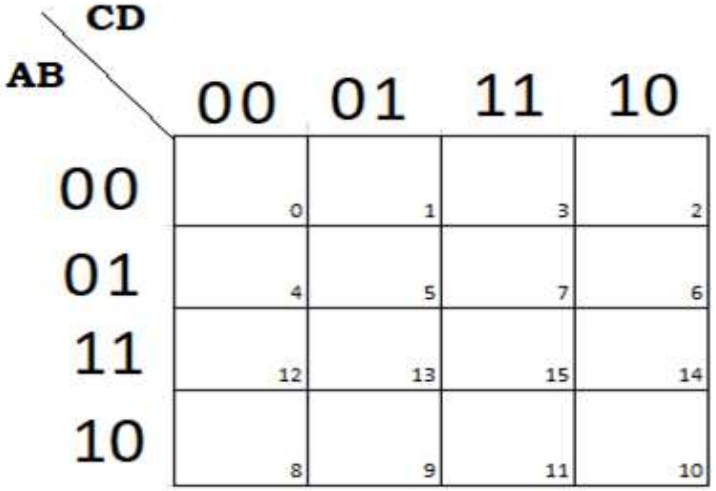
Two variable (Inputs- A,B)



Three variable (Inputs- A,B,C)



Four variable (Inputs- A,B,C,D)



Procedure to minimize Boolean expression by K-map:

1. We have to cheek, number of variables (Inputs).

(i)If the maximum number in the Boolean expression is ≤3, it is 2 variable function.

(ii)If the maximum number in the Boolean expression is ≤7, it is 3 variable function.

(iii)If the maximum number in the Boolean expression is ≤15, it is 4 variable function.

Note: Some times, in the question itself, inputs will be given.

Ex: Y(A,B,C)=∑(0,4,5,7)

2. Check the given question is Minterms or Maxterms. If ∑ is given, it is Minterms. In K-map, for the given decimal location, we have to enter 1. In remaining location, we have to enter 0.

If ∏ is given, it is Maxterms. In K-map, for the given decimal location, we have to enter 0. In remaining location, we have to enter 1.

3. Draw the K-map and fill it. (use step 1 & 2)

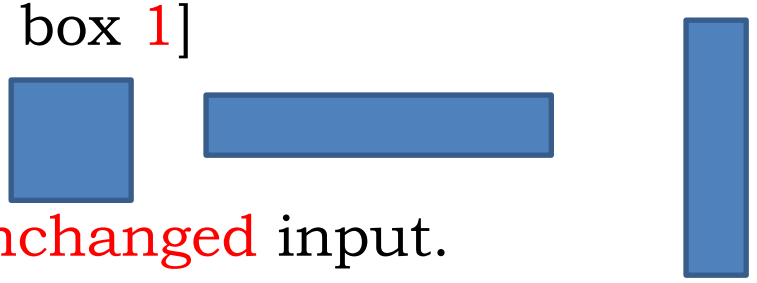
4 (a) Solution Procedure for SOP method

(i) We have box ALL the 1.

(ii) Larger the box, smaller the equation. Since all are minimization problem, we have chose larger box.

(iii) The number of 1's inside the box must be 2^n. [ie we have to try boxing 16 , if not possible we have to try boxing 8, if not possible we have to try boxing 4, if not possible we have to try boxing 2, if not possible we have to box 1]

(iv) The shape of the box must be square or rectangular. ie



(v) For each box, we have to find unchanged input. For that, we have see K-map from right to left, then bottom to top. The unchanged input within the box should be **product**. The product of one box should be sum with next box.[In input, 0 are assigned with bar letter and 1 are assigned with unbar letter]

(vi) Overlapping is allowed to make larger box.

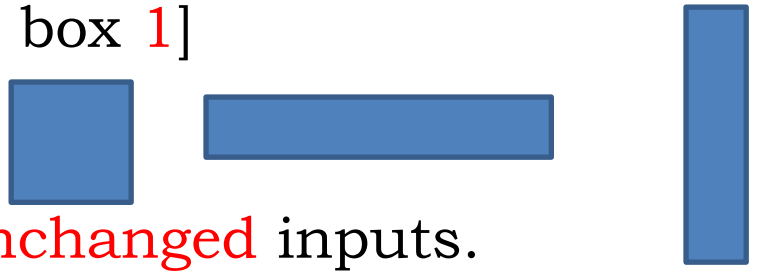
4 (b) Solution Procedure for POS method

(i) We have box ALL the 0.

(ii) Larger the box, smaller the equation. Since all are minimization problem, we have chose larger box.

(iii) The number of 0's inside the box must be 2^n. [ie we have to try boxing 16 , if not possible we have to try boxing 8, if not possible we have to try boxing 4, if not possible we have to try boxing 2, if not possible we have to box 1]

(iv) The shape of the box must be square or rectangular. ie



(v) For each box, we have to find unchanged inputs. For that, we have see K-map from right to left, then bottom to top. The unchanged input within the box should be **summed**. The sum of one box should be product with next box.[In input, 1 are assigned with bar letter and 0 are assigned with unbar letter]

(vi) Overlapping is allowed to make larger box.

K-MAP-SOP METHOD

1 Simply the following Boolean expression

$Y(A,B,C) = \sum m(1,2,3,6,7)$

Method 1: Boolean Algebra

Binary of minterms: 001, 010, 011, 110, 111

$Y = A'B'C + A'BC' + A'BC + ABC' + ABC$

$Y = A'B'C + A'B[C' + C] + AB[C' + C]$

$Y = A'B'C + A'B + AB$

$Y = A'B'C + B[A + A']$

$Y = A'B'C + B$

$Y = A'C + B$

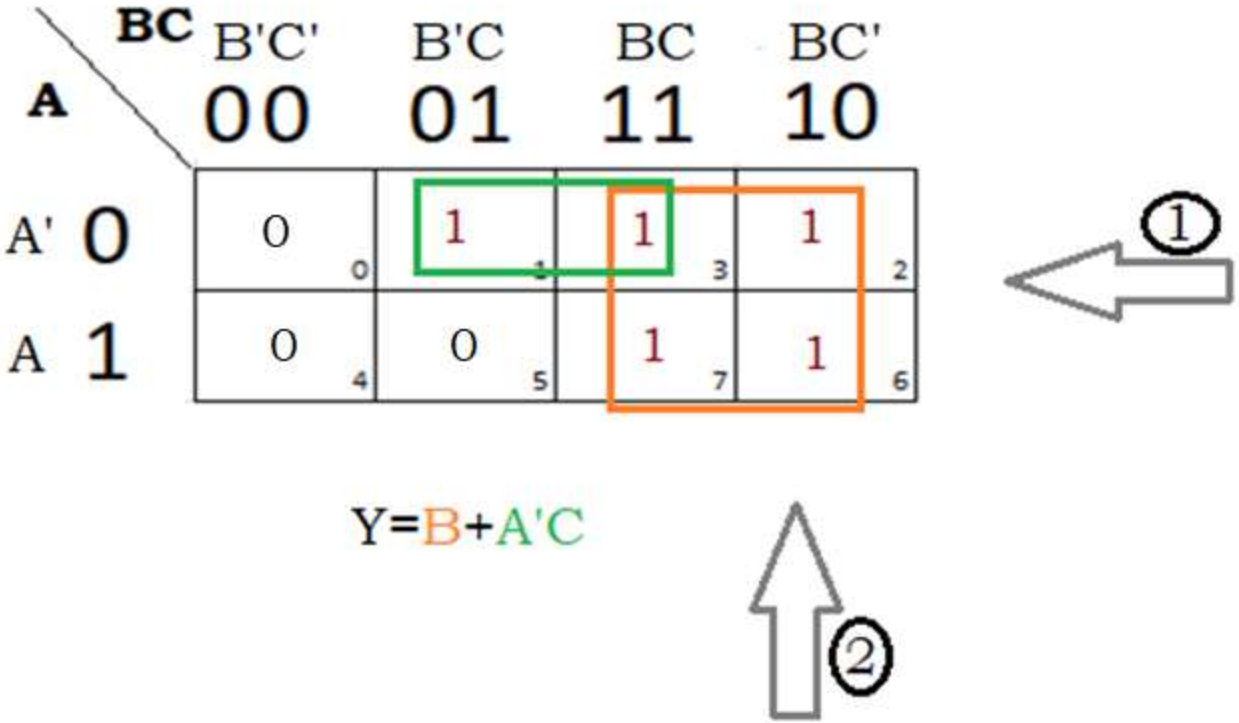
$B + B'X = B + X$

1 Simply the following Boolean expression

$Y(A,B,C) = \sum m(1,2,3,6,7)$

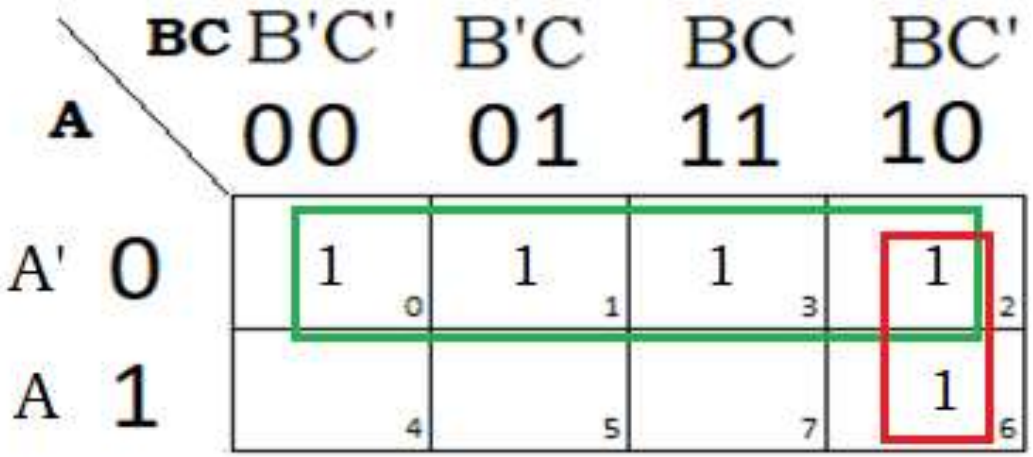
Method 2: K-MAP

Three variable (Inputs- A,B,C)



2 Simply the following Boolean expression

$Y(A,B,C) = \sum m(0,1,2,3,6)$

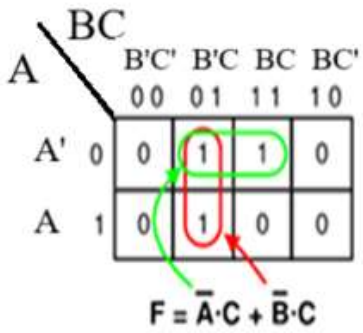


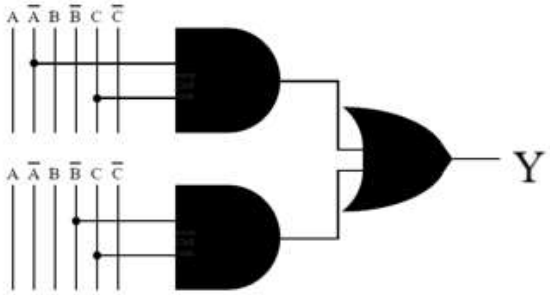
$Y = A' + BC'$

3 Variable K-Maps Examples (SOP)

Simply the Boolean function and implement it using logic Gates

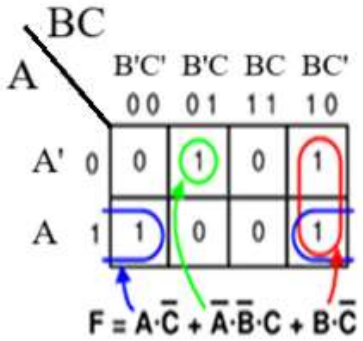
$$Y(A,B,C) = \sum m(1,3,5)$$

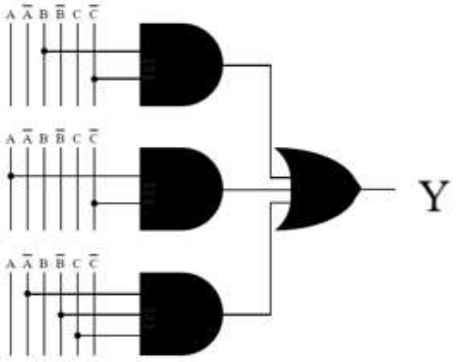




Simply the Boolean function and implement it using logic Gates

$$Y(A,B,C) = \sum m(1,2,4,6)$$

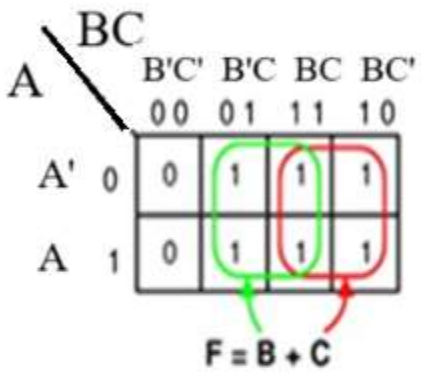


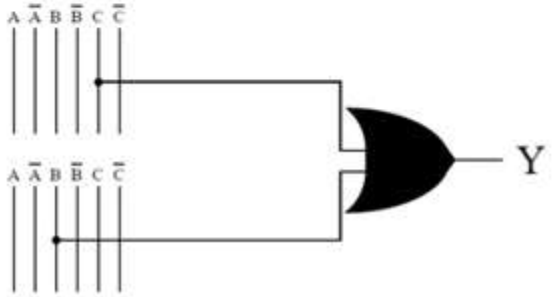


3 Variable K-Maps Examples (SOP)

Simply the Boolean function and implement it using logic Gates

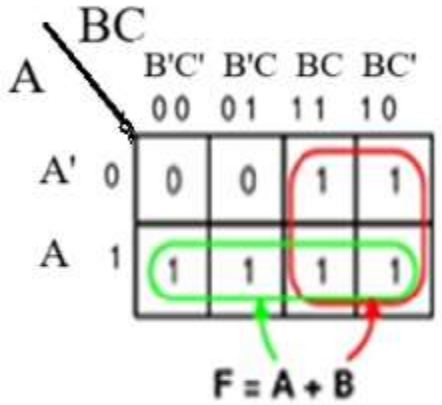
$$Y(A,B,C) = \sum m(1,2,3,5,6,7)$$

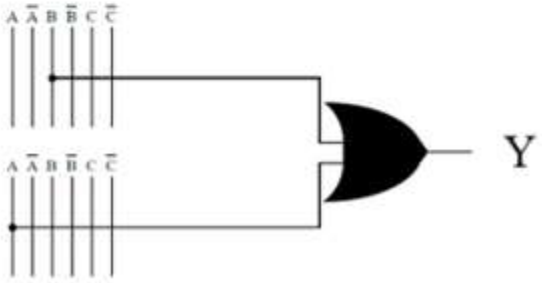




Simply the Boolean function and implement it using logic Gates

$$Y(A,B,C) = \sum m(2,3,4,5,6,7)$$

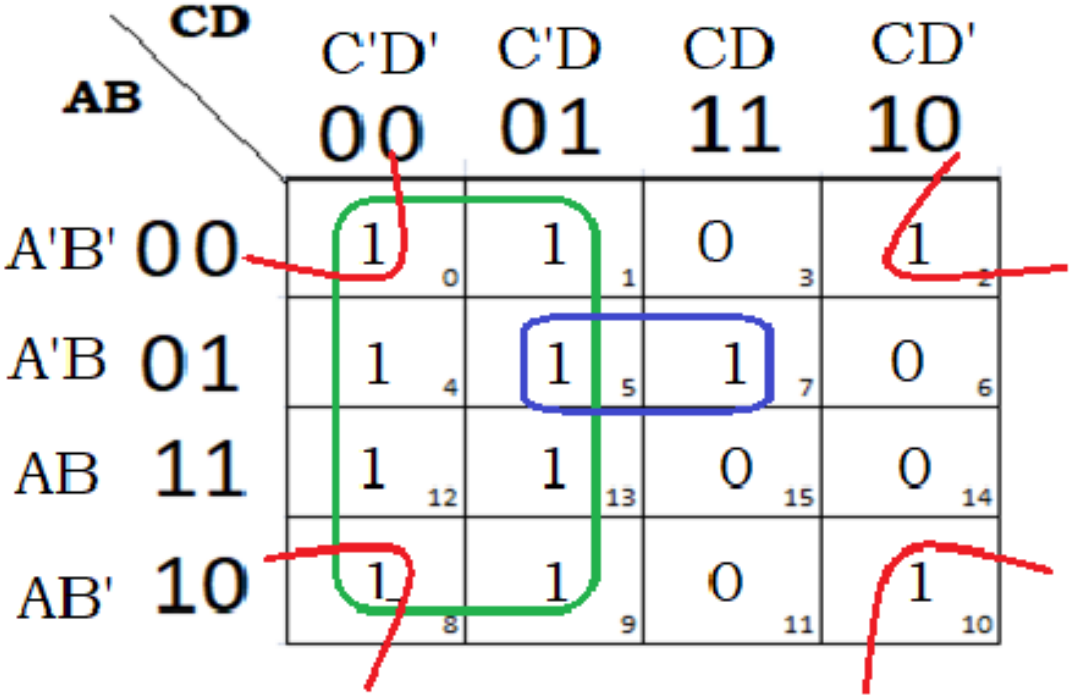




4 Variable K-Map (SOP)

3. Simply the following Boolean expression and implement it using logic gates

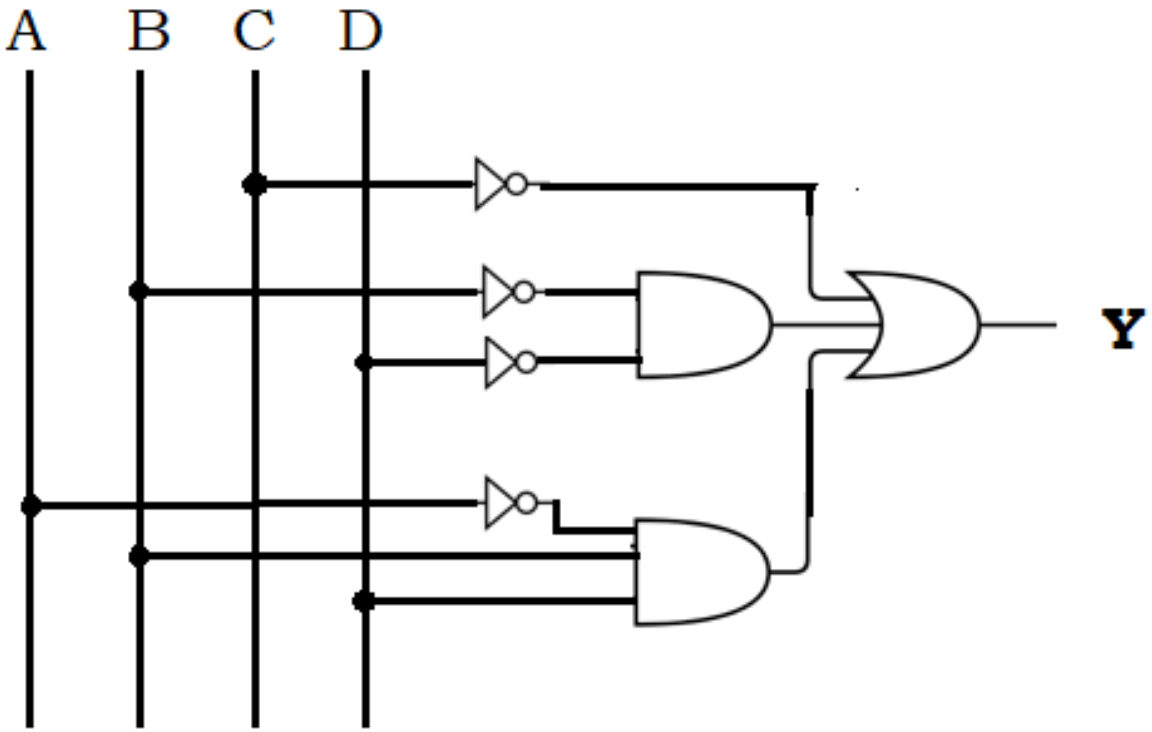
$Y(A,B,C,D) = \sum m(0,1,2,4,5,7,8,9,10,12,13)$



$Y = C' + B'D' + A'BD$

Implementation

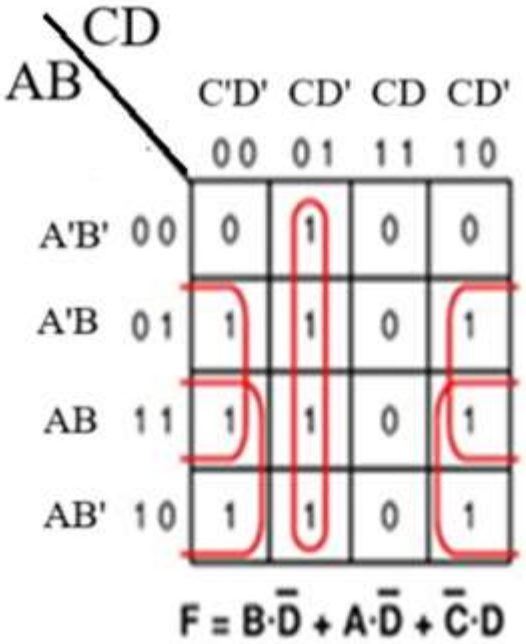
Y=C'+B'D'+A'BD

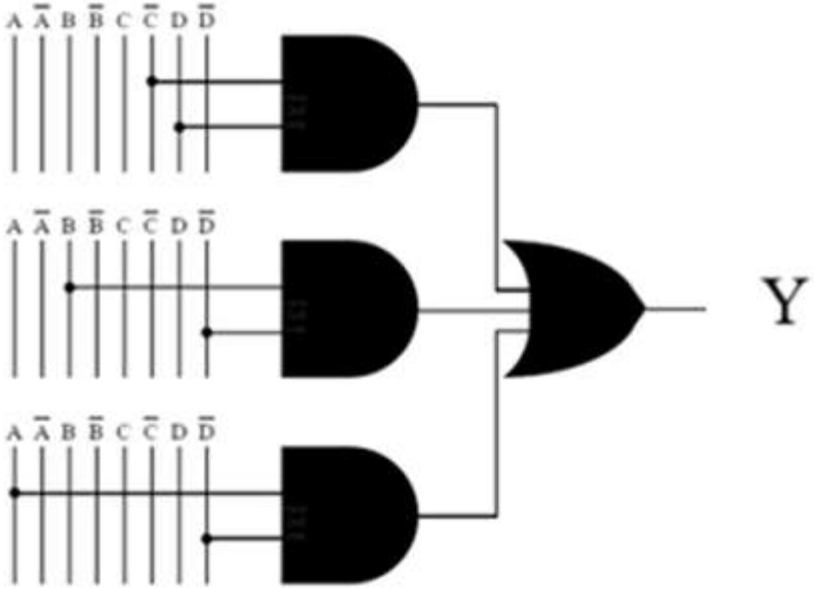


4 Variable K-Maps Examples (SOP)

Simply the Boolean function and implement it using logic Gates

$$Y(A,B,C,D) = \sum m(1,4,5,6,8,9,10,12,13,14)$$

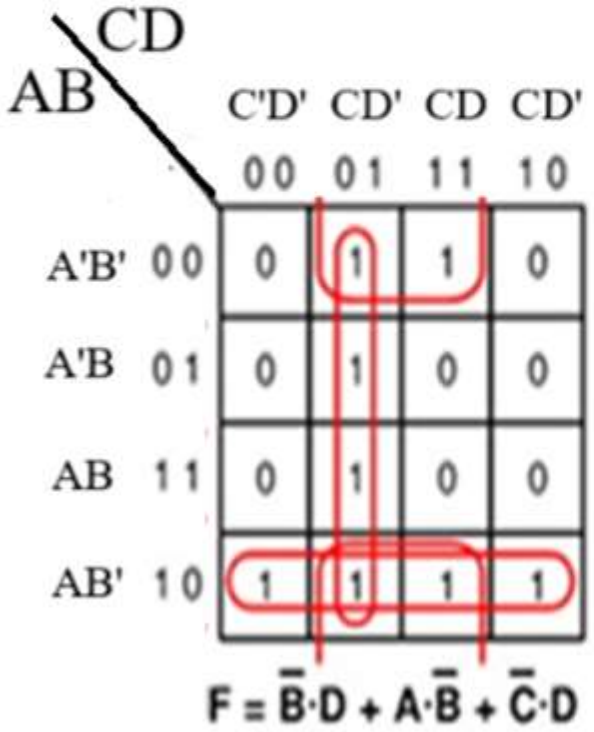


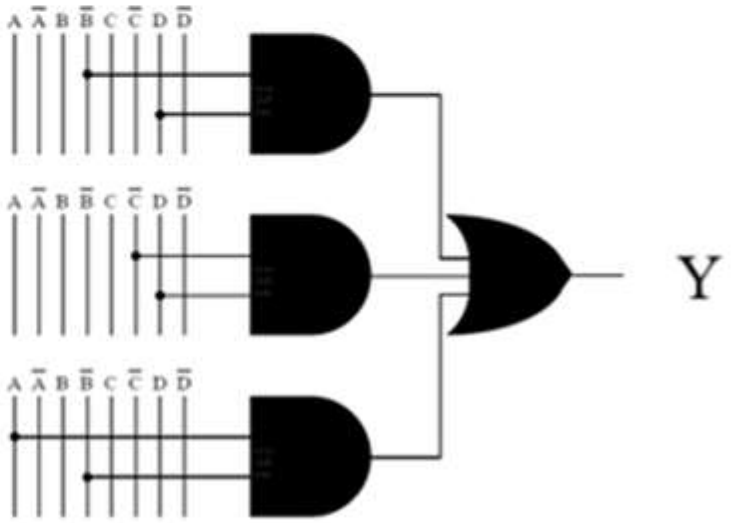


4 Variable K-Maps Examples (SOP)

Simply the Boolean function and implement it using logic Gates

$$Y(A,B,C,D) = \sum m(1,3,5,8,9,10,11,13)$$

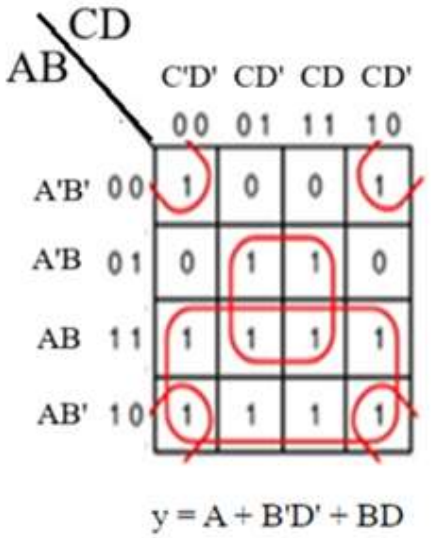




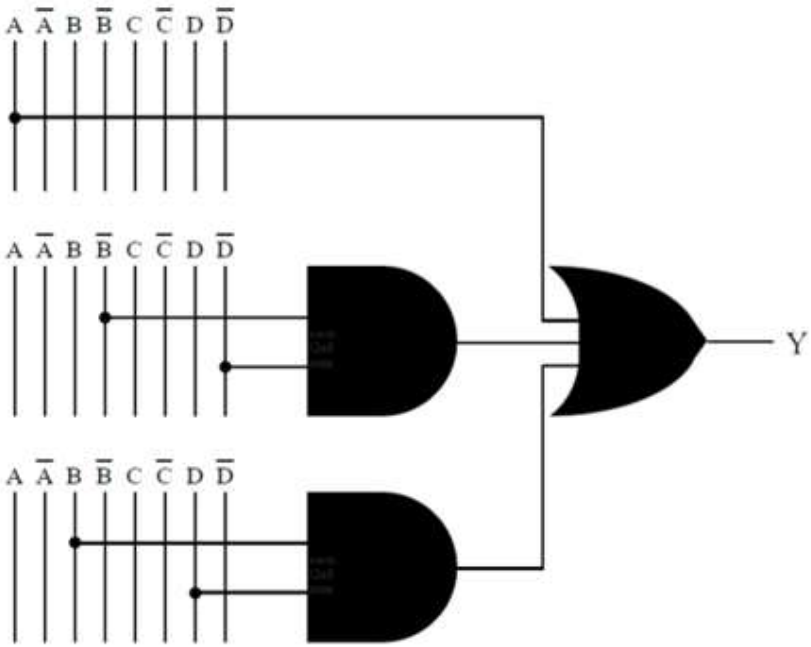
4 Variable K-Maps Examples (SOP)

Simply the Boolean function and implement it using logic Gates

$$Y(A,B,C,D) = \sum m\,(0,2,5,7,8,9,10,11,12,13,14,15)$$



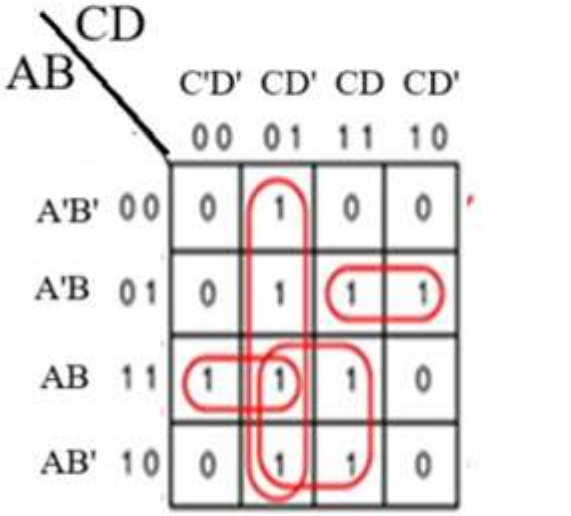
y = A + B'D' + BD



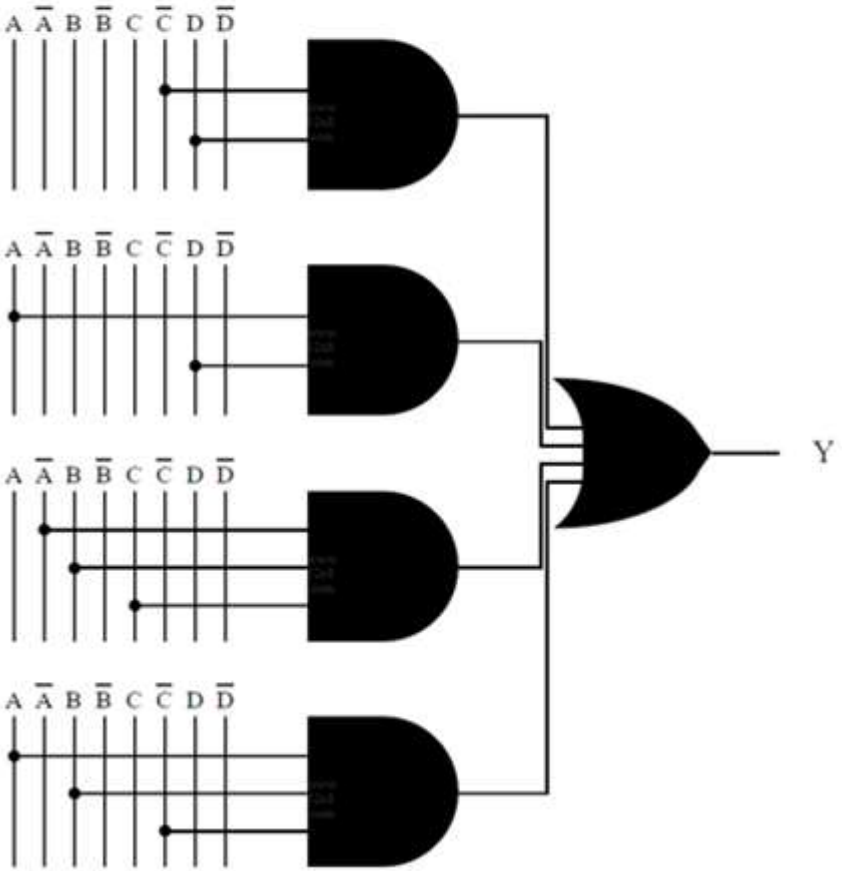
4 Variable K-Maps Examples (SOP)

Simply the Boolean function and implement it using logic Gates

$$Y(A,B,C,D) = \sum m(1,5,6,7,9,11,12,13,15)$$



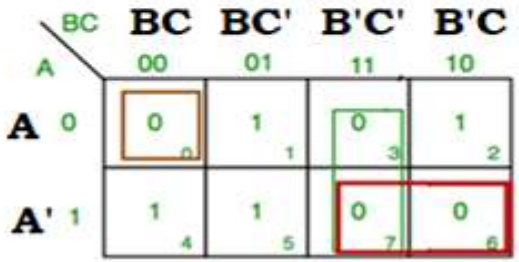
$$F = \bar{C}\cdot D + A\cdot B\cdot \bar{C} + \bar{A}\cdot B\cdot C + A\cdot D$$



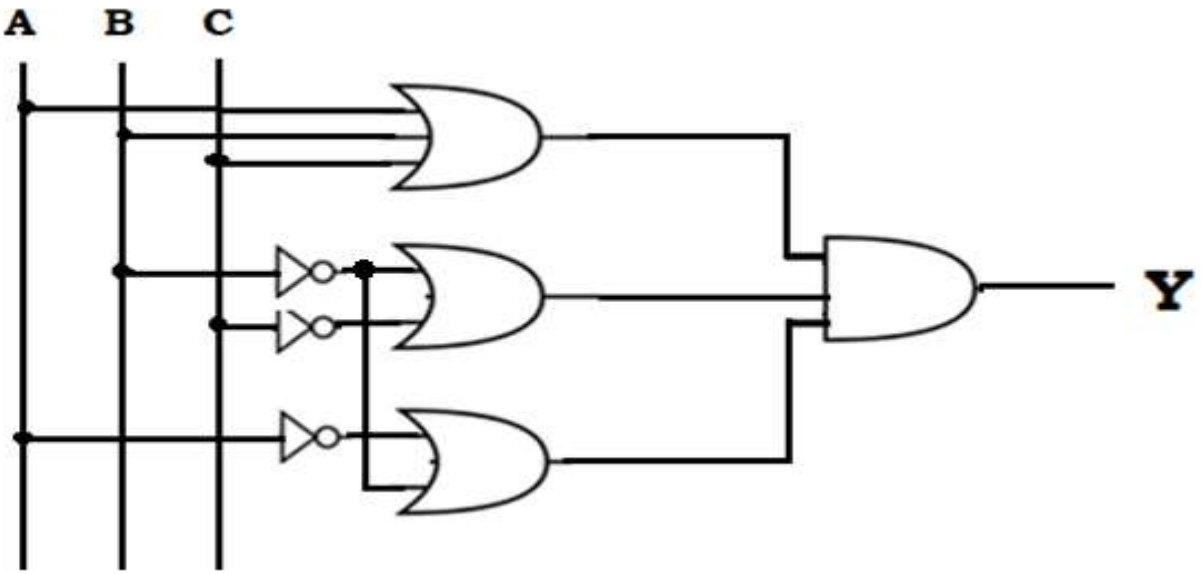
K-MAP-POS METHOD

1. Simply the following Boolean expression by POS method and implement it using logic gates

$Y(A,B,C) = \prod m(0,3,6,7)$



$Y = (A+B+C).(B'+C').(A'+B')$



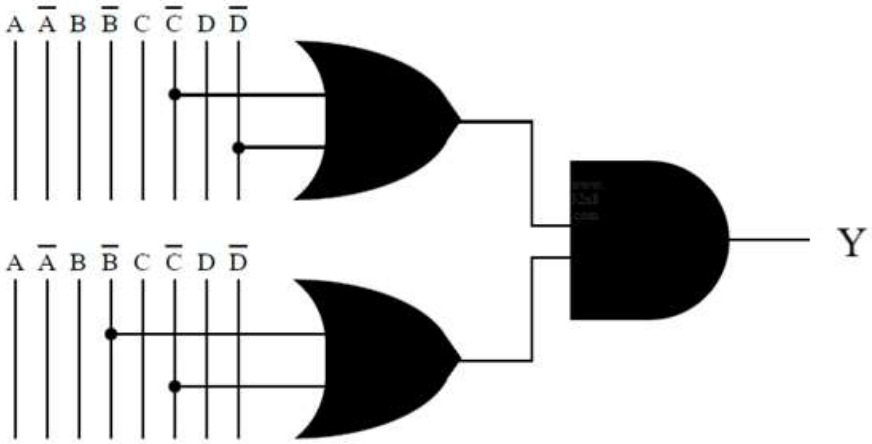
2

Simply the Boolean function by POS method and implement it using logic Gates

$Y(A,B,C,D) = \sum m(0,1,2,4,5,8,9,10,12,13)$

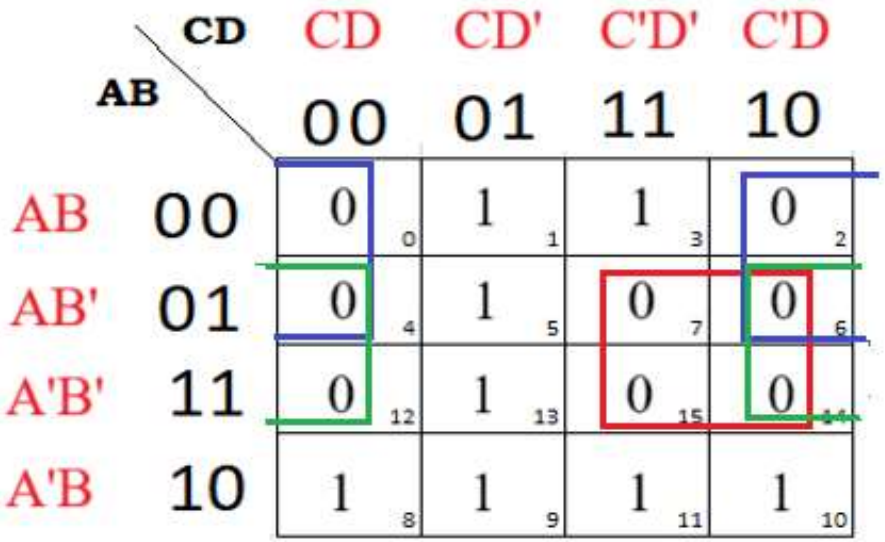
AB \ CD	CD (00)	CD' (01)	C'D' (11)	C'D (10)
AB (00)	1 (0)	1 (1)	0 (3)	1 (2)
AB' (01)	1 (4)	1 (5)	0 (7)	0 (6)
A'B' (11)	1 (12)	1 (13)	0 (15)	0 (14)
A'B (10)	1 (8)	1 (9)	0 (11)	1 (10)

$Y = (B'+C') * (C'+D')$



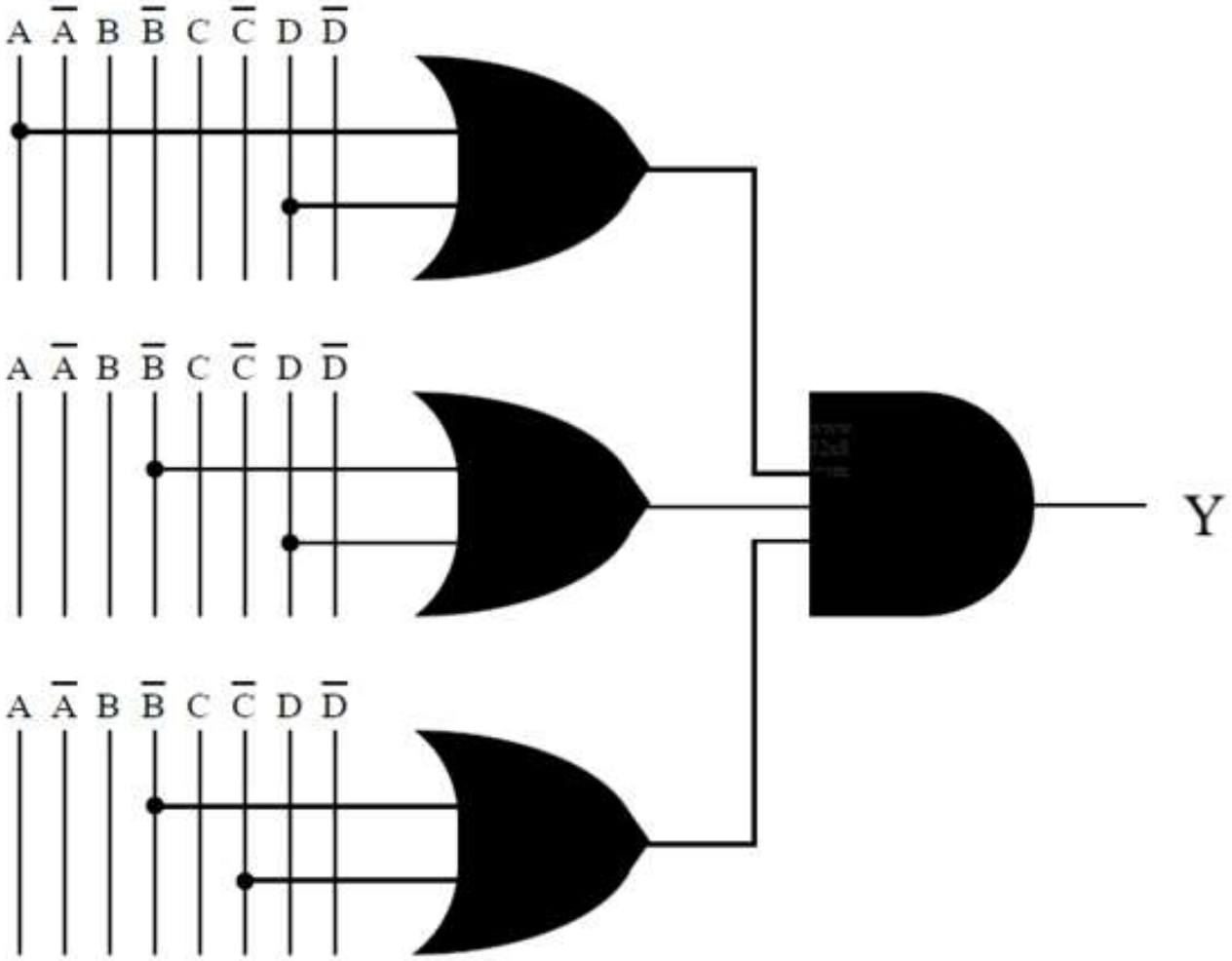
3. Simply the Boolean function by POS method and implement it using logic Gates.

Y= Π M (0,2,4,6,7,12,14,15)

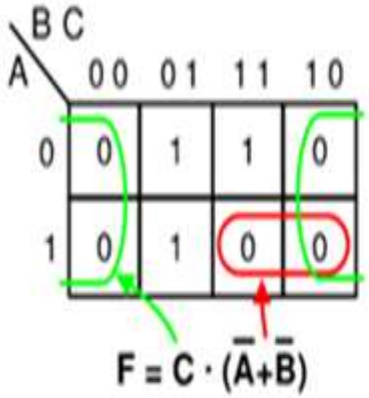


Y= (A+D)* (B'+D) *(B'+C')

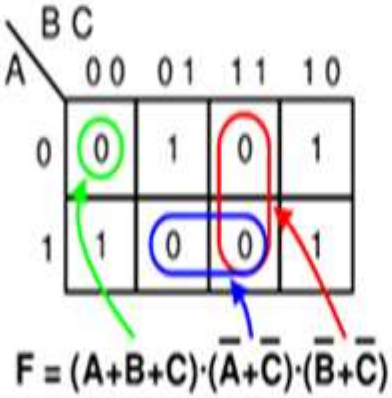
Implementation it using logic Gates



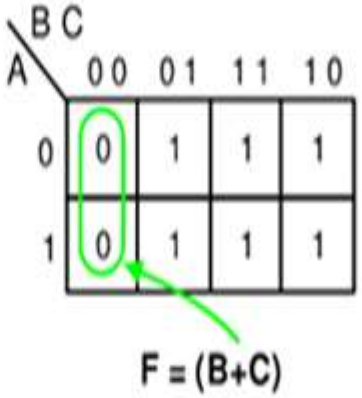
3,4-Variable K-Maps Examples [POS]



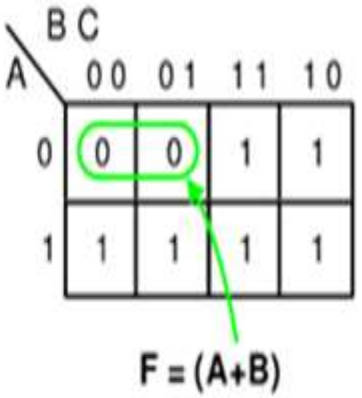
$F = C \cdot (\bar{A}+\bar{B})$



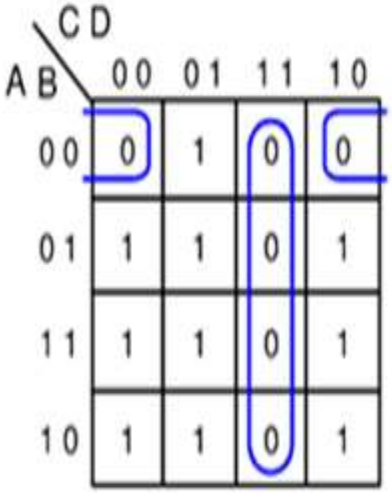
$F = (A+B+C)\cdot(\bar{A}+\bar{C})\cdot(\bar{B}+\bar{C})$



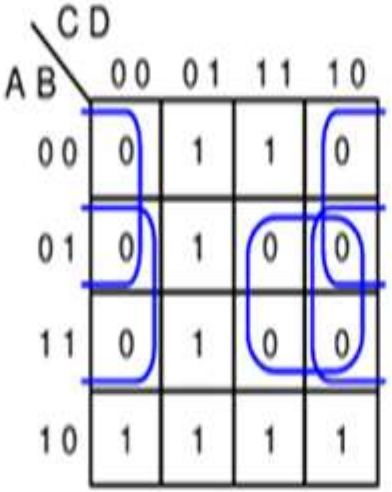
$F = (B+C)$



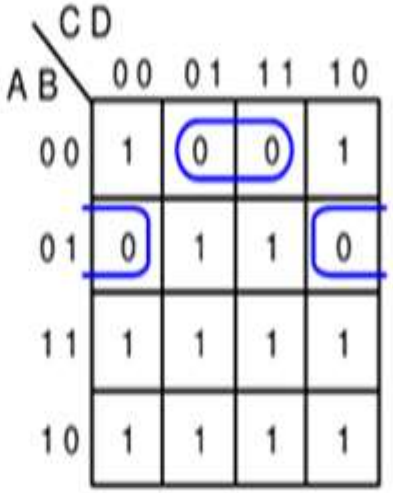
$F = (A+B)$



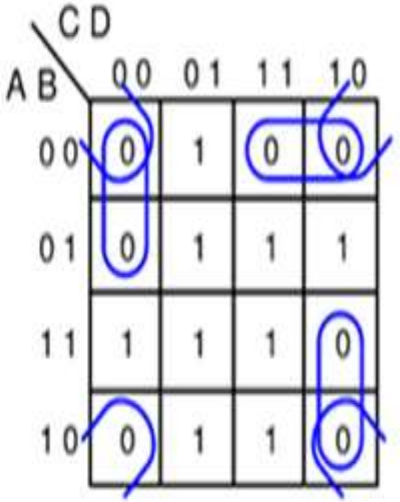
$F = (A+B+D)\cdot(\bar{C}+\bar{D})$



$F = (A+D)\cdot(\bar{B}+D)\cdot(\bar{B}+\bar{C})$



$F = (A+B+\bar{D})\cdot(A+\bar{B}+D)$



$F = (A+C+D)\cdot(A+B+\bar{C})\cdot(\bar{A}+\bar{C}+D)\cdot(B+D)$

UNIVERSITY QUESTIONS

1

UQ June2023

Simplify the following Boolean expressions using k-map and implement the simplified expressions using logic gates.

(i) $Y(A,B,C,D)=\Sigma m(1,5,6,7,9,11,12,13,15)$ 9

(ii) $Y(A,B,C,D)=\Pi m(0,3,6,7)$ 6

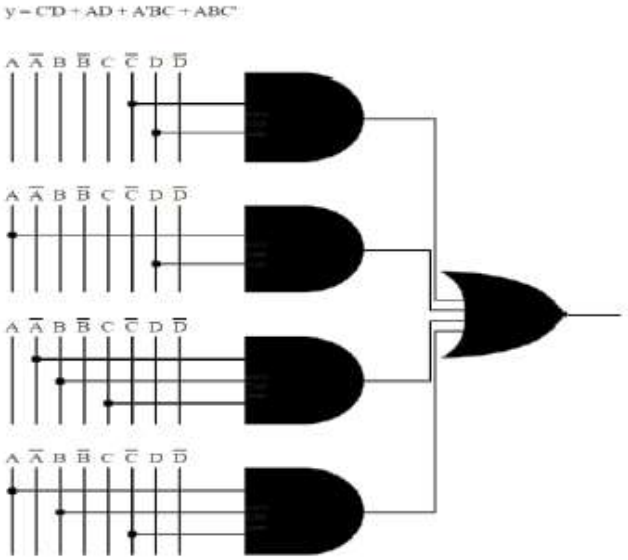
In question, it is not mentioned SOP or POS method. So students can solve by any method

(i) $Y(A,B,C,D)=\Sigma m(1,5,6,7,9,11,12,13,15)$

AB \ CD	00	01	11	10
00	0	1	0	0
01	0	1	1	1
11	1	1	1	0
10	0	1	1	0

$y = C'D + AD + A'BC + ABC'$

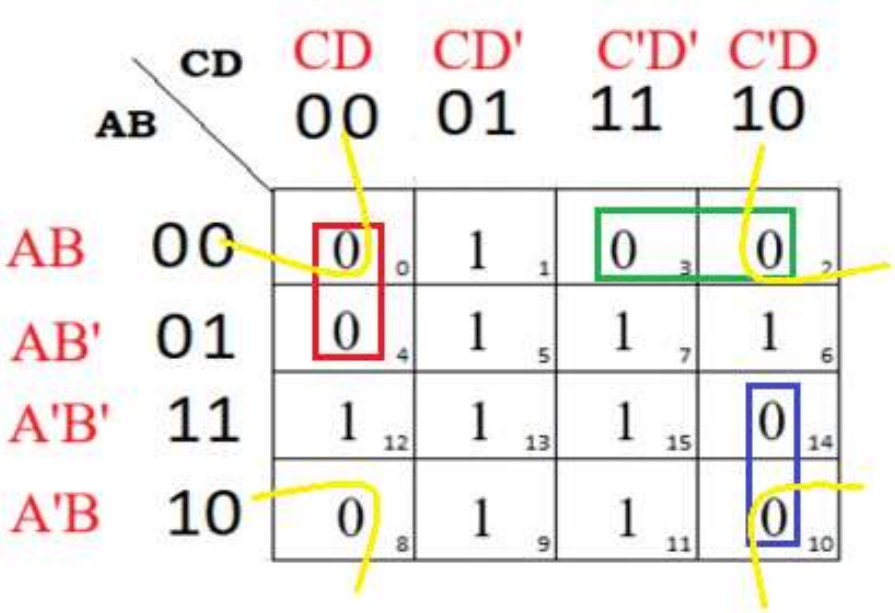
(6M)

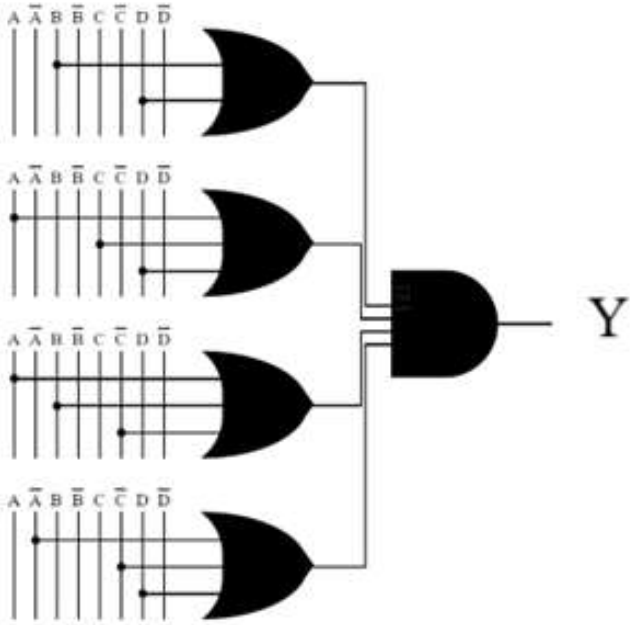


(3M)

(i) $Y(A,B,C,D)=\Sigma m(1,5,6,7,9,11,12,13,15)$

Same problem, POS method



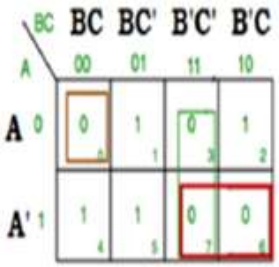


Y= (B+D) *(A+C+D)* (A+B+C')* (A'+C'+D)

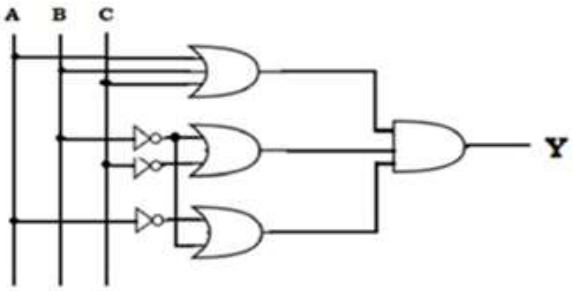
In question, it is not mentioned SOP or POS method. So students can solve by any method

ii. POS Method

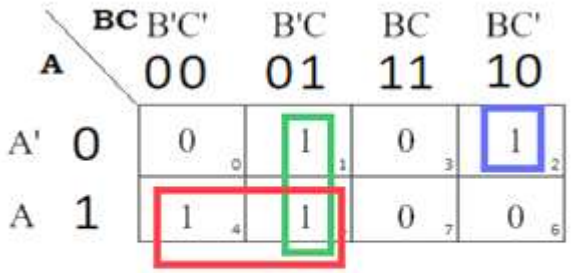
$Y(A,B,C) = \prod m(0,3,6,7)$



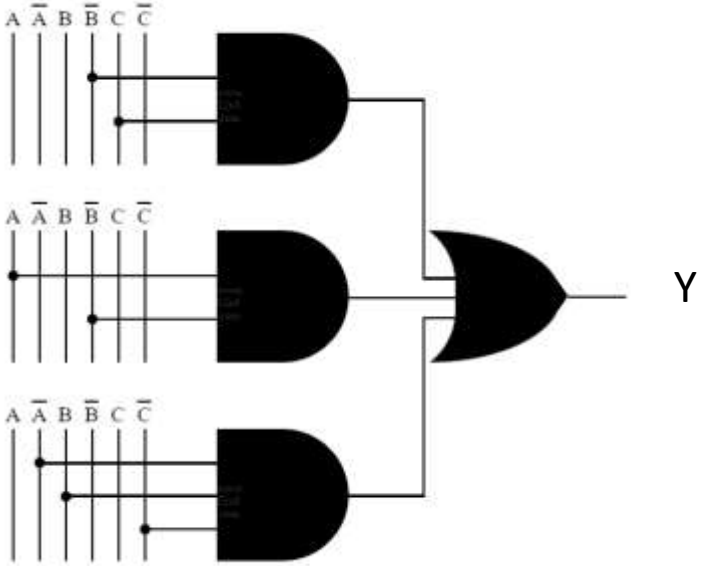
$Y = (A+B+C).(B'+C').(A'+B')$



Same Problem, SOP method



$y = B'C + AB' + A'BC'$



2

UQ June 2022 & May 2023

Simplify the following Boolean expressions using k-map and implement the simplified expressions using logic gates.

$Y(A,B,C,D)=\sum_m(0,1,2,4,5,7,8,9,10,12,13)$

$Y(A,B,C,D)=\pi_M(3,6,11,14,15)$

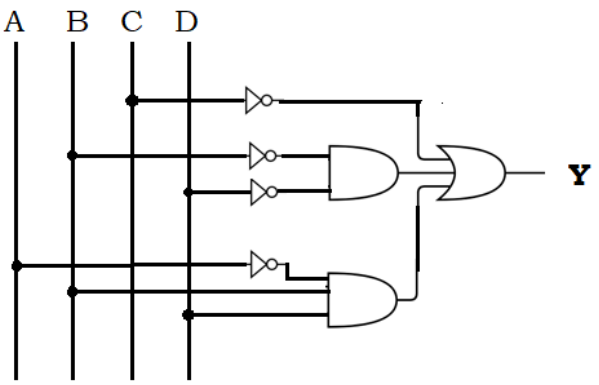
Y (A,B,C,D)= ∑m (0,1,2,4,5,7,8,9,10,12,13)

AB \ CD	C'D' (00)	C'D (01)	CD (11)	CD' (10)
A'B' (00)	1 (0)	1 (1)	0 (3)	1 (2)
A'B (01)	1 (4)	1 (5)	1 (7)	0 (6)
AB (11)	1 (12)	1 (13)	0 (15)	0 (14)
AB' (10)	1 (8)	1 (9)	0 (11)	1 (10)

Y=C'+B'D'+A'BD

Implementation

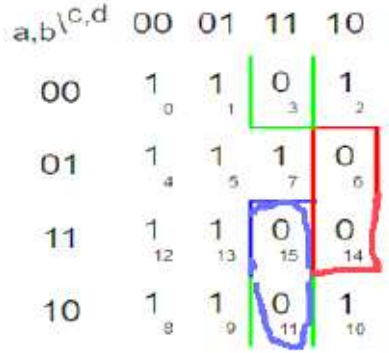
Y=C'+B'D'+A'BD



$$Y(A,B,C,D) = \pi_M(3,6,11,14,15)$$

a,b\c,d	00	01	11	10
00	1 (0)	1 (1)	0 (3)	1 (2)
01	1 (4)	1 (5)	1 (7)	0 (6)
11	1 (12)	1 (13)	0 (15)	0 (14)
10	1 (8)	1 (9)	0 (11)	1 (10)

(b'+c'+d) * (b+c'+d') * (a'+b'+c')

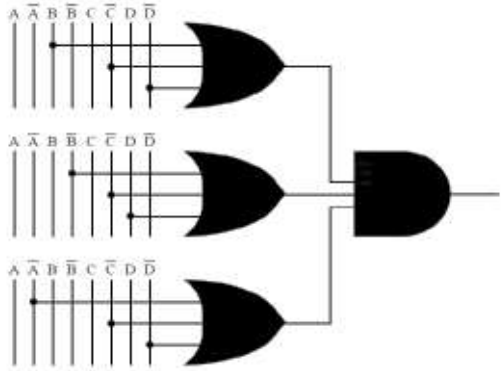


(b + c' + d') (b' + c' + d) (a' + c' + d')

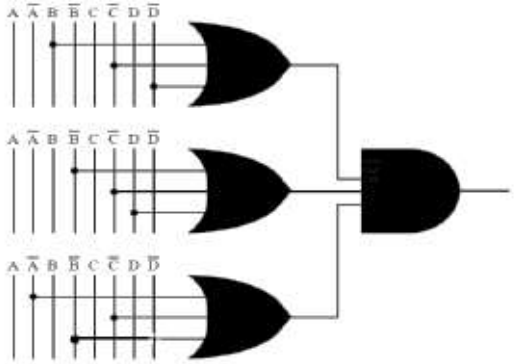
(3M)

Note: Two Expressions are coming for the different grouping. If anyone answer is there, give mark.

(b'+ c + d) * (b+c+d') * (a'+c'+d')



(b'+ c + d) * (b+c+d') * (a'+b'+c')



(3M)

3

Find the minimal Sum of Products for the Boolean expression, $Y(A,B,C,D) = \sum m(1,2,3,4,9,10,11,12,15)$ and implement it using Gates.

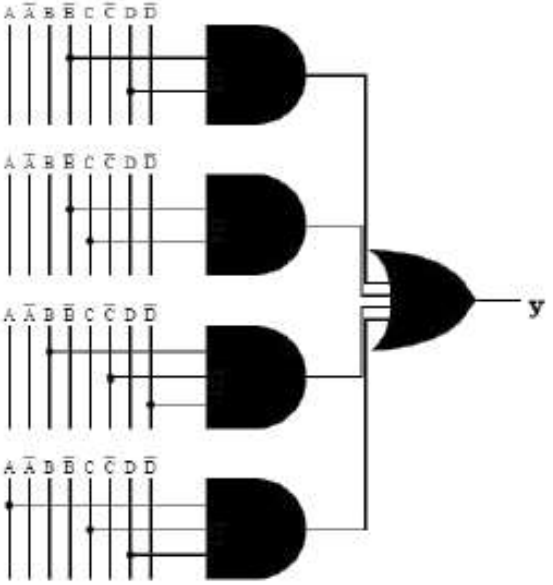
UQ Jan 2023- 8 marks

22.b

	$\overline{C}.\overline{D}$	$\overline{C}.D$	$C.D$	$C.\overline{D}$
$\overline{A}.\overline{B}$	0	1	1	1
$\overline{A}.B$	1	0	0	0
$A.B$	1	0	1	0
$A.\overline{B}$	0	1	1	1

$y = B'D + B'C + BC'D' + ACD$

(6 Marks)



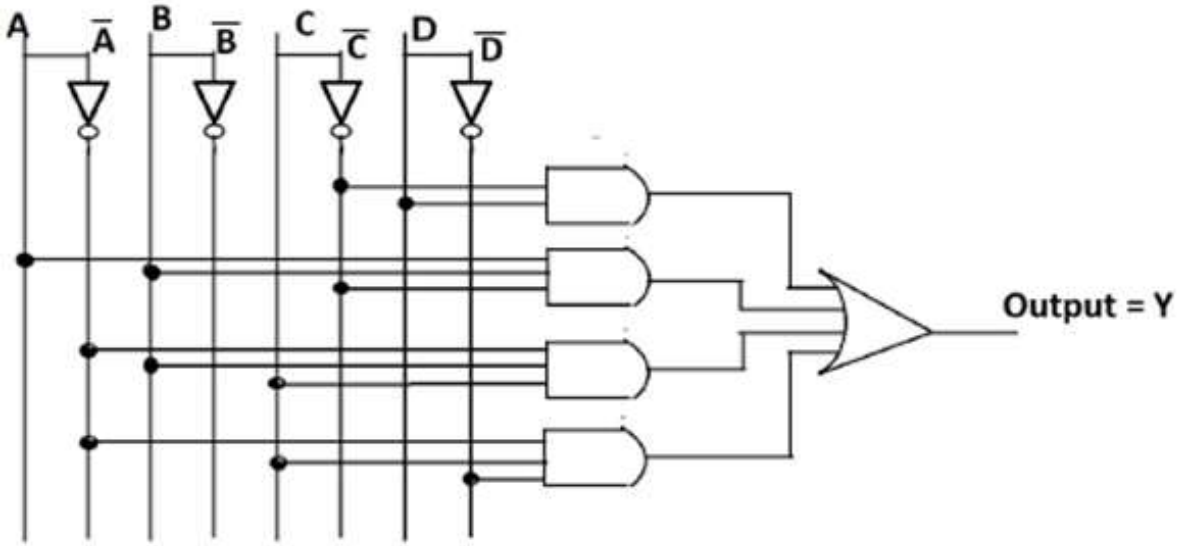
(2 Marks)

4

11.(b) Simplify the Boolean function F(A,B,C,D) = ∑m(1,2,5,6,7,9,12,13) using k-map and implement it using gates.

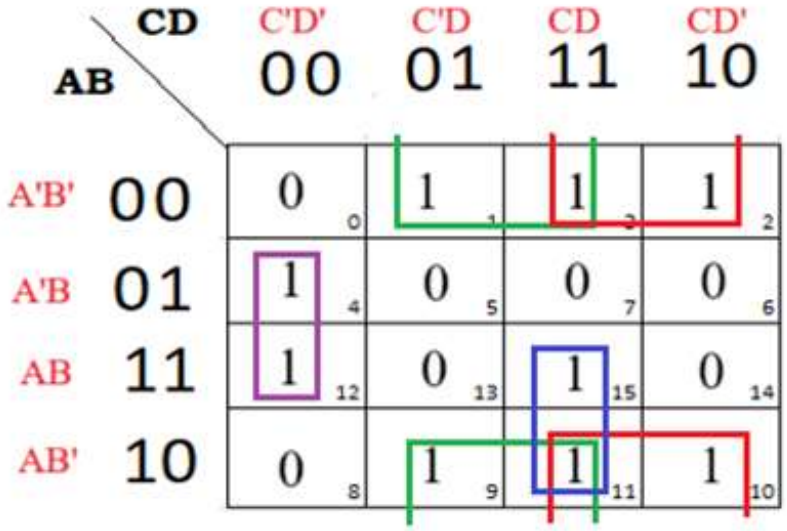
AB \ CD	C'D' (00)	C'D (01)	CD (11)	CD' (10)
A'B' (00)		1		1
A'B (01)		1	1	1
AB (11)	1	1		
AB' (10)		1		

$$Y = \bar{C}D + AB\bar{C} + \bar{A}BC + \bar{A}C\bar{D}$$



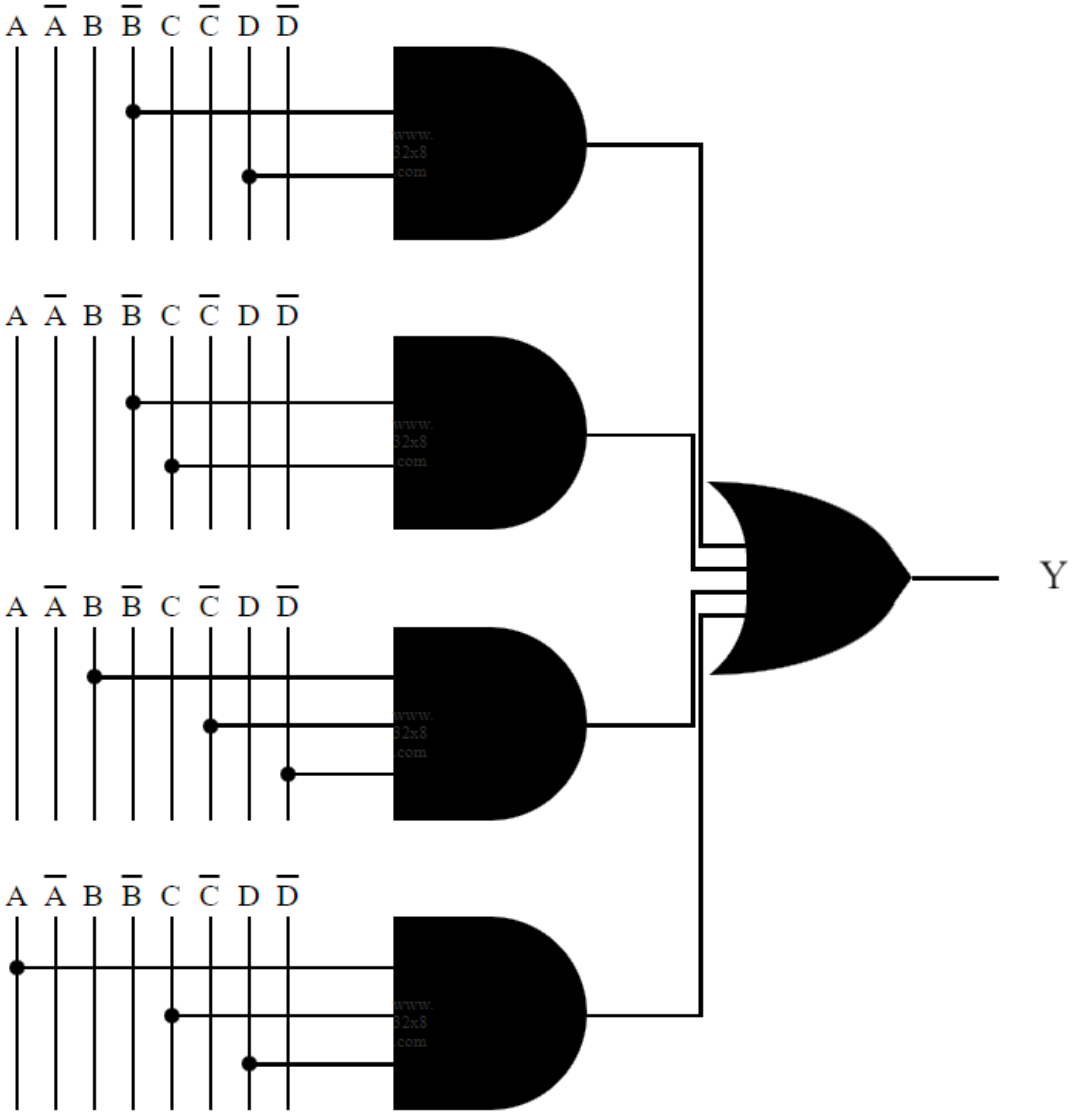
5

Simplify the Boolean expression Y(A,B,C,D) = Σm (1,2,3,4,9,10,11,12,15) using K-map and implement it using logic gates.



Y=B'D+ B'C+ BC'D' + ACD

Implementation it using logic Gates



6

Simplify the Boolean expression Y(A,B,C,D) = ∑m (0,1,2,4,6,7,10) using K-map and implement it using logic gates.

Map

	$\bar{C}\bar{D}$	$\bar{C}D$	CD	$C\bar{D}$
$\bar{A}\bar{B}$	1	1	0	1
$\bar{A}B$	1	0	1	1
AB	0	0	0	0
$A\bar{B}$	0	0	0	1

Map Layout

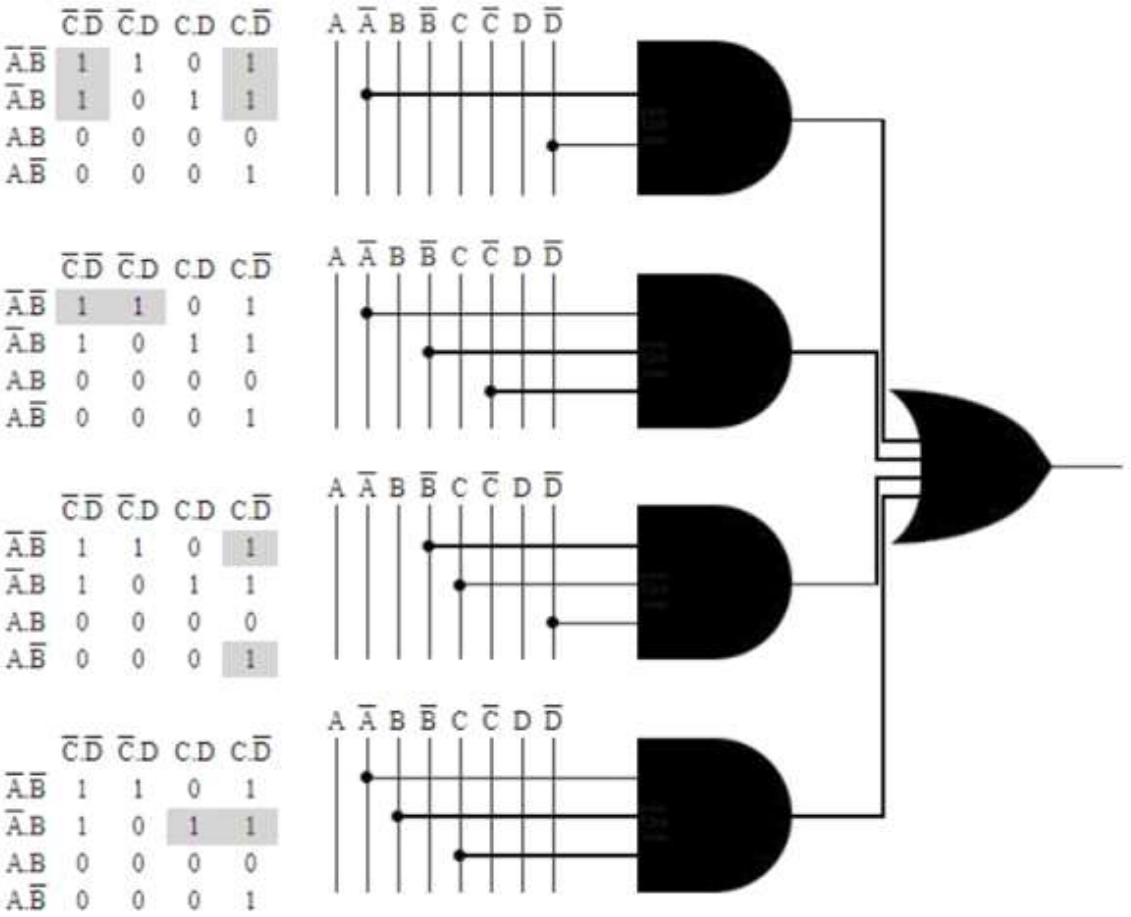
	$\bar{C}\bar{D}$	$\bar{C}D$	CD	$C\bar{D}$
$\bar{A}\bar{B}$	0	1	3	2
$\bar{A}B$	4	5	7	6
AB	12	13	15	14
$A\bar{B}$	8	9	11	10

Groups

(0,2,4,6)	$\bar{A}\bar{D}$
(0,1)	$\bar{A}\bar{B}\bar{C}$
(2,10)	$B\bar{C}\bar{D}$
(6,7)	$\bar{A}BC$

Clear

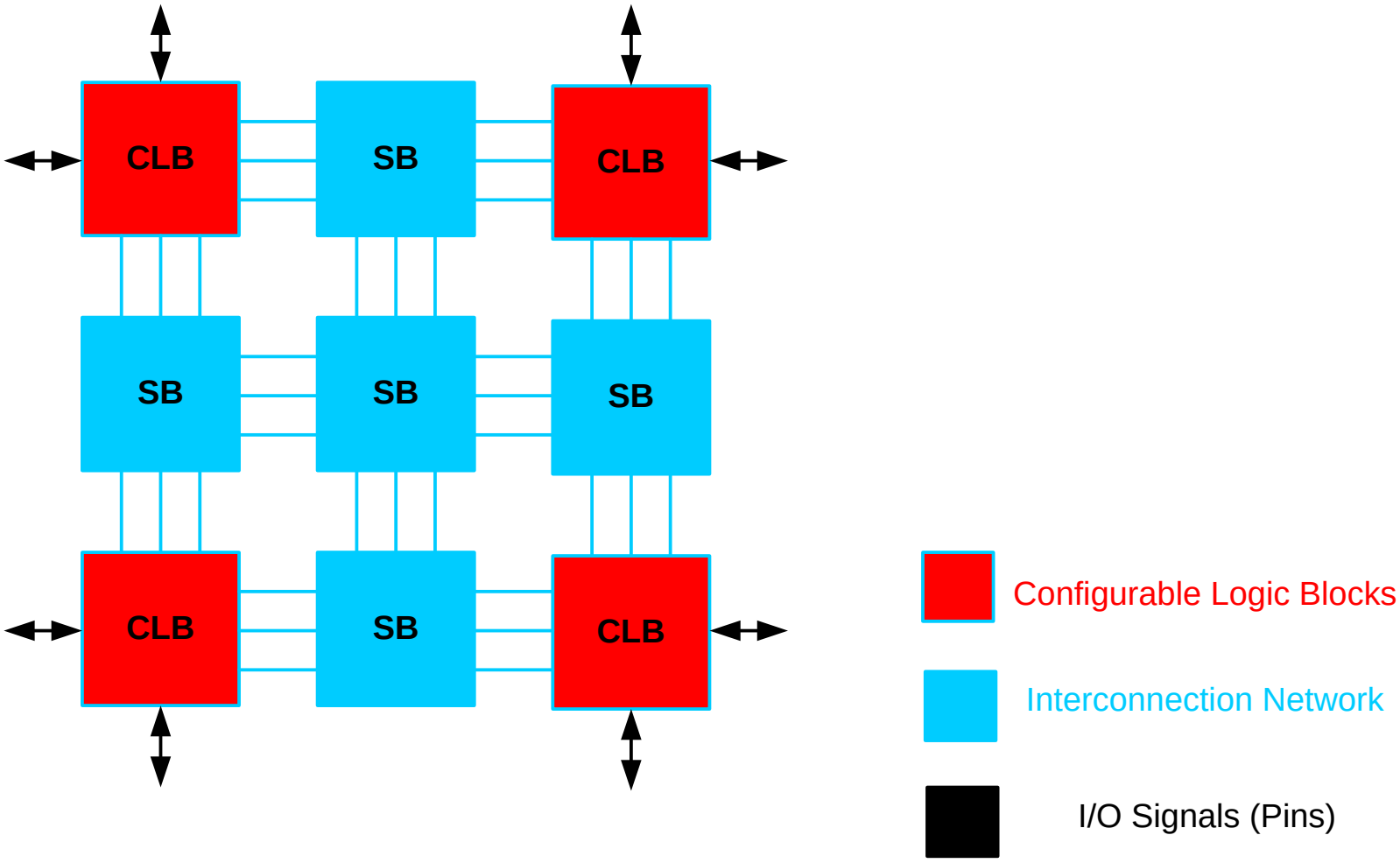
$y = A'D' + A'B'C' + B'CD' + A'BC$



FPGA

- A Field-Programmable Gate Array (FPGA) is an integrated circuit that can be configured by the user to emulate any digital circuit as long as there are enough resources.
- The FPGA configuration is generally specified using a hardware description language (HDL)
- An FPGA can be seen as an array of Configurable Logic Blocks (CLBs) connected through programmable interconnect (Switch Boxes).

FPGA structure



Simplified CLB Structure