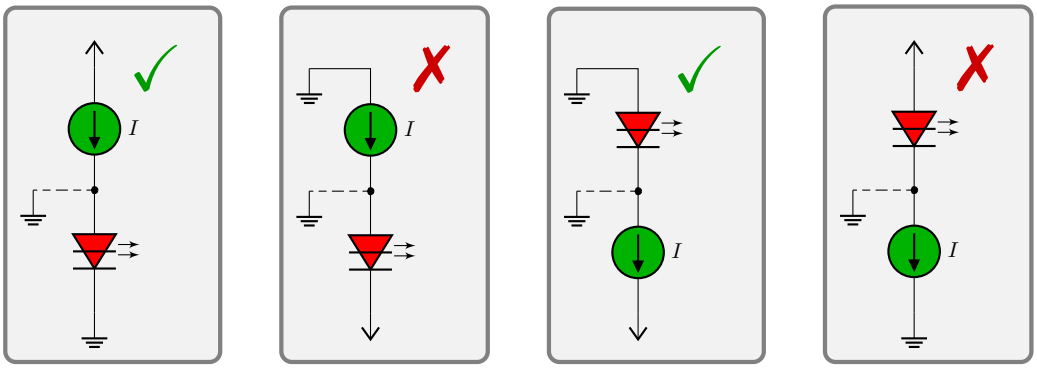
1.8. Current Sources

Throughout this work the concept of current sources is widely used, for example section 1.3 discusses a current source to drive laser diodes and the temperature controller discussed in section 1.9 uses a current source to measure the resistance of a temperature sensitive resistor. While there are many more use cases, this section will limit the discussion to a few examples used by the devices presented in this work. Namely, this is a unidirectional transconductance amplifier with an operational-amplifier and a field-effect transistor and a bidirectional Howland current pump invented by Bradford Howland in 1962 and first published in 1964 by Sheingold [75]. The discussion will start with the properties of the ideal current source and, based on that, develop a more accurate model. The models developed typically represent the static, time-independent case unless explicitely stated. First, the unidirection current source is treated, then the bidirectional Howland current pump is discussed.

1.8.1. Current Sink and Current Source

The question whether to use a current source or a current sink is elemental for the design of a laser driver. Figure 1.30 shows different configuration of current sinks and sources with respect to the laser diode.



(a) Source with grounded LD. (b) Source with floating LD. (c) Sink with grounded LD. (d) Sink with floating LD.

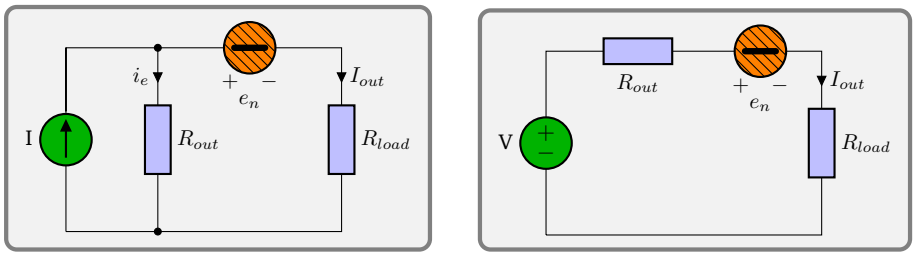
Figure 1.30.: Different configuration of current sinks and sources with respect to the laser diode. A green checkmark denotes a fail-safe configuration when accidentally shorting one or more pins of the diode to the laser chassis, illustrated by a dashed connection.

The most practical configuration depends on the laser diode and safety aspects in terms of protecting the laser diode. The protection of the laser diode is discussed first. The laser resonator is assumed grounded in our setup. While not intended, there are numerous ways to accidently short the diode to ground and since there are no immediate consequences arrising from it, when the controller is disconnected, it might easily be overlooked. This blunder should not bear the risk of destroying an expensive laser diode. To ensure this, a configuration where the laser diode is shorted out instead of the current source or sink must be chosen. That way, the laser diode is automatically removed from the circuit in case of an error condition. Choosing between a current sink and a current source is more subtle. If the can of the laser diode is connected to anode, a current sink can be considered, to keep the can at ground

potential. This is not an issue with our laser design though, because the laser diode mount is floating. Another aspect is the electronics side. A current source is typically implemented using p-channel field-effect transistors, while current sinks are using n-channel transistors and additionally the input of a current source is referenced to the positive supply, while the sink is referenced to the negative supply. Using the negative supply as a reference for control signals brings more challenges than vice versa, because typically integrated components like digital-to-analog converters prefer working with positive voltages and would need additional support to be floated to a negative reference. This makes a current source simpler to implement in this scenario and this work focusses on the current source, but in principle all methods derived can be applied to a current sink as well.

1.8.2. Ideal Current Source

The ideal current source as shown in figure 1.31 has two major properties besides the output current I_{out}, the output impedance and the compliance voltage, which are best understood when looking at the two equivalent representations of a current source separately. On the left in figure 1.31a, the Norton representation can be seen. Norton's theorem reduces any linear circuit to a current source, shown in green, with a parallel resistance R_{out}, usually called output resistance or impedance. On the right, the Thévenin representation can be see, which simplifies a circuit as a voltage source, also shown in green, with a series resistance.



(a) Norton representation. (b) Thévenin representation.

Figure 1.31.: An ideal current source with output impedance R_{out} and noise e_n.

First, the output impedance is discussed. Ideally, R_{out} is infinite and all current is forced to flow through the load. Given a finite output impedance leads to a decreased accuracy of I_{out}, because it is influenced by the load impedance as

$$I_{out} = I_{set} \cdot \frac{R_{out}}{R_{load} + R_{out}} \,. \tag{1.61}$$

In addition to a decreased accuracy, inserting a noise voltage source between the current source and the load as shown in figure 1.31 in orange, has the same effect as a changing load resistance and due to the finite output impedance R_{out}, any voltage noise e_n translates to current noise i_n through the load as

$$i_n = \frac{e_n}{R_{load} + R_{out}} \approx \frac{e_n}{R_{out}} \,, \tag{1.62}$$

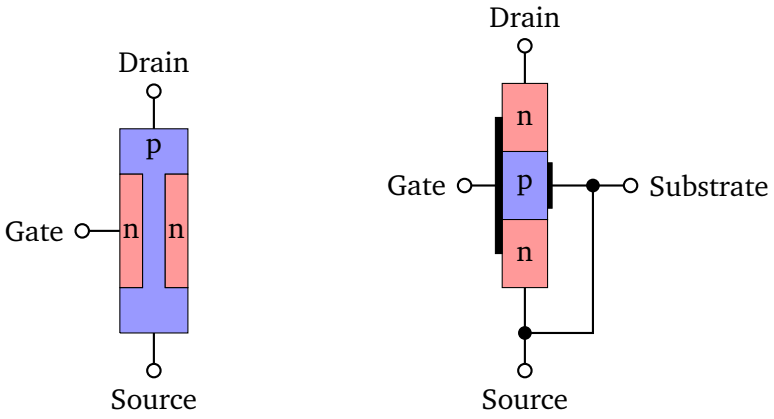
again making a high output impedance desirable to supress noise sources between the current source and the load.

Going to figure 1.31b of a current source in Thévenin representation allows to discuss the compliance voltage property. As it was said above, the output impedance of an ideal current

source is infinite and so is the maximum output voltage of said current source. A finite output impedance immediately implies a finite supply voltage to keep the current to a finite limit, which dictates a maximum output voltage. This is called the compliance voltage.

1.8.3. The Field-Effect Transistor Current Source

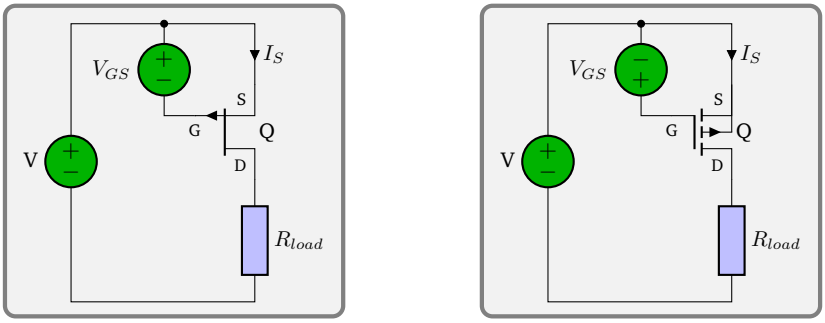
Given the limited supply voltage of a real current source drives the need for a resistive element that has a finite resitance and infinite, or very high, frequency dependent dynamic impedance to react to load changes. One such pass element, having these properties, is a field-effect-transisistor (FET). A junction-gate field-effect transistor (JFET) or metal–oxide–semiconductor field-effect transistor (MOSFET) can be used either as a current source or sink, depending on its doping. A p-channel FET, which uses a positve doping of the channel, is a current source, while an n-channel FET works as a current sink. This discussin is focussing on the p-channel FET with MOSFETs at its center, because it covers the bulk of the laser current driver design in section 1.3.



(a) P-Channel JFET. (b) P-Channel MOSFET.

Figure 1.32.: The simplified semiconductor structure of a JFET and a MOSFET.

The difference between a JFET and a MOSFET, is the gate structure as illustrated in figure 1.32. While a MOSFET has an insulated gate, the JFET does not. This reduces the gate leakage current, typically by about three orders of magnitude, and allows to forward bias the device since there is no diode, resulting in larger current handling capacity. So for low currents up to a few mA or low noise applications, JFETS are preferred, while MOSFETs can handle several hundred ampere. The same mathematical approach can be applied to both types of FETs though. The other difference between a JFET and a MOSFET is the fact that JFETs are only available as depletion-mode (normally-on) devices, while MOSFETs are available as both depletion and enhancement (normally-off) devices. The reason is the gate structure as mentioned above. An enhancement-mode device does not conduct, when the gate-to-source voltage $V_{GS} = 0\,\mathrm{V}$, so $|V_{GS}|$ must be increased or enhanced for the device to allow conduction. This is not possible with an uninsulated gate like a simple p-n junction of a JFET, which would then start conducting start leaking. A p-channel depletion-mode device on the other hand conducts at $V_{GS} = 0\,\mathrm{V}$ and $|V_{GS}|$ must be decreased or depleted to reduce the current, which is not possible with the uninsulated gate, because the p-n junction is reverse biased. The annotated circuit symbol and the quantities used to discuss the device properties are shown in figure 1.33.



(a) P-channel JFET. (b) P-channel MOSFET.

Figure 1.33.: Basic p-channel FET circuit.

A p-channel FET has its source (S) connected to the positive supply and the drain (D) is connected to a more negative voltage, typically the load. For the MOSFET the gate (G) is biased below the source to allow conduction. The source is is usually connected to the substrate for solitary devices as shown in figure 1.32b. This will be assumed in all further discussions and the consequences of a substrate, that is biased differently are omitted here. The interested reader may look up these details in [4].

As it was mentioned above, if appropriately biased, a FET can be considered a voltage controlled current source. This property can be seen in figure 1.34.

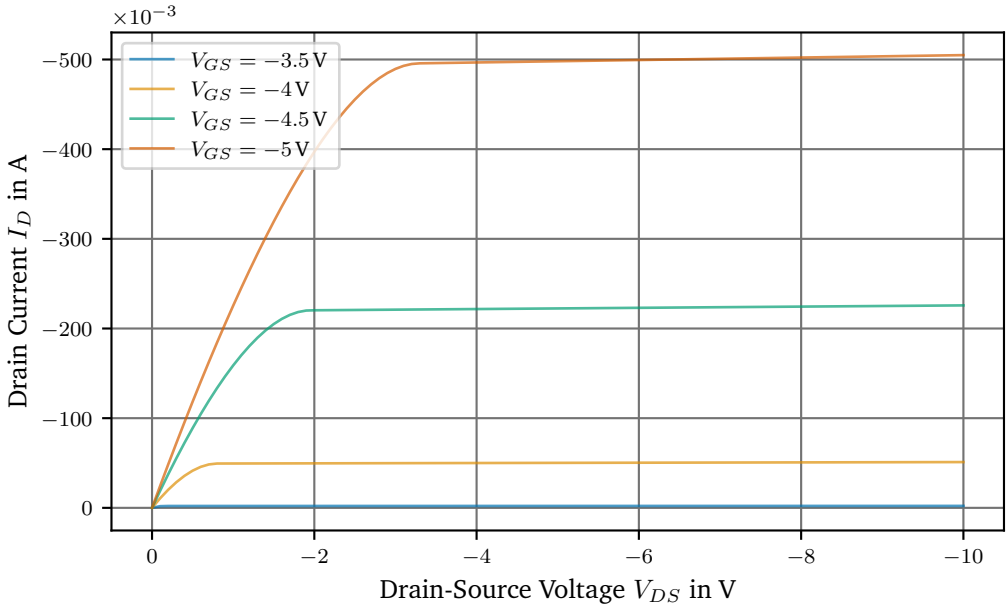


Figure 1.34.: Simulated drain current for different gate bias voltages of an `IRF9610` p-channel MOSFET.

Figure 1.34 shows the current I_D flowing out of the drain of a p-channel MOSFET over the drain-to-source voltage V_{DS} that is applied accross the FET. For illustrative purposes an example p-channel MOSFET was chosen and its *Simulation Program with Integrated Circuit Emphasis* (SPICE) model [10, 31] was used to generate the data, yet the overall shape is the

same for all FETs. For more information on modelling MOSFETs in SPICE, [14, p. 442] can be consulted. There are two regions, the first region, where $V_{DS} > V_{GS} - V_{th}$, demonstrates an almost linear linear correlation of the channel current and the voltage across the device. This is called the ohmic region, where the MOSFET behaves much like a (gate-) voltage controlled resistor and can be described [78] as

$$I_{D,ohmic} = \underbrace{\kappa(V_{GS} - V_{th})V_{DS}}_{\text{ohmic}} - \underbrace{\frac{1}{2}\kappa V_{DS}^2}_{\text{pinch off}} . \tag{1.63}$$

For small voltages V_{DS} the output current is proportional to the applied voltage V_{DS} accross the channel, just like a normal resistor, hence calling its name: ohmic region. As the voltage increases further I_D starts leveling off, because V_{DS} starts affecting the channel conductivity. The channel is slowly getting pinched off at one end and becomes tapered. The reason is, that the voltage V_{DS} is dropped accross the length of the channel. This voltage drop is linear with V_{DS}, resulting in a $-V_{DS}^2$ dependency of the current, reducing the conductivity of the channel. V_{th} is called the threshold voltage of a MOSFET or pinch-off voltage V_p in case of a JFET and is the voltage at which a current starts flowing.

The parameter κ is a device specific parameter and depends on process parameters and the geometry of the device.

$$\kappa = \kappa' \frac{W}{L} = \mu C_{ox} \frac{W}{L} \tag{1.64}$$

μ is the electron mobility, which is about $1350\,\mathrm{cm}^2/\mathrm{V}$ for n-channel MOSFETs and about $540\,\mathrm{cm}^2/\mathrm{V}$ for p-channel MOSFETs [73]. C_{ox} is the gate-oxide capacitance per unit area and determined by the thickness t_{ox} of the silicon dioxide layer of the gate

$$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}} \approx \frac{3.9 \cdot \epsilon_0}{t_{ox}} \approx \frac{3.45 \times 10^{-11}\,\mathrm{F/m}}{t_{ox}} , \tag{1.65}$$

W is the width of the channel, and L is the length of the channel.

The letter κ is used here instead of the usual k as it is used by Sedra et al. [73] to avoid confusion with the Boltzmann constant k_B. Unfortunately, κ is not well controlled [32], because it is not just determined by the size, but also the doping of the material. While the size of the structure can be well controlled to within a few nm using lithography masks, the doping is a matter of temperature and time in a diffusion furnace. The ohmic mode of operation is, for example, used in linear voltage regulators to control the output voltage of the regulator, forming a low impedance voltage source, not the desired current source. This brings up the next region to discuss.

Once the voltage V_{DS} has reached $V_{GS} - V_{th}$, the channel is fully pinched off, any further increase in V_{DS} will not lead to an increase in I_D, in other words the output resistance becomes infinite. The MOSFET is said to be pinched-off or in saturation. In practice there still is a small influence of V_{DS} on the channel. While the depth can no longer decrease as its length is 0 at one end already, the channel will retract a small amount in length with increasing V_{DS}. This is taken into account by the factor λ, called channel-length modulation. The drain current in saturation can now be described [78] as

$$I_{D,sat} = \underbrace{\frac{1}{2}\kappa \left(V_{GS} - V_{th}\right)^2}_{\text{ideal FET}}(1 + \lambda V_{DS}) . \tag{1.66}$$

The parameter λ is the first order Taylor exapansion of the length dependence of κ and typically is small and on the order of $0.01\,\mathrm{V}^{-1}$ to $0.05\,\mathrm{V}^{-1}$ for p-channel MOSFETs [67, p. 23]. It mainly depends on the length of the channel to which it is inversely proportional, since the channel length defines the slope of the tapered channel. Sometimes the value $\frac{1}{\lambda}$ is also referred to as the Early voltage V_A. It is noteworthy, that more modern processes choose a smaller channel length to reduce the on-state resistance of the MOSFET, because the main application of a MOSFET nowadays is as a switch. The reduced channel length makes the MOSFET more susceptible to the channel length modulation effect. This will be discussed in more detail in section 1.8.7, when choosing a suitable MOSFET.

Going back to figure 1.34 the effect of the channel-length modulation can be seen as a small slope of I_D in the saturation region.

Combining the previous equations, the FET drain current behaviour can be summed up as

$$I_D = \begin{cases} 0 & \text{if } V_{GS} - V_{th} < 0 \\ \kappa(V_{GS} - V_{th})V_{DS} - \frac{1}{2}\kappa V_{DS}^2 & \text{if } V_{GS} - V_{th} >= 0 \text{ and } V_{DS} < V_{GS} - V_{th} \\ \frac{1}{2}\kappa \left(V_{GS} - V_{th}\right)^2 (1 + \lambda V_{DS}) & \text{if } V_{GS} - V_{th} >= 0 \text{ and } V_{DS} \geq V_{GS} - V_{th} \end{cases} \tag{1.67}$$

The saturation region is the region of interest for building a high output impedance current source, because for a wide range of V_{DS}, the current remains almost constant and can be adjusted using the gate voltage V_{GS}. As a reminder, for the p-channel MOSFET, all voltages are reversed. V_{GS}, V_{th}, V_{DS}, κ and I_D are negative. Some datasheets therefore only give the magnitude of those quantities. The important aspect to remember, is that for the p-channel enhancement-mode MOSFET the gate must be biased negative with respect to the source pin by a least the threshold voltage ($V_{GS} < V_{th}$ or $|V_{GS}| > |V_{th}|$) to turn the transistor on and allow current to flow.

Before proceeding to the precision current source in section 1.8.4, the concept of conductance and transconductance must be explored. The transconductance describes the relationship of the input voltage with the output currrent. The conductance is a measure for how well current flows from input to output. The transconductance g_m and the channel conductance g_{DS} are defined as

$$g_{m,sat} \coloneqq \left.\frac{\partial I_{D,sat}}{\partial V_{GS}}\right|_{V_{DS}=const} = \kappa \left(V_{GS} - V_{th}\right)(1 + \lambda V_{DS}), \tag{1.68}$$

$$= \sqrt{2\kappa I_D (1 + \lambda V_{DS})} \approx \sqrt{2\kappa I_D} \tag{1.69}$$

$$g_{DS,sat} \coloneqq \left.\frac{\partial I_{D,sat}}{\partial V_{DS}}\right|_{V_{GS}=const} = \frac{1}{2}\kappa \left(V_{GS} - V_{th}\right)^2 \lambda \tag{1.70}$$

$$= \frac{I_D}{\frac{1}{\lambda} + V_{DS}} = \frac{1}{R_o} \approx I_D \lambda\,. \tag{1.71}$$

The transconductance g_m, as a measure of the current gain with respect to the gate-source voltage of the MOSFET, is proportional to the square root of the drain current I_D. The inverse of the channel conductance g_{DS} is called output resistance R_o and discussed below. Typically the V_{DS} term in the denominator of the output resistance in equation 1.71 can be neglected.

The meaning of g_m and g_{GS} can be best understood, when looking at a mathematical model of the MOSFET. These models come in varying complexity and either as a large-signal or small-signal model. Only the latter is used here. The small-signal model, is a first-order Taylor approximation around the working point, for a constant gate-source voltage V_{GS} and constant

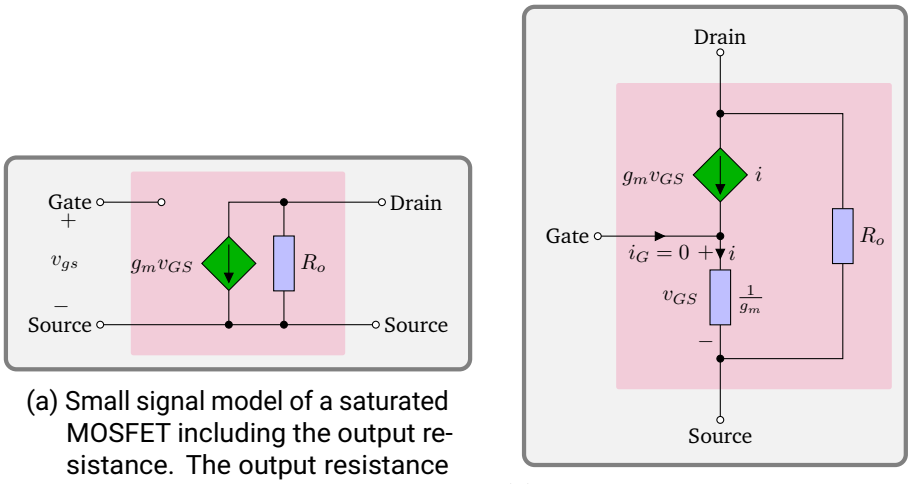
drain-source V_{DS}, hence both g_m and g_{GS} are constants.

$$I_D \approx \frac{\partial I_D}{\partial V_{GS}} \Delta V_{GS} + \frac{\partial I_D}{\partial V_{DS}} \Delta V_{DS} \tag{1.72}$$

$$= g_m \Delta V_{GS} + g_{DS} \Delta V_{DS} \tag{1.73}$$

$$= g_m v_{GS} + \frac{1}{R_o} v_{DS} = i_D \tag{1.74}$$

The lower case letters denote the variables of the small-signal model as they only change very little compared to the working point parameters. From 1.74 it can be seen, that the g_{DS} term adds to the output current and is proportional to v_{DS}. Comparing with figure 1.31a, this the proportionality constant can be identified as $\frac{1}{R_o}$ like proposed above. Just like the ideal current source in figure 1.31, the model can be given in the Norton or Thévenin representation both shown in figure 1.35.



(a) Small signal model of a saturated MOSFET including the output resistance. The output resistance models the channel-length modulation as given by equation 1.74.

(b) MOSFET model in Thévenin representation.

Figure 1.35.: Equivalent MOSFET models in Norton and Thévenin representations.

A detailed graphic derivation of the Thévenin representation can be found in [73]. The Thévenin representation will prove especially valuable, when treating circuits with a resistance in the source leg. The small-signal model now shows, that the output impedance is dependent on the channel-length modulation λ and v_{DS}. Typically, $\frac{1}{\lambda} \gg v_{DS}$, so λ is the most important factor governing the output impedance of a MOSFET.

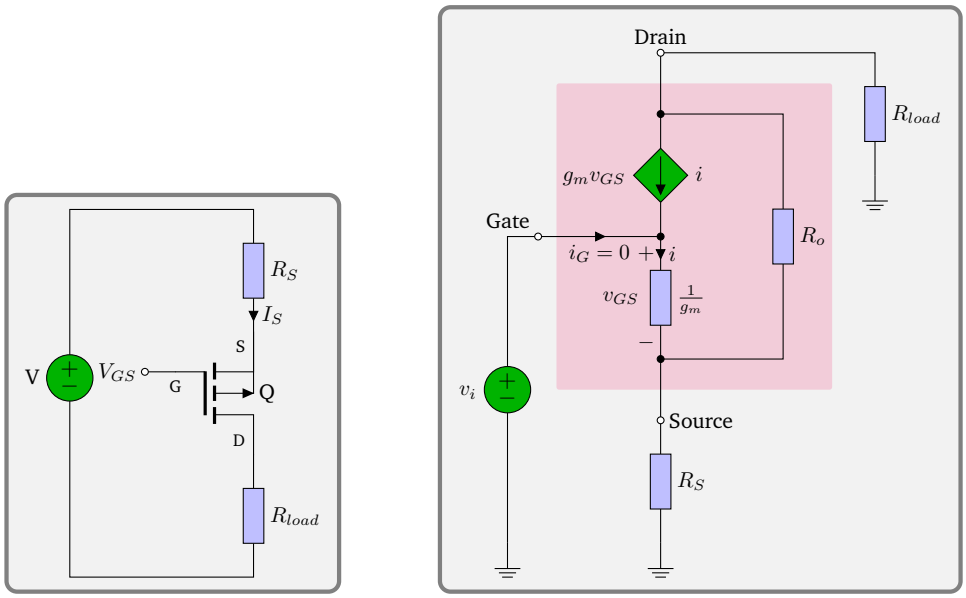
To give an example of the output impedance of a MOSFET, parameters were taken from the aforementioned SPICE model of the `IRF9610`. Do note, that these parameters of a model are tuned to match certain operating conditions by their creatros and only present an estimation of the real MOSFET. Using the example parameters from 1.8 $I_D = 250\,\text{mA}$, $\lambda = 4\,\text{mV}^{-1}$, $V_{DS} = 3.5\,\text{V}$ yields

$$R_{out} = R_o \left(I_D = 250\,\text{mA}, \lambda = 4\,\text{mV}^{-1}\right) = 1014\,\Omega \overset{V_{DS}=0}{\approx} 1\,\text{k}\Omega\,, \tag{1.75}$$

which is not very convincing as a current source. The small impact of V_{DS} on the output impedance can be seen when dropping the V_{GS} term, which leads to an output impedance of $1\,\text{k}\Omega$. Usually, in textbooks, this dependence is therefore neglected. To improve R_{out}, the focus thus lies on the λ dependence. The model derived from equation 1.74 can be used to do so, leading to the precision current source presented next.

1.8.4. Precision Current Source

In the previous section 1.8.3 it was shown in equation 1.74, that the output impedance of a MOSFET depends on the channel-length modulation λ and is too low for practical purposes. On the quest to improve the output impedance of the MOSFET circuit 1.35a, the most obvious solution would be to simply add a source resistor R_S into the circuit as shown in in figure 1.36a. At first glance, this may seem to only add a series resistance to R_o, but the attempt is more interesting and will lead to an even better solution.



(a) P-channel MOSFET with source resistor R_S to improve the output impedance R_{out}.

(b) Equivalent small-signal Thévenin model.

Figure 1.36.: Circuit of a MOSFET with source degeneration resistor and equivalent Thévenin model.

Before calculating the output impedance, we shall have a look at v_{GS} and the input signal v_i derived from it. With the introduction of the sense resistor R_S, v_i no longer equals v_{GS}, because $\frac{1}{g_m}$ now forms a voltage divider with R_S and it follows

$$v_{GS} = v_i \frac{\frac{1}{g_m}}{R_S + \frac{1}{g_m}} = v_i \frac{1}{1 + g_m R_S} \,. \tag{1.76}$$

This implies a reduction in gain, by the factor $\frac{1}{1+R_S g_m}$ compared to the previously discussed approach. The cause of this reduction is negative feedback. To understand this, imagine, that with a constant v_i and hence a constant current I_D flowing, a changing load resistance is trying to modulate I_D. Any increase in I_D will cause the voltage across R_S to rise, reducing v_{GS}, because v_i is still constant. The decreasing v_{GS} will then reduce I_D, thus introducing negative feedback. Having realized there is negative feedback present, it can be postulated, that the reduction in input sensitivity, or effective transconductance, will passed on to the output impedance. This very interesting relationship will now be derived.

To calculate the output impedance, figure 1.36b can be simplified by grounding v_i, because there is no AC component as there is no current flowing through the insulated MOSFET gate

and is not modulated. The load R_{load} resistance must is replaced by an AC test voltage v_{load} to modulate I_D. These changes result in the small signal model shown in figure 1.37. As a sidenote, this configuration is also called a common-gate amplifier.

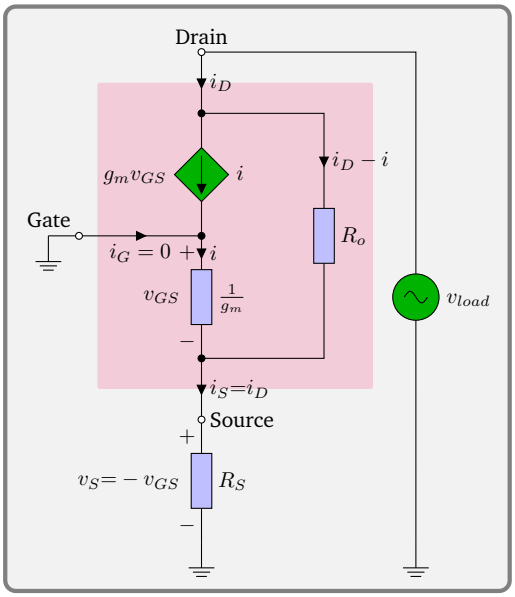


Figure 1.37.: Small signal model of the common-gate amplifier with source resistance R_S.

The (dynamic) output impedance is given by

$$R_{out,cg} = \frac{v_{load}}{i_D}\,, \tag{1.77}$$

with $i_D = i_S$, since there is no gate current. v_{load} can easily be calculated by looking at figure 1.37 and is the total voltage across R_o and R_S. v_{GS} can also be found, because the gate is grounded. With the resistance $\frac{1}{g_m}$ at one end, the voltage at the source pin must be $-v_{GS}$.

$$\begin{aligned} v_{load} &= (i_D - i)\, R_o + i_S R_S \\ &= (i_D - g_m v_{gs})\, R_o + i_D R_S \\ &= (i_D + g_m i_D R_S)\, R_o + i_D R_S \end{aligned} \tag{1.78}$$

Using equations 1.77 and 1.78 gives

$$R_{out,cg} = (1 + g_m R_S)\, R_o + R_S \tag{1.79}$$

for the output impedance.

This result is interesting, as it can be be immediately seen, that the output impedance scales very quickly with the transconductance g_m and R_S. As it was already speculated above, the reduction in the transconductance $\frac{1}{1+g_m R_S}$ of the MOSFET is transfered to the output impedance, which is increasing by the inverse of the loss in transconductance.

Going back to the quest for increased output impedance, it is appararent, that increasing R_S quickly raises the output impedance, as it scales with $gm_m R_o$, but it would come at the cost of a significantly reduced compliance voltage. So, other means need to be explored. As we have seen, the scale factor $gm_m R_o$ is explained by feedback and this brings up another solution.

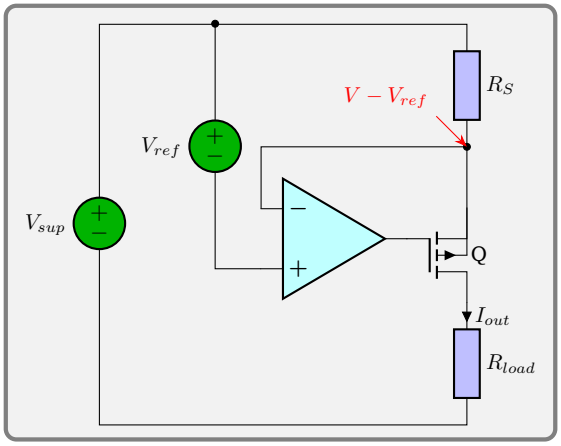


Figure 1.38.: Transconductance amplifier with a p-channel MOSFET.

The amount of feedback can be increased further using an operational amplifier (op-amp) as shown in figure 1.38.

The output impedance of this transconductance amplifier is amplified by the open-loop gain of the op-amp as shown in appendix A.3, while the transfer function greatly simplified and found to be

$$\begin{aligned} R_{out} &\approx A_{ol}\left(g_m R_o R_S + R_o + R_S\right) \\ I_{out} &\approx \frac{V_{ref}}{R_S} \end{aligned} \tag{1.80}$$

In addition to the increased output impedance, the current $I_D = I_{out}$ can now steered by adjusting V_{ref} and is, given sufficient loop gain of the op-amp, no longer dependent on the MOSFET, but rather only on the sense resistor R_S.

This has the added benefit, that it is possible to leverage the tight accuracy and precision of a resistor, over the poor specifications of a MOSFET. Resistors can be manufactured with tolerances of less than $100\,\mu\Omega/\Omega$, which is orders of magnitude better than FETs, which can be matched to low % values with patience.

Using the example parameters from table 1.8, the output impedance in staturation can now be calculated again for $I_{out} = 250\,\text{mA}$ and the ideal `IRF9610` model with the addition of an idealized `AD797` op-amp using the worst-case specifications.

$$R_{out} \approx 2\,\text{V}\,\mu\text{V}^{-1}\left(0.64\,\text{S}\cdot 1014\,\Omega\cdot 30\,\Omega + 1014\,\Omega + 30\,\Omega\right) \approx 40\,\text{G}\Omega \tag{1.81}$$

From these consideration, it can be seen, that the open-loop gain and the unity-gain bandwidth of the op-amp essentially determine the properties of the current source, given that $R_{id} \gg R_S$ and $R_o \gg R_S$. This will be important for selecting an operational amplifier later.

The next section will focus on the MOSFET and discuss the compliance voltage of the current source, which was only briefly touched during the introdution. It will give rise to criteria for selecting a MOSFET for the precision current source.

1.8.5. Compliance Voltage

The compliance voltage of a current source is the maximum voltage it can output to maintain the requested output current. For an ideal current source, the compliance voltage is infinite, but obviously limited in the physical world.

The precision current source discussed in section 1.8.4 has several limiting factors of the compliance voltage, which shall be discussed now. The compliance voltage is taxed most at the maximum output current $I_{out,max}$. So for the following discussion, the output is always treated as set to maximum.

Looking at figure 1.38 of the precision current source it is immediately evident, that the output voltage can be calculated by subtracting the voltage accross the source resistor V_{R_S} and the MOSFET V_{DS} from the supply voltage V_{sup}

$$V_{out} = V_{sup} - V_{R_S} - V_{DS} = V_{sup} - V_{ref} - V_{DS}\,.$$

The voltage V_{R_S} is given by equation 1.80 and equal to the setpoint voltage and hence given by the system parameters. This leads to the question of the minimum working point voltage V_{DS} at $I_{out,max}$. As a reminder, from equation 1.67 and figure 1.34 one can see, that the drain current is almost constant over V_{DS} in the saturation region and in the ohmic region is proportional to V_{DS}. The transition point from the ohmic region to the saturation region is at $V_{DS} = V_{GS} - V_{th}$ and putting this into equation 1.67 yields for the drain current

$$\begin{aligned} I_D &= \frac{1}{2}\kappa V_{DS}^2\,(1 + \lambda V_{DS}) \\ \Rightarrow V_{DS} &\approx \sqrt{\frac{2I_D}{\kappa}} && (1.82) \\ &\approx 784\,\text{mV} && (1.83) \end{aligned}$$

The latter result was calculated using the example parameters from table 1.8. At this point it can already be postulated, that the MOSFET will severly change in its function as a current source for $V_{DS} < 0.78\,\text{V}$. To quantify this, one has to look at the output impedance of the transconductance amplifier once again. In the last section, the output impedance was only treated for the staturation region, but this time, R_{out} must must be considered over a wide range of V_{DS}, thus not only in the saturation region, but also in the ohmic region. Instead of using the small-signal model as before, which assumed only small changes of V_{DS}, a large-signal model must applied, which also includes the non-linear nature of the piece-wise defined equation 1.67 of the drain current.

For the sake of simplicity, a SPICE simulation of figure 1.38 was carried out in LTSpice [57]. Solving this analytically, bears no educational value over the numerical solution shown below as will be seen. Additionally, the SPICE simulation also offers the opportunity to add additional, parasitic elements to the model to evaluate their effect, for example, the capacitive nature of the MOSFET gate.

The simulation itself is numerically fairly challenging and the typical approaches will lead to the limits of the numerical precision. To make simulation possible, the large-signal model is broken down into several small segements. For each these segments, the small-signal models at its respective working point is evaluated and then the result joined back together to reconstruct the large-signal model sought. How this is done in detail, is shown in appendix A.4 as it is beyond the scope of this section. The final result was calculated for two different frequencies, one frequency was deliberately chosen so low ($1\,\mu\text{Hz}$), that it is well below the dominant pole

of the op-amp, meaning, that the full open-loop gain applies and the other frequency chosen was $1\,\text{MHz}$, were the gain had dropped to $10\,\text{V/V}$. This is shown in figure 1.39.

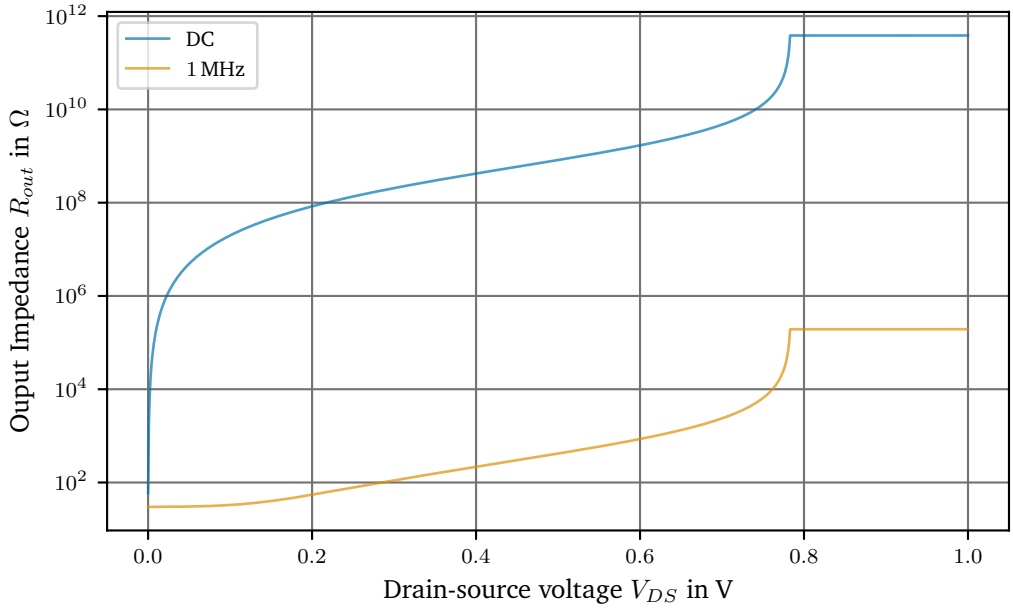


Figure 1.39.: Simulated output impedance for the precision current source from figure 1.38 at DC and $1\,\text{MHz}$ over the drain-source voltage.

Looking at figure 1.39 clearly shows the effect of entering the ohmic region of the MOSFET. Over a range of about $100\,\text{mV}$ below the $0.78\,\text{V}$ calculated above, the output impedance drops by two orders of magnitude and then keeps dropping at an exponential rate with decreasing V_{DS}. The same effect applies to the output impedance at $1\,\text{MHz}$, although the starting value is around $200\,\text{k}\Omega$ due to the reduced gain from the op-amp at $1\,\text{MHz}$. It can also be seen, that R_{out} levels off at $30\,\Omega$, the value of the sense resistor.

This overall effect of leaving the saturation region is so drastic, that the compliance voltage must be defined in such a way, that the MOSFET remains in saturation and this leads to

$$V_{comp} = V_{sup} - V_{ref} - \sqrt{\frac{2I_D}{\kappa}}\,. \tag{1.84}$$

Now turning to the supply voltage, it is limited by the op-amp which must drive the gate of the MOSFET all the way up to the supply to turn off the current source. The reference voltage is, unless one divides it down, which is a delicate matter, dictated by the reference chosen. This, unfortunately, leaves only little room for the MOSFET and it must be carefully chosen not limit the compliance voltage too much.

At this point a fallacy, the author has observed multiple times must addressed. In order to address the limited compliance voltage, one may be tempted to use multiple MOSFETs in parallel to divide the current between the MOSFETs and thereby reduce the voltage that needs to be dropped across the FET proportional to $\frac{1}{\sqrt{N}}$, where N is the number of MOSFETs paralleled.

Imagine the following modified circuit of the precision current source shown in figure 1.40 with two MOSFETs in parallel. For clarity the gate resistors required are not included.

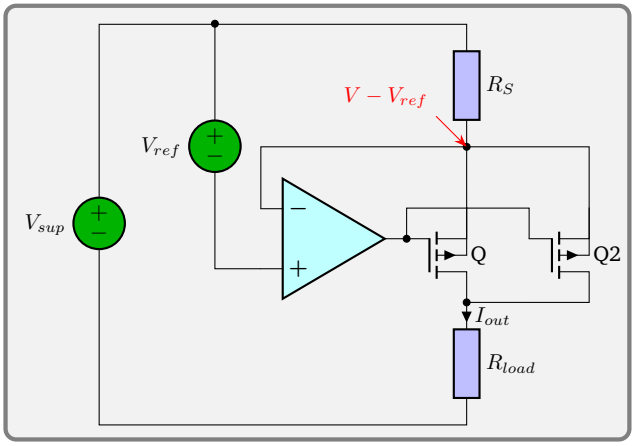


Figure 1.40.: Transconductance amplifier with two p-channel MOSFETs in parallel.

While at first, this seems like a solution to the limited V_{DS}, it is not that easy and a bad idea for number of reasons given here. The first reason is, MOSFET specifactions are very loose, notably the threshold voltage V_{th}, the transconductance g_m and the capacitances, but the latter is of little concern here. Paralleling MOSFETs works well under certain conditions, when using the MOSFETs as a switch, not as a current source. It seems to be a common misunderstanding, that MOSFETs are imune to thermal runaway. This is true, when using them as a switch fully turned on and in the ohmic region. In this case, there a two effects occuring, the first is, that the (absolute) value of V_{th} decreases with temperature, thus increasing I_D and the second effect is, $R_{DS,on}$ is rising with temperature [11]. But here, the MOSFET is operating in pinch-off and not the ohmic region, $R_{DS,on}$ has no influence on the current, therefore, the only effect at work is the decreasing V_{th}, so depending on how bad the imbalance in V_{th} of the paralled MOSFETs is, one MOSFET will gobble up most of the current and power. Adding source resistors, can compensate for this by pushing down the source voltage as the current goes up. This will then reduce V_{GS}. The size of the resistor depends on the transconductance g_m and the temperature coefficent of V_{GS}, which is around 1.5 to $2\,\mathrm{mV/K}$ [25]. Unfortunately, $1\,\Omega$ or $2\,\Omega$, will already eat up, most of the benefits gained in compliance voltage as will be shown below. A detailed analyis of paralleling MOSFETs can be found in [24].

The second reaon, why paralleling MOSFETs is a bad idea can be found, when remembering equation 1.67. We know that the transition from the undesirable ohmic region to the saturation region is

$$V_{DS} \geq V_{GS} - V_{th} \tag{1.85}$$

Looking at 1.40, we see that V_{GS} is set by the op-amp and is the same for both MOSFETs, but V_{th} is device specific and according to the datasheet of our example `IRF9610` [35] V_{th} values can show a spread of as much as -2 to $-4\,\mathrm{V}$, although [60] suggests, that MOSFETs from the same reel show a spread of only $\pm 125\,\mathrm{mV}$ of V_{th} within the same batch for consecutive devices. The $125\,\mathrm{mV}$ was found for the `BUK7S1R5-40H` [59], which was sampled in this report. The number given in the report is for 3σ and assuming the datasheet values are also referring to 3σ, the value found in the report is about twice as good as the datasheet value of 2.4 to $3.6\,\mathrm{V}$. Assuming similar numbers for `IRF9610` MOSFET used in our examples, this leads to $\pm 208\,\mathrm{mV}$ for the `IRF9610`, again applying 3σ. Using this number, a Monte Carlo simulation (not quite, because the dice were biased to yield a Gaussian distribution) was run using LTSpice, simulating the circuit shown in figure 1.40 and also the original circuit using only one MOSFET.

The current source was set to $250\,\text{mA}$ as per table 1.8. The load voltage was set to

$$V_{DS,parallel} = \sqrt{\frac{2\frac{I_d}{2}}{\kappa}} \approx 555\,\text{mV}\,, V_{DS,single} = \sqrt{\frac{2I_d}{\kappa}} \approx 784\,\text{mV}\,.$$

$\frac{I_D}{2}$ was used for the parallel configuration to show the effect assuming perfect current sharing between the MOSFETs. Additionally, $V_{DS,parallel} + 1\sigma$ was also investigated. 4000 samples were drawn and the spread of the output impedance was calculated for each circuit. The results are shown as a histogram in figure 1.41. The counts give the number of cases for each bin of the output imdedance.

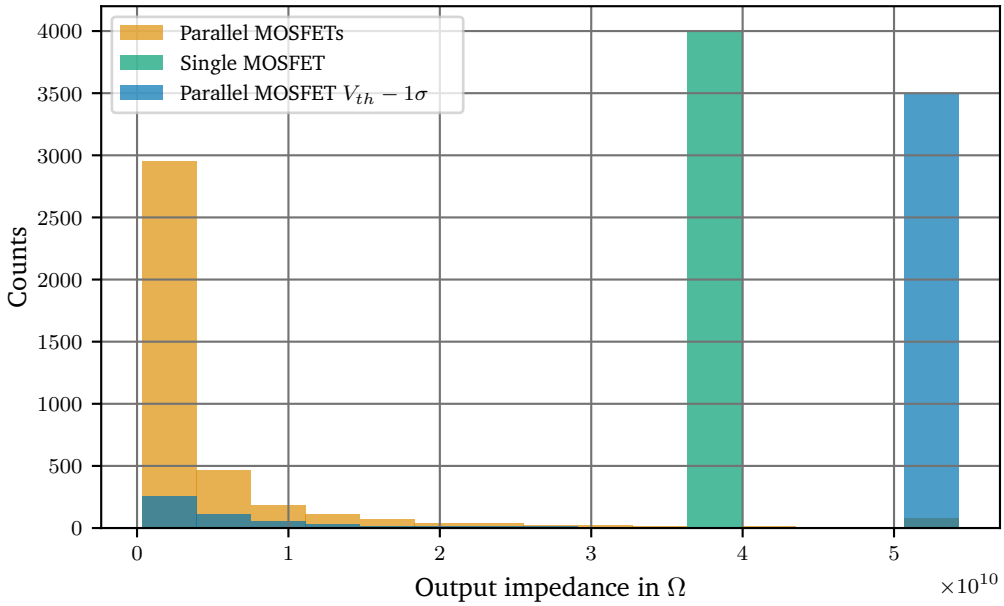


Figure 1.41.: Results of a Monte Carlo simulation of the output impedance for different configurations of MOSFETs.

Unsurprisingly, there is no variance of the output impedance in the single MOSFET case in accordance to what we have learnt in appendix A.3. The op-amp gain simply supresses all device properties of the MOSFET. The slight variation of g_m for different samples was not simulated, because this variation stems from the variation of κ and goes as $\frac{1}{\sqrt{\kappa}}$, so its effect is not as pronounced as the threshold.

In case of two mosfets, the output impedance varies over an order of magnitude from about 1.8 to $52\,\text{G}\Omega$. Even when increasing the drain-source voltage by $1\sigma = 70\,\text{mV}$ to $625\,\text{mV}$ on average, the spread is still an order of magnitude. Only when increasing V_{DS} to around $700\,\text{mV}$, the situation stabilizes, but then the net gain from this measure has shrunk to a meager $84\,\text{mV}$. We can see from this simuation, that the system-to-system spread becomes very unstable in tough situations. This instability can also be brought into the system by temperature effects as V_{th} is temperature dependent as discussed above. This is a designers nightmare, because these devices are no longer interchangeable in situations of high load currents and load impedances. Additionally, they may suffer from thermal runaway if each individual MOSFET is not layed to carry the full current. As a final remark: Do not parallel MOSFETs in saturation, ever.

1.8.6. Noise Sources

The fundamentals of different types of noise were already introduced in section 1.6. Here, a subset of these noise types is treated. It is expected, that the dominant noise observed in this circuit is $\frac{1}{f}$-noise at low frequencies and white wideband-noise. All noise components will be converted to the so-called input referred notation to make the noise sources comparable. This can be easily understood, when looking at two amplifiers with different gain. If both of them add a fixed amount of noise to the output signal, the absolute amount of noise may be the same, but the signal to noise ratio shows a different picture. To compare these amplifiers it is useful to divide the noise by the transfer function (gain) of the amplifier. This is called input-referred noise, since it treats the noise in relation to the input signal. Additionally, when calculating noise figures, the noise bandwidth is always considered to be 1 Hz.

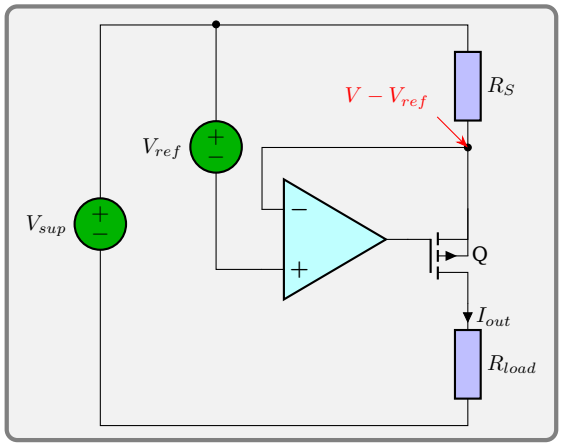


Figure 1.42.: Transconductance amplifier with a p-channel MOSFET. Repeated from page 56.

Noise sources are ubiquitous in the circuit in figure 1.38 on page 56, repeated here as figure 1.42 for clarity. The resistor R_S, the MOSFET, the op-amp, the setpoint voltage V_{ref} and the supply voltage V_{sup} can all contribute noise to the output current. Fortunately, some of those noise contributions are either very small or are well suppressed in this design, so each component must be briefly discussed.

Starting with the supply voltage V_{sup}, it can be seen, that any change of this voltage affects the string R_S-Q-R_{load}. From equation A.8, we know that if the op-amp gain is high, that is, within the bandwidth of the op-amp, all disturbances of the voltage accross R_S will be suppressed and the output current is only defined by the reference input and R_S. Looking closer, the supply noise is present at the inverting and non-inverting input of the op-amp with the same magnitude. If there is no current flowing into the op-amp pins, which is true for low frequecies, the noise is affecting both pins equally and it will be suppressed by the common-mode-rejection ratio (CMRR) of the device. Fortunately, this is a strong quality of precision op-amps and values of more than $1\,\mu V\,V^{-1}$ are not uncommon. The op-amp will therefore take care of the supply noise at low frequencies. At high frequencies the parasitic capacitance of the input pins and the reduced gain and CMRR come into play, reducing the CMRR and the gain also drop at high frequencies. To take care of this, it is therefore prudent to filter the supply for high frequency noise.

The next noise source is the reference voltage. The reference is directly connected to the input and its noise dictates most of the circuit noise. While the high-frequency noise can again be filtered to some extend, the low frequency noise, which is mostly $\frac{1}{f}$-noise can not be filtered

as was shown in section 1.6.1, so it must be kept low from the start and the reference selected for low flicker noise.

The MOSFET as a noise source is considered in appendix A.5 and the interested reader may find the derivation of the MOSFET noise within our circuit there. The two types of noise that need to be considered are the flicker noise of the MOSFET and its wideband thermal noise as calculated in equation A.20

$$i_n = \sqrt{\underbrace{4k_BT\frac{2}{3}g_m}_{\text{thermal}} + \underbrace{\frac{K_f I_D}{C_{ox}L^2}\frac{1}{f}}_{\text{flicker}}}\,.$$

To calculate the input referred noise and show that the MOSFET noise will be suppressed by the op-amp, the current noise needs to be divided by the open-loop gain derived as equation A.7

$$e_{n,FET} = \frac{i_n}{A_f} = \frac{\sqrt{4k_BT\frac{2}{3}g_m + \frac{K_f I_D}{C_{ox}L^2}\frac{1}{f}}}{\frac{A_{op}}{R_S}\frac{g_m(R_o||R_S||R_{id})}{g_m(R_o||R_S||R_{id})+1}}\,. \tag{1.86}$$

Looking at the parameters from table 1.8, we find $(R_o||R_S||R_{id}) \approx R_S$ and e_n can be simplified to

$$\begin{aligned} e_{n,FET} &\approx \frac{\sqrt{4k_BT\frac{2}{3}g_m + \frac{K_f I_D}{C_{ox}L^2}\frac{1}{f}}}{A_1\frac{1}{R_S+\frac{1}{g_m}}} \\ &\approx \frac{R_S+\frac{1}{g_m}}{A_1}\sqrt{4k_BT\frac{2}{3}g_m + \frac{K_f I_D}{C_{ox}L^2}\frac{1}{f}} \\ &\overset{A_1\to\infty}{=} 0 \end{aligned}$$

Unless the MOSFET transconductance g_m or the gain of the op-amp A_1 become very small, the noise of the MOSFET is very well suppressed. This means, that if the wideband thermal noise contribution is small (it is, see A.5) and the flicker noise corner frequency is within the bandwdith of the op-amp, the noise contribution from the MOSFET can be neglected.

The noise contribution from the sense resistor R_S is the (approximated) Johnson–Nyquist noise, which when transformed to its Norton representation can be written as current noise

$$i_{n,R} = \sqrt{\frac{4k_BT}{R_S}}\,. \tag{1.87}$$

Additionally, it was shown, that depending on the material of the resistive element, a flicker noise component can also be present. This is especially prevalent in carbon and tick-film resistors [22, 61]. While thin-film resistors are less noisy, their performance varies greatly between different models [74], so their make and model must be carefully selected for the application. Foil and wirewound resistors were shown to perform best and have almost no flicker noise [74, 9]. Using a high quality resistor the flicker noise can be neglected and only the thermal noise must be taken into account.

The sense resistor is part of the feedback network and therefore it contributes fully to the noise of the transimpedance amplifier. Input referred, the current noise must be divided by the closed-loop gain A_f given by A.2.

$$e_{n,R} = i_{n,R}\cdot\beta \approx i_n \cdot R_S = \sqrt{4k_BTR_S} \tag{1.88}$$

The final component to be discussed is the operational amplifier. Although the op-amp is a rather complex device, its noise can be modeled by a small number of noise sources. This noise model of the op-amp is shown in figure 1.43.

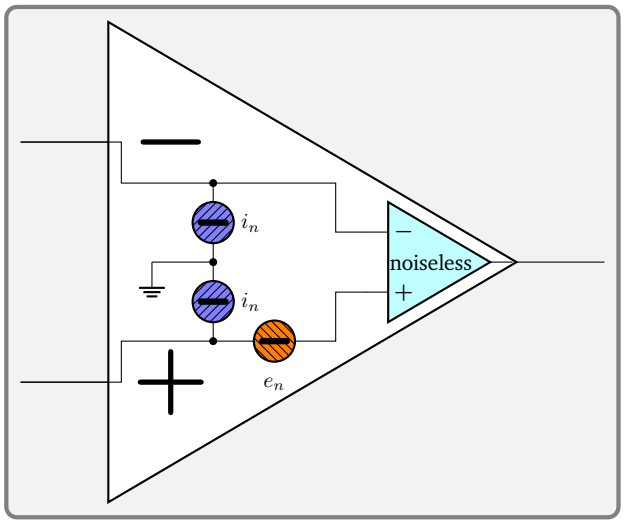


Figure 1.43.: Noise model of the operational amplifier.

In figure 1.43 we can see, that there are three noise sources required to treat the op-amp. The input voltage noise e_n and two input current noise sources i_n. The current noise noise source are assumed to be mostly uncorrelated. This assumption will lead to an upper bound as can seen from figure 1.44, which shows the the input differential amplifier, that is the first stage of a typical bipolar op-amp.

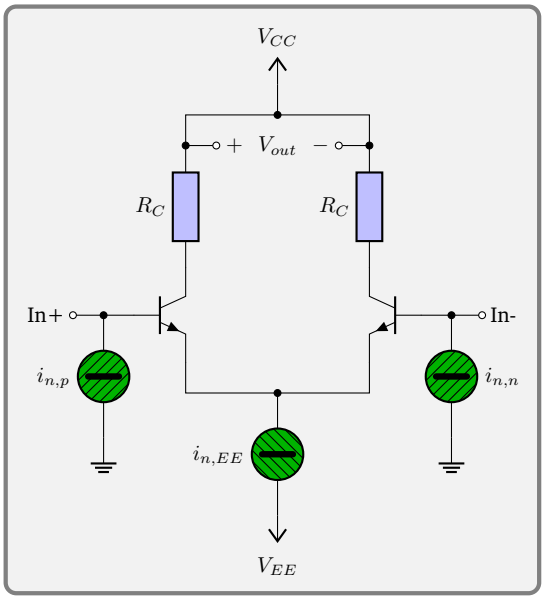


Figure 1.44.: Bipolar op-amp input stage with noise sources.

Of the three noise sources $i_{n,p}$ and $i_{n,n}$ are uncorrelated, because it is the input bias current of the individual transistors, and only the effect of $i_{n,EE}$ is correlated, because the current of

the emitter bias current souce is equally distributed between the two input transistors. Since effects of equal magnitude and sign cancel out due to the differential nature of the input stage, correlated effects are suppressed. An equal magnitude can be assumed, because the gain of the two transistors is well matched, due to their close proximity on the semiconductor die. Therefore assuming all noise is uncorrelated, presents an upper bound. A more detailed analysis can be found in [27], if interested. Due to the matching of the transistors, the magnitude $i_{n,p}$ and $i_{n,n}$ are also closely matched, hence in our model, they are assumed equal.

As we have done before in this section with referring all noise sources to the input, the same was done manufacturer and they are given in the datasheet. The two current noise sources can not be combined into the input voltage noise, because the depend on the external impedances connected to the op-amp. Given the complete circuit as in figure 1.42 it is possible to calculate the full noise contribution of the op-amp

$$e_{n,op} = \sqrt{e_n^2 + e_{n,+}^2 + e_{n,-}^2} \tag{1.89}$$

given that the noise sources are uncorrelated. The input referred noise $e_{n,-}$ of the inverting input can be calculated in a similar fashion as e_{n_R} in equation 1.88. It is likewise part of the feedback network and must therefore be divided by the closed-loop gain A_f as before.

$$e_{n,-} \approx i_n \cdot R_S \tag{1.90}$$

The current noise of the input can be translated by looking at the input impedance. This will be determined by the output filter of the reference voltage, which is required to remove the high frequency noise as discussed above. Assuming an RC-filter of first order, the output impedance can be calculated from the transfer function of the low-pass filter, derived in equation 1.17

$$\begin{aligned} R_{out,filt} &= R_{filt} \cdot A = \frac{R_{filt}}{1 + sR_{filt}C} \\ \lim_{s\to 0} R_{out,filt} &= R_{filt} \\ \lim_{s\to \infty} R_{out,filt} &= 0\,. \\ e_{n,-} &\approx \frac{i_n R_{filt}}{1 + sR_{filt}C} \end{aligned} \tag{1.91}$$

As it can be seen, for high frequecies, the output impedance goes to 0, while for low frequencies it is R_{filt}. If the filter corner frequency $\omega_0 = \frac{1}{RC}$ is close to or at the flicker noise corner frequency of the reference voltage, it means that there is almost no wideband current noise contribution as well. The only the $\frac{1}{f}$ component of the op-amp current noise multiplied with R_{filt} should be lower than the reference noise to have negligible impact. This leads to the total noise of the op amp

$$e_{n,op} = \sqrt{e_n^2 + (i_n R_S)^2 + \left|\frac{i_n R_{filt}}{1 + sRC}\right|^2}\,. \tag{1.92}$$

To conclude, table 1.4 is given as a reference for the noise contributions in the low-frequency and also the wideband domain. From this table, it can be seen, that the only wideband-noise contributors are the reference resistor and the op-amp. The low-frequency contributors are the voltage reference and the op-amp, since they have a strong flicker noise component. A low-noise, precision op-amp typically has far less low frequency noise than a voltage reference and the dominant low frequency contributor is the voltage reference.

Noise component	Low frequency	Wideband
V_{sup}	≈ 0	≈ 0
MOSFET	≈ 0	≈ 0
V_{ref}	$\sqrt{e_{n,ref}^2 + 4k_BTR_{filt}}$	≈ 0
R_S	$\sqrt{4k_BTR_S}$	$\sqrt{4k_BTR_S}$
Op-amp	$\sqrt{e_n^2 + i_n^2(R_S^2 + R_{filt}^2)}$	$\sqrt{e_n^2 + i_n^2R_S^2}$

Table 1.4.: Input referred noise components of the transimpedance amplifier. Multiply by $\frac{1}{R_S}$ to get the output referred current noise.

1.8.7. Component Selection

This section deals with selecting the right components for the precision current source presented in section 1.8.4. The focus lies on the requirements defined in section 1.3, notably tables 1.3.1 and 1.3.2. Most attention will be on the MOSFET, the operational amplifier and the voltage reference. We will start with the voltage reference, because this will define several parameters down the road. Then, the op-amp is discussed, for which several examples from scientific publications and other alternatives are shown and the best solution is presented. Finally, the selection parameters for the MOSFET will be elaborated. The reader must warned though, that the lineup of p-channel MOSFETs in production is decreasing, with more and more products being discontinued in favor of n-channel MOSFETs and the examples may be outdated.

Numerous laser driver designs can be found in literature [48, 72, 20, 89, 30, 86, 87] and those can be divided into two groups. High power drivers for quantum cascade lasers typically featuring a compliance voltage of more than $10\,\mathrm{V}$ and output currents of up to serveral ampere based on the work of Taubman and medium power devices for laser diodes having a lower compliance voltage of around $2\,\mathrm{V}$ and able to driver a few hundred mA based on the work of Libbrecht et al. Our requirements mostly fall into the latter category, except for the compliance voltage, which is targeted to be $\geq 8\,\mathrm{V}$. All these drivers share one common aspect, though, the type of voltage reference. Most laser drivers in literature and commercial products are designed around low-noise, low-drift buried Zener diode voltage references, namely the `LM399` [49] or `LTZ1000` [50].

Component	Voltage	Temperature coefficent	Stability	Package
`LT1021`	$7\,\mathrm{V}$	2 to $5\,\mu\mathrm{V}/(\mathrm{V\,K})$	$15\,\mu\mathrm{V}/(\mathrm{V}\sqrt{\mathrm{kh}})$	SO-8
`LT1027`	$5\,\mathrm{V}$	1 to $2\,\mu\mathrm{V}/(\mathrm{V\,K})$	not specified	SO-8
`LM399`	$7\,\mathrm{V}$	0.3 to $1\,\mu\mathrm{V}/(\mathrm{V\,K})$	$8\,\mu\mathrm{V}/(\mathrm{V}\sqrt{\mathrm{kh}})$	TO-46
`ADR1399`	$7\,\mathrm{V}$	0.2 to $1\,\mu\mathrm{V}/(\mathrm{V\,K})$	$7\,\mu\mathrm{V}/(\mathrm{V}\sqrt{\mathrm{kh}})$	TO-46
`LTZ1000`	$7.2\,\mathrm{V}$	$0.05\,\mu\mathrm{V}/(\mathrm{V\,K})$	$0.3\,\mu\mathrm{V}/(\mathrm{V}\sqrt{\mathrm{kh}})$	TO-99
`ADR1000`	$6.6\,\mathrm{V}$	$<0.2\,\mu\mathrm{V}/(\mathrm{V\,K})$	$0.2\,\mu\mathrm{V}/(\mathrm{V}\sqrt{\mathrm{kh}})$	TO-99

Table 1.5.: List of buried Zener diodes and selected properties.

The buried types of voltage references are *Zener* diodes, that are created within the bulk silicon using ion implantation. This reduces noise due to surface contamination [76]. These diodes are not true Zener diodes, but called Zeners nonetheless and use a mix of Zener and avalanche breakdown to compensate the temperature coefficient. The Zener effect is the tunneling of electrons through the barier from the valence band to conduction band. It has a negative temperature coefficient, because in increase in temperature reduces the size of the bandgap. Avalanche breakdown, on the other hand describes the mechanism, that free electrons (due to temperature) are accelerated to such energies, that they knock out other electrons, causing a avalanche of electrons. This effect has a positive temperature coefficient, because a higher temperature results in more free carriers, that cause leakage but no avalanche. While the zero temperature coefficient point is around $5\,\mathrm{V}$, this operating point implies a high succeptibility to changes in the reverse current. So typically the Zener voltage is shifted slightly upwards to result in a net positive coefficent, which is then compensated by the negative temperature coefficent of a forward biased diode [76]. This results in the typical Zener diode voltage of around $6.2\,\mathrm{V} + 0.7\,\mathrm{V} = 6.9\,\mathrm{V}$. In comparison to other types of diodes, buried Zeners have the best stability and lowest noise. In order to achieve high stability and low noise,

$V_{ref} \approx 7\,\mathrm{V}$ is therefore pretty much set in stone. Table 1.5, lists some commercially available buried Zener diodes. All diodes are manufactured by Analog Devices as they are the sole manufacturer left to produce these kind of diodes.

Choosing a voltage reference can be done according to table 1.3.1. A temperature coefficent of $\leq 1\,\mu\mathrm{A}/(\mathrm{A\,K})$ rules out any non-hermetic unheated voltage reference. Using a hermetic package improves the stability against humidity as the epoxy used for an SO-8 package is hydrophilic and swells when exposed to water vapour causing pressure on the die, resulting in a change of the output voltage. The hermetic voltage references can be divided into two groups, the `LM399` and the newer `ADR1399` in one group and the `LTZ1000` and its newer counterpart `ADR1000` in aother. While the `LM399` requires very few external components, the external circuit for the `LTZ1000` is far more elaborate requiring more parts and space. Additionally, the `LTZ1000` is more than four times the price of the `LM399` in quantities of 10 at the time of writing. Last but not least, the stability and temperature coefficent of the `LTZ1000` cannot be matched by the performance of the sense resistor, so the sense resistor gives a lower bound of about $0.5\,\mu\mathrm{A}/(\mathrm{A\,K})$. Unless the better low frequency noise performance is absolutely required, the `LM399` and `ADR1399` are the more economical parts. The performance of those two references will be discussed in section **??**.

With the maximum reference voltage of $7\,\mathrm{V}$ known, a sense resitor between $14\,\Omega$ ($500\,\mathrm{mA}$) and $28\,\Omega$ ($250\,\mathrm{mA}$ is required. Combined with the requirement for a low noise output, this limits the choice of op-amps to bipolar low-noise devices or discrete implementations. Table 1.6 lists some choices compiled from the literature sources, which will now be discussed.

Component	Wideband-noise	Low frequency noise	Temperature coefficent
`LT1028`	$0.85\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$	$35\,\mathrm{nV_{p-p}}$	$0.2\,\mu\mathrm{V/K}$
`AD797`	$0.9\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$	$50\,\mathrm{nV_{p-p}}$	$0.2\,\mu\mathrm{V/K}$
`ADA4898`	$0.9\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$	not specified	$1\,\mu\mathrm{V/K}$
`ADA4004`	$1.8\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$	$150\,\mathrm{nV_{p-p}}$	$0.7\,\mu\mathrm{V/K}$
`AD8671`	$2.8\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$	$77\,\mathrm{nV_{p-p}}$	$0.3\,\mu\mathrm{V/K}$

Table 1.6.: List of low-noise precision bipolar operational amplifiers with typical performance properties.

The low value of the sense resistor makes a bipolar op-amp the preferred choice, because they have a very low voltage noise and their current noise and input bias current do not interfere with such a low value resistor. While a discrete solution using matched jfets or bipolar transistors may push the input noise even lower, the temperature stability, circuit complexity and again the size speaks against this option, so the disussion will be limited to integrated solutions only. To find a reference point for the choice of op-amp, the thermal noise of the sense resistor must looked at. The $28\,\Omega$ sense resistor has a thermal noise of

$$e_n\,(23\,^\circ\mathrm{C}) = 0.67\,\mathrm{nV}/\sqrt{\mathrm{Hz}}\,.$$

This means, that even the lowest noise op-amp from table 1.6 dominates the wideband-noise. The `AD8671` chosen by [20] only makes sense, because they have chosen a very large filter resistor R_{filt} of $2 \times 3\,\mathrm{k\Omega}$. The `ADA4004` was used by Moglabs in the `DLC-202`, again likely due to the high values of R_{filt} used. The `ADA4898` might seem like a good choice at first sight but the very limited (in terms of precision op-amps) open-loop gain of $0.14\,\mathrm{V/\mu V}$ makes this op-amp a cheap, but poor choice. The final choice is between the `AD797` and the `LT1028`,

both op-amps have very similar specifications, but there is a peculiarity in the datasheet of the LT1028 [91]. While there is a current noise spectrum, there is no voltage noise spectrum to be found in the datasheet. The author assumes a good deal of specsmanship at this point. The publication by Libbrecht et al. already blames the LT1028 for a noise peak around $400\,\mathrm{kHz}$. This peak is also included in the noise models for the op-amp and was additionally confirmed by the author with a measurement. This peak is the reason why Seck et al. found the AD797 to be higher noise than the AD797. Additionally to the superior noise performance, the AD797B has excellent specifications overall. The open-loop gain is between 2 to $20\,\mathrm{V/\mu V}$, the supply rejection is greater than $1\,\mathrm{\mu V/V}$, the bias current is almost constant between 20 to $100\,^\circ\mathrm{C}$ and the unity gain bandwidth is around $10\,\mathrm{MHz}$. Finally it does have a very high output drive capability of $50\,\mathrm{mA}$, which allows to drive fairly large MOSFETs. These features make the AD797 the ideal op-amp for those low-value sense resistors, although it puts limits on the maximum filter resistor to limit the low frequency current noise contribution.

Finally, the choice of MOSFETs can be discussed. As it was shown in section 1.8.3 in equation 1.66, the channel length modulation playes an important role in increasing the channel conductance g_{DS} and limiting the output impedance. To reduce the channel length modulation a longer channel is preferred. Manufacturers do not give these numbers, nor the manufacturing process. Older technologies like the planar (lateral) FET is better suited for operating in the saturation region than the modern trench (vertical) FET. Trench MOSFETs are geared towards a low on-state resistance $R_{DS,on}$, which is important for MOSFETs in switching applications, but their lower resistance comes from a shorter channel. One of the few planar MOSFETs still available on the market is the HEXFET, which was designed for switching applications, but prooves useful nonetheless as we will see. High voltage MOSFETs also have longer channels than low voltage MOSFETs, so browsing for MOSFETs, that are rated for 60 to $100\,\mathrm{V}$ or more can narrow down the candidates. While the output impedance is a factor worth keeping in mind, the most important aspect is, whether the MOSFET can drive the load regarding the compliance voltage. To outline the problem, we can again refer to the example parameters from table 1.8.

Assuming a supply voltage of $15\,\mathrm{V}$ and the AD797 op-amp, the current source supply voltage V_{sup} is then limited to about 11 to $12\,\mathrm{V}$, because the AD797 is no rail-to-rail op-amp and its output only swings to within $3\,\mathrm{V}$ of the rail (minimum) and the input is limited to within $2\,\mathrm{V}$ of the rail (minimum). Considering the maximum V_{ref} at full output of $7\,\mathrm{V}$ and a load voltage of $3\,\mathrm{V}$ in case of the L785H1 [42] used as an example in this section leaves only

$$V_{DS,min} = V_{sup} - V_{ref} - V_{load} = (11 \text{ to } 12)\,\mathrm{V} - 7\,\mathrm{V} - 3\,\mathrm{V} = (1 \text{ to } 2)\,\mathrm{V} \tag{1.93}$$

for the MOSFET – a serious challenge.

To find a suitable MOSFET, one has to consult the *Typical Output Characteristics* graph in the datasheet. Using the maxium output current specifaction it is possible to estimate the minimum drain-source voltage V_{DS} to keep the MOSFET in saturation at the given maxium output current. This again narrows down the list of candidates.

The final aspect is the capacitive nature of the MOSFET gate. This property was brushed in appendix A.5 and the parasitic capacitances can be found in figure A.8. The AD797 can drive fairly large capacitive loads and several hundred pF are possible. It is best to keep the input capacitance C_{iss} below $500\,\mathrm{pF}$. Do remember the output impedance of the AD797, is about $10\,\Omega$ at $1\,\mathrm{MHz}$ and rising by an order of magnitude at $10\,\mathrm{MHz}$. The $500\,\mathrm{pF}$ results in an impedance of around $300\,\Omega$ dropping by an order of magnitude at $10\,\mathrm{MHz}$, so keeping capacitance low, allows a higher bandwidth of the current source.

Using these guidelines, searching a MOSFET across a lot of manufactures can still be tedious, but, for example, the distributor Digikey allows filtering and sorting by voltage and input capacitance. The follwing MOSFETs in table are given as an example and can be chosen for their respective current ranges.

MOSFET	Maximum V_{DS}	Input capacitance C_{iss}	Current range
`IRF9610`	$200\,\mathrm{V}$	$170\,\mathrm{V}$	100 to $250\,\mathrm{mA}$
`IRF9Z10`	$50\,\mathrm{V}$	$270\,\mathrm{V}$	250 to $500\,\mathrm{mA}$
`IRF9Z14`	$60\,\mathrm{V}$	$270\,\mathrm{V}$	250 to $500\,\mathrm{mA}$

Table 1.7.: Example MOSFETs for a current source and recommended current ranges.

The current range of the MOSFETs in table 1.7 is given based on the datasheet, making sure, that the MOSFET can be biased into saturation for the estimated minimum V_{DS} according to 1.93. The `IRF9Z10` is a lower voltage version of the `IRF9Z14` and the `IRF9Z14` should be preferred if available. Those MOSFETs starting with *IRF* are all HEXFETs formerly made by International Recitfier, whose MOSFET business was bought by Vishay in 2007.

1.8.8. Current Source Example Parameters

Throughout this section, example calculations are performed to give the reader an idea of real-life parameters derived from the theoretical models. These parameters are summarized in table 1.8, including their origin.

Parameter	Value	Source
MOSFET drain current I_D	$250\,\mathrm{mA}$	`L785H1` [42]
MOSFET κ	$0.813\,\mathrm{A\,V^{-2}}$	`IRF9610` SPICE model [10]
MOSFET channel length modulation λ	$4\,\mathrm{mV^{-1}}$	`IRF9610` SPICE model [10]
MOSFET source voltage	$3.5\,\mathrm{V}$ to $4\,\mathrm{V}$	section **??**
Source/Sense Resistor R_S	$30\,\Omega$ or $50\,\Omega$	section **??**
Op-amp differential input impedance R_{id}	$7.5\,\mathrm{k\Omega}$	`AD797` [90]
Op-amp open-loop gain A_{ol}	$2\,\mathrm{V\,\mu V^{-1}}$	`AD797` [90]
Op-amp gain bandwidth product GBP	$10\,\mathrm{MHz}$	`AD797` [90]

Table 1.8.: Parameters used throughout this section and their sources.

A.3. The Transconductance Amplifier with a MOSFET

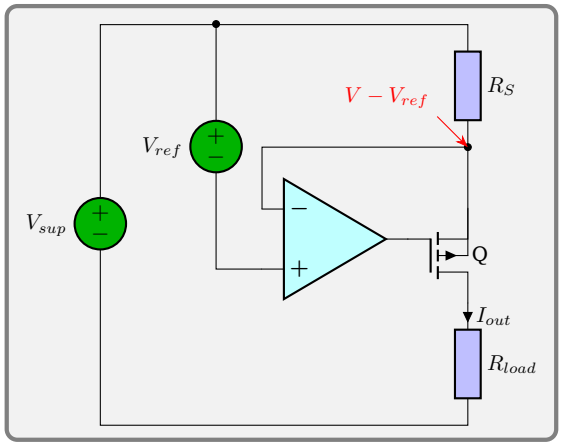


Figure A.1.: Transconductance amplifier with a p-channel MOSFET.

The amplifier shown in figure A.1 is a feedback transconductance ampplifier as discussed in [73]. Its transfer function can be derived using the techniques presented in section 1.5.1. As a reminder, the general transfer function is definded as:

$$P(s) = \frac{I_{out}}{V_{ref}} \equiv A_f \,. \tag{A.1}$$

The closed-loop transfer function is sometimes also called gain-with-feedback A_f [73] or noise-gain.

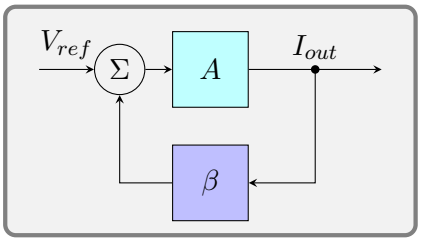


Figure A.2.: Block diagram of an amplifier with feedback β and gain A.

For the system shown in figure A.2, the closed-loop gain A_f can be written as

$$A_f = \frac{A}{1 + A\beta} \overset{A\to\infty}{=} \frac{1}{\beta} \,. \tag{A.2}$$

For the ideal transconductance amplifier with infinite open-loop gain A it follows, that the gain is simply reduced by the feedback factor β. For the MOSFET source voltage shown in figure A.1, β can be easily determined by inspection. The ideal op-amp with infinite open-loop gain A_{ol} has the same voltage at the inverting and non-inverting input. This means that below R_S at the source node of the MOSFET denoted in red, the voltage must be $V - V_{ref}$. This implies, that the voltage V_{ref} is dropped across R_S, defining I_{out}. Using equation A.2, β can be calculated

$$A_f = \frac{I_{out}}{V_{ref}} = \frac{\frac{V_{ref}}{R_S}}{V_{ref}} = \frac{1}{R_S} \approx \frac{1}{\beta} \,. \tag{A.3}$$

Calculating the transconductance amplifier gain A requires a little more work and it is useful to switch to the small-signal model of the circuit. To build the small-signal model, a number of simplifications can be applied. In the same same way as it was done for the MOSFET with a source resistor in figure 1.37 on page 55, the AC component of V_{ref} can be set to zero, because it is considered constant and so can the supply voltage V. The load is also considered constant and hence shorted to ground. In order to ground V_{ref}, the non-inverting input of the MOSFET must be disconnected, because there still is the voltage v_id connected to it. The model includes the differential input resistance R_{id} between the inverting and non-inverting input of the op-amp, because for bipolar input op-amps, the differential input resistance can be as low as a few kΩ and must be considered. The common-mode input resistance of the op-amp inputs is typically serveral dozens of MΩ or higher and can be safely neglected. This leads to the small signal model shown in figure A.3. The MOSFET model is the Thévenin model introduced in figure 1.36b on page 54. Do note, that this model is for low frequencies only, as it neglects capacitive effects of the op-amp and mosfet. Capacitors are treated as having infinite impedance in this model.

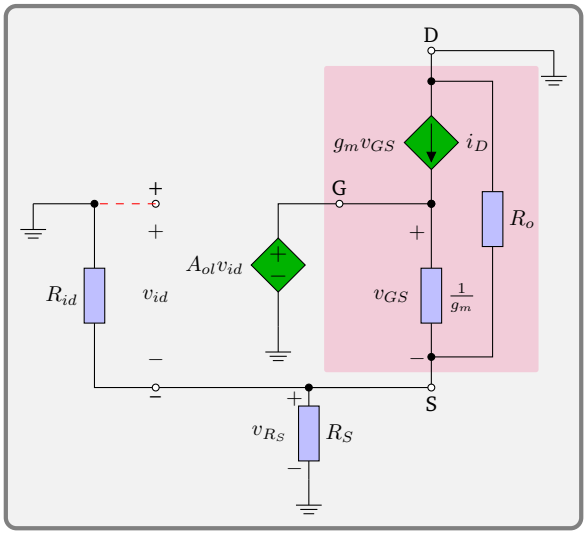


Figure A.3.: Small signal model for a transconductance amplifier with a MOSFET as shown in figure A.1

From the model in figure A.3, the following equations can be extracted in a similar fashion as it was done for the common-gate amplifier and equation 1.78 on page 55.

$$v_{GS} = A_{ol} v_{id} - V_{R_S} \tag{A.4}$$

$$V_{R_S} = i_D \left(R_o || R_S || R_{id}\right) = g_m v_{GS} \left(R_o || R_S || R_{id}\right) \tag{A.5}$$

$$\begin{aligned} A\beta = \frac{V_{R_S}}{V_{id}} &= \frac{g_m v_{GS} \left(R_o || R_S || R_{id}\right)}{\frac{1}{A_{ol}} \left(1 + g_m \left(R_o || R_S || R_{id}\right)\right) v_{GS}} \\ &= A_{ol} \frac{g_m \left(R_o || R_S || R_{id}\right)}{1 + g_m \left(R_o || R_S || R_{id}\right)} \end{aligned} \tag{A.6}$$

Dividing by R_S yields the open-loop gain of the transconductance amplifier, a quantity, that is interesting for calculating the MOSFET noise contribution:

$$A = \frac{A_{ol}}{R_S} \frac{g_m \left(R_o || R_S || R_{id}\right)}{1 + g_m \left(R_o || R_S || R_{id}\right)} \tag{A.7}$$

This leads to the closed-loop transfer function

$$A_f = \frac{A_{ol}}{R_S} \frac{g_m \left(R_o||R_S||R_{id}\right)}{(A_{ol}+1) g_m \left(R_o||R_S||R_{id}\right) + 1} \,, \tag{A.8}$$

and finally the output impedance of the transconductance amplifier can be calculated using the output impedance of the common-gate amplifier 1.79, calculated on page 55.

$$\begin{aligned} R_{out} &= (1 + A\beta)\, R_{out,cg} \\ &= \left(1 + A_{ol} \frac{g_m \left(R_o||R_S||R_{id}\right)}{1 + g_m \left(R_o||R_S||R_{id}\right)}\right) \left(g_m R_S R_o + R_o + R_S\right) \\ &\overset{A_{ol} \gg 1}{\approx} A_{ol} \frac{g_m \left(R_o||R_S||R_{id}\right)}{1 + g_m \left(R_o||R_S||R_{id}\right)} \left(g_m R_S R_o + R_o + R_S\right) \,. \end{aligned} \tag{A.9}$$

Equation A.9 can be simplified for typical applications by approximation of $g_m \left(R_o||R_S||R_{id}\right)$. Using the example parameters for the `IRF9610` in saturation used previously on page 53 and additionally the ADI `AD797` [90] op-amp $g_m \left(R_o||R_S||R_{id}\right)$ with the following parameters

$$\begin{aligned} &I_D = 250\,\mathrm{mA}\,, \lambda = 4\,\mathrm{mV}^{-1}\,, V_{DS} = 3.5\,\mathrm{V}\,, R_S = 30\,\Omega\,, \\ &R_{id} = 7.5\,\mathrm{k}\Omega\,, \kappa = 0.813\,\mathrm{A\,V}^{-2}\,, A_{ol} = 20\,\mathrm{V\,\mu V}^{-1} \end{aligned}$$

one finds

$$\begin{aligned} R_o &= \frac{I_D}{\frac{1}{\lambda} + V_{DS}} = 1014\,\Omega \\ g_m &= \sqrt{2\kappa I_D \left(1 + \lambda V_{DS}\right)} = 0.642\,\mathrm{S} \\ g_m \left(R_o||R_S||R_{id}\right) &\approx g_m R_S \approx 29.03 \\ \frac{g_m \left(R_o||R_S||R_{id}\right)}{1 + g_m \left(R_o||R_S||R_{id}\right)} &\approx 0.97 \end{aligned}$$

Using typical parameters, it can be seen, that dropping the $\frac{g_m(R_o||R_S||R_{id})}{1+g_m(R_o||R_S||R_{id})}$ term will only lead to error of about 3 %. Given the datasheet uncertainties for the MOSFET related parameters on the order of 50 % to 100 %, it can be safely neglected, leading to the following approximations

$$\begin{aligned} R_{out} &\approx A_{ol} \left(g_m R_o R_S + R_o + R_S\right) \\ A_f &\approx \frac{1}{R_S} \,. \end{aligned} \tag{A.10}$$

The approximation for the output impedance holds true when $g_m R_S \gg 1$, which typically is the case. While R_S might become small, this is compensated by an increase in g_m in our application, because a smaller source resistor implies a higher output current, demanding a MOSFET with a higher transconductance, so the product of $g_m R_S$ remains constant.

It can therefore be said, that the op-amp is simply amplifying the output impedance of the MOSFET with the source resistor and the closed-loop gain is defined entirely by R_S, a very convenient property.

If the model is to be considered at frequencies $\omega > 0$, A_{ol} can be replaced by the first order approximation of the op-amp gain as

$$A_1(\omega) = \frac{A_{ol}}{\sqrt{1 + \left(\frac{\omega}{\omega_c}\right)^2}} \,, \tag{A.11}$$

which is valid for most compensated op-amps, which have a dominant pole at $\omega_c \approx 1\,\mathrm{Hz}$.

A.4. Simulating Current Source Properties in LTSpice

This section explains some more advanced concepts of LTSpice [57] to simulate device properties and circuit properties used when working with the current source presented in section 1.8.4. This section does not aim at explaining the basic functions of LTSpice, but rather some special functions. It is left to the interested reader to acquire those basic skills. The example presented here, allows to generate the MOSFET *Typical Output Characteristics* plot found in datasheets, the transconductance of a MOSFET and the (dynamic) output impedance of a current source. The typical output characteristics can be used to compare the model with the datasheet or with measurements taken. Comparing these model parameters with the datasheet can establish confidence, that the simulation results can be transferred to a real circuit.

A.4.1. MOSFET Typical Output Characteristics

The output characterisic is a graph found in all MOSFET datasheets and is shown below in figure A.4.

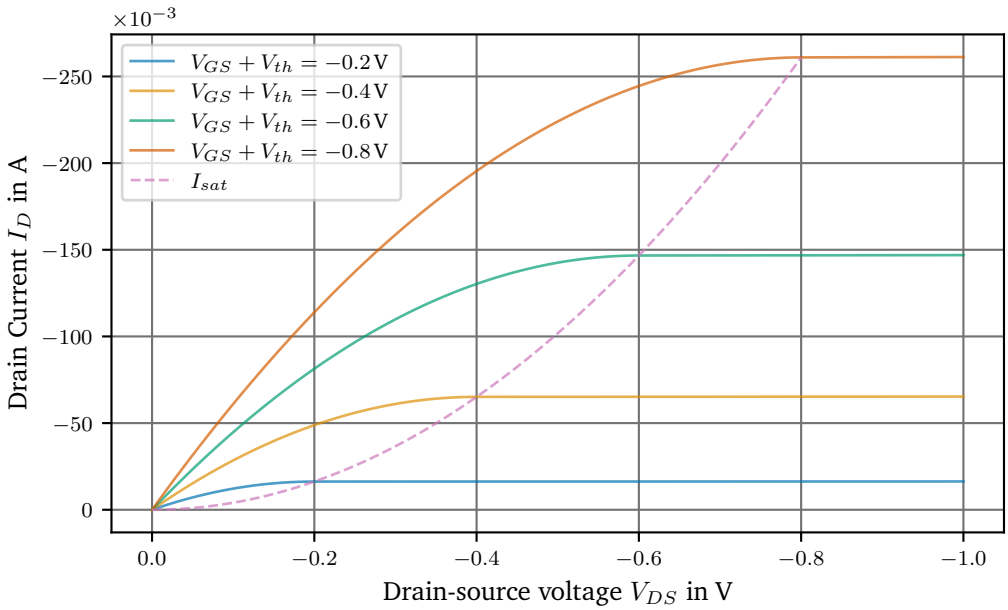
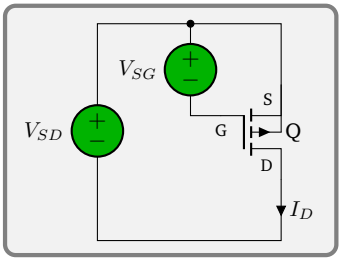


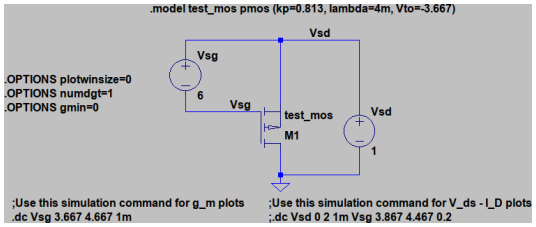
Figure A.4.: Simulated drain current over the drain-source voltage, also called output characteristics of a MOSFET

Plotting this graph allows to compare the model to the datasheet or the measured values in order to tweak the model. To create this graph the simulation file found in the folder `source/spice/mosfet_gm-id.asc` as part of this document can be used. The SPICE simulation for the output characteristics of the MOSFET simulate the following circuit shown in figure A.5a.

Do note, that the V_{DS} and V_{GS} are inverted and given as V_{SD} and V_{SG}. The reason is, that the plotter in LTSpice works better with positive numbers to guess the correct scaling of the axis. Figure A.5b shows the same circuit drawn in LTSpice. The MOSFET parameters are entered using the **.model** syntax



(a) P-channel MOSFET under test.



(b) LTSpice model.

Figure A.5.: P-channel MOSFET circuit and its LTSpice model.

.**model** test_mos pmos (kp=0.813, lambda=4m, Vto=−3.667)

with the parameters $\kappa = 0.813\,\mathrm{A\,V^{-2}}$, $\lambda = 4\,\mathrm{mV^{-1}}$ and $V_{th} = -3.667\,\mathrm{V}$. The options **plotwinsize** and **numdgt** make sure, that LTSpice does not compress the output data and increases the floating point precision. This is important, because I_D spans a large range values. Setting **gmin** to 0 prevents LTSpice from adding small transconductance to every pn-junction, thus changing the MOSFET model. Finally, the most important command is the **.dc** command, which instructs LTSpice to step the voltage sources V_{SD} and V_{SG} to evaluate I_D over V_{SD}. The command

.**dc** Vsd 0 2 1m Vsg 3.867 4.467 0.2

steps the voltage source V_{SD} from $0\,\mathrm{V}$ to $2\,\mathrm{V}$ in steps of $10\,\mathrm{mV}$ and for each step of V_{SD}, steps V_{SG} from $0.2\,\mathrm{V} - \mathrm{V_{th}}$ to $0.8\,\mathrm{V} - \mathrm{V_{th}}$ in steps of $200\,\mathrm{mV}$. Plotting

Id(M1)

results in the plot shown in figure A.4, which can be found in datasheets as the *Typical Output Characteristics* plot. To draw a line in the graph showing the point where the MOSFET enters the saturation region, denoted I_{sat} in figure A.4, as given by equation 1.67, add the following plot command to the graphing window and resecale the axis.

0.5∗0.813∗1A/1V∗∗2∗V(vsd)∗∗2

This command must be adjusted for the value of κ and do note, that κ is entered with units of $\mathrm{A/V^2}$ to correctly display the output in A.

A.4.2. MOSFET Transconductance

Another interesting property to plot is the transconductance g_m of the MOSFET. Again, using the same model used previously in figure A.5b and from equation 1.68 we known that g_m is defined as

$$g_m = \left.\frac{\partial I_D}{\partial V_{GS}}\right|_{V_{DS}=const}.$$

To derive g_m, we need to generate values of $I_D(V_{GS})$. This can again be done by stepping V_{GS}

.**dc** Vsg 3.667 4.667 1m

To produce a smooth plot, the the steps size of V_{SG} was decreased to 1 mV. V_{DS} is now fixed and can be set using the voltage source V_{SD}. The MOSFET is intentionally biased into the saturation region at $V_{DS} = -1\,\text{V}$ as can be seen in figure A.4.

LTSpice is now able to numerically differentiate the data, which can be invoked by by plotting

```
−d(Id(M1))
```

The minus sign comes from the inverted $V_{SG} = -V_{GS}$. To plot g_m over I_D, the formula for g_m given above needs to entered manually into the *Expression Editor* by right clicking the expression label on top of the graph. Finally, the x-axis must be changed to $Id(M1)$, leading to the plot in figure A.6.

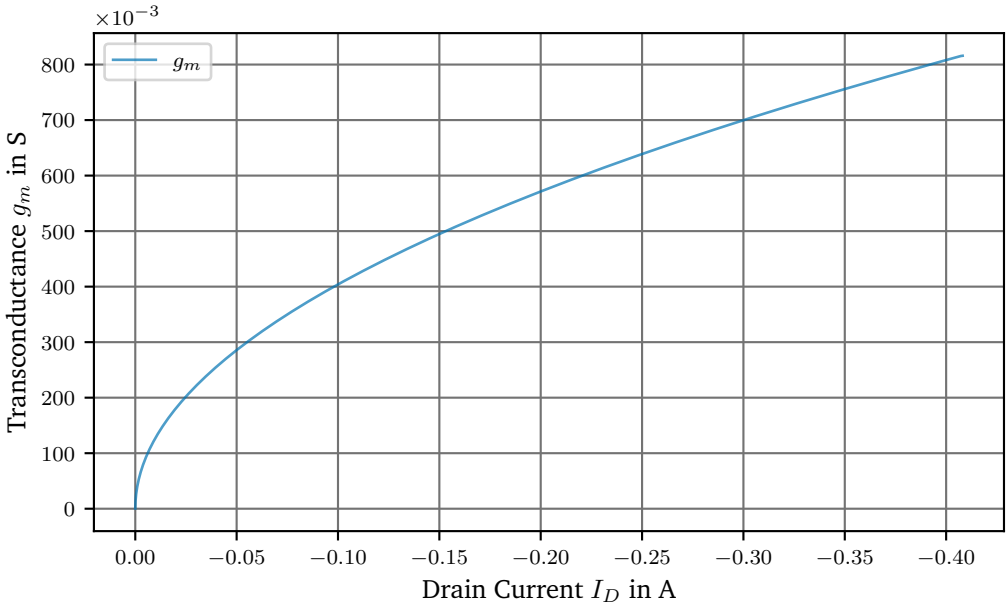


Figure A.6.: Simulated transconductance in saturation at $V_{DS} = -1\,\text{V}$.

As expected from equation 1.68, g_m is proportional to the square root of I_D when the MOSFET is in saturation.

As a sidenote, if the MOSFET model includes gate leakage, this leakage current may influce the calculation of g_m, especially at very low currents. In this case, it it better to plot the positive derivative of the source current $Is(M1)$, which does not include the leakage current.

```
d(Is(M1))
```

A.4.3. Output Impedance

This sections will explain how to calculate the dyncamic output impedance using LTSpice. The example circuit used, is the precision current source from section 1.8.4. The dynamic output impedance was defined in equation 1.71 as the inverse of the conductance leading to

$$R_{out} = \frac{1}{\frac{\partial I_D}{\partial V_{DS}}}\,.$$

Using the technique presented in the previous section, the obvious solution would be to again use the **.dc** sweep command and then numerically differentiate the result. Unfortunately this will lead to disappointing results, because the output impedance in question is very large and the limits of the numerical precision will be reached, nicely demonstrating the boundries of numercial methods. LTSpice allows to increase the numeric precision to double using the option **numdgt**

.**options** numdgt=15

Unfortunately, this only forces LTSpice to interally use the double floating point number format, which does have a precision of 53 bit which means $\log_{10}\left(2^{53}\right) = 15.95$ decimals. So instead of using the large-signal model of the MOSFET, it becomes more convenient to evaluate the small-signal model

$$R_{out} = \frac{v_{load}}{i_D} = \frac{v_{DS}}{i_D}$$

at several different points of V_{DS}, therefore reconstructing the large-signal model from rasterized versions of the small-signal model. For the small-signal model, $v_{DS} = v_{load}$, because the supply voltage and the voltage across the sense resistor can be considered constant, so any change in the voltage across the load must cause the opposite change in the source-drain voltage $v_{SD} = -v_{DS}$.

To run this simulation the small-signal simulation must be used and additionally some commands not available through the graphical user interface need to be entered by hand.

The LTSpice simulation is shown in figure A.7 and will now be explored.

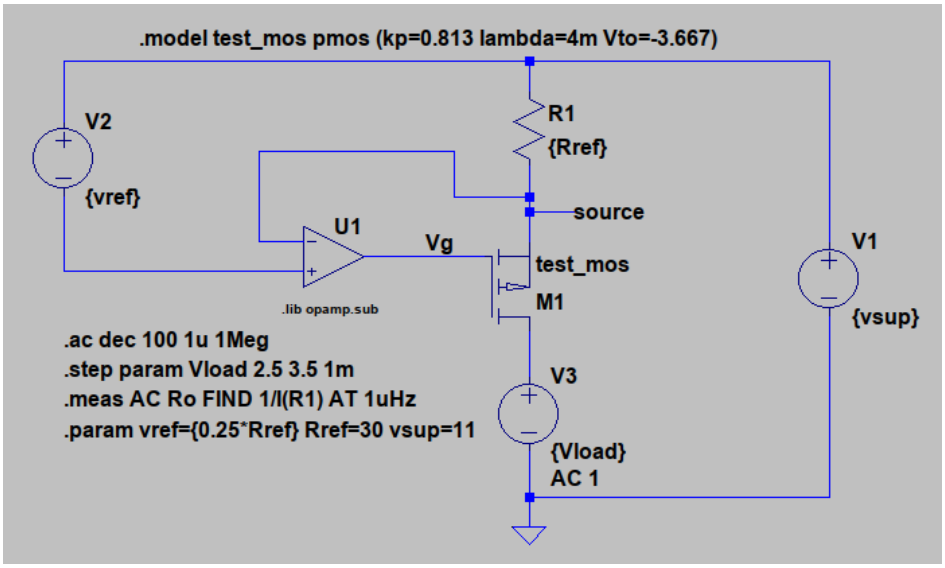


Figure A.7.: LTSpice model.

The simulation uses the same MOSFET model as above and adds an ideal op-amp to control the loop. The op-amp model has a open-loop gain of 2×10^6 and a gain-bandwidth product of 10 MHz as can be approximated from the the datasheet of the AD797 [90] and is also given in table 1.8. This leads to a 3 dB corner frequency of 5 Hz, which will be interesting later.

To access the small-signal model the **.ac** command is used, because LTSpice uses the small-signal model to calculate the ac response of a circuit at a given working point. The command

```
.ac dec 100 1u 1Meg
```

calculates the ac response from $1\,\mu\text{Hz}$ to $1\,\text{MHz}$ with $100\,\text{points/decade}$. Additionally, as discussed, the load will be stepped, by stepping voltage source in the source leg of the MOSFET. We use a voltage source in this case instead of a resistor, because the AC impedance of a laser diode is typically very small. For the working point, it does not matter whether V_{load} is resistive or not. To step the voltage source, the command

```
.step param Vload 2.5 3.5 1m
```

is used to change V_{load} from $2.5\,\text{V}$ to $3.5\,\text{V}$ in steps of $1\,\text{mV}$, which is exactly the maximum V_{DS}, which is $V_{sup} - V_{ref} = 3.5\,\text{V}$. This is done to show the effect of the complete loss of regulation. The last thing to do, is to extract the desired output impedance from the many stepped small-signal simulations. This can be done using the **.meas** command telling LTSpice to save a single value at certain frequency from each step.

```
.meas AC Ro FIND 1/I(R1) AT 1uHz
```

The **.meas** command shown will save the value of $\frac{1}{i_D} = \frac{1}{I(R1)}$ at $1\,\mu\text{Hz}$ to the (error) log file whenever the **.ac** command is run. The value of v_{DS} was already set to $1\,\text{V}_{\text{rms}}$ in the LTSpice simulation as shown in figure A.7, thus $\frac{1\,\text{V}}{I(R1)} = R_{out}$. The current through sense resistor instead of i_D was chosen because it is numerically more stable and since there is no gate current it is the same as i_D. The frequency were the R_{out} is measured was chosen to be well below the corner frequency of the op-gain, which was calculated above to be $5\,\text{Hz}$. This gives the near DC output impedance of the current source.

To plot the values stored in the log file, click on *View* in top menu, then *SPICE Error Log*. Now right-click on the error log and select *Plot stepp'ed .meas data*. This will open a new plot window showing the output impedance curve.

Those results are discussed in more detail in section 1.8.5.

A.5. MOSFET Noise Sources

This section gives the reader a quick overlook of the noise sources found in MOSFETs. A good overview of different types of noise in MOSFETs can also be found in [51] and goes beyond the scope presented here.

The MOSFET wideband noise can be attributed to thermal noise in the channel [16]. Der Ziel developed a model for the thermal noise in the saturation region of the MOSFET, while the classic Johnson–Nyquist noise [37] can be used for the ohmic region as it behaves like a voltage controlled resistor. This results in the noise density of

$$i_{n,thermal} = \begin{cases} \sqrt{4k_B T \frac{2}{3} g_m} & \text{saturation} \\ \sqrt{4k_B T g_{DS}} & \text{ohmic} \end{cases} \tag{A.12}$$

Using the example parameters from table 1.8, one finds

$$\begin{aligned} g_m &= \sqrt{2\kappa I_D \left(1 + \lambda V_{DS}\right)} = 0.642\,\text{S} \\ T &= 25\,^\circ\text{C} \end{aligned}$$

$$i_{n,thermal} \approx 83.9\,\text{pA}/\sqrt{\text{Hz}}\,, \tag{A.13}$$

the equivalent noise of a resistor $R_D = \frac{3}{2g_m} = 2.3\,\Omega$.

A more detailed analysis, which also points out the limits of the model above can be found in [88].

Additionally the MOSFET also suffers from shot noise due to leakage through the gate, but this can be neglected because this leakage current is very small and even a relatively large current of $1\,\text{mA}$ only produces

$$i^2_{n,shot} = \sqrt{2eI_D} \tag{A.14}$$

$$\approx 1.8\,\text{pA}/\sqrt{\text{Hz}}\,. \tag{A.15}$$

Shot noise becomes interesting, when the MOSFET is used well below threshold or at higher frequencies, because, then the parasitic gate-drain capacitor C_{GD} will leak from the input to the ouptut as can be seen in figure A.8. Figure A.8 shows the different parasitic capacitances of a MOSFET.

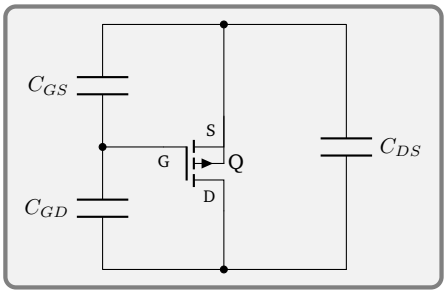


Figure A.8.: Parasitic capacitances of a MOSFET.

These capacitances can also be found in datasheets, although not directly, because there they are defined as

$$C_{iss} = C_{GD} + C_{GS} \quad \text{input capacitance} \tag{A.16}$$

$$C_{oss} = C_{DS} + C_{GD} \quad \text{output capacitance} \tag{A.17}$$

$$C_{rss} = C_{GD} \quad \text{reverse transfer capacitance}\,. \tag{A.18}$$

Regarding low frequencies, MOSFETs also show strong flicker noise. We know from section 1.6.1, that the sources of flicker noise are not clearly understood, so there are several theories regarding flicker noise models for MOSFETs.

An an empirical model given by [51, 67] can be used to describe the flicker noise as

$$i_{n,flicker} = \sqrt{\frac{K_f I_D}{C_{ox} L^2} \frac{1}{f}} \,. \tag{A.19}$$

This model is presented here, because it is also supported and easy to implement in LTSpice. While the parameter K_f is approximately $2 \times 10^{-10}\,\text{fC}^2/\mu\text{m}^2$ [51] for p-channel MOSFETs, the gate width and length W, L are device specific und unfortunately not given by the manufacturers. The typical corner frequency for MOSFETs, though, is between a few hundred kHz and a few dozen MHz depending on the size of the transistor. Larger transistors tend to show lower noise. Hence older processes are prefered in this regard. Given that the noise is uncorrelated, the total noise of the MOSFET in saturation can be written as

$$i_n = \sqrt{4k_B T \frac{2}{3} g_m + \frac{K_f I_D}{C_{ox} L^2} \frac{1}{f}} \tag{A.20}$$

As a reminder, the MOSFET is a (transconductance) amplifier, that takes a voltage at the input and outputs a current. To make the noise figures comparable, the noise is divided by the gain g_m. This called the input referred noise. The input referred (voltage) noise e_n is given by:

$$e_{n,thermal} = \sqrt{4k_B T \frac{2}{3 g_m}} \tag{A.21}$$

$$e_{n,flicker} \overset{1.69}{\approx} \frac{K_f}{2\kappa C_{ox} L^2} \frac{1}{f} \tag{A.22}$$

We can see, that flicker noise is fully determined by process parameters in this model.