Tutorial 1: Processors and Caching

Question 1: Pipelining

Consider the pipelined execution of the following operations:

```
R4 = R3 + R2
R7 = R6 | R5
R8 = R7 – R4
```

1. How many clock cycles would it take to complete these operations on a canonical RISC machine with no operand forwarding?
2. How many clock cycles would it take if the EX stage output could be forwarded to its input?
3. How many clock cycles would it take if the EX and MEM stage outputs could be forwarded to the EX input?
4. Now assume that the second operand of the OR has to be fetched from L2 Cache with a 10 cycle latency and loaded in to R5 before use. Draw pipelining diagram[1] with four operations in flight, showing the duration of the stall and how long the execution would take overall now

Question 2: Caching

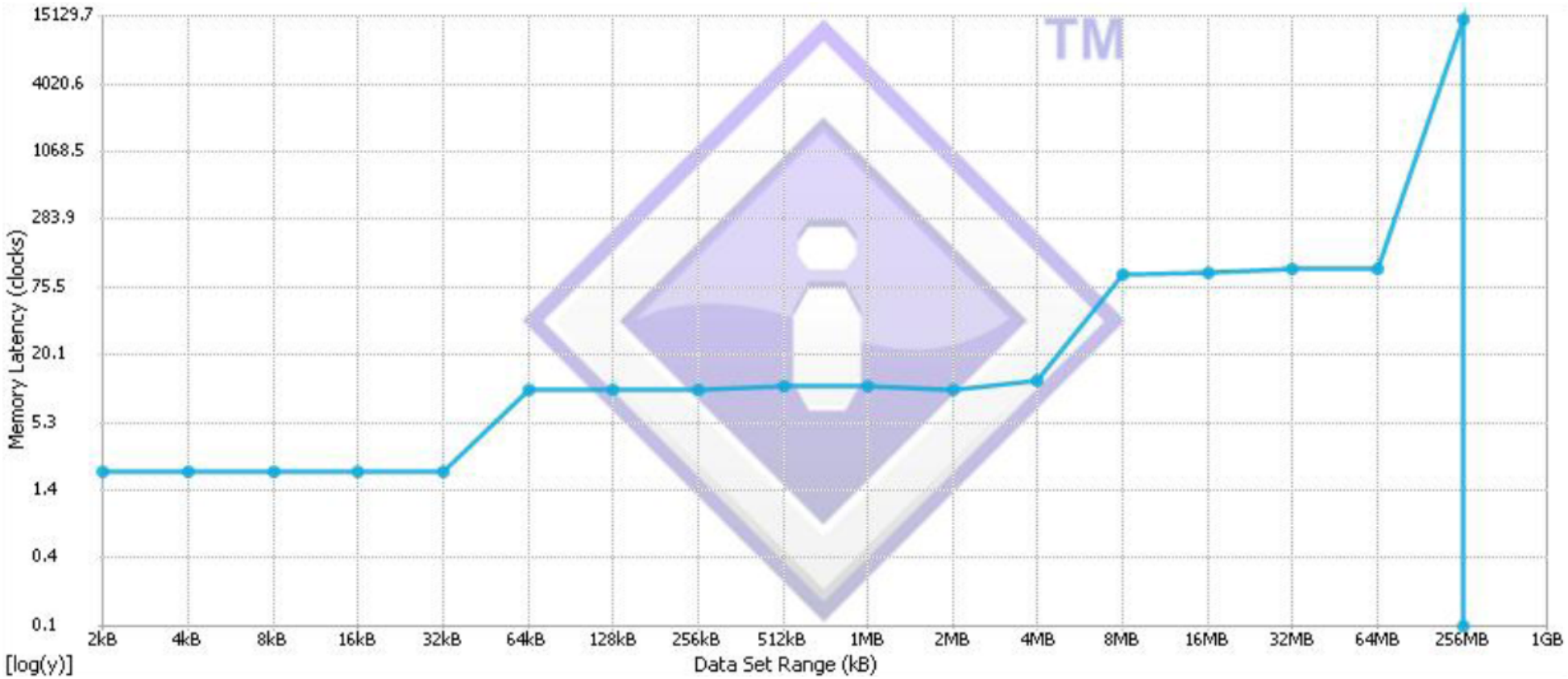
Referring to the memory access latency benchmark on the next slide (and ignoring the last point at 0 which is a bug in the plotter!), answer the following:

1. How many levels of cache does the processor have and (roughly) how big is each one? How big is Main Memory (RAM)?
2. One of the caches is 6MB, is it most likely to be Direct or Associative?

The plot is of steady-state sequential access latency. That is, a loop is run that accesses each memory location in turn, from address 0 up to the length under test. This loop is run several thousand times in succession and latency of each access timed and averaged. This means that any different timing on the first run through can be ignored.

Note that these values are only sampled at the discrete points marked. The lines between points are for visual purposes only.

1http://eng.anu.edu.au/courses/ENGN8537/notes/es03-processors.html#/step-22


15129.7
4020.6
1068.5
283.9
75.5
20.1
5.3
1.4
0.4
0.1
[log(y)]
Memory Latency (clocks)
2kB
4kB
8kB
16kB
32kB
64kB
128kB
256kB
512kB
1MB
2MB
4MB
8MB
16MB
32MB
64MB
256MB
1GB
Data Set Range (kB)
TM