School of Science, Engineering & Technology

Assessment 4 (Prerequisite part): Printed Circuit Board (PCB) Design and Construction

EEET2602: Engineering Design 2

Aims

This is the **prerequisite part** of the Assessment 4: Group Design Project Report on Final Circuits.

The aims of Assessment 4 are:

- Aim 1: To design a Voltage Regulated Power Supply.
- Aim 2: To design a Printed Circuit Board (PCB) of this circuit in Cadence PCB editor.
- Aim 3: To Construct and Experimentally Test the functionality of this PCB.

This part will cover Aim 1 and Aim 2. This is not a marked assessment but based on the submission of students' Gerber files in this assignment, the school technicians will manufacture the PCBs, and that only if the students have the PCBs available, they can process to the next steps of the Assessment 4.

References

- N. Mohan, T. Undeland and W. P. Robbins, *Power Electronics, Converters, Applications and Design*, 3rd Edition, Wiley, New York, 2003.
- S. Sedra, K. C. Smith, *Microelectronic Circuits*, 6th Edition, Oxford University Press, 2011.
- National Semiconductor, "LM1576-ADJ/LM2576-ADJ Simple Switcher™ 3 Amp Step-Down Voltage Regulator", TL/H/11052 datasheet, Dec. 1990.
- On Semiconductor, "Surface Mount Schottky Power Rectifier", MBRS340T3/D datasheet, Aug. 2021.

Equipment

- Laboratory equipment: Digital Multi-Meter (DMM), Voltera V-one PCB Milling machine
- Circuit board components: normal diodes (D1, D2, D3, D4), Schottky diode (D5), Linear Regulator IC (U1), capacitors (C1, C2, C3, C4), resistors (R1, R2, R3, R4), inductors (L1, L2)

Safety

- The lab session will be strictly supervised by the Course Coordinator.
- You are required to show the circuit and get permission first before powering up the circuit.
- Unauthorized experiments or procedures **must not** be attempted.

1 Design requirements

Students are required to design a PCB for the schematic shown in Figure 1 below.

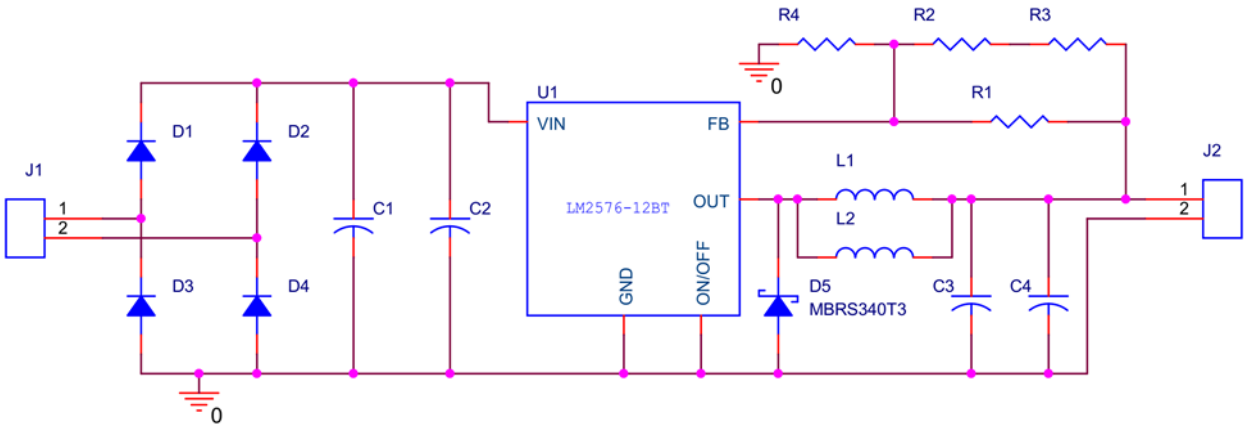


Figure 1. Linear Voltage Regulator Schematic

Students will need to make use of the design process which were taught in the and to design the PCB with dimension of 80mm x 50mm as shown in Figure 2. Components' names and some of the footprints' hints are given in Table 1.

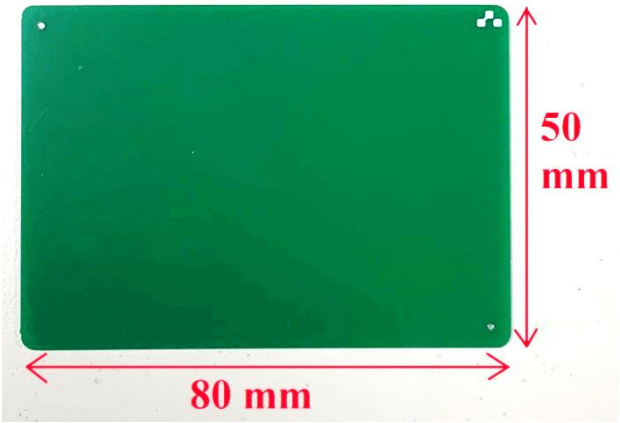


Figure 2. PCB dimensions

Table 1. Components used in the Linear Voltage Regulator board

Device	Model	Name on Schematic	Footprint type
Diode (normal)	1N4001	D1, D2, D3, D4	Find it yourself by measuring from the parts I gave you
Diode (Schottky)	MBRS340T3	D5	Find it yourself from the datasheet
Linear Regulator IC	LM2576	U1	Find it yourself from the datasheet
Inductor	220uH	L1, L2	INDP125125X600N
Capacitor	330uF	C1, C2, C3, C4	Find it yourself by measuring from the parts I gave you
Resistor	8.2kΩ	R3	Find it yourself by measuring from the parts I gave you
Resistor	1.3kΩ	R4	Find it yourself by measuring from the parts I gave you
Resistor	2.4kΩ	R1, R2	Find it yourself by measuring from the parts I gave you
Header	Header2	J1, J2	Jumper2

Design the PCB layout of the circuit, with the following constraints:

- Minimum trace width: 30 mils
- Minimum hole diameter: 30 mils
- Minimum pad zize: 90 mils
- Maximum space between components: 200 mils
- Design must be 1-side (choose TOP or BOTTOM layer only)
- Team's Number must be shown in your design

2 Special Hints

2.1 Footprint of the inductors, Schottky Diode MBRS340T3, and IC chip LM2576

The process of footprints choosing is time-consuming and that it requires a lot of effort to work out on it. Randomly picking a footprint or choosing a footprint without careful consideration can lead to inappropriate footprint that is not well-fit with the component, causing the PCB stop working, and resulting in the failure of Assessment 4. While you spent your time to measure the pads, look up on the PDF file about footprints that is available on Canvas, you may find it impossible to find out the footprint for our inductors L1 and L2. In the actual design, engineers will need to create the footprint by themselves. However, you are now at the "beginner" level of PCB design, creating the footprint may be overwhelming for you. Therefore, I give you the footprint for the inductors. Below are the steps to import the new footprint into your design library:

- Step 1: Download the ZIP files here: https://rmit.instructure.com/courses/104898/pages/eeet2602-assessment-4-pcb-footprint
- Step 2: Extract the ZIP file, you will see that there are 3-4 files (1 .DRA file, 1 .PSM file, and 1 or 2 .PAD file) in each ZIP file.
- Step 3: Copy all the files mentioned in Step 2 and paste them into the folder: **C:\Cadence\SPB_17.2\share\pcb\pcb_lib\symbols**

Now you successfully have the footprint for your inductors, Schottky Diode, and IC chip LM2576.

2.2 Routing and Spacing

The trace (also known as line) is the connection lines between pins of components in the PCB as shown in Figure 3. The trace width can be set when do routing (connecting pins). In PCB editor, from the toolbar select the symbol Add-connect  → set the Line width to minium of 30 mils.

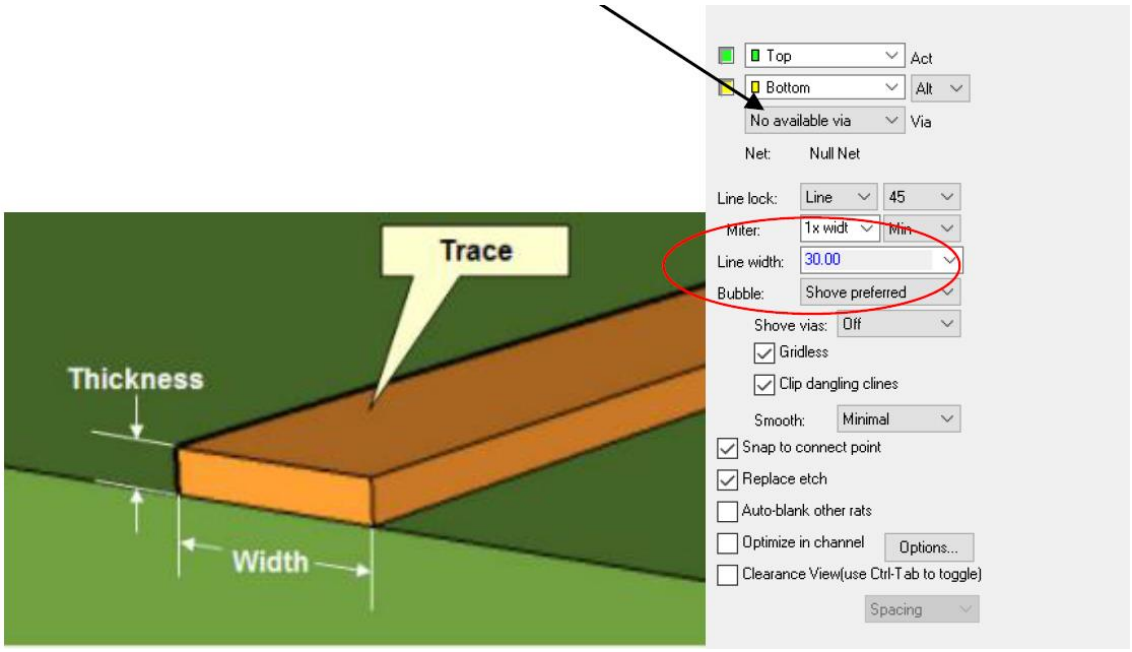


Figure 3. Tracing and Routing

The spacing between all components can be checked by setting the grid with the spacing of top and bottom layer of 200 mils (from menu bar, select Setup->Grids). For this assessment, the maximum spacing of two components is 200 mils.

2.3 Hole size and Pad size

The hole size and the pad size are shown in Figure 4.

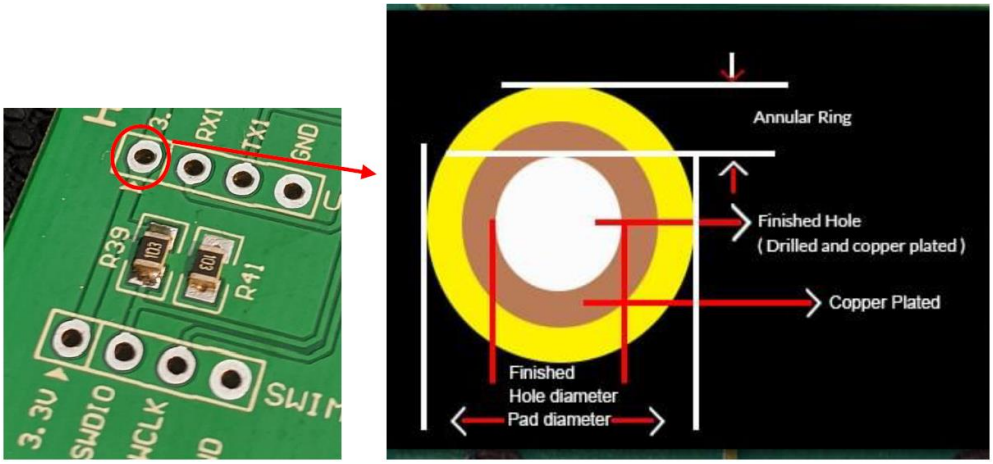


Figure 4. Holes and pads

In PCB editor, from the menu bar, select Tools → Padstack → Replace and then move the pointer to every pad of all components. For example, the pad can be seen as in Figure 5, the padstack name is PAD60CIR36D (pad diameter 60 mils, hole diameter 36 mils, the pad is circle). This pad can be replaced clicking the symbol "…" to find the suitable pad from the library. Check the pad of all components to ensure that the hole diameter >30 mils and the pad diameter >90 mils.

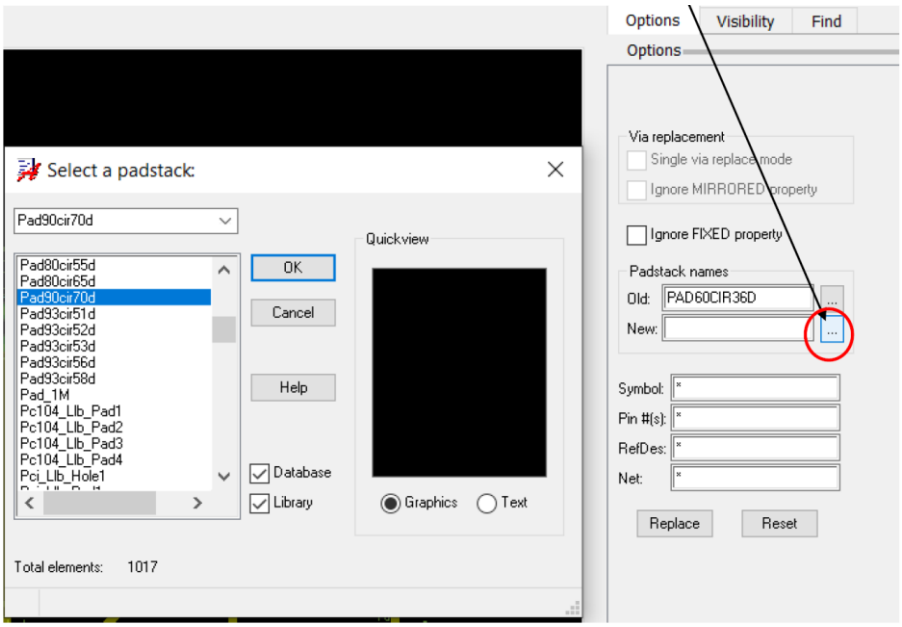


Figure 5. Padstack dialogue

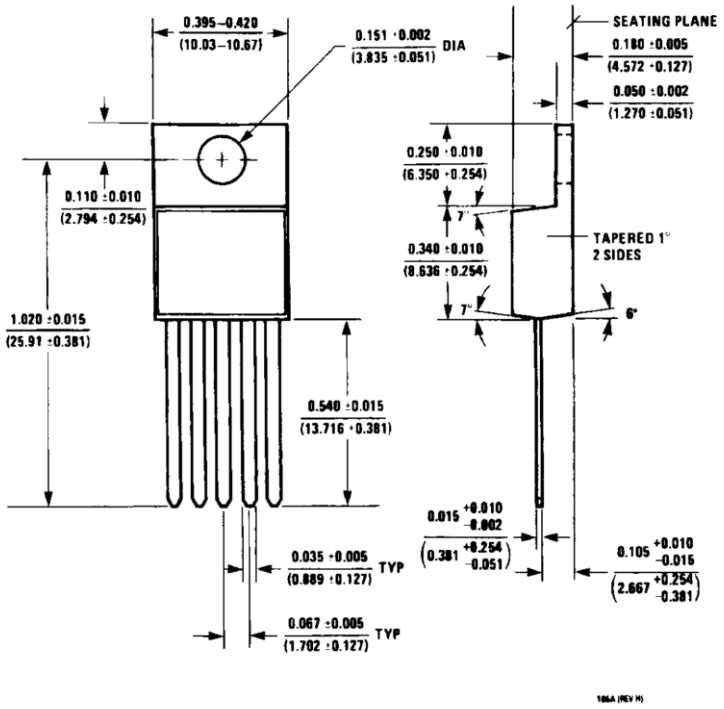
3 PCB Design Submission

For your PCB Design submission, you need to: generate a compressed Gerber file (MUST BE ZIP ONLY, no RAR files allowed) AND submit it onto Canvas. The file must be named with the following convention: **EEET2602_AS4_TeamNumber_PCB_Gerber.zip**

The ART files you MUST compressed into your zip file are: BOARD_OUTLINE, BOTTOM, TOP, SILKSCREEN_TOP, SILKSCREEN_BOTTOM, SOLDERMASK_BOTTOM, SOLDERMASK_TOP, and the DRL file. So, totally 8 files in the ZIP compressed file.

4 Appendix 1: LM2576 Linear Voltage Regulator IC datasheet

Physical Dimensions inches (millimeters) (Continued)



5-Lead TO-220 (T)
Order Number LM2576T-ADJ
NS Package Number T05A

5 Appendix 2: MBRS340T3 Schottky Diode datasheet

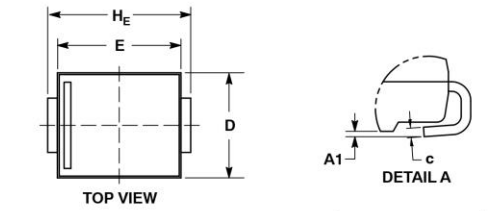
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

SCALE 1:1

SMC 2–LEAD
CASE 403AC
ISSUE B

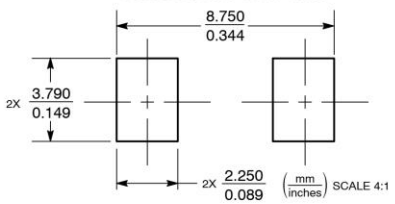
DATE 27 JUL 2017



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.254mm PER SIDE.
4. DIMENSIONS D AND E TO BE DETERMINED AT DATUM H.
5. DIMENSION b SHALL BE MEASURED WITHIN THE AREA DETERMINED BY DIMENSION L.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	1.95	2.61	0.077	0.103
A1	0.05	0.20	0.002	0.008
A2	1.90	2.41	0.075	0.095
b	2.90	3.20	0.114	0.126
c	0.15	0.41	0.006	0.016
D	5.55	6.25	0.219	0.246
E	6.60	7.15	0.260	0.281
HE	7.75	8.15	0.305	0.321
L	0.75	1.60	0.030	0.063

RECOMMENDED
SOLDERING FOOTPRINT*



*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC
MARKING DIAGRAM*

XXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb–Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb–Free indicator, "G" or microdot " ▪", may or may not be present.