[**4**]4.1224On the left,Threshold voltage variation with the fin-height at 30nm of T_{fin}. On the right, Short Channel Effects variation with fin-height at 30nm of T_{fin}[**4**]figure.caption.30

SCALING LIMITS OF FINFET STRUCTURE

Integrated Systems Technology

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Contents

Chapter 1

INTRODUCTION

1.1 SOI FinFET Technology

The SOI technology has given a great impulse to the development of new devices such as FinFETs that nowadays are substituting standard planar transistors.
The advantage of FinFET technology is to overcome the problem of SCE (Short Channel Effect) and especially the influence of DIBL (Drain Induced Barrier Lowering) when scaling the device over a certain lengths.

The FinFET is able to reduce the I_{off} because the thinner channel of the device allows to have a better control of the own current. In fact in the case of bulk planar transistors the channel area underneath the gate is too deep and part of the channel is too far away from the gate to be well-controlled, and the result is higher leakage power (static/stand-by power). This benefit of FinFET allows for reductions of threshold voltage and hence supply voltage. Moreover the device exhibits little or no body effect because FinFET channels are fully depleted.

1.1.1 FinFET preparation

The basic process to produce FinFET follows this step: atomic layer deposition (ALD) for gate dielectric; deposition of PolySilicon gate depletion; gate etching; Si_3N_4 for spacers; S/D implant (light blue part in fig.1.1) and silicidation. To prepare the fin (blue part in left fig.1.1), which is the treaky part of the process we can choose to similar methods: **SIT** (sidewall image transfer) or **SAQP**(self aligned quadruple patterning).

These methods consist on photoresist deposition on amorphous Si (this layer is called Mandrels) and is used to prepare the spacers of SiO_2. Than removal of Mandrels (etching Si) and etching also the hard mask to expose the fin. The key point of the procedure is that is not photolitography process but a controlled etching process and the width of the fin is lower than the precision allowed by photolitography.
For a good electrostatic control (to mantain $DIBL < 100\frac{mV}{V}$) we must have the Fin thickness (FT) lower than half of the gate length:

$$FT < \frac{L}{2}$$

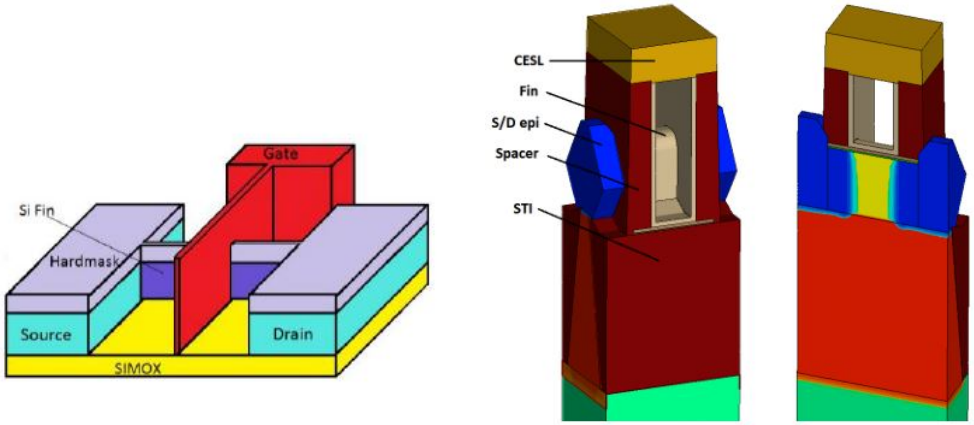

Figure 1.1: Finfet structure (left). Finfet structure with cross section with validate dopant activation (right)

1.2 Advantages of SOI Finfet

FinFET can be made with the same process from *bulk* silicon to reduce the cost of the process, but is less ideal and the SOI one is much better from electrical point-of-wiew and simpler since we dont need to dope the Si under the fin to create p or n MOS.

Using SOI wafer we have no problem of insulation and we don't need to define active areas.

Chapter 2

DOUBLE GATE FINFET SCALING

2.1 Introduction

Several analytical models already present in literature were implemented in MATLAB [3]. The aim was to realize an electrostatical analysis of a DG FinFET and to investigate on advantages and limits of such three-dimensional FET. The implemented models were used to analyze long channel and short channel FinFET, so that a scaling behaviour of FinFET could be studied.

Next sections will be dedicated to the theoretical explanation of some of technological problems linked with scaling, than results on simulations of such models will be analyzed.

2.2 Finfet scaling properties

The considerations taken in this chapter are extracted by [4][2].

Also known as self-aligned double-gate MOSFET, FinFET has a vertical multi-gate structure that allows superior electrostatics over gate control, thus reducing the short channel effect and allowing the VLSI (very large scale integration) to continue.
The name FinFET comes from a vertical fin-like channel that is surrounded by the self-aligned gate like showed in 1.1

FinFET replaced the planar MOSFET and became the industry standard because of their similarities. Majority of the fabrication steps are similar if not the same as in a making of the MOSFET, meaning that the technology is already tested and developed. In addition to physical properties, the properties of the model itself will also be discussed. There are numerous differences to conventional models that have to be taken into account when simulating on such a small scale objects, because some of the simplifications applied on the larger scale transistors are now producing significantly bigger errors compared to empirical results.

The table 2.1 contains some of the key dimensions that characterize the FinFET. It's possible to see that they don't scale uniformly since manufacturing process of the nanometer dimensions has different problems.

Tech. node	Gate length	W_{bottom}	W_{top}	Fin Height
22nm	25	17	17	40
14nm	25	15	5/10/15	35
10nm	20	8	8	27
7nm	15	7	5	30

Figure 2.1: Characteristic dimensions of all four technology nodes(nm)[4]

The table 2.2 shows like the doping profile concentration changes according to technological scaling. Source and drain concentration remains similar taking more attention to steep doping profile in order to avoid diffusion phenomena.

Channel doping concentration changes since constant downsize of the channel dimensions requires smaller number of dopants to achieve the same concentration. The number of dopants became so small that their behavior is not statistically predictable anymore.
Channel dopants became an error source, so a need for an undoped channel region arise especially for technological nodes 10 nm and 7 nm.

Tech. node	S/D	Channel	Channel stop
22nm	1.5e+20	1.5e+19	1.5+19
14nm	2e+20	2e+18	2e+18
10nm	2e+20	1e+15	2e+18
7nm	1e+20	1e+15	2e+18

Figure 2.2: Overview of doping profiles for all four technology nodes (cm^3)[4]

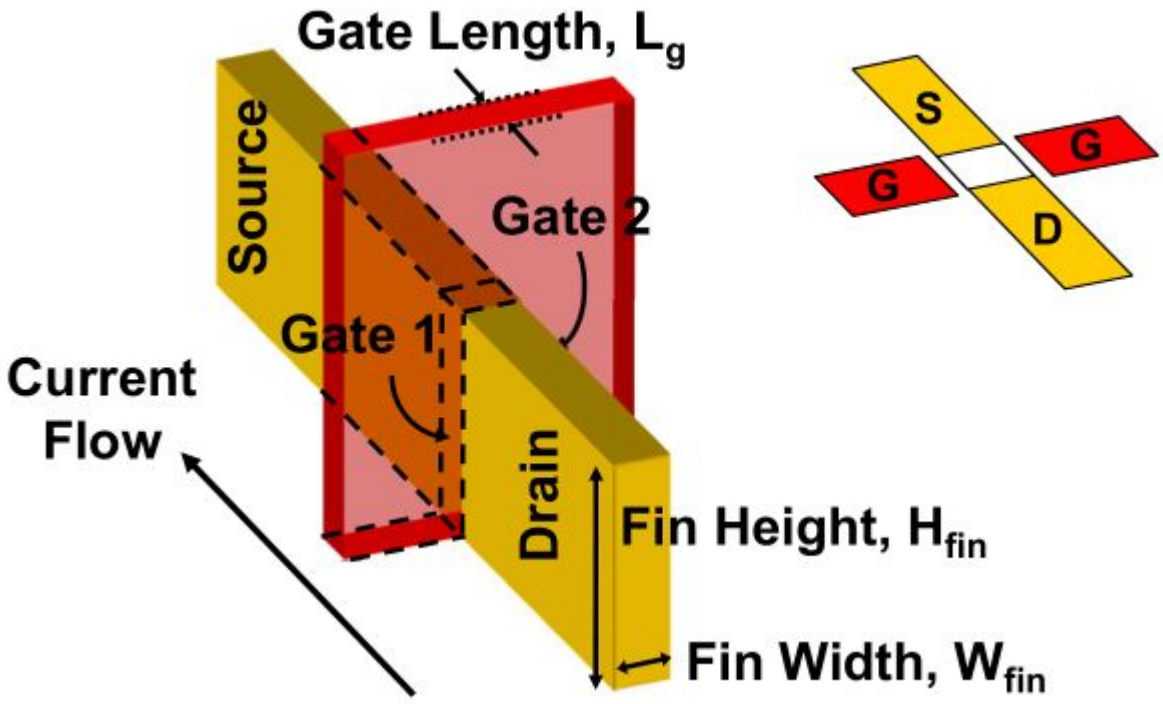

Figure 2.3: Finfet double gate main geometric parameters

2.2.1 Low-power, standard performance and high performance FinFET

Nowadays application requires to achieve low power consumption as good performance especially in battery based application. A key role can be changing working function of transistors. Three different modes by changing the metal gate work function can be obtained as in fig. 2.4.

The last one is proportional to gate barrier height and thus to the threshold voltage of the transistor. To create a low-power device, reducing leakage currents is a crucial importance step, which can be achieved through higher threshold voltage.

On the other hand, lower threshold voltage makes higher drain current possible as well as shorter response time, both crucial for a high performance device. The threshold voltage can also be adjusted with the gate length of the transistor, what is certainly a less effective option then workfunction modulation that is anyway a part of the production process since two different band gaps for pMOS and nMOS are created anyway.

Doping adjustments are also possible but unwanted in the manufacturing process so the multi workfunction remains the best approach, in fig. 2.4 is represent an nFINFET comparison of drain current in different modes such as linear, saturation and off current with different workfunctions.

The fin height can also play a significant role in the power/performance trade-off. Namely, tall fins can increase the transistors delay what is definitely an unwanted effect when it comes to high performance FinFETs.

At the same time, taller fins lower the leakage current thanks to their electrostatic superiority. Some chips use two different fin heights for this purpose: taller for LP and shorter for HP.

The simulation of the device varying the fin height will be done in the next section. Contrary the workfunction will be constant in our simulation

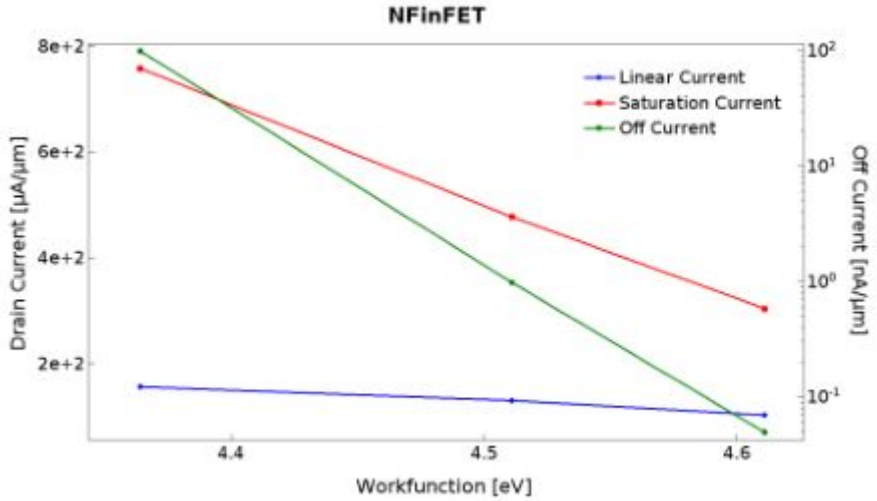

Figure 2.4: different-mode-operations[4]

2.2.2 Fin width & Fin height

The production of a narrow fin with consistent dimensions is a challenging process. Narrower fin would permit further gate scaling but the $R_{S/D}$ increases due to the implant damage.

The image 2.5 shows this dependancy for different technology. It is possible to see that nMOS suffers severely from fin width scaling respect to pMOS this because the poorer re-crystallization of As-implants compared to BF_2 after the extension implantation/activation.

To improve this problem different techniques can be explored like the optimizer implant and annealing process. This improvement did not only reduce the extension resistance, but the drain-induced barrier lowering (DIBL) and I_{on}/I_{off} ratio have also been improved.

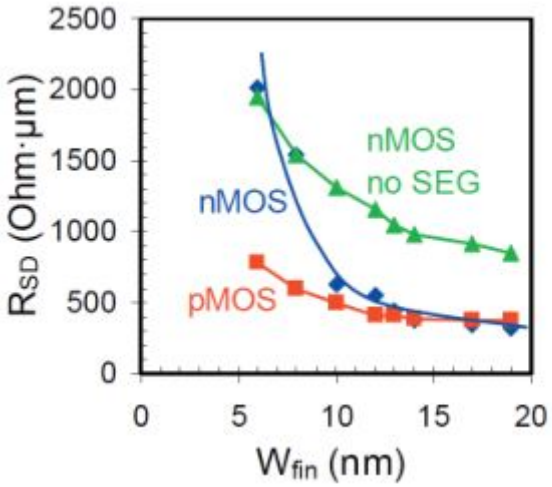

Figure 2.5: Resistance vs fin-width

Another important key metric is linked to a physical parameters : threshold voltage roll-off. The fin width (W_{fin}) and height (H_{fin}) influence threshold voltage.

In particular is important that these parameters shows a ratio higher enough to produce a fin-like structure. The critical height needed for the saturation depends on the fin width so that larger W_{fin} requires larger H_{fin} to reach saturation.

It is fundamental to know this problem in charge to avoid that device exhibits characteristics much closer to the planar MOSFET when the fin width is much larger than the fin height.

The simulations in next section show the different behaviour in SCE varying the fin width and fin height (fixing the other parameters).

2.2.3 Fin shape

The last point is the relationship between SCE with fin-shape.

The rectangular-cross-section channel device showed almost ideal subthreshold slope, where in the trapezoidal and triangular cross-section-channel devices an increase in subthreshold slope and off current were observed.

But the problem is that rectangular fin-shape involves in unwanted corner effects in the fin. Corner effect occurs because of the higher electrical field density in the corners of the fin, causing the premature inversion. That means that corners have lower threshold voltage than the rest of the fin, creating independent channels with different threshold voltages.

Optimization of the fin shape is one of key considerations for a FinFET performance. As already mentioned at the previous node, fin should have rounded corners in order to avoid unwanted corner effect. Tapered fin is suggested and three different shapes are take into account showed in figure 2.6.

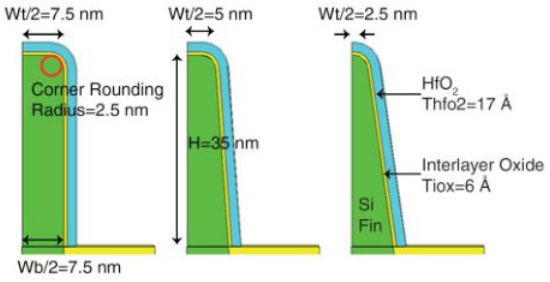

Figure 2.6: three-different-shapes-14nm[4]

All three fin shapes have fin width of 15 nm at the bottom (W_b), one fin shape has the same width at the top (W_{top} = 15 nm), other two fins are linearly shrinking to W_{top} = 10 nm and W_{top} = 5 nm creating a tapered fin shape. The heights is fixed for all cases.

Fin shape has to be investigated together with the fin body doping concentration. The trade-off comes from the fact that insufficient fin body doping leads to the increase in SCE leakage current under the active fin region and decrease in the GIDL due to BTBT at the interface between the drain and the fin body.

Different fin shapes achieve different values of both of the unwanted effects, so the optimal doping concetration must be met. Different key metrics are analyzed for different fin-shape like showed in figure 2.7

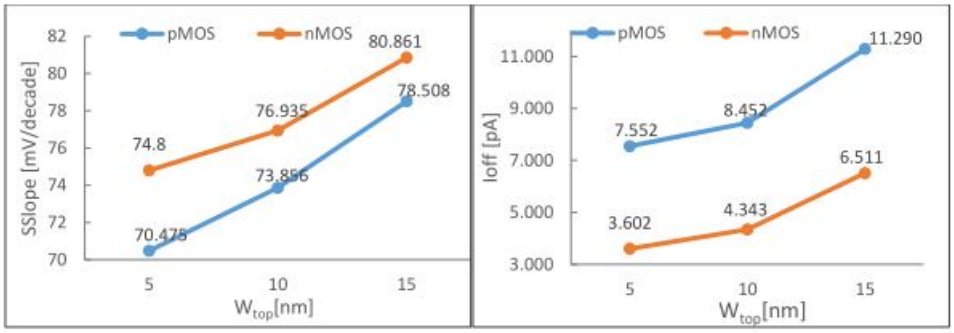

Figure 2.7: SS and leakage current properties 14 nm[4]

Three main aspect can be highlighted in the image 2.7

1. It is clearly observable that the tapered fin shape exhibits superior characteristics over the rectangular cross-sectional fin shape.
2. lower I_{off} when fin area decreases
3. The ratio between I_{on} and I_{off} rises when W_{top} decrease because the I_{oon} decreases slower than I_{off}

The simulations in next section show the different behaviour in SCE varying the W dimension for a rectangular cross section (fixing the other parameters).

2.2.4 Mobility

The model of mobility required the knowledge of the temperature and of the total silicon doping N to obtain the value of μ_e from the following empirical relation:

$$\mu_e = 88T_n^{-0.57} + \frac{7.410_8 T_{-2.33}}{1 + [N/1.2610^{17} T_n^{2.4}]0.88T_n^{-0.146}} \tag{2.1}$$

Some mobility curves obtained from our simulations for different temperatures and as a function of the doping level are depicted in 2.8

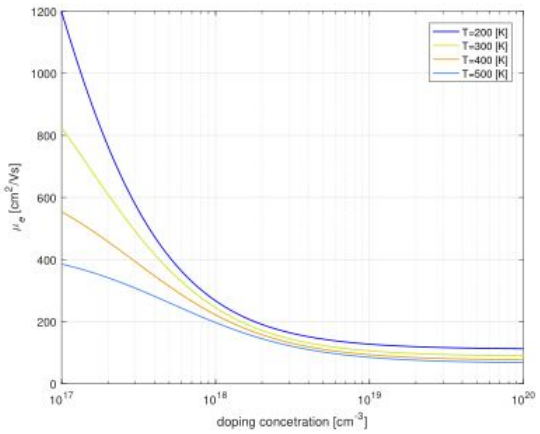

Figure 2.8: mobility-temperature-model

Since we have found some possible acceptable doping values for different scaling we want evaluate which is the corresponding μ_e. The values of evaluated doping are the ones in table 2.1

Node(nm)	Channel doping(cm^3)	mobility road map(cm^2/Vs)	mobility computed(cm^2/Vs)
22	1.5e+19	250	99.83
14	2e+18	200	171.63
10	1e+15	150	1350
7	1e+15	120	1350

Table 2.1: Mobility scaling calculation

For other experiments we take into account fixed value for mobility equal to 200 (cm^2/Vs). Taking it fixed we want to evaluate which is the impact of others parameters (geometrical ones) showed in fig. 2.1

Chapter 3

MODELING OF DOUBLE GATE FINFET

3.1 Taur model

A Double Gate FinFET can be modeled as first approximation as a very thin body DG MOSFET. Considering this, a continuous analytic IV model is derived using Pao-Sah integral with no charge sheet approximation [3].

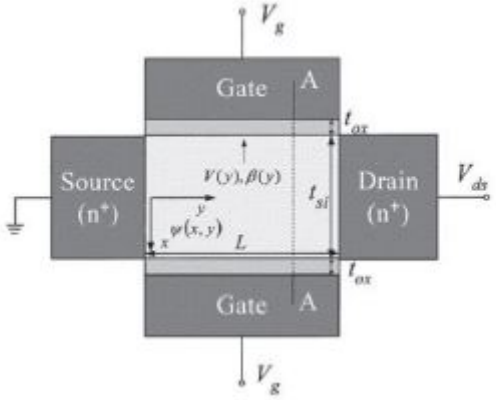

Figure 3.1: Schematic diagram of DG-MOSFET[3]

3.1.1 Model description

This model presents a continuous analytic current–voltage (I–V) model for double-gate (DG) MOSFETs. It is derived from closed-form solutions of Poisson's equation, and current continuity equation without the charge-sheet approximation. The entire $I_{ds} = (V_g, V_{ds})$ characteristics for all regions of MOSFET operation: linear, saturation, and subthreshold, are covered under one continuous function, making it ideally suited for compact modeling.

If cutting along the vertical direction of the Si film is done, Poisson's equation can be derived as follows:

$$\frac{d^2\phi}{dx^2} = \frac{q}{\epsilon_{si}} n_i exp \frac{q(V-\phi)}{kT} \tag{3.1}$$

where ϕ is the electrostatic potential, q is the electronic charge, n_i is the intrinsic carrier density, ϵ is the silicon permittivity, kT/q is the thermal voltage, and V is the electron quasi-Fermi potential.

By integrating twice the above expression, surface potential can be evaluated:

$$\phi(x) = V - \frac{2kT}{q} ln \left[\frac{t_{si}}{2\beta} \sqrt{\frac{q^2 n_i}{2\epsilon_{si} kT}} \cos \frac{2\beta x}{t_{si}} \right] \tag{3.2}$$

The current can be derived integrating I_{ds} on dy and expressing dV/dy as (V/$d\beta$)(dβ/dy). So, Pao-Sah's integral can be written as:

$$I_{ds} = \mu \frac{W}{L} \int_0^{V_{ds}} Q_i(V) dV = \mu \frac{W}{L} \int_{\beta_s}^{\beta_d} Q_i(\beta) \frac{dV}{d\beta} \tag{3.3}$$

Where β_s and β_d are the solutions of β equation, respectively for V=0 and $V = V_{ds}$. Solving the β function as function of the gate voltage, this analytical model lead the evaluation of the FET characteristic for all operating regions.

The results are showed in the following lists where the parameters are explained in the table 3.1:

- Linear current

$$I_{ds} = 2\mu C_{ox} \frac{W}{L} (V_g - V_t - \frac{V_{ds}}{2}) V_{ds} \tag{3.4}$$

- Saturation current

$$I_{ds} = 2\mu C_{ox} \frac{W}{L} [(V_g - V_t)^2 - \frac{8\epsilon_{ox} t_{ox} k^2 T^2}{q^2 \epsilon_{ox} t_{ox}} \exp \frac{q(V_g - V_0 - V_{ds})}{kT} \tag{3.5}$$

- Subthreshold current

$$I_{ds} = \mu \frac{W}{L} kT n_i t_{si} \exp \frac{q(V_g - \Delta\varphi)}{kT} (1 - \exp \frac{qV_{ds}}{kT}) \tag{3.6}$$

The Threshold voltage V_t can be expressed in the following way :

$$V_t = V_0 + \delta \tag{3.7}$$

where V_0 and δ can be described in the following way :

$$V_0 = \Delta\phi + \frac{2kT}{q} \left[ln \frac{2}{t_{si}} \sqrt{\frac{2\epsilon_{si} kT}{q^2 n_{si}}} \right] \tag{3.8}$$

$$\delta = \frac{2kT}{q} ln \left[\frac{(V_g - V_0)q}{4rkT} \right] \tag{3.9}$$

δ is a second-order effect (0.05 V).

Symbols	Description
ϕ	electrostatic potential
n_i	intrinsic carrier density
ϵ_{si}	silicon permittivity
kT/q	thermal voltage
V_g	V to front gate and back gate
$\Delta\phi$	metal work function
t_{si}	silicon thickness
t_{ox}	oxide thickness
ϵ_{ox}	oxide permittivity
μ_e	effective mobility
W	device width
Q	total mobile charge per unit gate area.

Table 3.1: Parameters explanation

3.2 Fasarakis model

This model has been created for short-channel triple-gate FET. But if the top gate oxide is much thicker than the gate oxide on the two sides it is possible to use it for DG FinFET.

Several effect has been taken into account respect the Taur model:

- QME (quantum-mechanical effects).
- Short-channel effects as:
  - Threshold-voltage shifts;
  - DIBL
  - Subthreshold slope degradation

The model can be extended to a DG FinFET by changing the effective channel width definition:

$$W_{TG} = H_{fin} + \frac{W_{fin}}{2} \tag{3.10}$$

$$W_{DG} = 2 * H_{fin} \tag{3.11}$$

Where W is the effective channel width of a Triple Gate and of a Double Gate FinFET, respectively.

The formulas used for Fasarakis model are taken in [3].

Chapter 4

Result evaluation

4.0.1 Matlab implementation of Taur & Fasarakis

In the image 4.1 you can find the input parameters used in matlab implementation. The simulation points n are the number of gate voltage that you consider in the current simulation: for each gate voltage an output characteristic $I_{ds}(V_{ds})$ is obtained. Instead the MATLAB variable V_{ds} is a vector of dimension n containing all the drain voltages that you want to select in order to obtain the corresponding drain current. Every time you need to change the analyzed structure and perform a simulation you can simply change the input file without changing any parameter in the main function.

Quantity name	Description	u.m. (S.I.)	Variable name
T	Temperature	K	T
N	Doping concentration	cm^{-3}	N
V_g	Gate voltage	V	Vg_vector
n	Gate simulation points		n
t_{ox}	Oxide thickness	m	t_ox
t_{si}	Silicon thickness	m	t_si
V_{ds}	Drain voltage	V	Vds
n_d	Drain simulation points		nd
V_s	Source voltage	V	Vs
L	Channel length	m	L
μ_e	Effective mobility	$cm^2/(V\ s)$	mu_cm
ε_{ox}	Oxide relative permittivity		eps_ox_r
$q\phi_m$	Metal workfunction	eV	qPhi_M

Figure 4.1: input-parameters-matlab-model

Given the geometric parameters of the device the Matlab input parameters are derived in the following way

$$T_{si} = H_{fin} \tag{4.1}$$

$$W_{eff} = H_{fin} * 2(rectangular - cross - section) \tag{4.2}$$

4.1 Models result

4.1.1 Overview

The short channel effect has the consequence that there is a less efficient capacitive control of the gate and due to this fact the electric field along the channel has a bigger influence. The electric field under the region of the gate is 2-D and it is due the gate and due to pn junction between source and drain.

The solution to solve these drawback caused by SCE is to increase the capacitive control of the gate and we did some simulation (divided in three different point) in which varying some parameters it is possible to obtain a better efficient of the control gate.

DG underlap FinFET shows a well known effect “Threshold voltage roll-off”. The distance between drain and source reduces with the gate-length and hence the channel potential is now more pronounced to the drain electric field. So, the gate potential required to invert the channel is reduced because of the drain electric field encroachment on the channel region increases with decreased gate-length.

This effect is also linked with SS and DIBL effect that cause the lost of channel control[2].

4.1.2 Effects of gate-length variation on DG FinFET structure

In this part we want validate the different models for the short channel.

The problem with taur model is that it doesn't take into account the short channel effect.

The fasarakis model is better in this term because takes into account the SCE. It is possible see this behaviour in the following images.

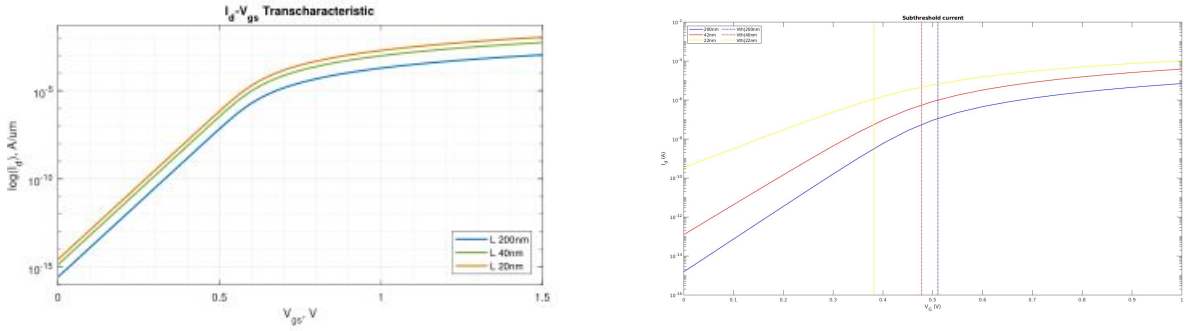

Figure 4.2: Taur model comparison fasarakis model

The results are investigated for L = 200, 40, 20 nm. In the image in left is showed Taur model 4.2 the leakage current varies of one order of magnitude varying the gate length from 200nm to 20nm, while the drive current remains quite stable.

The model seems to be a quasi ideal model, since going from 200nm to 20nm of channel length the transcharacteristic doesn't change. This is quite strange, because one of main issues of FinFETs is the increasing of leakage current and subthreshold slope when a short channel device is considered.

Taur model, which is also based on DG MOSFET modelling, results in a quite good approximation of the FinFET for a long channel device. But we know that it is not a good candidate for short channel FET since it doesn't vary with gate length reduction, so it is not so reliable.

In table 4.1 there are the main parameters evaluation for Taur model

$T_{ox} = 1nm, T_{si} = 30nm$, $W_{eff} = 60nm$			
Parameters	L =200nm	L = 40nm	L=20nm
I_{on}	8.71e-5	4.35e-4	8.71e-4
I_{off}	1.41e-17	7.02e-17	1.41-16
V_{th}	0.74	0.74	0.74

Table 4.1: I_{on}, I_{off} , V_{th} computation for a $V_d = 1V$ [TAUR MODEL]

Furthermore, the threshold voltage seems to be not influenced by channel length variation.

Contrary on the model represent on right the Fasarakis model shows an appreciable variation can be observed by varing the channel length.

The table 4.3 summaries the main results.

$T_{ox} = 1nm, T_{si} = 30nm$, $W_{eff} = 60nm$			
Parameters	L =200nm	L=40nm	L=20nm
I_{on}	1e-5	6e-4	1e-4
I_{off}	1e-15	1e-13	8e-9
$V_{th}(V)$	0.51	0.47	0.382
$SS(mV/dec)$	59.53	64.92	93.56

Table 4.2: I_{on}, I_{off} , V_{th} computation for a $V_d = 1V$[Fasarakis]

Where the Subthreshold Slope (SS) is the major parameter for calculating the leakage current. Furthermore, SS is calculated in the following way :

$$SS = \frac{\delta V_{gs}}{\delta \log_{10} I_{ds}} \tag{4.3}$$

In this case, there is a variation of 4 order of magnitude in leakage current if a long and short channel DG FinFET is taken into account. It can be observed an increase of 25% of subthreshold slope with reducing the gate length from 200nm to 20nm,and as consequence an increase of Vth of 30% is shown.

In conclusion the behaviour of devices is better simulated in Fasarakis model due to the fact that takes into account the short channel effect.

Graphically it is possible to see it because the curves of Taur model are parallel and is not observed an increasing of SS. This means that there isn't a subthreshold current degradation due to a lowering of potential barrier between the channel and the source and drain.

The variation is well visible instead on fasarakis model , the curves are not parallel and subthreshold current increases and there a slope degradation.

It is possible to compute the ratio between $\frac{I_{on}}{I_{off}}$

- L = 200nm ==> $\frac{I_{on}}{I_{off}} \simeq 10^{10}$
- L = 40nm ==> $\frac{I_{on}}{I_{off}} \simeq 10^{7}$
- L = 20nm ==> $\frac{I_{on}}{I_{off}} \simeq 10^{5}$

In this case when channel length is $200nm$ (long channel) the value of the ratio is the highest.

When channel length decreases there is a worse control of the channel current.

4.1.3 DIBL evaluation

In this section we want evaluate one of the most important effect due to DIBL. Reducing the size of the channel we expect that DIBL increases because the field due to the drain has more impact inside the channel 4.8.

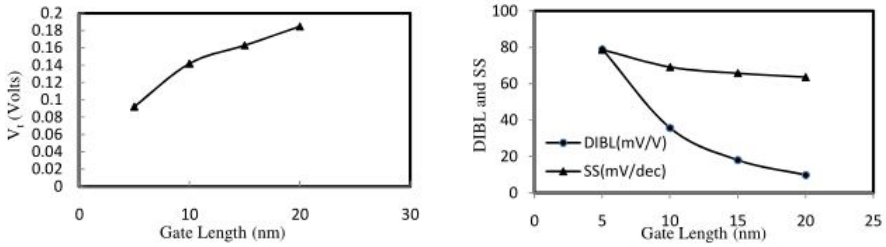

Figure 4.3: On the left Threshold voltage variation with gate-length. On the right Short Channel Effects variation with gate-length [2]

DIBL increases very sharply with decreased gate-length. The drain electric field encroachment on channel region increases at shorter gate-lengths. Subthreshold swing also increases with decreased gate-length. The gate now has less control over channel in subthreshold region because of the channel barrier potential is now controlled by the drain potential also.

The equation 4.4 shows how to compute the DIBL.

$$DIBL = \frac{Vth_{Vd=1} - Vth_{Vd=0.01}}{\Delta Vd} \tag{4.4}$$

This phenomena is just observable by the Fasarakis model and not by Taur. This because like showed in figure 4.4 the curves have the same slope and the same V_{th}(0.74V) in the different cases considered in the formula so theoretically the DIBL is zero.

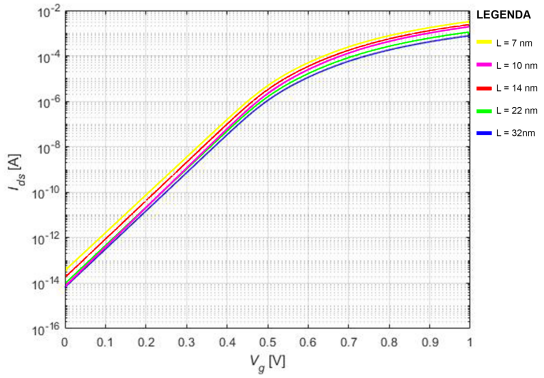

Figure 4.4: Channel length variation Taur model

In charge to compute the DIBL for fasarakis model we have to compute for different technological nodes the V_{th} at Vd=1V and V_{th} at Vd=0.01V like showed in the following images.

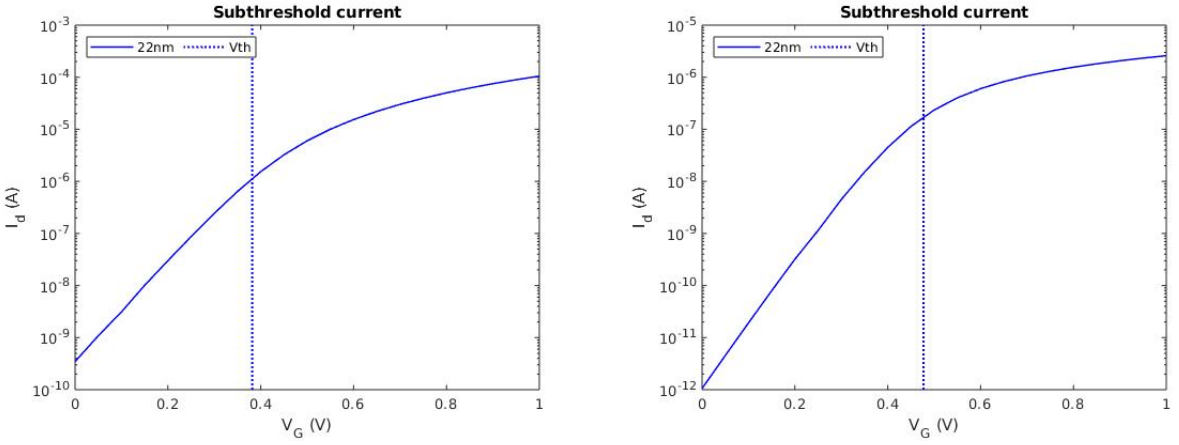

Figure 4.5: Transcharacteric evaluated at 22nm. On the left for Vd=1V and on the right for Vd=0.01V

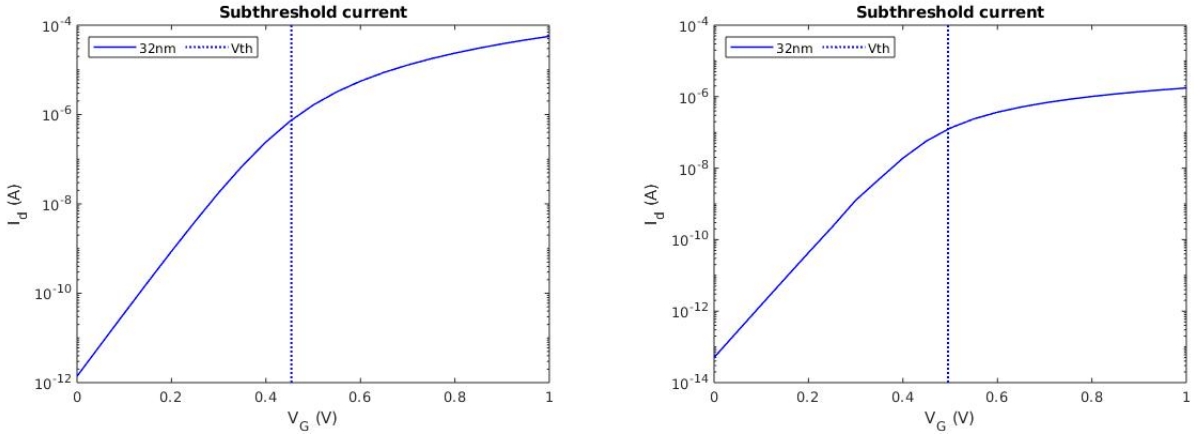

Figure 4.6: Transcharacteric evaluated at 32nm. On the left for Vd=1V and on the right for Vd=0.01V

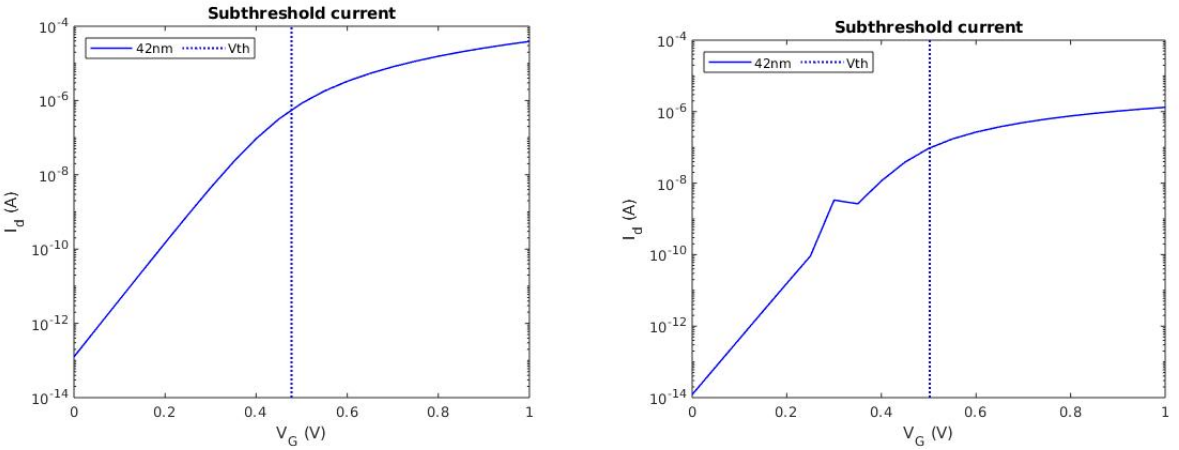

Figure 4.7: Transcharacteric evaluated at 42nm. On the left for Vd=1V and on the right for Vd=0.01V

The Fasarakis model has the validity until 22 nm. When Vd=1V the outputs under 22nm have non-sense. The outputs until 22 nm reproduce well the expected behaviour.

$T_{ox} = 1nm, T_{si} = 30nm$, $W_{eff} = 60nm$			
Parameters	L=40nm	L=32nm	L=22nm
$I_{on}(V_d = 1V)$	6e-4	5e-4	1e-4
$I_{off}(V_d = 1V)$	1e-13	9e-11	8e-9
$I_{on}(V_d = 0.01V)$	9e-5	8.5e-5	8e-5
$I_{off}(V_d = 0.01V)$	9e-13	5e-13	1e-12
$Vth_{Vd=1}(V)$	0.478	0.457	0.382
$Vth_{Vd=0.1}(V)$	0.502	0.496	0.477
$SS(mV/dec)$	64.92	70.51	93.56
$DIBL(mV/V)$	24	42	95

Table 4.3: I_{on}, I_{off} , V_{th} computation[Fasarakis]

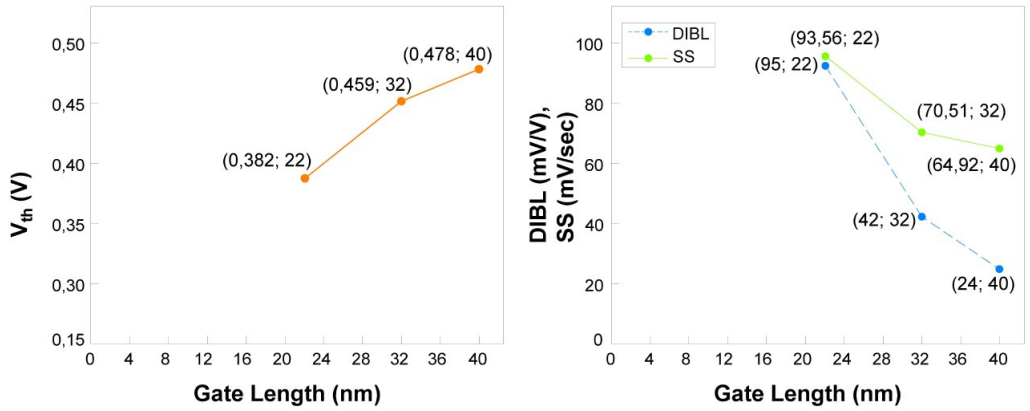

Figure 4.8: On the left Threshold voltage variation with gate-length. On the right Short Channel Effects variation with gate-length

In the table 4.3 it is also possible to compute the ratio between I_{on} and I_{off} that it is a parameter that represent how the current control is performed well

- L = 40nm ==> $\frac{I_{on}}{I_{off}} \simeq 10^9$
- L = 32nm ==> $\frac{I_{on}}{I_{off}} \simeq 10^7$
- L = 22nm ==> $\frac{I_{on}}{I_{off}} \simeq 10^5$

In this case when channel length decreases there is a worse control of the channel current.

4.1.4 Effects of fin-thickness variation on DG FinFET structure

In this part we want study how vary the electrostatic control effectiveness of the gate on the channel. The variable parameter in this case is the thickness of the Fin (W_{Top} and W_{bottom} that in our case present the same size: rectangular cross section).

It is expected that capacitive control of the gate decreases when the size of Fin increases.As a consequence the threshold voltage decreases and the subthreshold current increases like showed in the image 4.11.

This is due to electric field caused by the gate decreases and the device is more sensible of the field between source and drain.

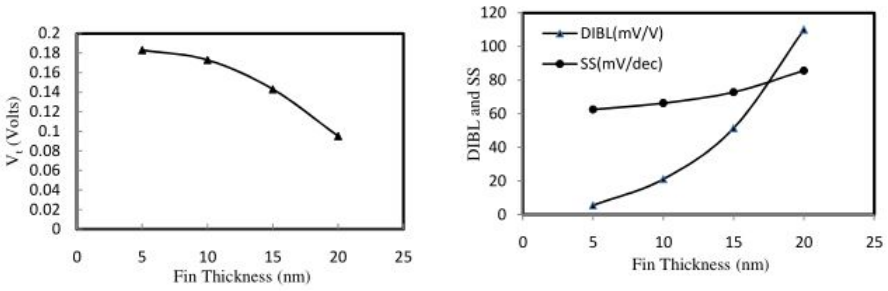

Figure 4.9: On the left,Threshold voltage variation with fin-thickness. On the right,Short Channel Effects variation with fin-thickness

For the Taur model is not possible to do this type of simulation because in the input model there isn't the possibility to choose W.

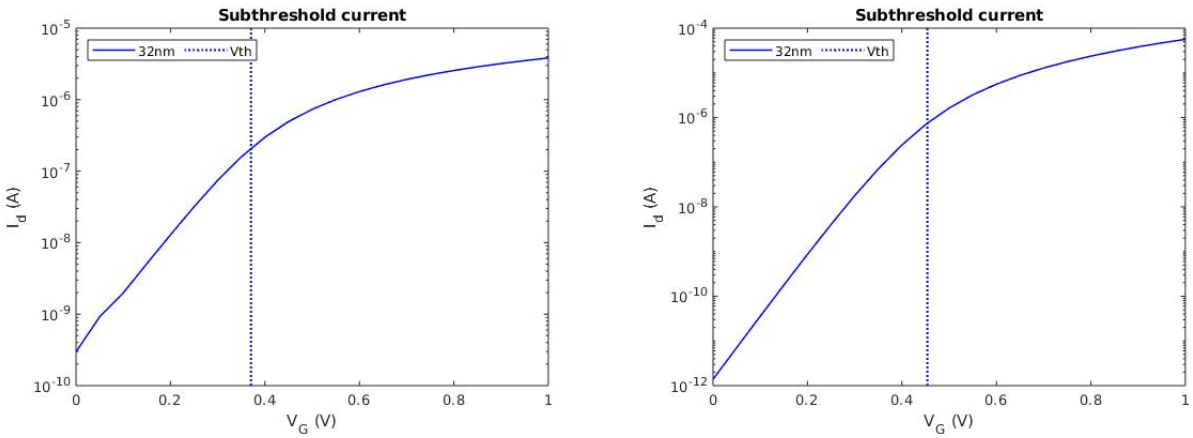

Figure 4.10: Transcharacteric evaluated at 32nm.On the left for W=30nm and on the right for W=10nm[2]

The table 4.4 shows the main results of W variation for fasarakis model

L =32nm		
Parameters	$W = 10nm$	$W = 30nm$
I_{on}	8.5e-5	6e-5
I_{off}	5e-13	8e-9
$V_{th}(V)$	0.496	0.37
$SS(mV/dec)$	67.69	137.2

Table 4.4: I_{on}, I_{off} , V_{th} computation for different W

The table 4.4 shows the threshold voltage variation with the fin-thickness.

Threshold voltage reduces with increased fin-thickness. At shorter channel lengths, the surface potential depends not only on capacitive coupling between the gate and the channel region but also on the capacitance of source/fin and drain/fin junction.

As the fin-thickness increases, the width of the source/fin and drain/fin depletion region increases, which decreases the source/fin and drain/fin junction capacitances, as a result the gate to surface potential coupling increases and hence the threshold voltage decreases with the increased film thickness.

Fin-thickness plays a very important role while deciding SCEs and DIBL increases with increased fin-thickness.

Drain electric field lowers the barrier of channel in case of thick silicon film devices because of reduced source/fin and drain/fin junction capacitances. Subthreshold swing also increases with fin-thickness. The reason behind this is that the gate control over channel region degrades with increased channel volume at constant drain and source proximity.

It is important to consider the effect of the ratio of gate-length (L) and fin-thickness (T_{fin}) on DIBL. This ratio limits the scaling of DG FinFET structure.

DIBL and subthreshold swing (SS) increases abruptly when the L/T_{fin} ratio fall below 1.5. This ratio is the most important factor which decides the short channel effects (respectively for W=10 and W=30).

For DG FinFET structure fin-thickness could be a dominating factor which decides the scaling capabilities[2].

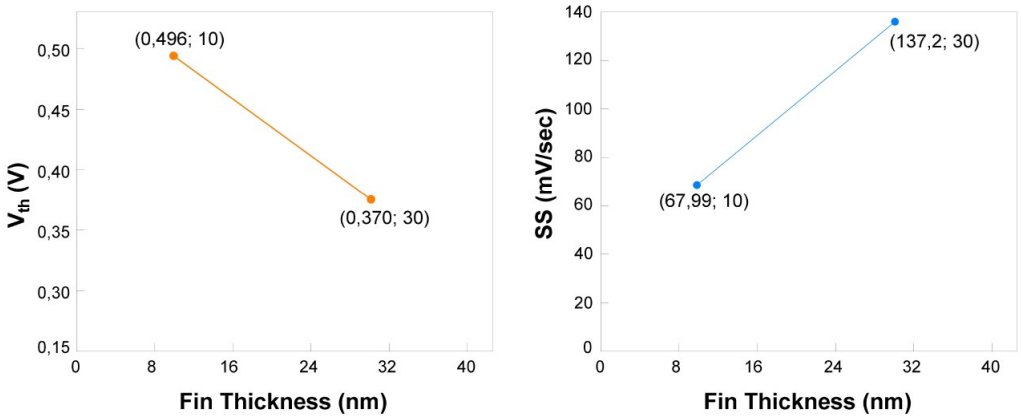

Figure 4.11: On the left, Threshold voltage variation with fin-thickness. On the right, Short Channel Effects variation with fin-thickness

4.1.5 Effects of fin-heights variation on DG FinFET structure(T_{si})

Increasing the Fin height T_{si} what it is expected (fixing the other parameters) is that the electrostatic gate control increases and as a consequence the threshold voltage increases and subthreshold current decreases.

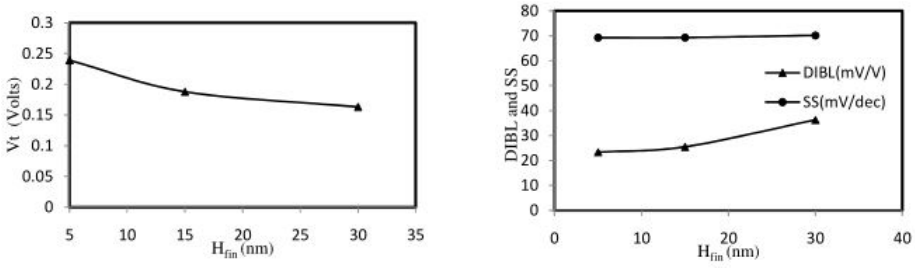

Figure 4.12: On the left,Threshold voltage variation with the fin-height at 30nm of T_{fin}. On the right, Short Channel Effects variation with fin-height at 30nm of T_{fin}[2]

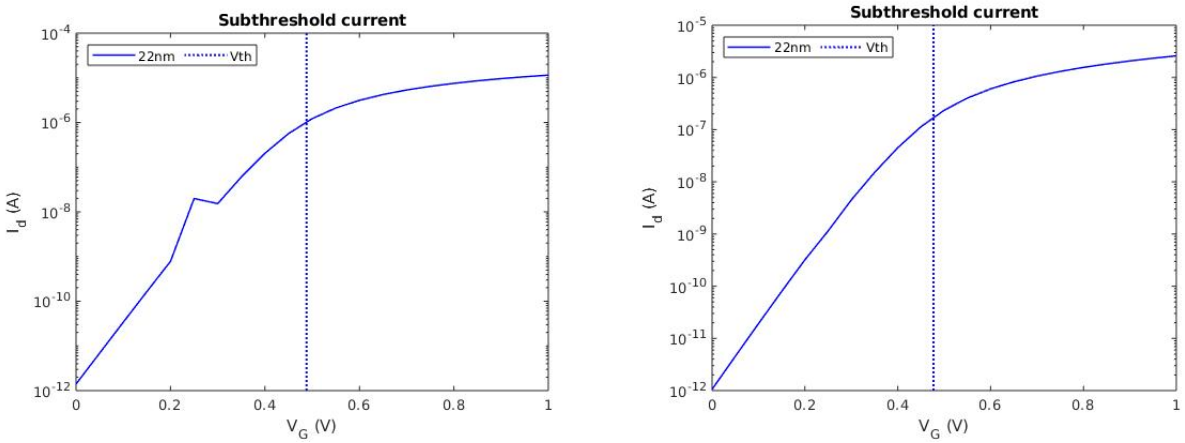

Figure 4.13: Transcharacteric evaluated at 22nm.On the left for H_{fin}=90nm and on the right for H_{fin}=30nm

L =22nm		
Parameters	$H_{fin} = 30$	$H_{fin} = 90nm$
I_{on}	8e-5	1e-5
I_{off}	1e-12	9e-11
$V_{th}(V)$	0.477	0.488
$SS(mV/dec)$	71.09	78.82

Table 4.5: I_{on}, I_{off} , V_{th} computation for different H_{fin} [Fasarakis]

L =22nm		
Parameters	$H_{fin} = 30$	$H_{fin} = 90nm$
I_{on}	7.92e-4	0.023
I_{off}	1.28e-16	1.15e-15
$V_{th}(V)$	0.74	0.74

Table 4.6: I_{on}, I_{off} , V_{th} computation for different H_{fin} [Taur]

The table 4.5 depicts the threshold voltage variation with the fin-height. Threshold voltage reduces with fin-height.

In the table 4.6this aspect is not visible for the problems of the model that previous discussed

At shorter channel lengths, the surface potential depends not only on capacitive coupling between the gate and the channel region but also on the capacitance of source/fin and drain/fin junction. As the fin-height increases, the width of the source/fin and drain/fin depletion region increases, which decreases the source/fin and drain/fin junction capacitances, as a result the gate to surface potential coupling increases and hence the threshold voltage decreases with increased fin- height.

DIBL also increases with the fin-height. The drain electric field lowers the channel barrier as we increases fin-height. Subthreshold swing also increases with fin-height. Gate loses its control over the channel with increased fin-height.

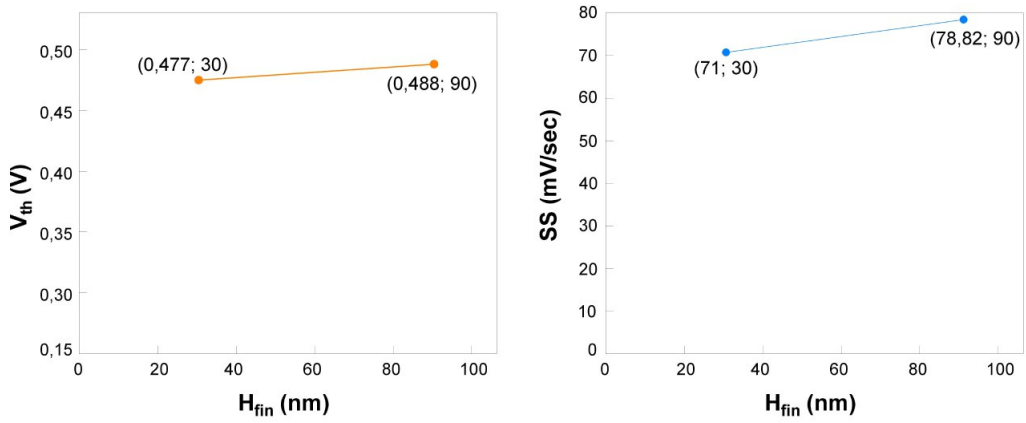

Figure 4.14: On the left,Threshold voltage variation with the fin-height at 30nm of T_{fin}. On the right, Short Channel Effects variation with fin-height at 30nm of T_{fin}

- $H_{fin} = 30$ ==> $\frac{I_{on}}{I_{off}} \simeq 10^6$
- $H_{fin} = 90$ ==> $\frac{I_{on}}{I_{off}} \simeq 10^7$

In this case when fin height decreases there is a worse control on the channel current.

4.1.6 Oxide thickness variation (T_{ox})

Increasing T_{ox} the consequence is that gate control decreases too.

This is due to the fact that increasing the thickness of the oxide we have less control of the gate because capacitance is less.

$$C = \frac{\epsilon_{ox}}{T_{ox}} \tag{4.5}$$

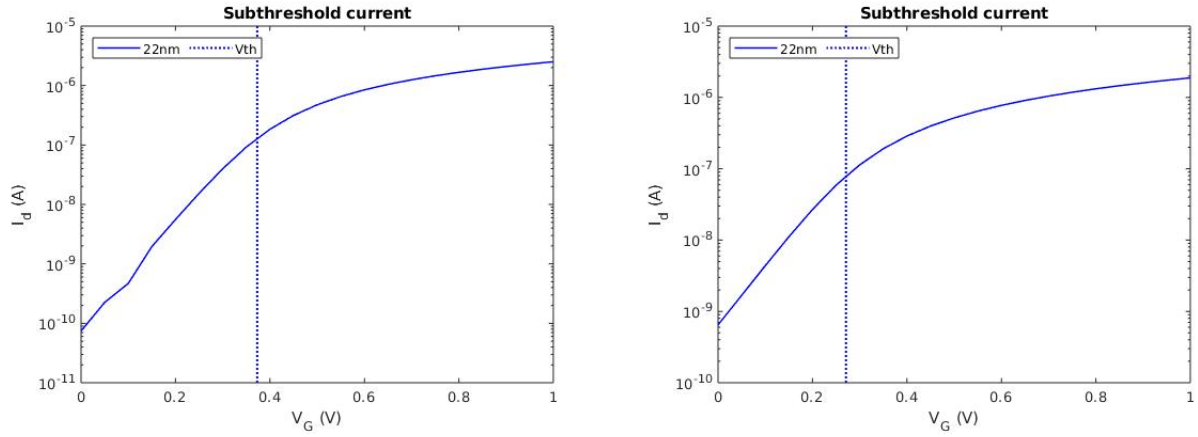

Figure 4.15: Transcharacteric evaluated at 22nm.On the left for T_{ox}=3nm and on the right for T_{ox}=5nm

L =22nm			
Parameters	T_{ox} =1nm	T_{ox} =3nm	T_{ox} =5nm
I_{on}	7.92e-04	3.94e-04	2.78e-04
I_{off}	1.28e-16	1.28e-16	1.28e-16
V_{th}	0,74	0,68	0,68

Table 4.7: I_{on}, I_{off} , V_{th} computation for different T_{ox} [Taur]

L =22nm			
Parameters	T_{ox} =1nm	T_{ox} =3nm	T_{ox} =5nm
I_{on}	8e-5	8.5e-5	9e-5
I_{off}	1e-12	2e-10	4e-9
V_{th}	0.477	0.373	0.271

Table 4.8: I_{on}, I_{off} , V_{th} computation for different T_{ox} [fasarakis]

The table 4.7 shows the results for Taur model. They report the problem discussed on the previous section about SCE

.

The table 4.15 shows the results for Fasarakis model. They show how the V_{th} decreases increasing the T_{ox} size.

It is possible to appreciate also how the I_{off} current increases of three order of magnitude passing from $T_{ox} = 1$ to $T_{ox} = 5$, contrary I_{on} current is stable enough.

As a consequence the ratio I_{on}/I_{off} will be less and so the device control is worse.

- $T_{ox} = 1nm$ ==> $\frac{I_{on}}{I_{off}} \simeq 10^7$
- $T_{ox} = 3nm$ ==> $\frac{I_{on}}{I_{off}} \simeq 10^5$
- $T_{ox} = 5nm$ ==> $\frac{I_{on}}{I_{off}} \simeq 10^4$

Chapter 5

Appendix - Scripts

Listing 5.1: Input Matlab code of taur model

```
1
%% input parameters transcharacteristics
3 % technological node of 50 nm (data from the previous project of finfet)
%  temperature [K]
5 T=300;
% doping concentration [cm^-3]
7 N=1.45e10;
% number of gate voltages in the simulation
9 n=100;
% gate voltage [V]
11 Vg_vector=linspace(0,1,n);
% oxide thickness [m]
13 t_ox=1*1e-9;
% silicon thickness [m]
15 t_si=10*1e-9;
% drain voltage [V]
17 Vds=1;
% source voltage [V]
19 Vs=0;
% device width [m]
21 W=1e-6;
% device channel length [m]
23 L=40e-9;
% oxide relative permittivity []
25 eps_ox_r=3.9;
% mobility [cm^2/(V*s)]; you must impose 300 to use the same value as [1]
27 %  mu_cm=200;
% It is also implemented the mobility model obtained in [2], and the
29 % mobility is a function of the temperature and of the doping level.
% In order to use the mobility model uncomment the following line:
31    mu_cm=mobility_function(T,N);  % mobility [cm^2/(V*s)]
% mobility [m^2/(V*s)]
33 mu=mu_cm*1e-4;
% metal parameter to select the gate type. You can select the type of gate
35 % by selecting the value of the variable "metal" as reported below:
% metal=0 -> midgap metal
37 % metal=1 -> p+ polygate
% metal=-1 -> n+ polygate
39 % otherwise -> the metal workfunction
% is setted as the value reported in qPhi_M (see below),
41 % by choosing the metal workfunction.
metal=10;
43 qPhi_M=4.65;     % metal work function [eV]
```

Listing 5.2: Input Matlab code of Fasarakis model

```
for jj = 1:length(Vd)

Vds = Vd(jj) - Vs(jj);

% virtual cathode position along the channel
ym = L/2 - lambdam/2.*log(((Vbi - VgPrime).*(exp(L/lambdam) - 1) + Vds*exp(L/lambdam))...
    ./((Vbi - VgPrime).*(exp(L/lambdam) - 1) - Vds));

A1Sym = A1(ym,lambdaSym);
A2Sym = A2(ym,lambdaSym);
A1Asym = A1(ym,lambdaAsym);
A2Asym = A2(ym,lambdaAsym);

% A1TG, A2TG calculation; for an ideal long channel FinFET, we would have
% A1TG = A2TG = 0 so ideal SS
A1TG = (2*Hfin*A1Sym + Wfin*A1Asym)./(2*Hfin);
A2TG = (2*Hfin*A2Sym + Wfin*A2Asym)./(2*Hfin);

% blocks are for ease of reading only
block1 = (A1TG.*(Vbi + Vds) + A2TG.*Vbi)./(1 - A1TG - A2TG);
block2 = Vt./(1 - A1TG - A2TG);

% Vth calculation
Vth = Vfb - block1 + block2.*log((Qth*Na)/(ni^2*Wfin));
% addition of QMEs
Vth_QME = Vth + deltaVth_QME;

%%%%%% CLM %%%%%%%%%%

VdSat = Vg - Vth;
% the TRAP factor takes into account the formula variation from [2] to [3]
VdEff = VdSat + (Vd(jj) - VdSat + 1).*(tanh(Vd(jj)./(VdSat + 1))).^2;
% channel length modulation value
dL = CLM*lambdaEff*log(1 + (VdEff - VdSat)/VE);
% normalized inversion charges determination
A = 4*exp((Vth + Vfb)/V0 - c1);
% this is different from the subthreshold slope factor eta
etaTG_prime = 1./(1 - 2*(A1TG + A2TG));
qi = @(V) LambW(exp((Vg - Vth - V)./(2*Vt).*(1 + 1/etaTG_prime))./...
    (A + exp((Vg - Vth - V)./(2*etaTG_prime*Vt))));
% normalized inversion charges
qis = qi(Vs(jj));
qid = qi(Vd(jj));

%%%% VST %%%%%%%%%
% saturation parameter
theta1 = theta1_0.*(1 + mu0*Vd(jj)./(vsat.*(L - dL))) + mu0.*2*Weff.*COx./(L - dL).*Rsd;
% real channel mobility
mu_real = mu0./(1 + VST.*theta1.*Vt.*qis);

%%
%  corner effects in tzFinFET
 f = 1 + TRAP*(1./(1 + C*exp((Vg - Vth)/0.005)./(1 + exp((Vg - Vth)/0.005))) - 1);

% drain current determination
% Id is a m x n matrix where m is the number of Vg values and n is the
% number of Vds values
Id_ideal (:,jj) = [mu0.*Weff*epsOx/tOx*(2*Vt)^2.*((qis - qid)/L + 0.5*(qis.^2 - qid.^2)./(
```

```
60 Id(:,jj) = [f.*mu_real.*Weff*epsOx/tOx*(2*Vt)^2.*((qis - qid)/L + 0.5*(qis.^2 - qid.^2)./(

62 end

64 % this prints the last (i.e. for max Vds) SS value directly to console
   SS = log(10)*Vt/(1 - (A1TG + A2TG))*1e3;
66
   fprintf('Threshold␣voltage:␣%.3f␣V\r\n',Vth_QME)
68 fprintf('Subthreshold␣Swing:␣%.2f␣mV/decade␣\r\n',SS)

70 end
```

Bibliography

[1] Chiola Fabi. “IST homework : Modeling of FinFET Devices Integrated system technology”. In: 2017.

[2] Ashwani K Rana Gaurav Saini. “Physical Scaling Limits of FinFET Structure: A Simulation Study”. In: 2011.

[3] Deborah Vergallo. “Analysis and Simulation of Emerging FET Devices: FinFET, TFET”. In: 2018.

[4] Veljko Vukicevic. “Evolution of FinFETs from 22nm to 7nm”. In: September 2019.