Compare three different algorithms

in terms of accuracy, delay and area

Goal: find a clever way to compare three schemes with respect to accuracy, delay and area.

Compared with of three whole algorithms block, see the deviation of the real results to the ideal results for the calculation of relative error. Power dissipation, consumed calculation time and area on the chip can also be compared between implementations.

In General:

1. We set a parameter A (later we could give 8 bit, 16 bit, 24 bit, 32 bit).
2. Set Input angle -pi/4 , -Pi/6, -Pi/8, 0, Pi/8, Pi/6, Pi/4. (use 2's complement: fixed point)
3. Build three Cordic architectures.
4. VHDL design in vivado -> Functional Simulation

For Area

VHDL design in vivado -> Functional Simulation -> Compare the number of registers in different design with the synthesized netlist to get roughly area estimation.

For Delay

VHDL design in vivado -> Functional Simulation -> Delay estimation from the simulation result (how many stages for all three designs from input to output) -> Synthesis (transfer the RTL into the register level netlist) With synthesis report, we can get roughly power estimation for these three designs.

For accuracy

Calculation result with non-approximation algorithm to get ideal result and calculate relative errors of approximated solutions.

We could compare three algorithms with 3 different parameters; In every parameter , we could know which one (compare with 3 algorithms) is the best.