

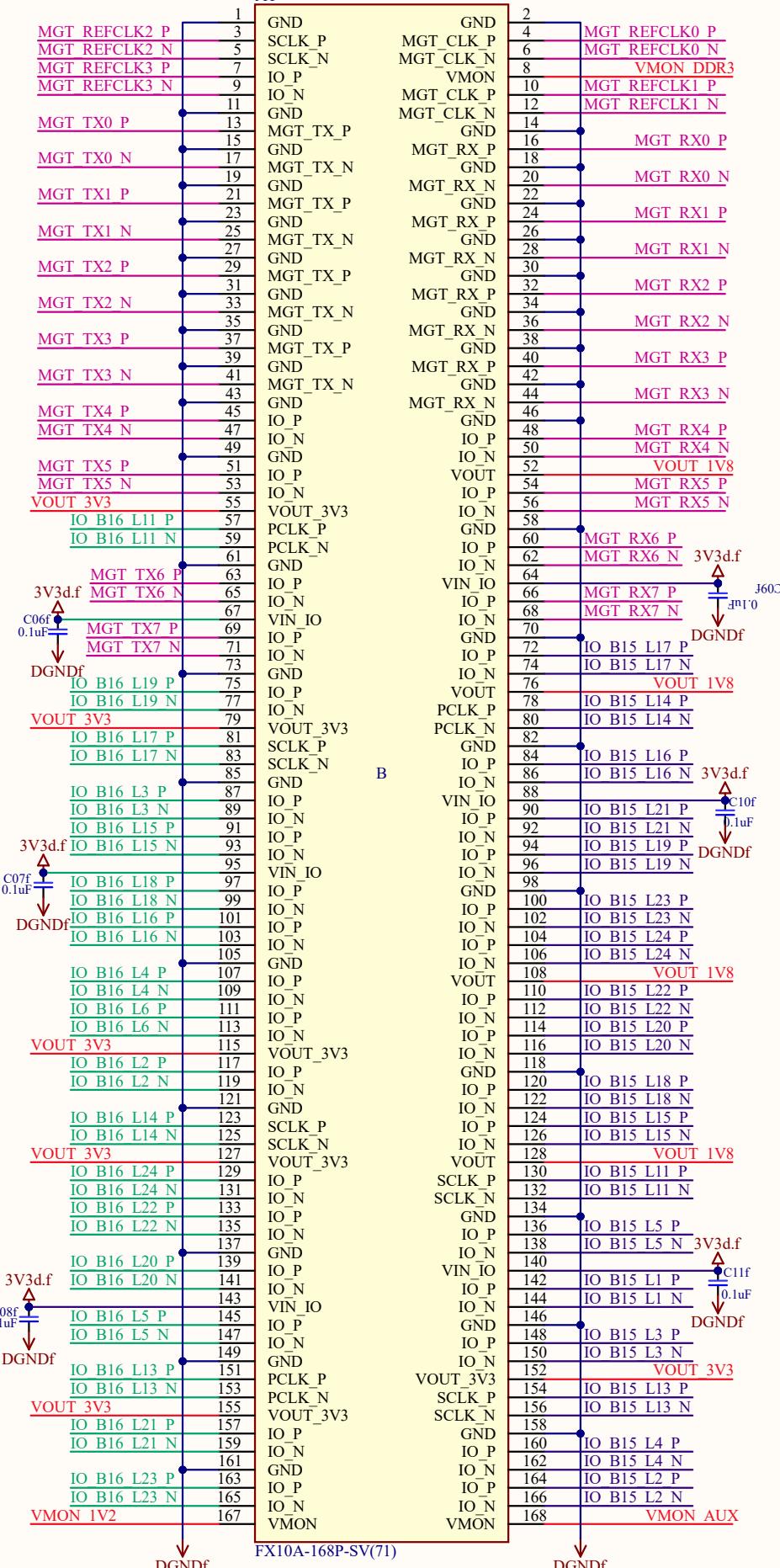
A

B

C

D

J1f



FX10A-168P-SV(71)

Title: Penn State Cd Clock FPGA Control System

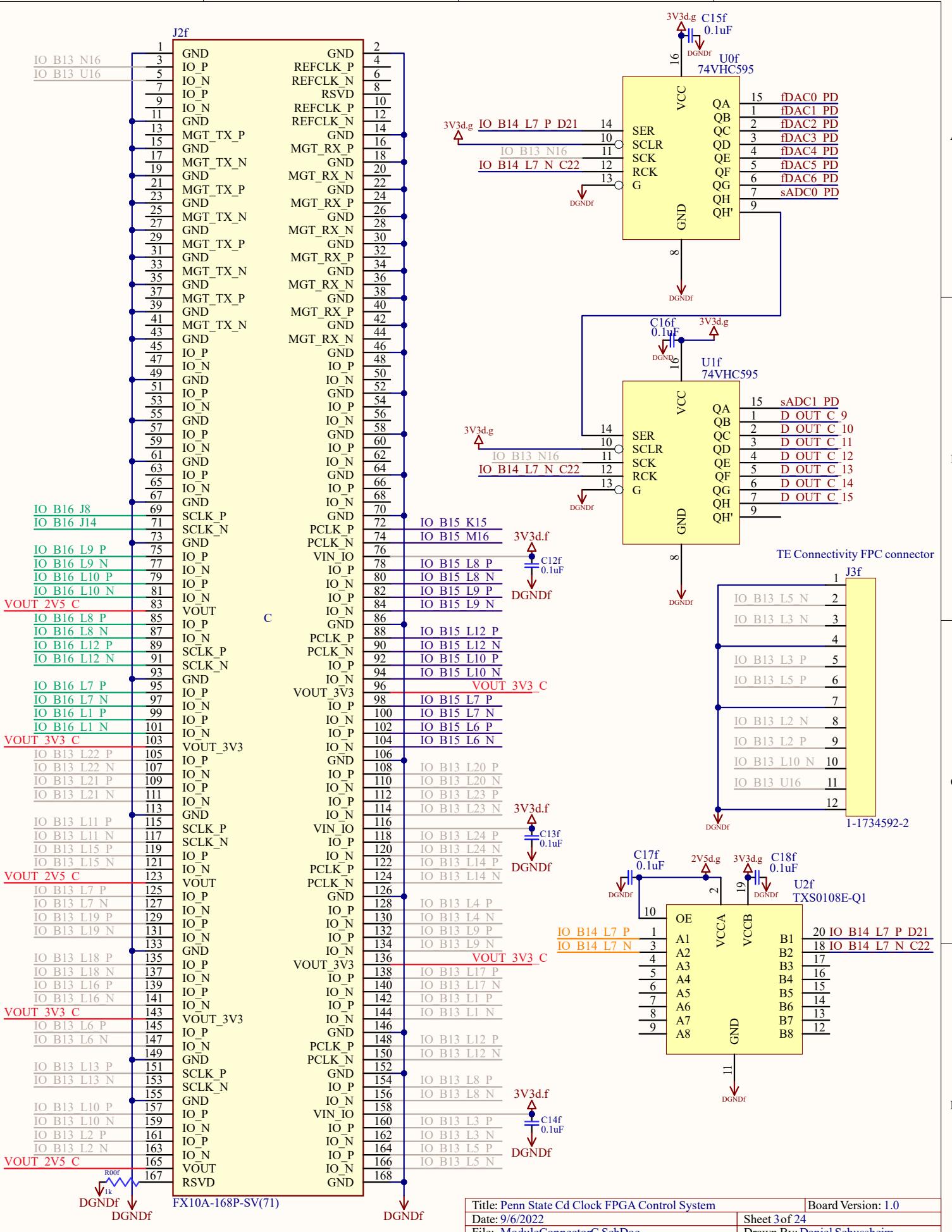
Board Version: 1.0

Date: 9/6/2022

Sheet 2 of 24

File: ModuleConnectorB.SchDoc

Drawn By: Daniel Schusheim

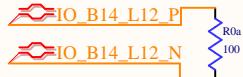


A

2V5d.f



FastADC0
LTC2194_0.SchDoc



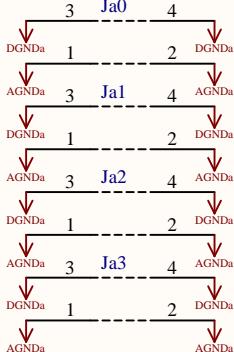
FastADC1
LTC2194_1.SchDoc

FastADC2
LTC2194_2.SchDoc

FastADC3
LTC2194_3.SchDoc

FastADC4
LTC2194_4.SchDoc

fADC GND pads



A

B

B

C

C

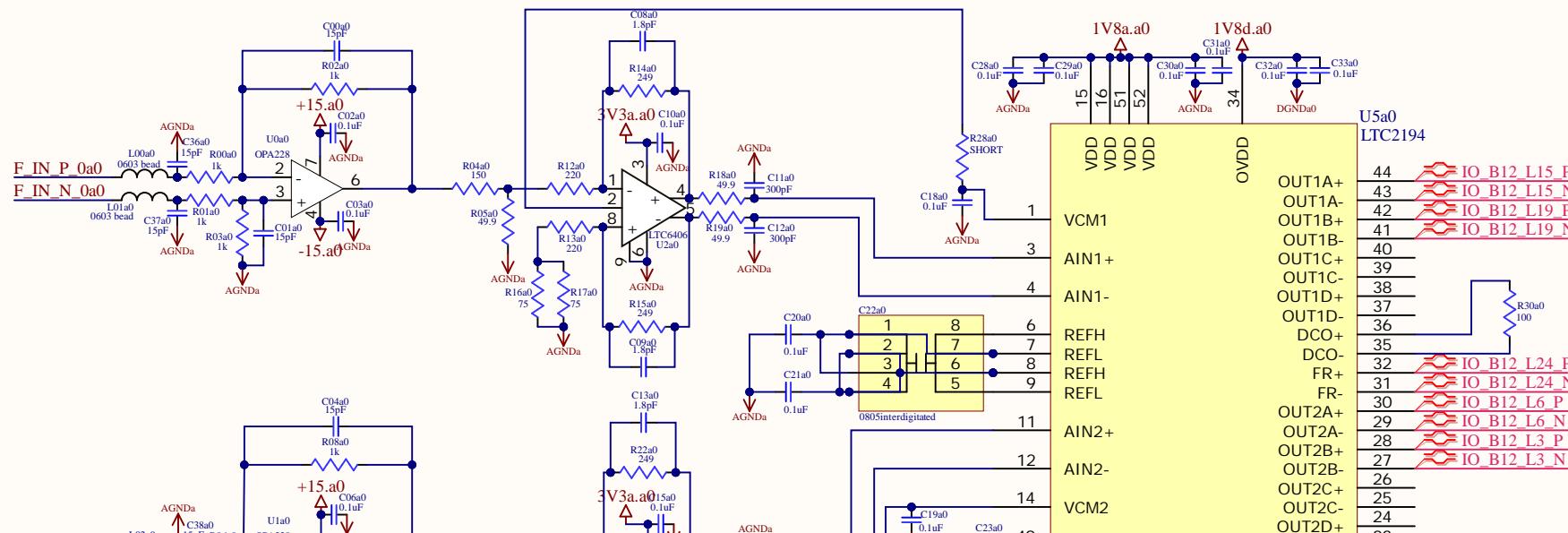
D

D

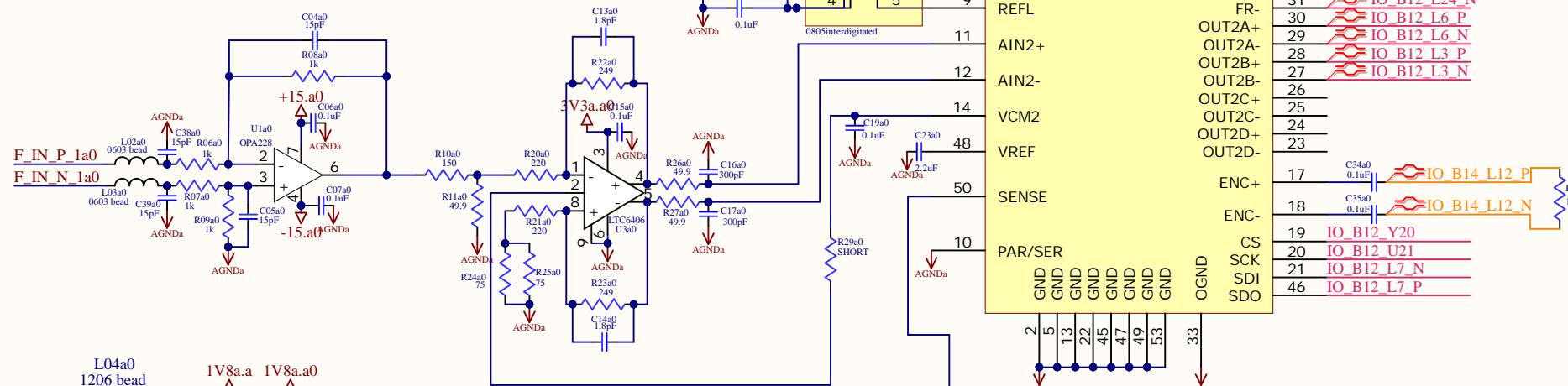
0603 bead is Wurth 7427926

1206 bead is Laird-Signal Integrity Products HZ1206C202R-10

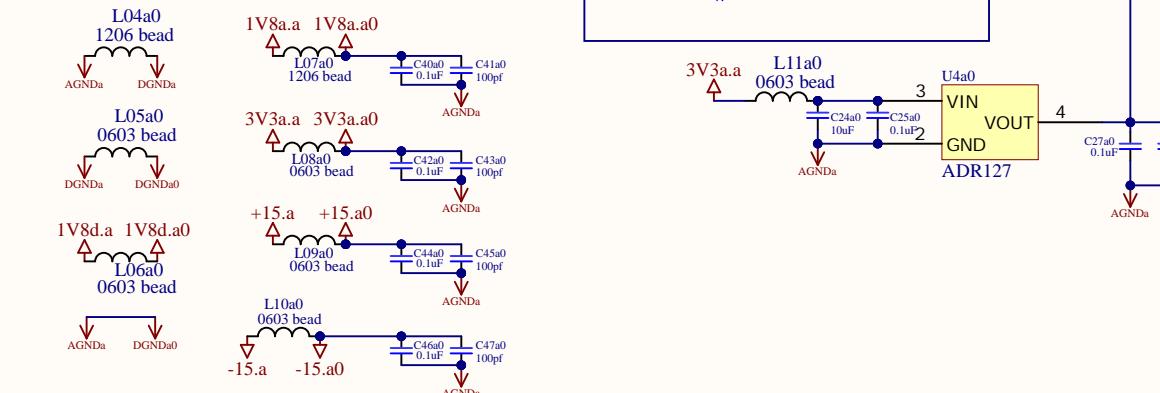
A



B



C



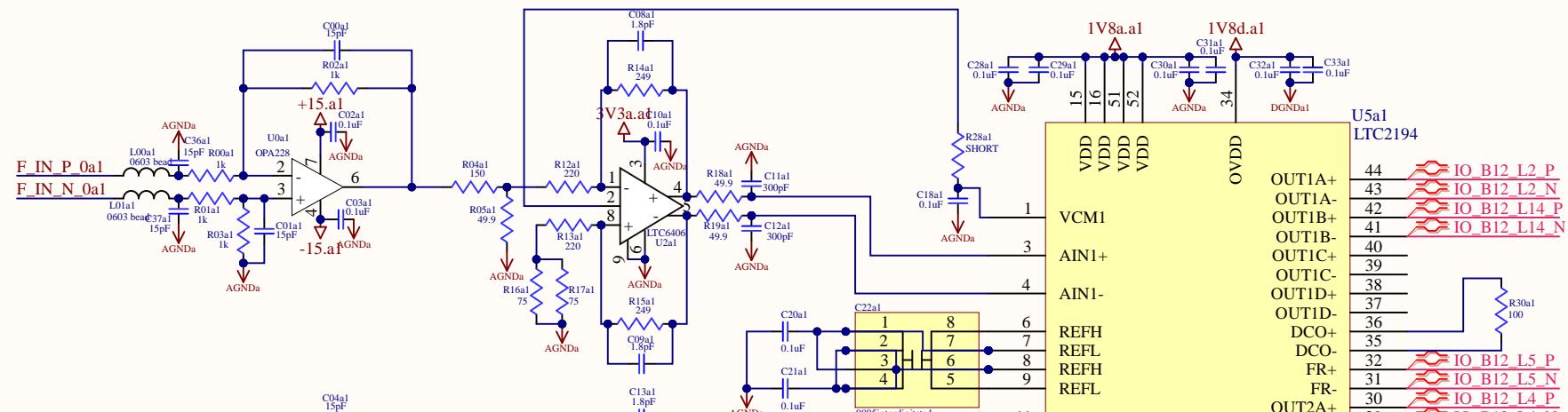
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Title: Penn State Cd Clock FPGA Control System		Board Version: 1.0
Date: 9/6/2022	Sheet 5 of 24	
File: LTC2194_0.SchDoc		Drawn By: Daniel Schusheim

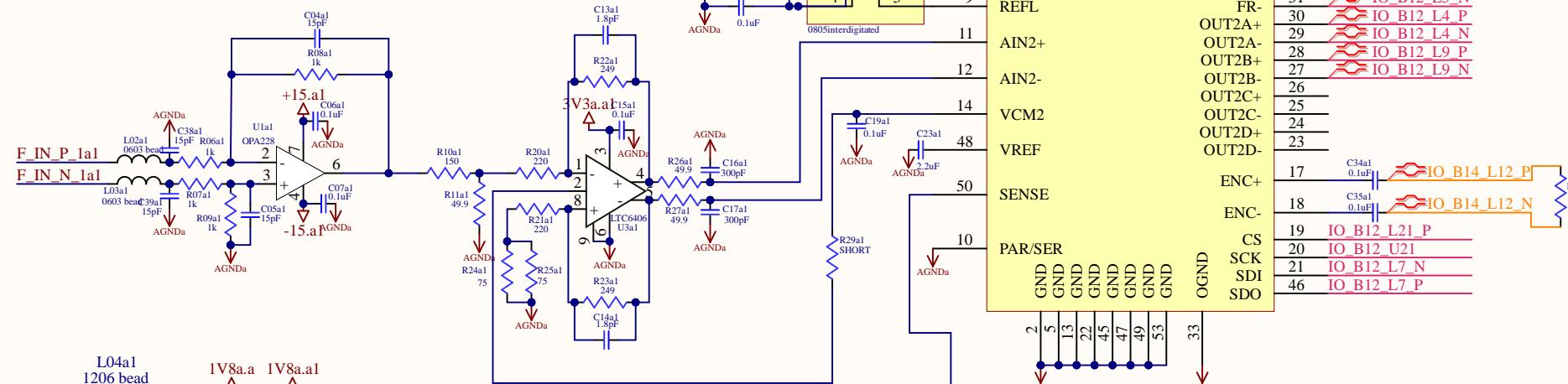
0603 bead is Wurth 7427926

1206 bead is Laird-Signal Integrity Products HZ1206C202R-10

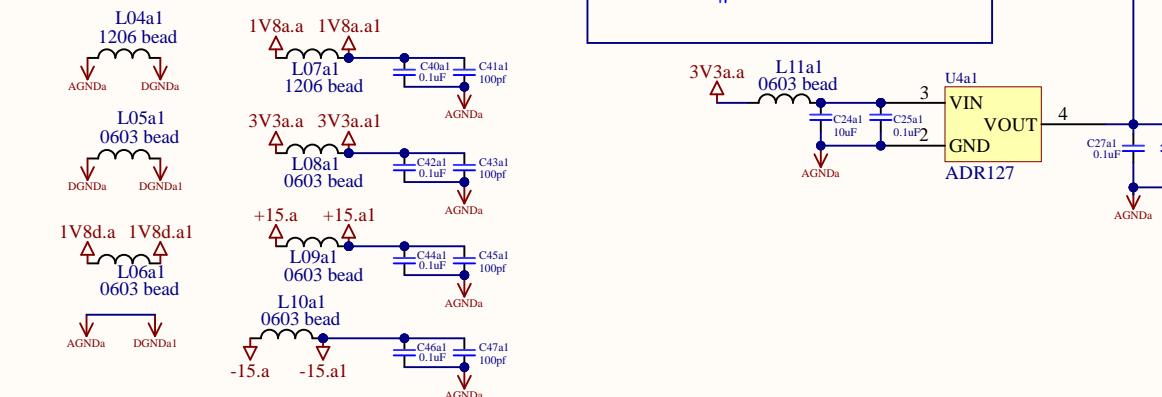
A



B



C



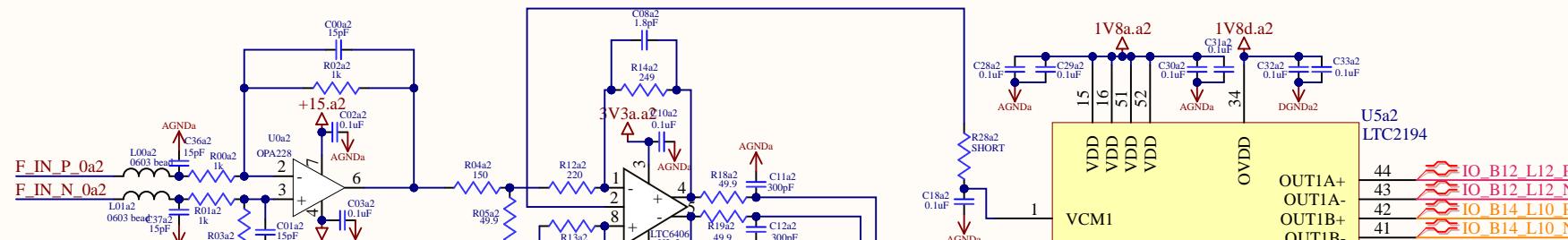
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Title: Penn State Cd Clock FPGA Control System		Board Version: 1.0
Date: 9/6/2022		Sheet 6 of 24
File: LTC2194_1.SchDoc		Drawn By: Daniel Schusheim

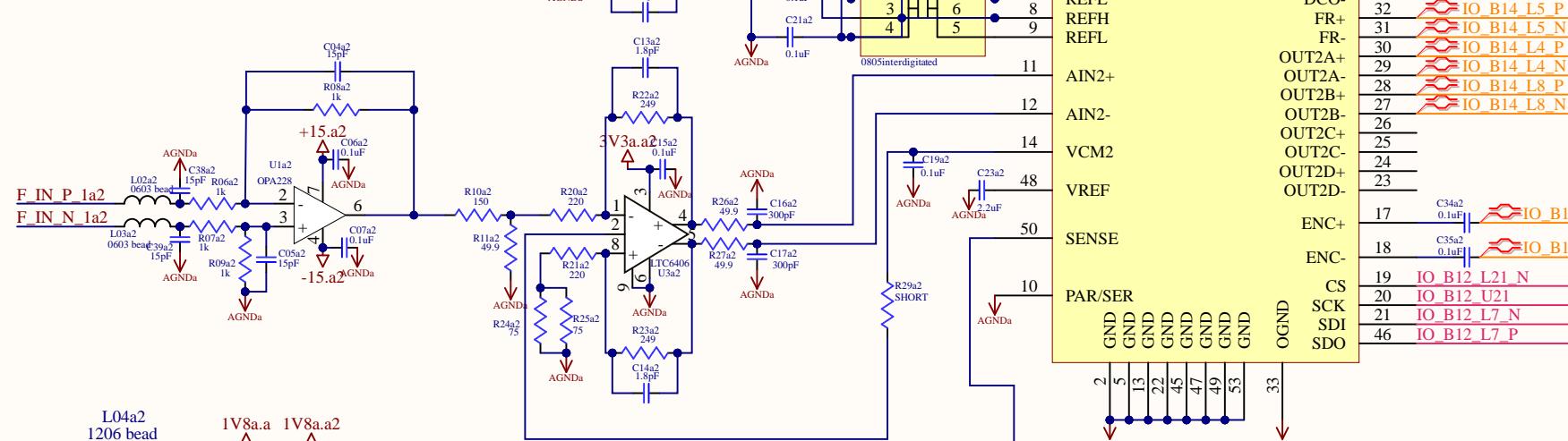
0603 bead is Wurth 7427926

1206 bead is Laird-Signal Integrity Products HZ1206C202R-10

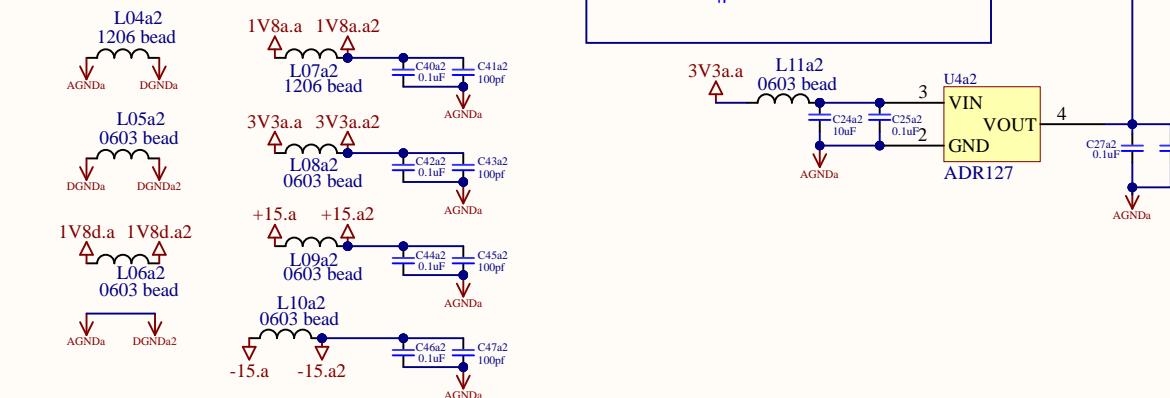
A



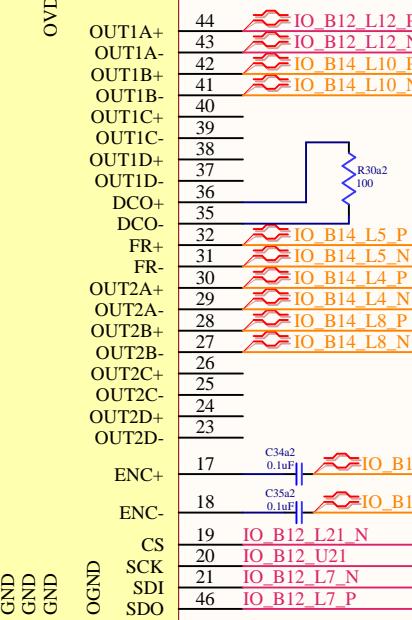
B



C



D



A

B

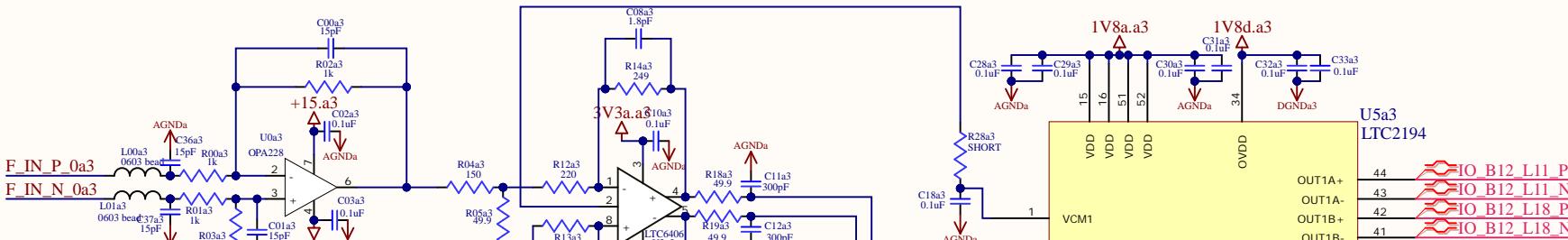
C

D

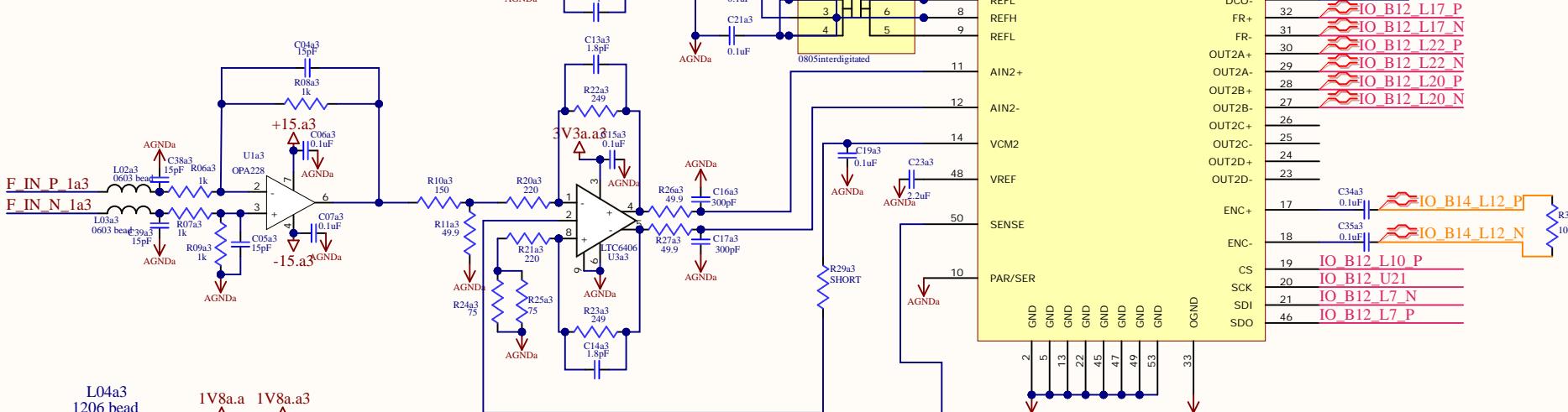
0603 bead is Wurth 7427926

1206 bead is Laird-Signal Integrity Products HZ1206C202R-10

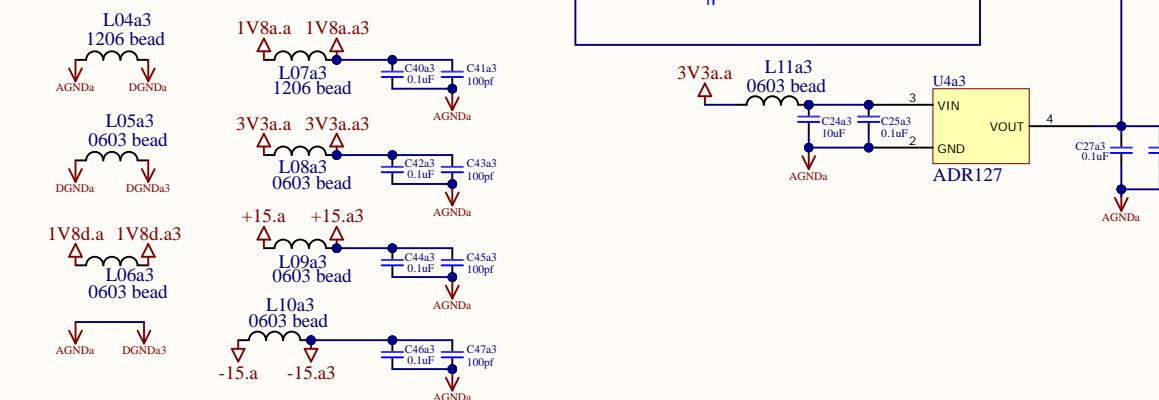
A



B



C



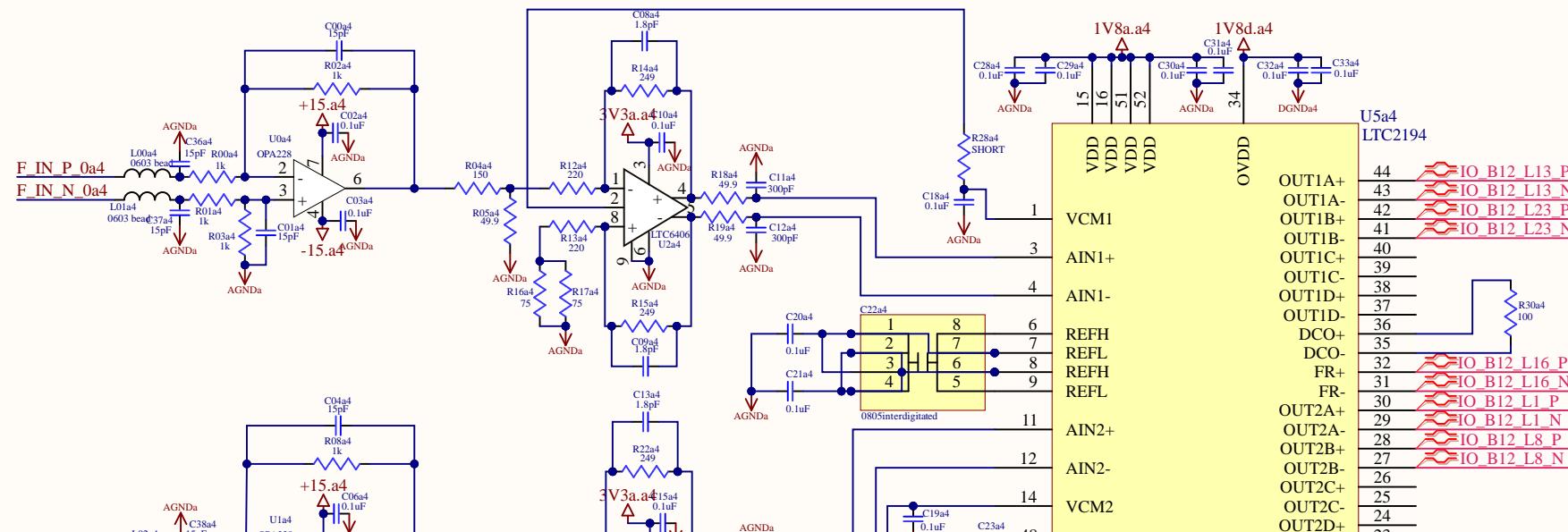
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Title: Penn State Cd Clock FPGA Control System		Board Version: 1.0
Date: 9/6/2022	Sheet 8 of 24	
File: LTC2194_3.SchDoc	Drawn By: Daniel Schusheim	

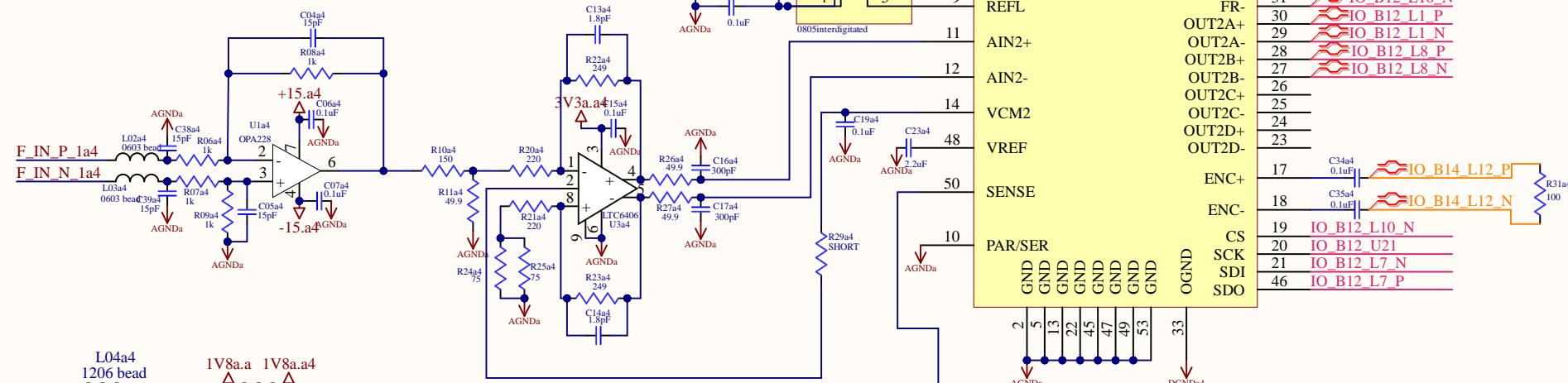
0603 bead is Wurth 7427926

1206 bead is Laird-Signal Integrity Products HZ1206C202R-10

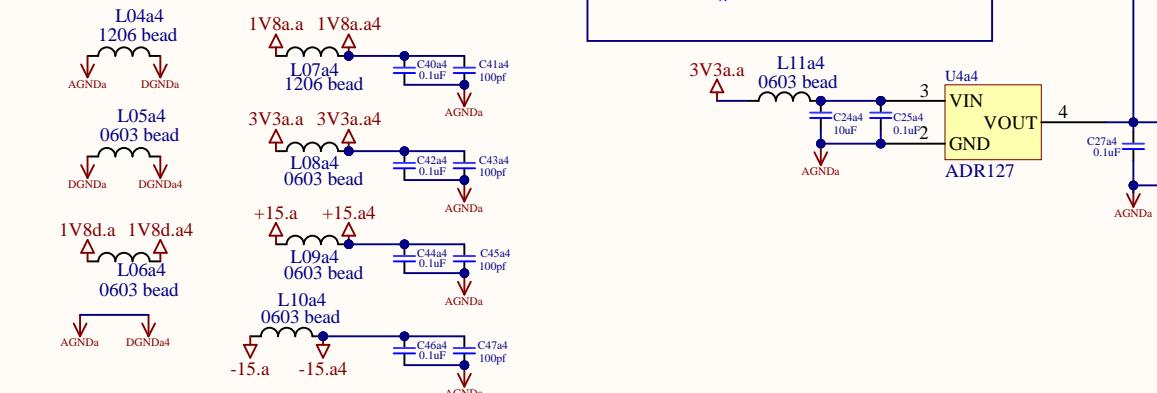
A



B



C



D



1

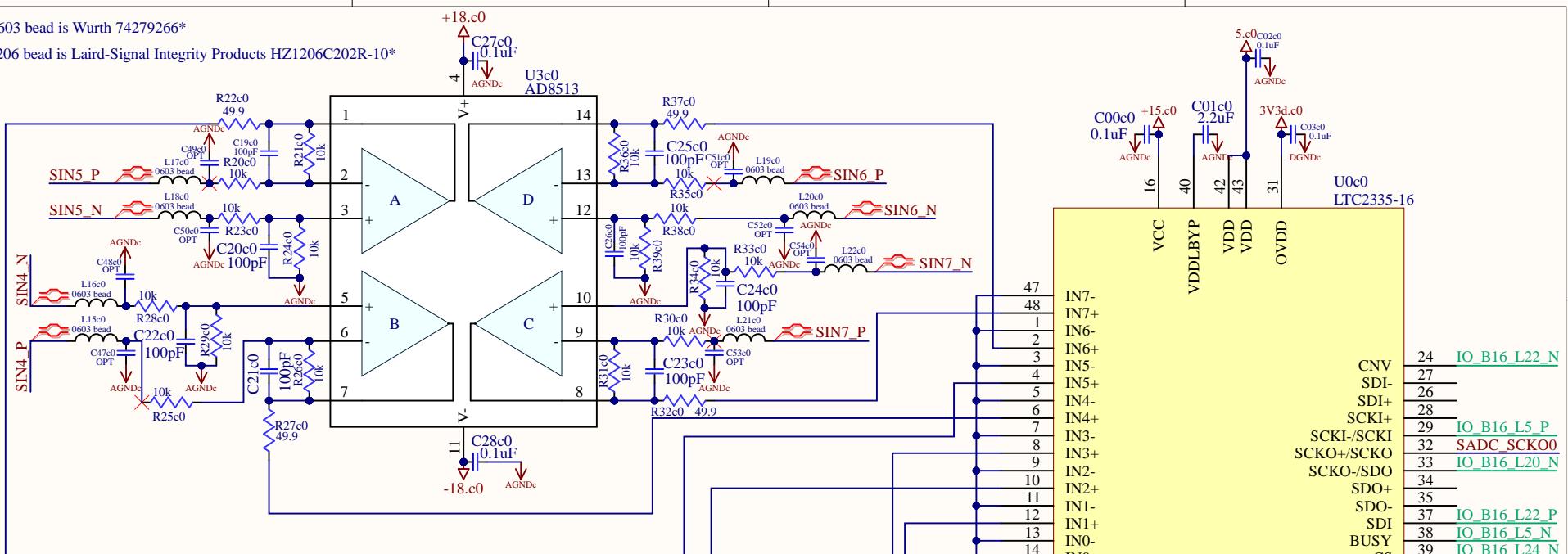
2

3

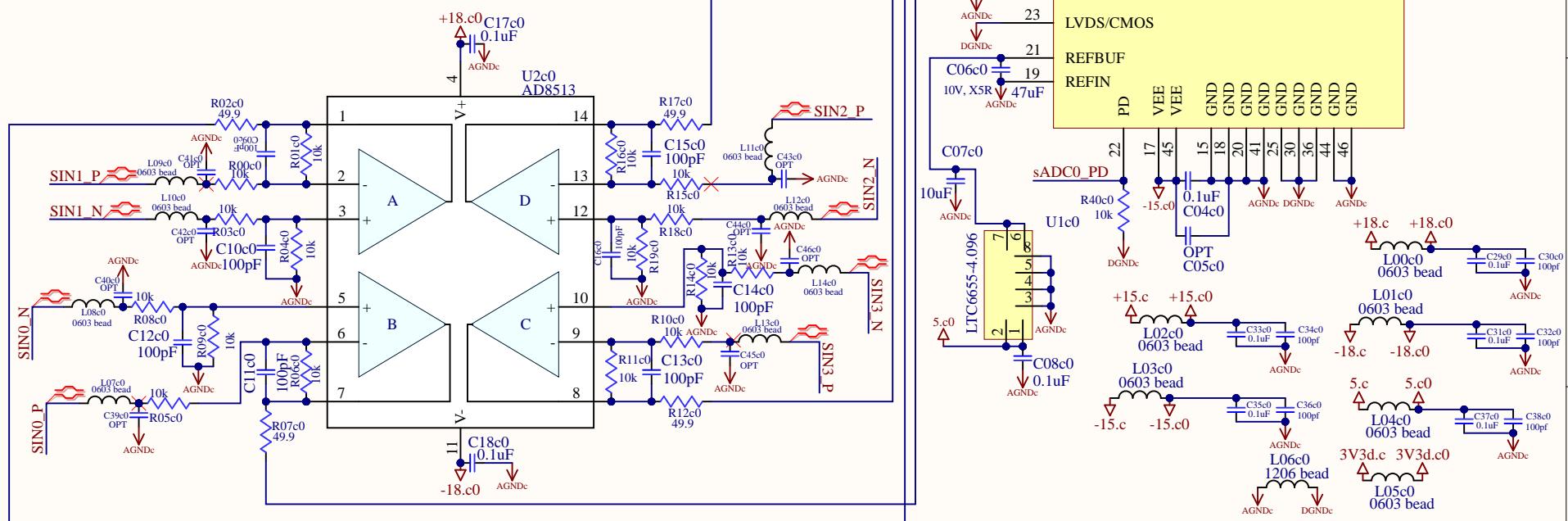
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A

0603 bead is Wurth 74279266
 1206 bead is Laird-Signal Integrity Products HZ1206C202R-10

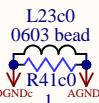


B



D

On layer 6 (BTM) the DGND and AGND are connected with a 0603 ferrite bead and a 1 Ω resistor in parallel. This gives a DC short-circuit and a maximum 1 Ω impedance at higher frequencies.



1

2

3

4

Title: Penn State Cd Clock FPGA Control System

Board Version: 1.0

Date: 9/6/2022

Sheet 10 of 24

File: LTC2335-16_0.SchDoc

Drawn By: Daniel Schusheim

1

2

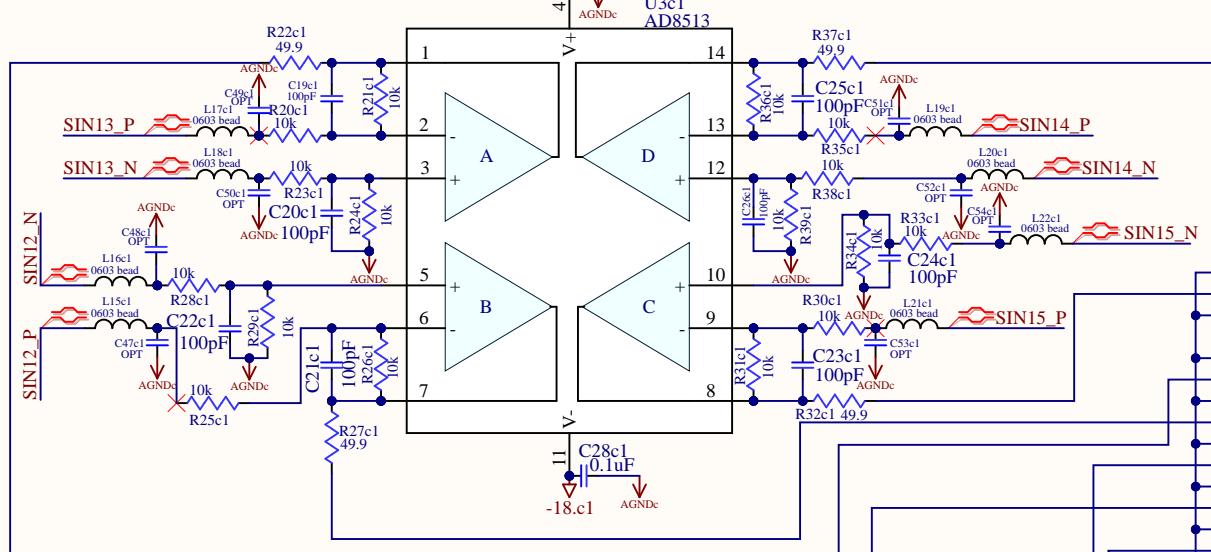
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4

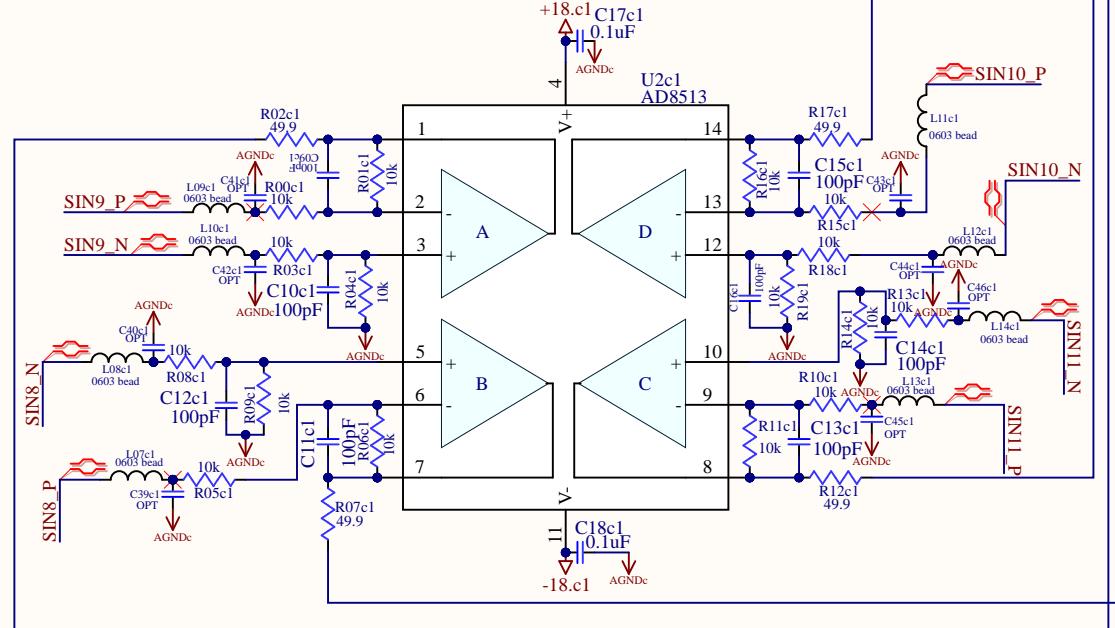
0603 bead is Wurth 74279266

1206 bead is Laird-Signal Integrity Products HZ1206C202R-10

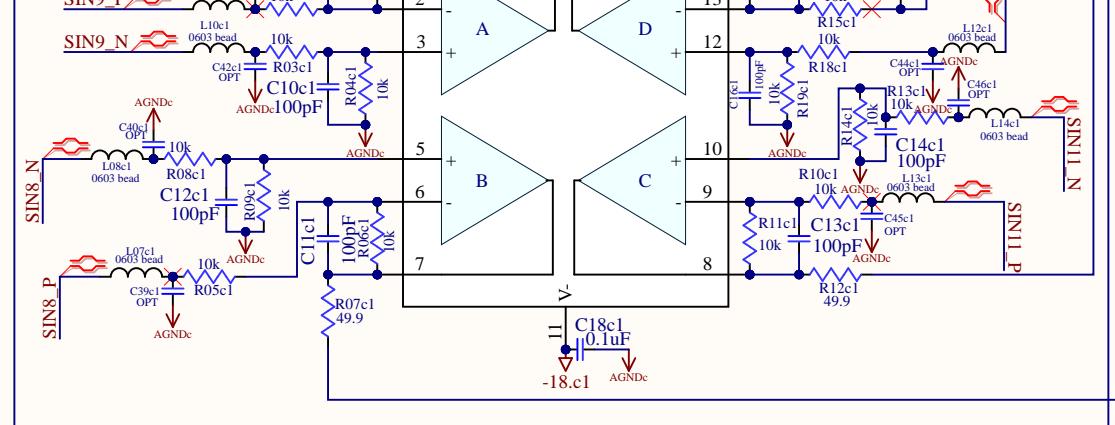
A



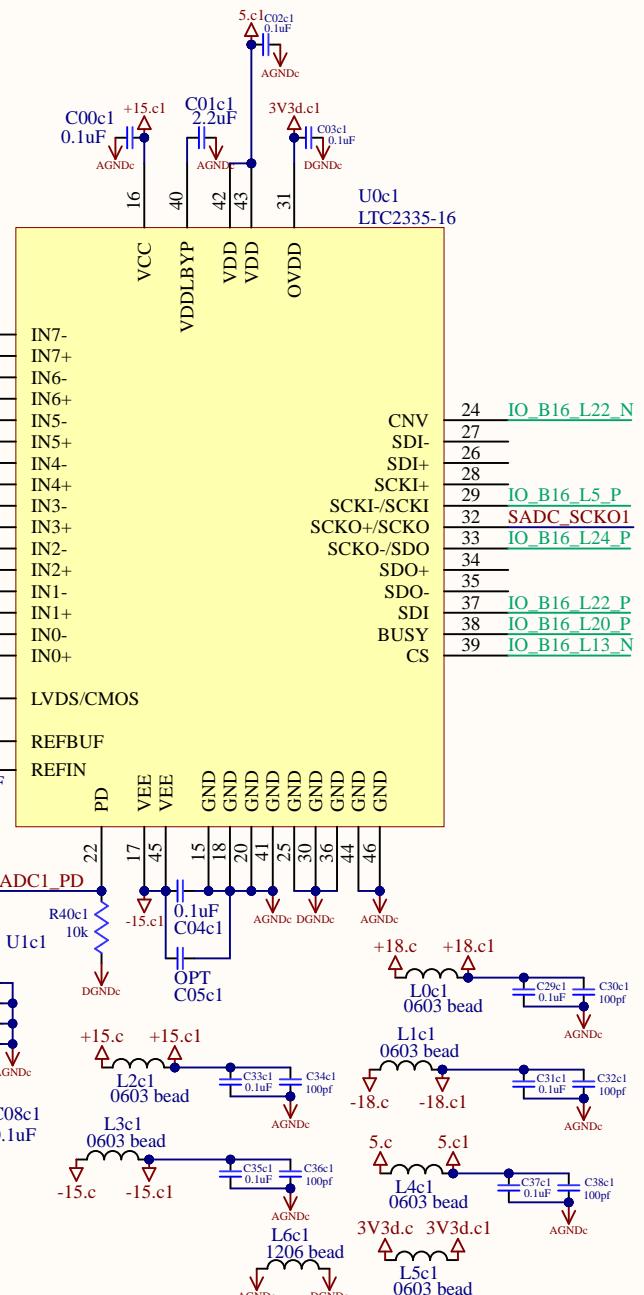
B



C



On layer 6 (BTM) the DGND and AGND are connected with a 0603 ferrite bead and a $1\ \Omega$ resistor in parallel. This gives a DC short-circuit and a maximum $1\ \Omega$ impedance at higher frequencies.



Title: Penn State Cd Clock FPGA Control System

Date: 9/6/2022

File: LTC2335-16_1.SchDoc

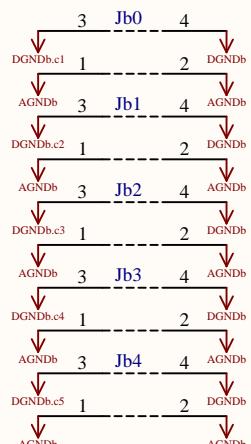
Board Version: 1.0

Sheet 11 of 24

Drawn By: Daniel Schusheim

A

A



B

B

U_MAX5875_0
MAX5875_0.SchDoc

U_MAX5875_3
MAX5875_3.SchDoc

U_MAX5875_1
MAX5875_1.SchDoc

U_MAX5875_4
MAX5875_4.SchDoc

U_MAX5875_2
MAX5875_2.SchDoc

U_MAX5875_5
MAX5875_5.SchDoc

C

C



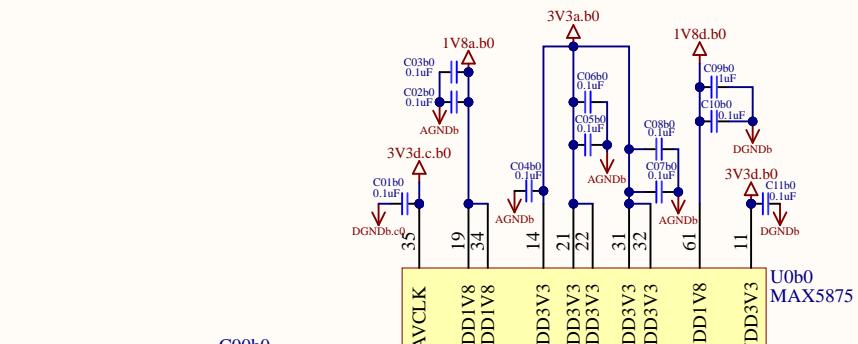
D

D

0603 bead is Wurth 74279266

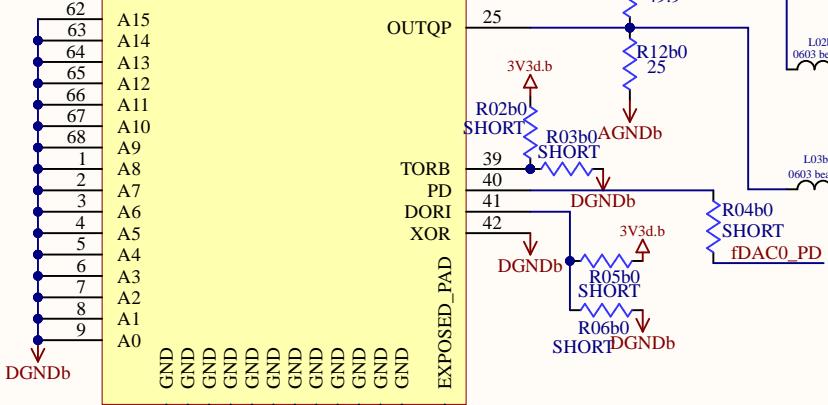
1206 bead is Laird-Signal Integrity Products HZ1206C202R-10

A

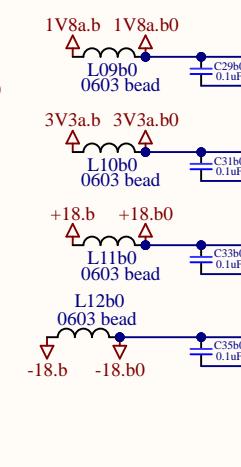
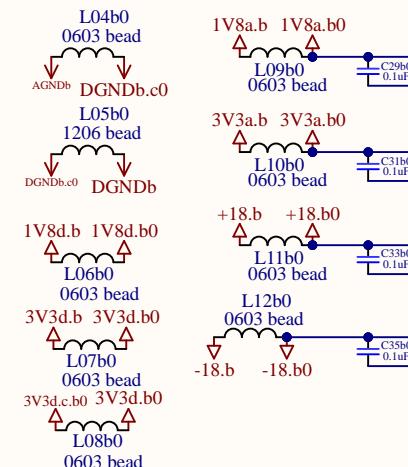
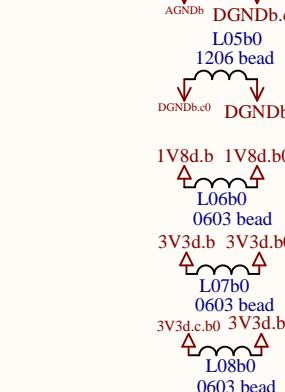


IO_B15_L17_P	37
IO_B15_L17_N	38
IO_B15_L14_P	44
IO_B15_L14_N	45
IO_B15_L16_P	46
IO_B15_L16_N	47
IO_B15_L21_P	48
IO_B15_L21_N	49
IO_B15_L19_P	50
IO_B15_L19_N	51
IO_B15_L23_P	52
IO_B15_L23_N	53
IO_B15_L24_P	54
IO_B15_L24_N	55
IO_B15_L22_P	56
IO_B15_L22_N	57
IO_B15_L20_P	58
IO_B15_L20_N	59
IO_B15_L20_N	60

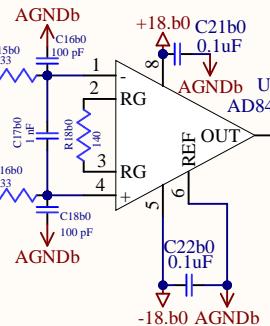
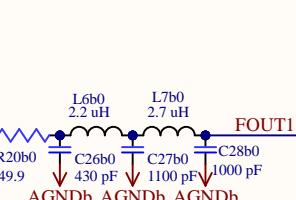
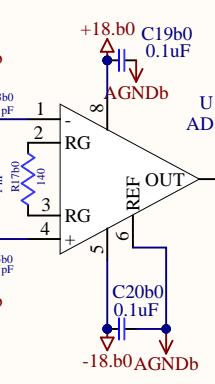
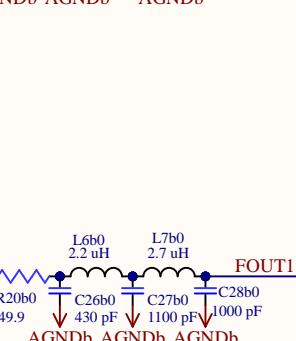
C



On layer 6 (BTM) the DGND and AGND are connected with a 0603 ferrite bead and a 1 Ω resistor in parallel. This gives a DC short-circuit and a maximum 1 Ω impedance at higher frequencies.



5 MHz, 5th order Chebychev filter for high impedance load.



5 MHz, 5th order Chebychev filter for high impedance load.



A

B

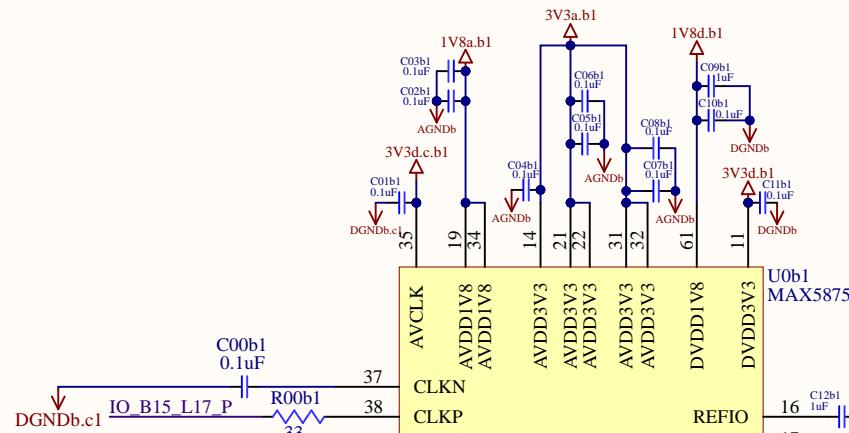
C

D

0603 bead is Wurth 74279266

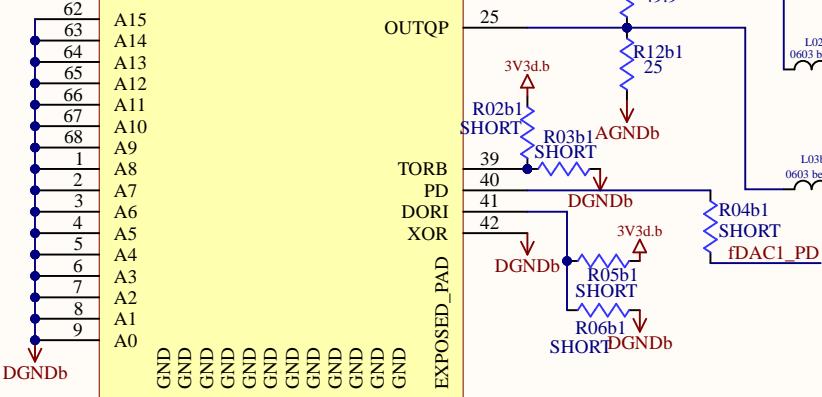
1206 bead is Laird-Signal Integrity Products HZ1206C202R-10

A

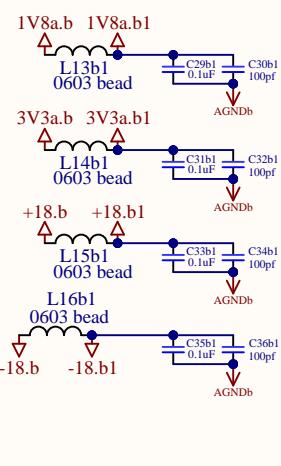


B
IO_B16_L17_P 37
C00b1 0.1uF
IO_B16_L11_P 38
R00b1 33
IO_B16_L11_N 44
IO_B16_L19_P 45
IO_B16_L19_N 46
IO_B16_L17_P 47
IO_B16_L17_N 48
IO_B16_L3_P 49
IO_B16_L3_N 50
IO_B16_L15_P 51
IO_B16_L15_N 52
IO_B16_L18_P 53
IO_B16_L18_N 54
IO_B16_L16_P 55
IO_B16_L16_N 56
IO_B16_L4_P 57
IO_B16_L4_N 58
IO_B16_L6_P 59
IO_B16_L6_N 60

C



D
On layer 6 (BTM) the DGND and AGND are connected with a 0603 ferrite bead and a 1 Ω resistor in parallel. This gives a DC short-circuit and a maximum 1 Ω impedance at higher frequencies.



5 MHz, 5th order Chebychev filter for high impedance load.
U1b1 AD8421
+18.b1 C19b1 0.1uF
L00b1 0603 bead
R07b1 25
L01b1 0603 bead
R08b1 49.9
R09b1 25
R10b1 25
R11b1 49.9
R12b1 25
R13b1 33
R15b1 33
R16b1 33
R19b1 49.9
R20b1 49.9
C13b1 100 pF
C15b1 100 pF
C20b1 0.1uF
C21b1 0.1uF
C22b1 0.1uF
C23b1 430 pF
C24b1 1100 pF
C25b1 1000 pF
L04b1 2.2 uH
L05b1 2.7 uH
L06b1 2.2 uH
L07b1 2.7 uH
FOUT2
FOUT3

A

Title: Penn State Cd Clock FPGA Control System		Board Version: 1.0
Date: 9/6/2022	Sheet 14 of 24	
File: MAX5875_1.SchDoc	Drawn By: Daniel Schusheim	

0603 bead is Wurth 74279266

1206 bead is Laird-Signal Integrity Products HZ1206C202R-10

A

B

C

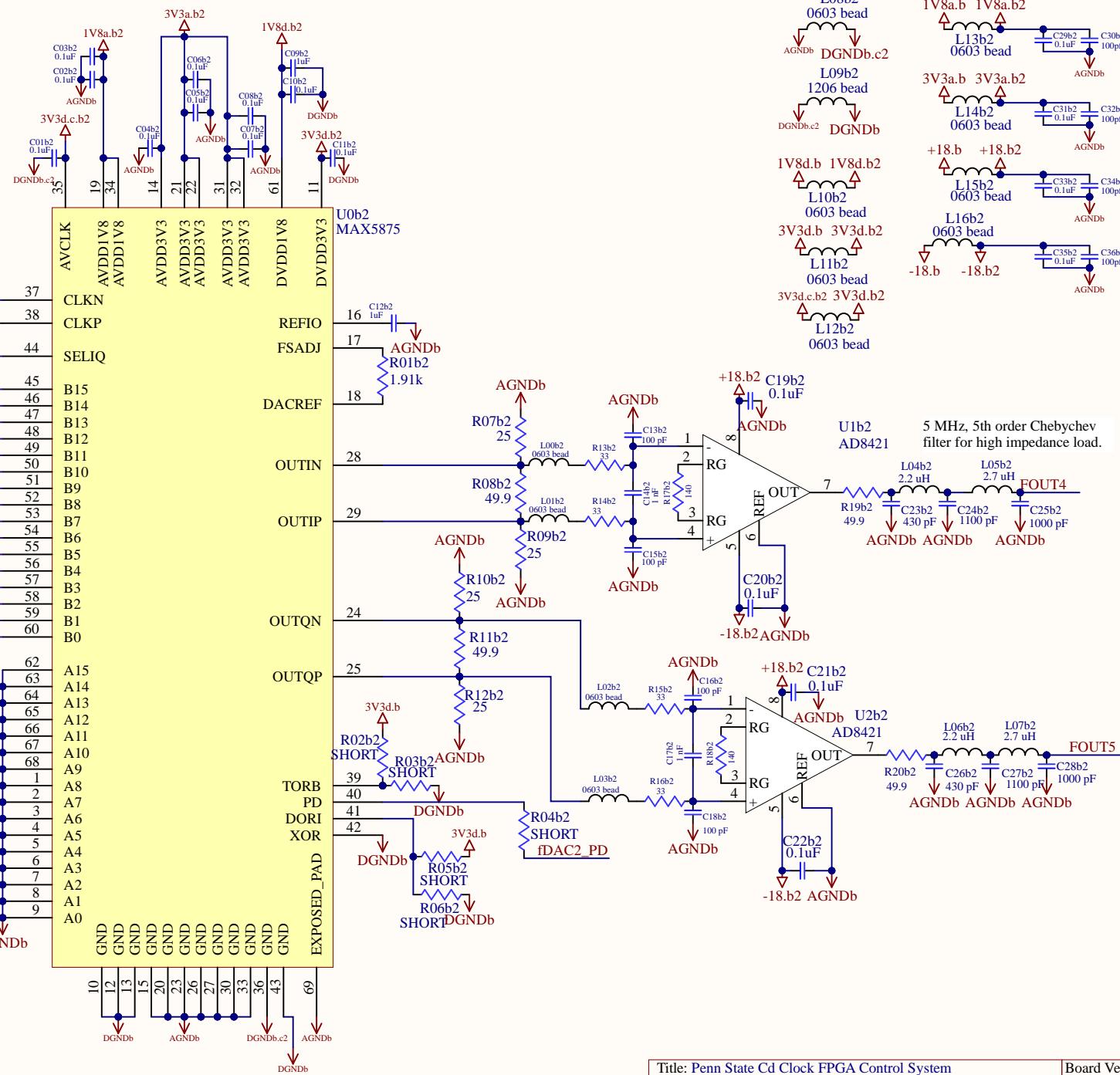
D

A

B

C

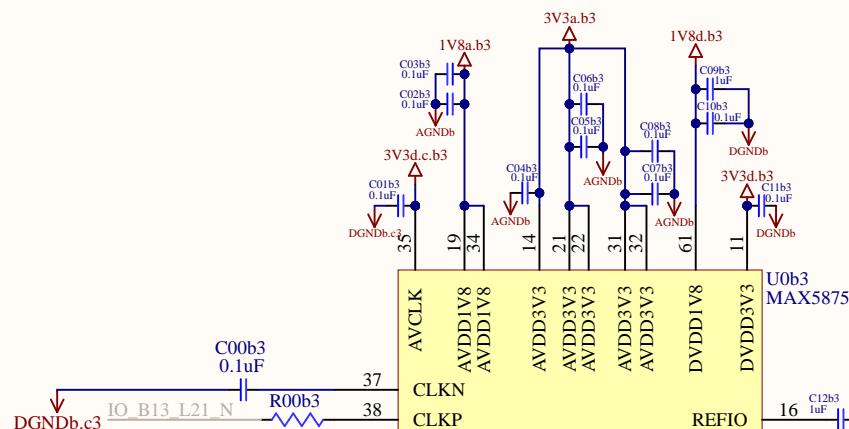
D



0603 bead is Wurth 74279266

1206 bead is Laird-Signal Integrity Products HZ1206C202R-10

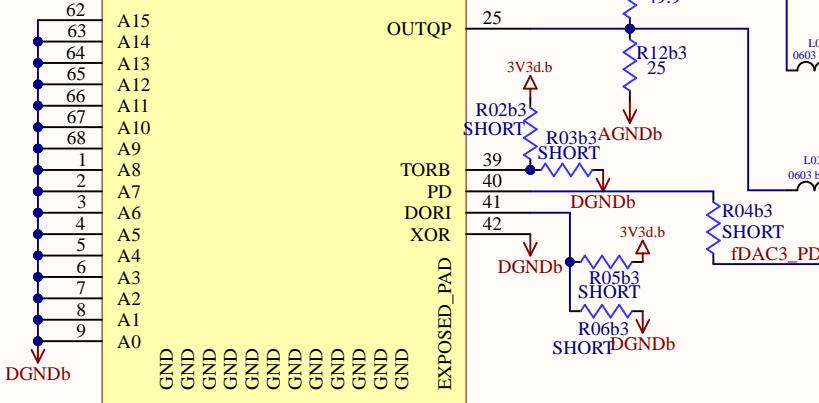
A



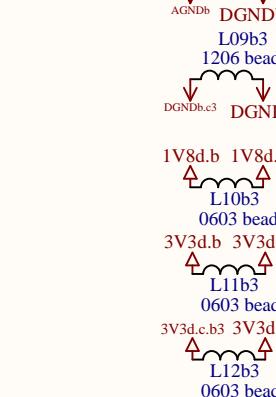
B

IO_B13_L21_N	45
IO_B13_L22_P	46
IO_B16_L1_N	47
IO_B16_L1_P	48
IO_B16_L7_N	49
IO_B16_L7_P	50
IO_B16_L12_N	51
IO_B16_L12_P	52
IO_B16_L8_N	53
IO_B16_L8_P	54
IO_B16_L10_N	55
IO_B16_L10_P	56
IO_B16_L9_N	57
IO_B16_L9_P	58
IO_B16_J14	59
IO_B16_J8	60

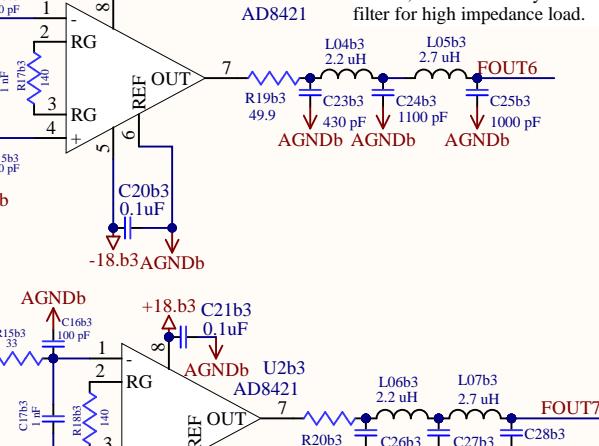
C



On layer 6 (BTM) the DGND and AGND are connected with a 0603 ferrite bead and a 1 Ω resistor in parallel. This gives a DC short-circuit and a maximum 1 Ω impedance at higher frequencies.



5 MHz, 5th order Chebychev filter for high impedance load.



Title: Penn State Cd Clock FPGA Control System

Date: 9/6/2022

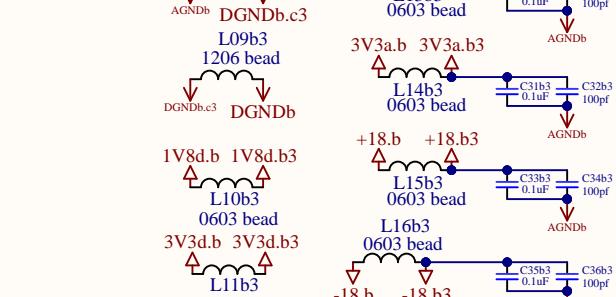
File: MAX5875_3.SchDoc

Board Version: 1.0

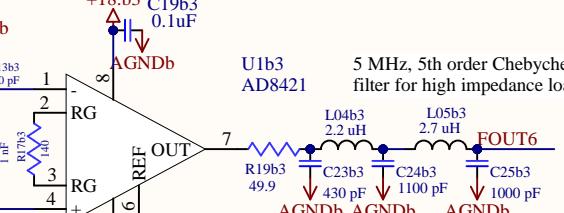
Sheet 16 of 24

Drawn By: Daniel Schusheim

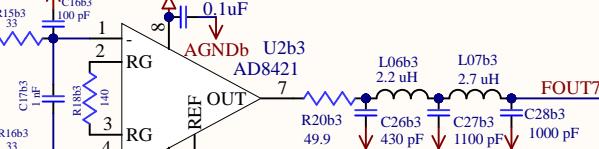
A



B



C



D

Title: Penn State Cd Clock FPGA Control System

Date: 9/6/2022

File: MAX5875_3.SchDoc

Board Version: 1.0

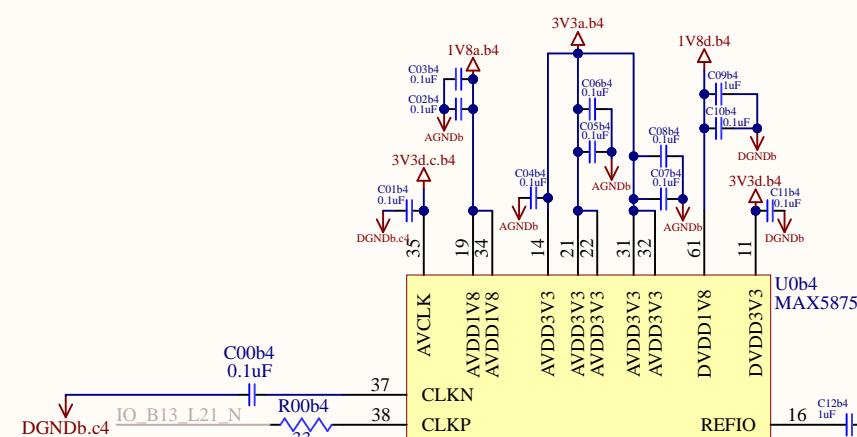
Sheet 16 of 24

Drawn By: Daniel Schusheim

0603 bead is Wurth 74279266

1206 bead is Laird-Signal Integrity Products HZ1206C202R-10

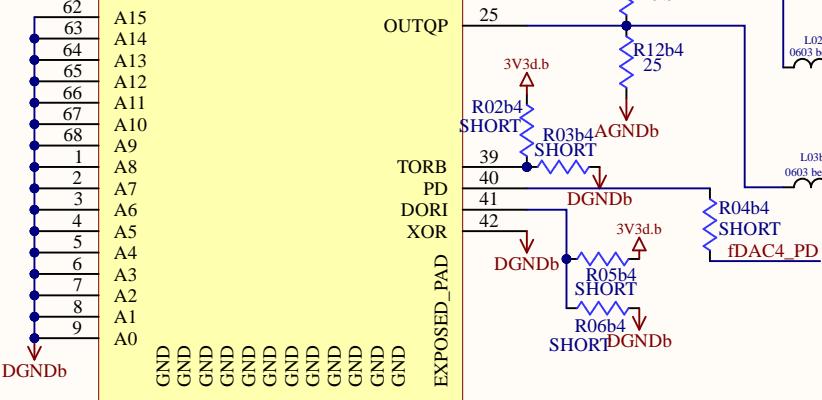
A



B

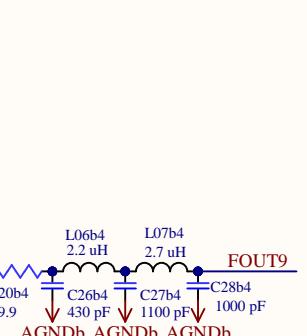
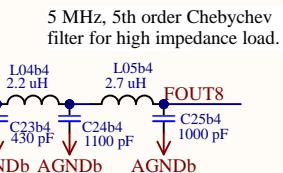
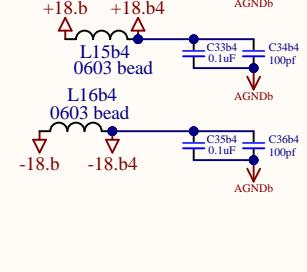
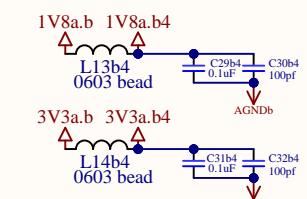
IO_B13_L21_N	45
IO_B13_L20_P	46
IO_B15_L6_N	47
IO_B15_L6_P	48
IO_B15_L7_N	49
IO_B15_L7_P	50
IO_B15_L10_N	51
IO_B15_L10_P	52
IO_B15_L12_N	53
IO_B15_L12_P	54
IO_B15_L9_N	55
IO_B15_L9_P	56
IO_B15_L8_N	57
IO_B15_L8_P	58
IO_B15_M16	59
IO_B15_K15	60

C



D

On layer 6 (BTM) the DGND and AGND are connected with a 0603 ferrite bead and a 1 Ω resistor in parallel. This gives a DC short-circuit and a maximum 1 Ω impedance at higher frequencies.

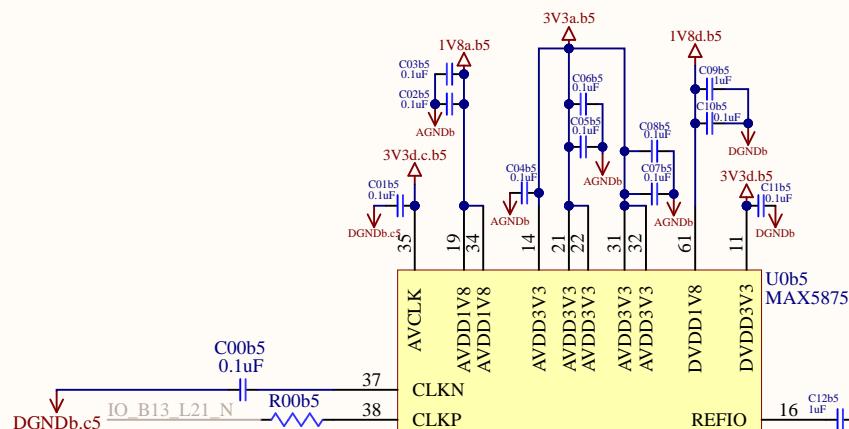


Title: Penn State Cd Clock FPGA Control System	Board Version: 1.0
Date: 9/6/2022	Sheet 17 of 24
File: MAX5875_4.SchDoc	Drawn By: Daniel Schusheim

0603 bead is Wurth 74279266

1206 bead is Laird-Signal Integrity Products HZ1206C202R-10

A



B

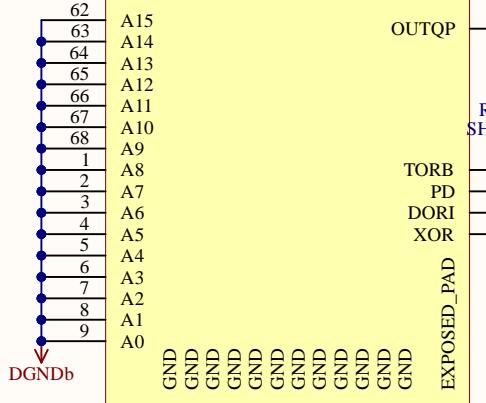
IO_B13_L10_P
IO_B13_L10_N
IO_B13_L13_P
IO_B13_L13_N
IO_B13_L6_N
IO_B13_L6_P
IO_B13_L16_N
IO_B13_L16_P
IO_B13_L18_N
IO_B13_L18_P
IO_B13_L19_N
IO_B13_L19_P
IO_B13_L7_N
IO_B13_L7_P
IO_B13_L15_N
IO_B13_L15_P
IO_B13_L11_N
IO_B13_L11_P

C

On layer 6 (BTM) the DGND and AGND are connected with a 0603 ferrite bead and a 1 Ω resistor in parallel. This gives a DC short-circuit and a maximum 1 Ω impedance at higher frequencies.



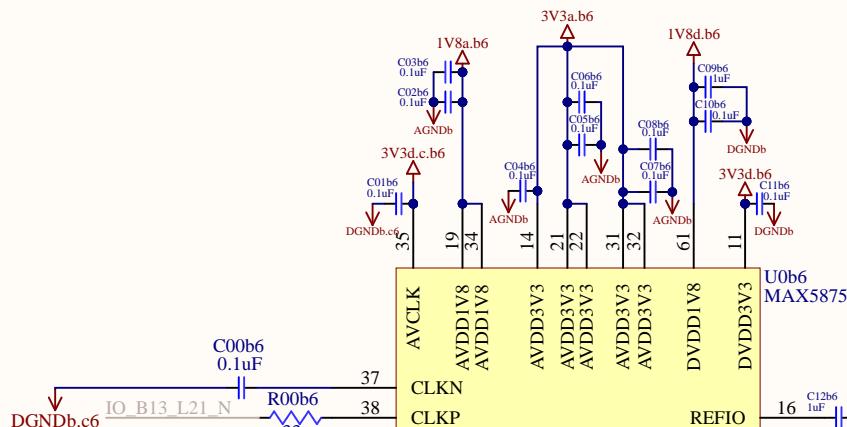
D



0603 bead is Wurth 74279266

1206 bead is Laird-Signal Integrity Products HZ1206C202R-10

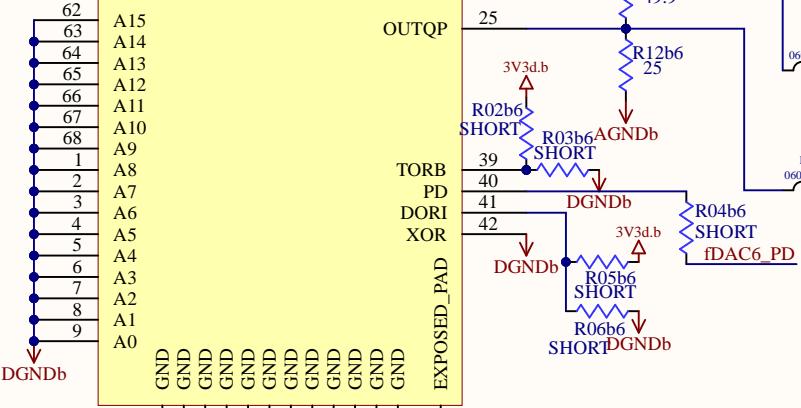
A



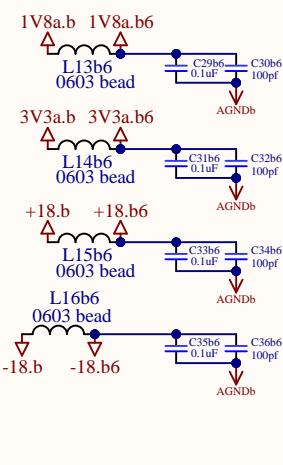
B

IO_B13_L21_N	37
IO_B13_L8_N	38
IO_B13_L8_P	44
IO_B13_L12_N	45
IO_B13_L12_P	46
IO_B13_L1_N	47
IO_B13_L1_P	48
IO_B13_L17_N	49
IO_B13_L17_P	50
IO_B13_L9_N	51
IO_B13_L9_P	52
IO_B13_L4_N	53
IO_B13_L4_P	54
IO_B13_L14_N	55
IO_B13_L14_P	56
IO_B13_L24_N	57
IO_B13_L24_P	58
IO_B13_L23_N	59
IO_B13_L23_N	60

C

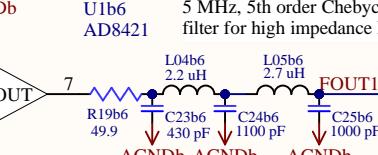


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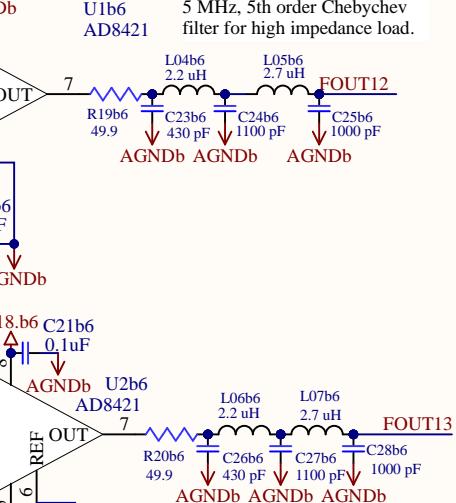


A

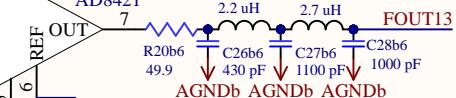
5 MHz, 5th order Chebychev filter for high impedance load.



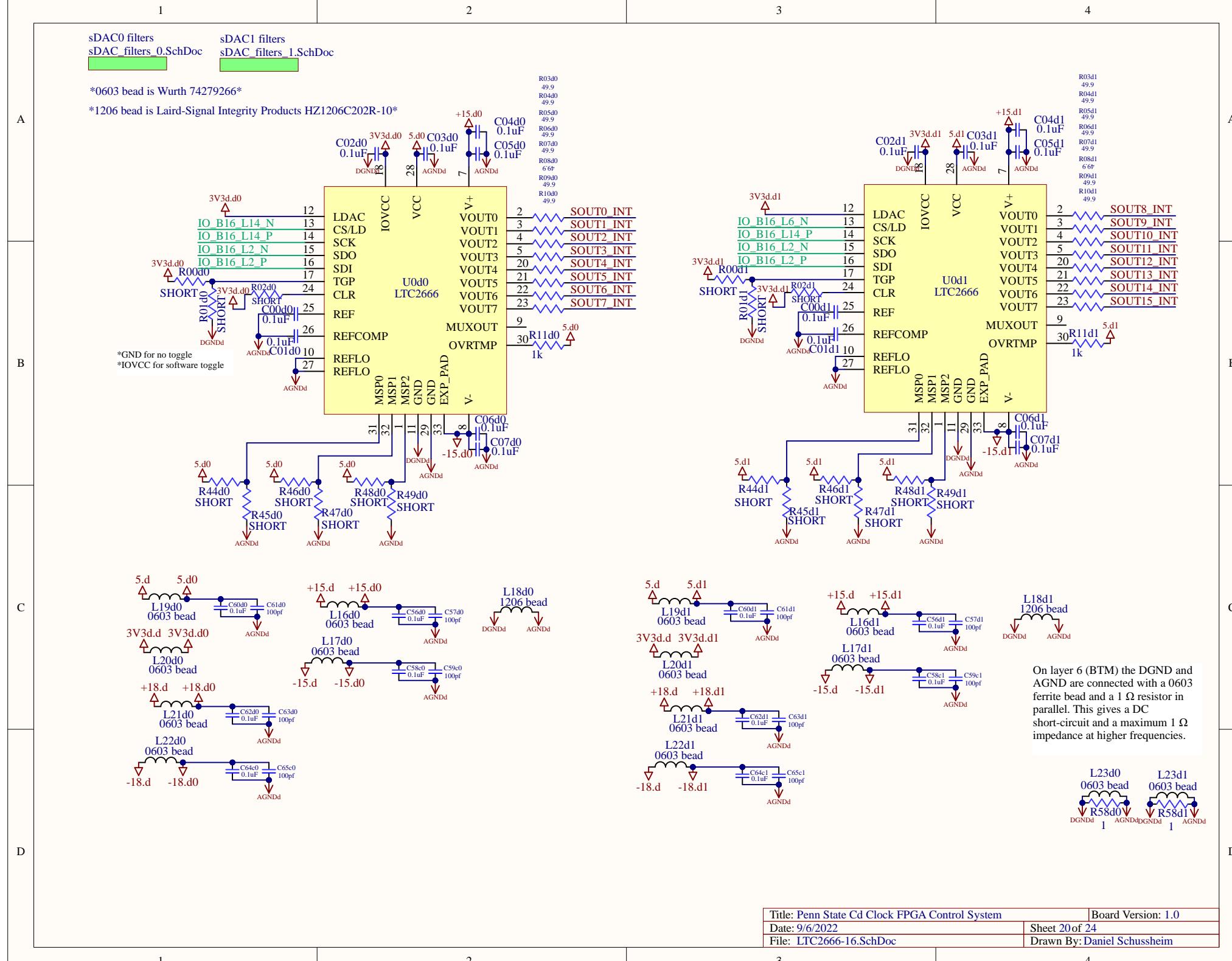
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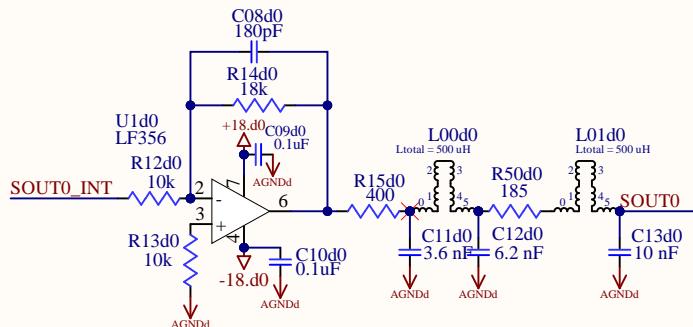
C



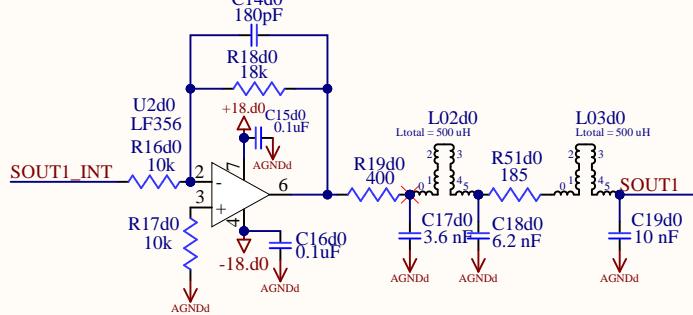
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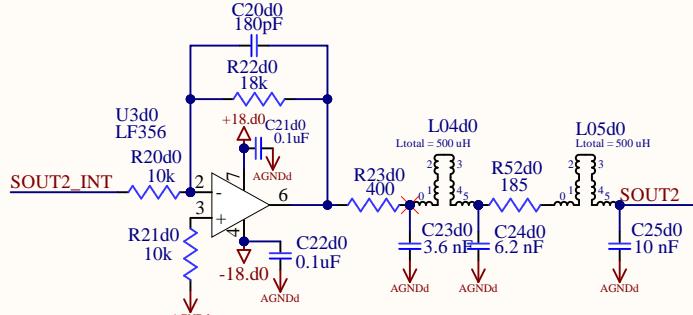
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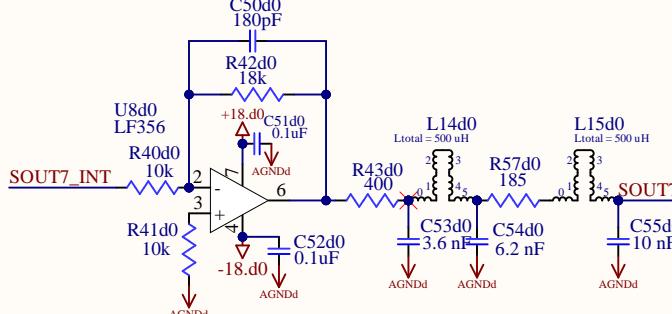
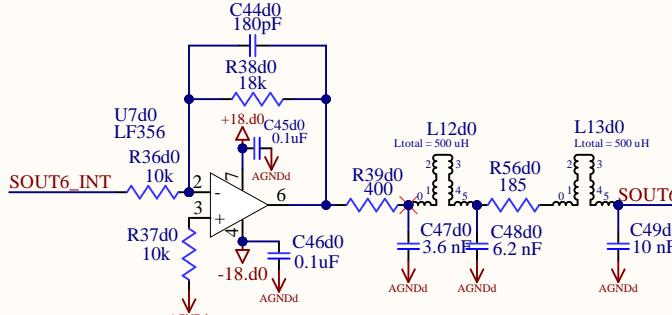
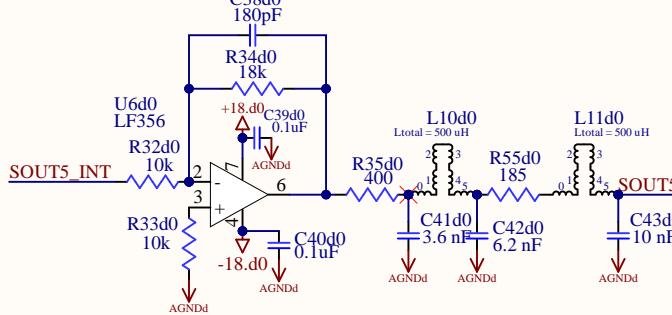
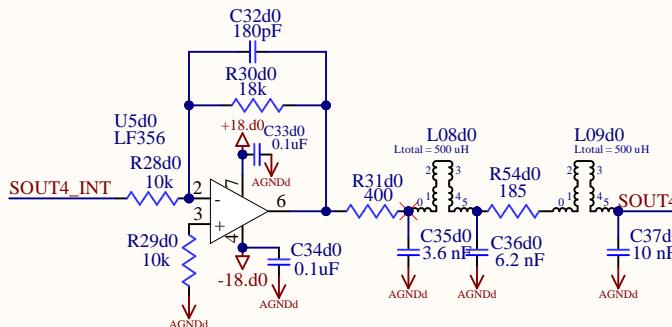
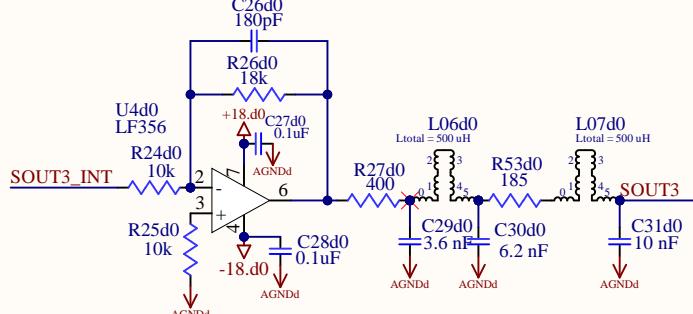
B



C



D

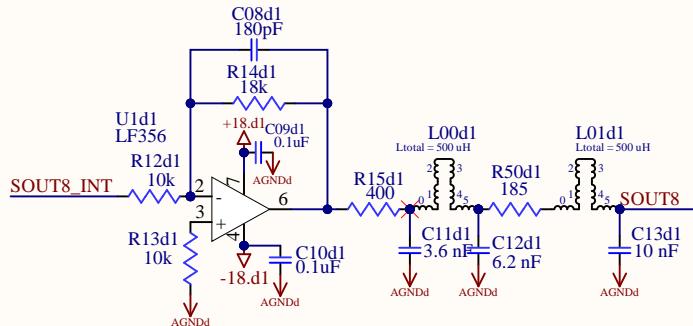


Outputs have 5th order filters with a 20 kHz cutoff, to suppress 50 kHz glitches, and a steeper roll down above 300 kHz, to further suppress higher harmonics. The filters are configured to drive high impedance outputs.

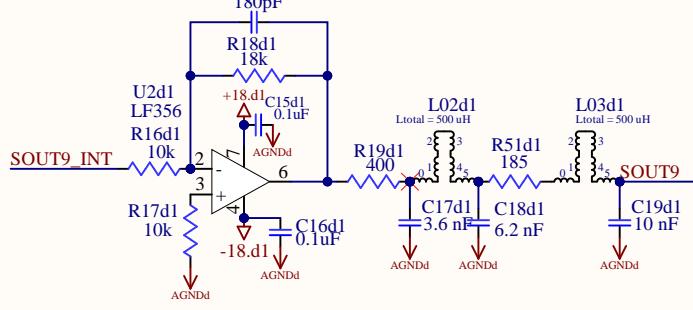
Inductances >100 μ H are made of up to 6 series inductors. Here, we use 5 \times 100 μ H R50d0 and one short.

Title: Penn State Cd Clock FPGA Control System	Board Version: 1.0
Date: 9/6/2022	Sheet 21 of 24
File: sDAC_filters_0.SchDoc	Drawn By: Daniel Schusheim

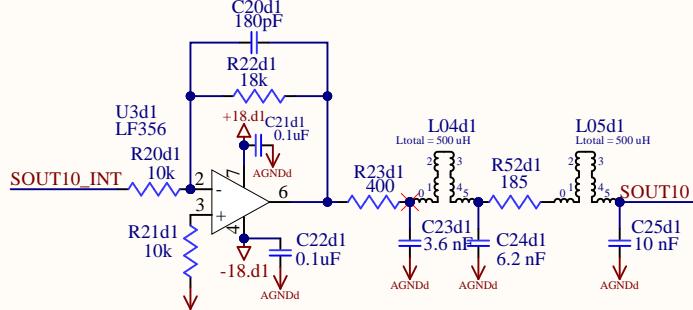
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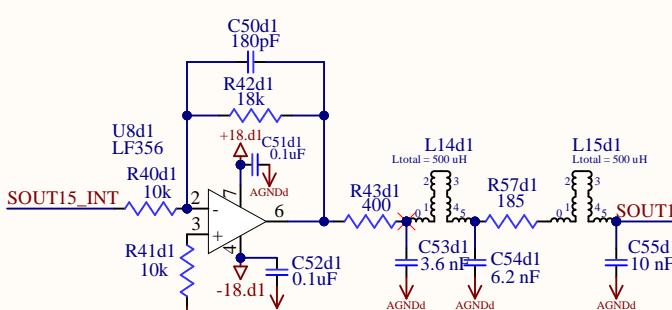
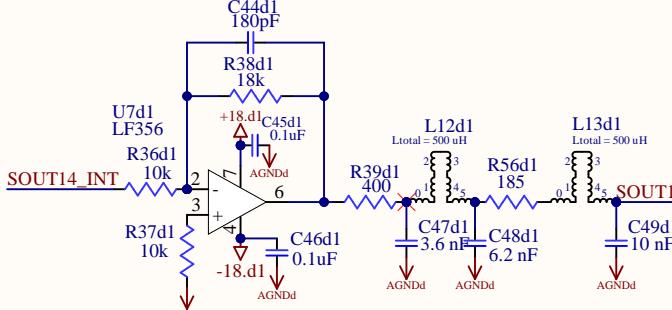
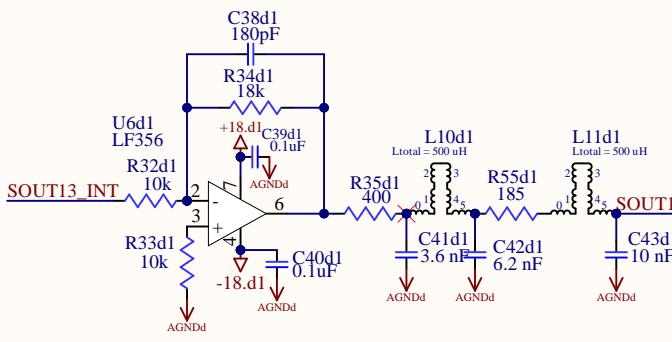
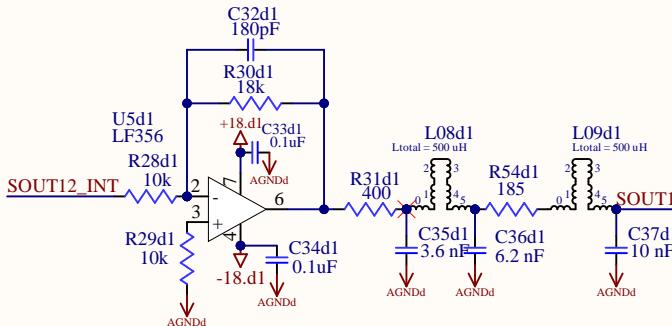
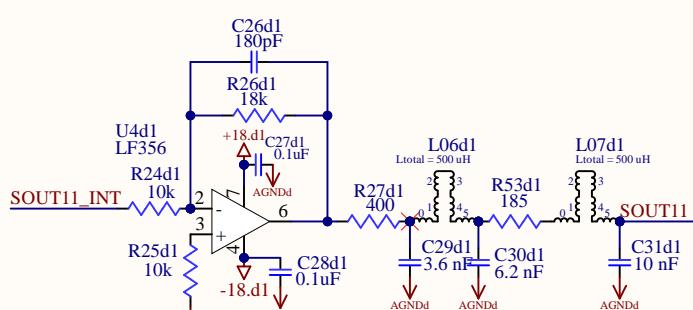
B



C



D



Outputs have 5th order filters with a 20 kHz cutoff, to suppress 50 kHz glitches, and a steeper roll down above 300 kHz, to further suppress higher harmonics. The filters are configured to drive high impedance outputs.

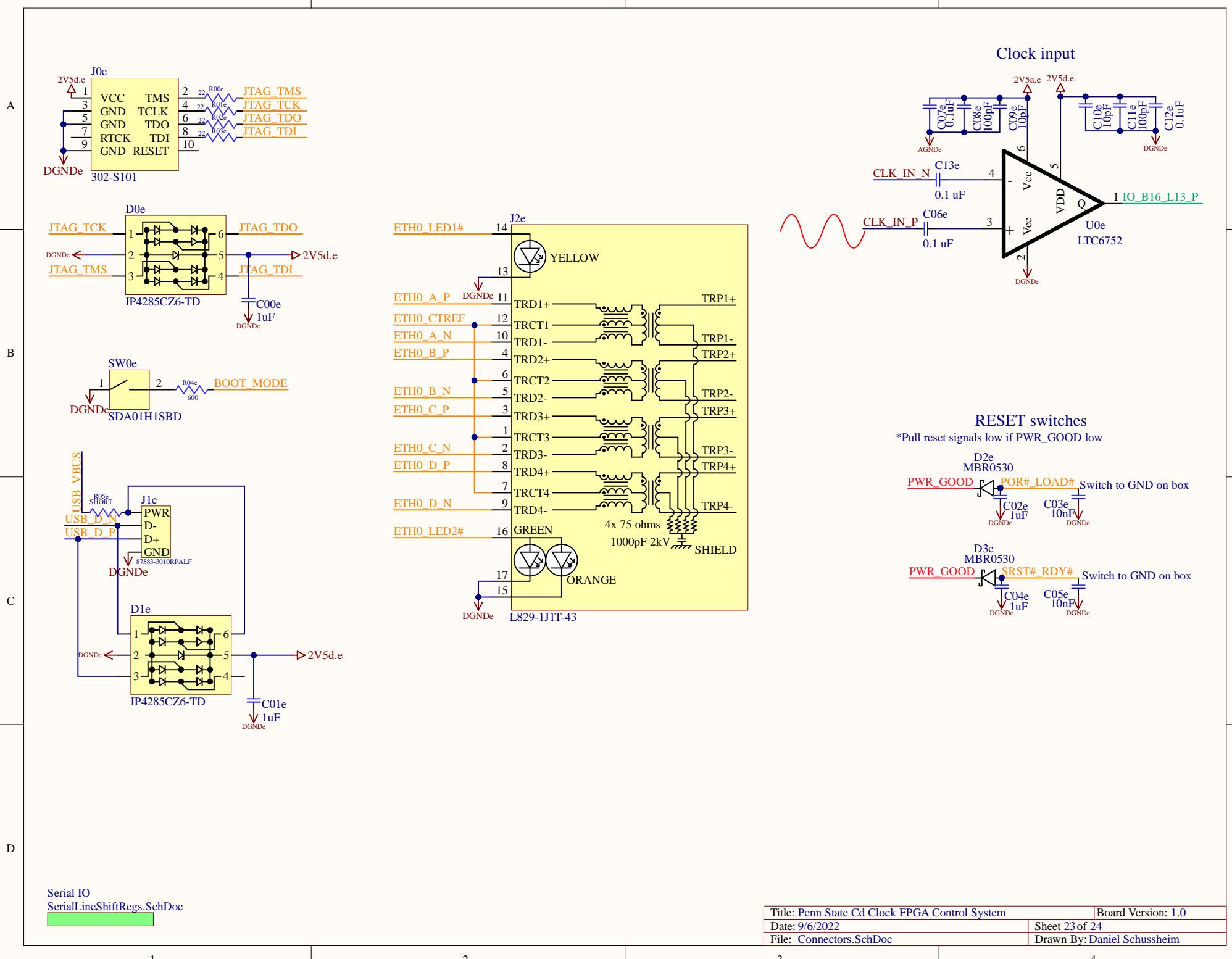
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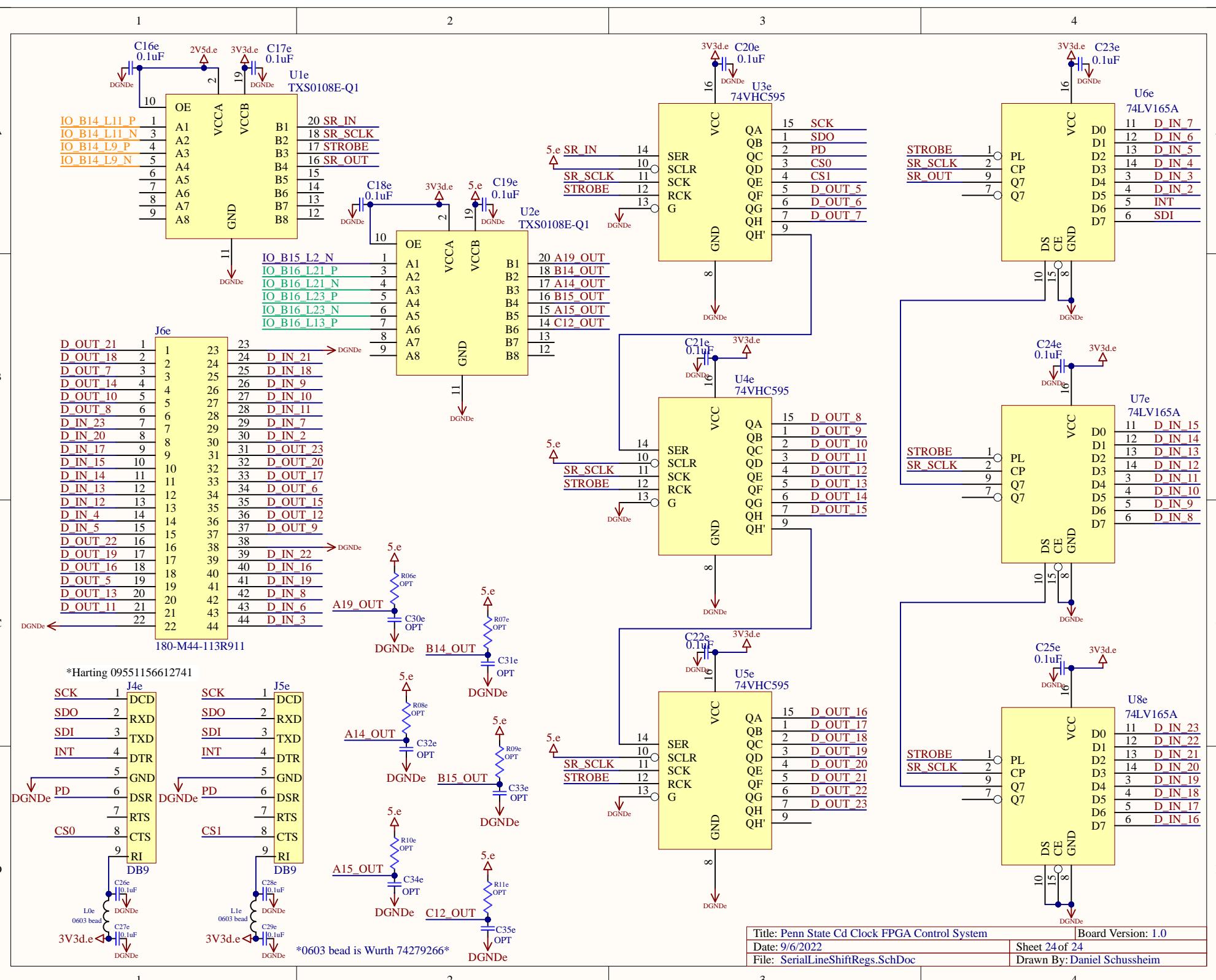
A

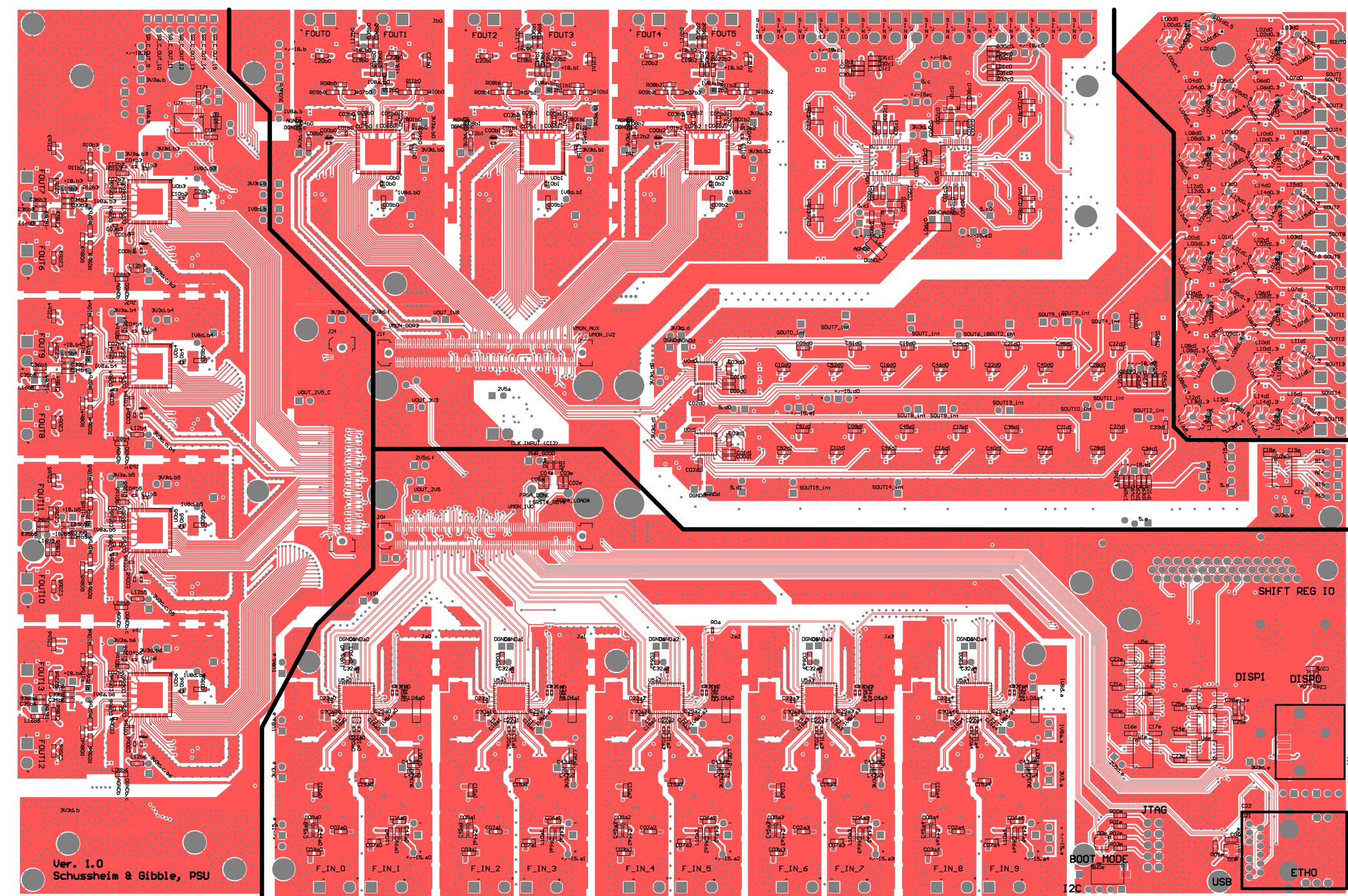
B

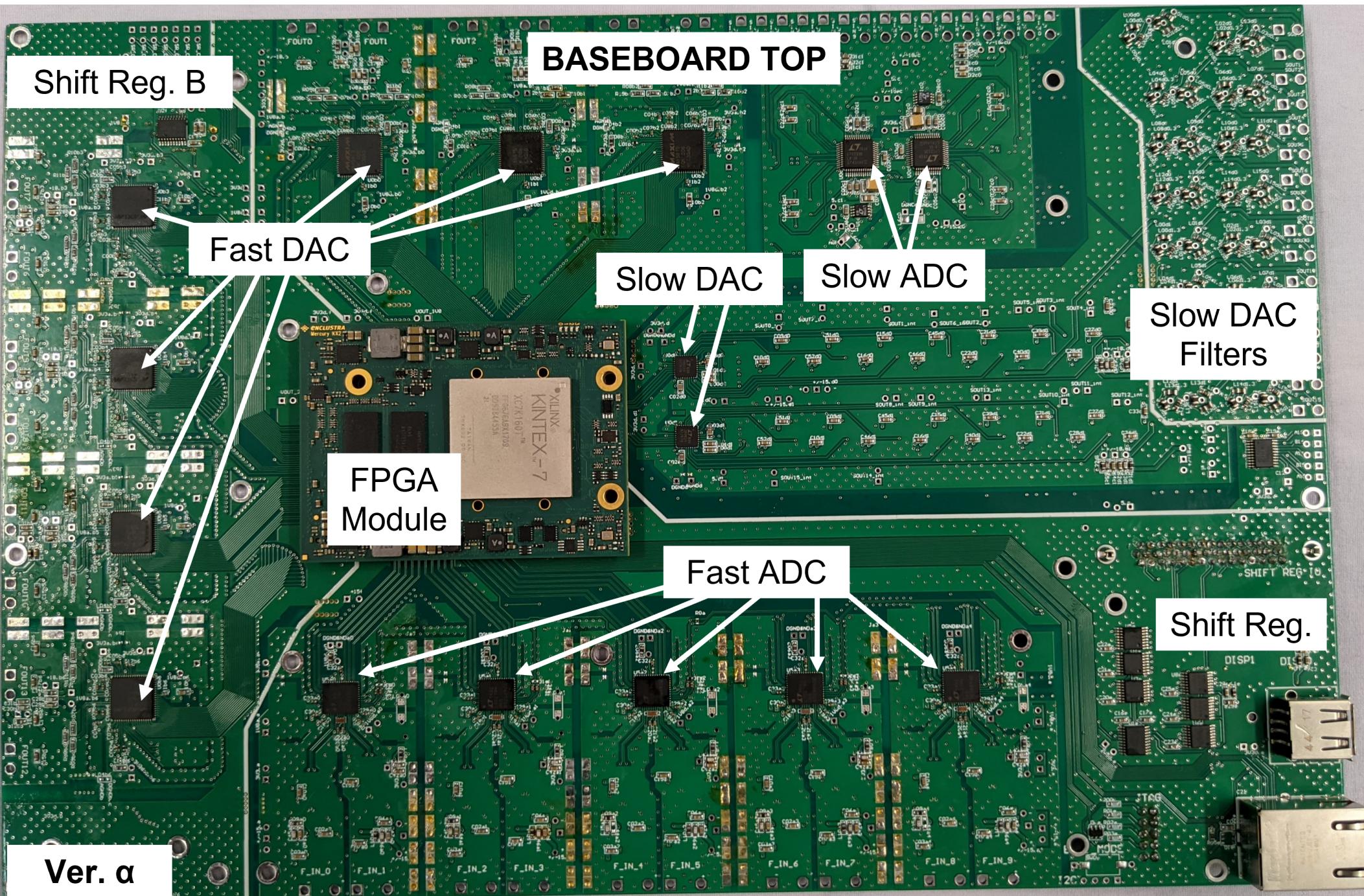
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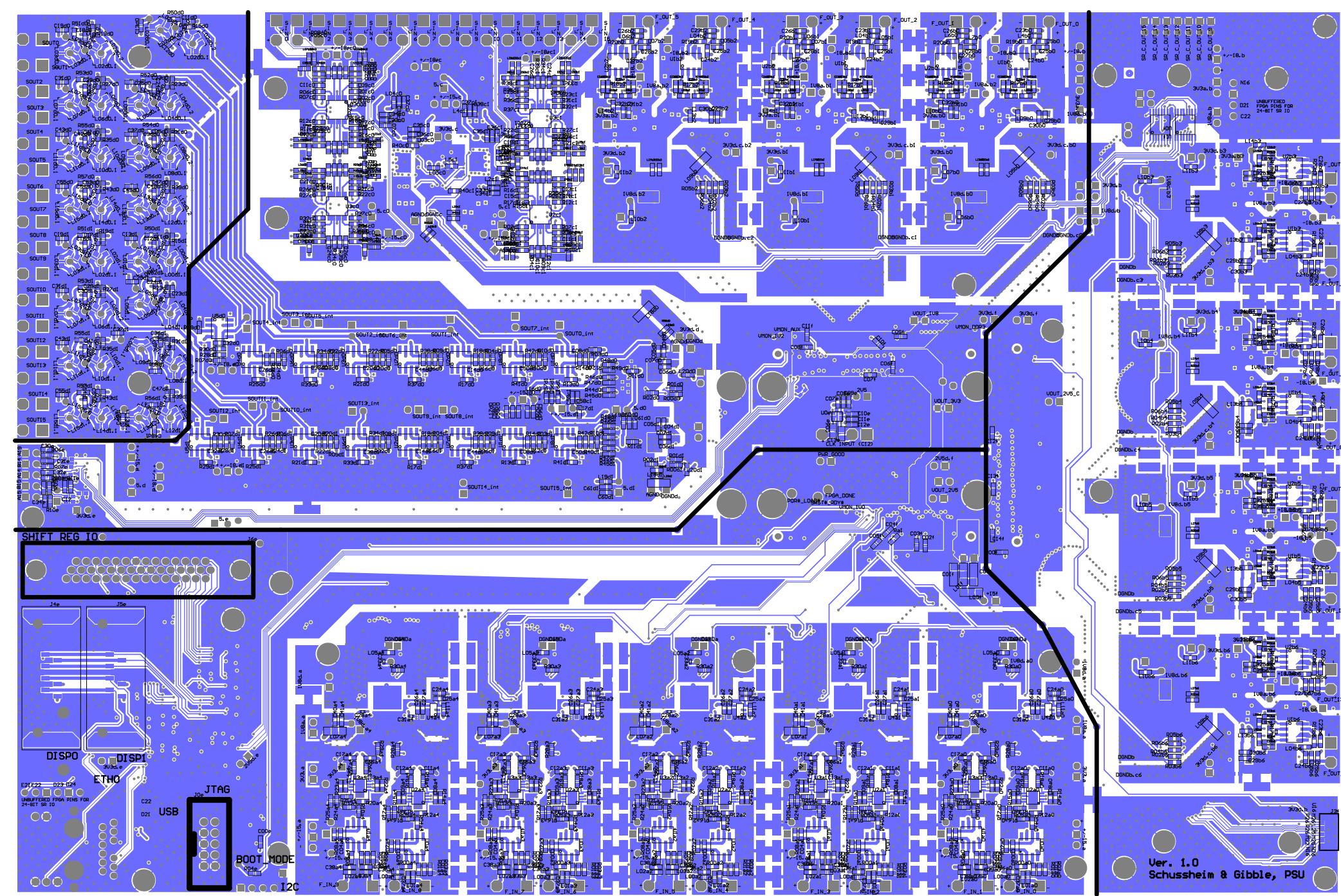
D











BASEBOARD BOTTOM

Slow DAC
Filters

Slow ADC
input amps

Fast DAC
output amps

Slow DAC
output amps

Digital I/O
Connector

Fast ADC
input amps

Display
Connectors

Shift Reg.

Shift Reg. B

FPC Conn.

Ver. α

JTAG
Connector