|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| ALU | | | | | |
| sel\_a | **sel\_b** | **OP1** | **OP2** | **Operación** | **Resultado** |
| 0 | 0 | 0 | 0 | AND | ab |
| 0 | 0 | 0 | 1 | OR | a+b |
| 0 | 0 | 1 | 0 | XOR | aXORb |
| 1 | 1 | 0 | 1 | NAND | (ab)' |
| 1 | 1 | 0 | 0 | NOR | (a+b)' |
| 1 | 0 | 1 | 0 | XNOR | aXNORb |
| 0 | 1 | 1 | 0 |
| 1 | 1 | 0 | 0 | NOT | NOR |
| 1 | 1 | 0 | 1 | NAND |
| 0 | 0 | 1 | 1 | Suma | a+b |
| 0 | 1 | 1 | 1 | Resta | a+(-b) |

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Archivo De Registros | | | | | |
| CLR | **CLK** | **WR** | **SHE** | **DIR** | **Operación** |
| 1 | x | x | x | x | archivo[0,…,15]=0 |
| 0 | ↑ | 1 | 0 | x | archivo[write\_reg]=write\_data |
| 0 | ↑ | 1 | 1 | 0 | >> |
| 0 | ↑ | 1 | 1 | 1 | << |
| x | x | x | x | x | read\_data1=archivo[read\_reg1] |
| read\_data2=archivo[read\_reg2] |

|  |  |  |
| --- | --- | --- |
| Memoria De Datos | | |
| CLK | **WD** | **Operación** |
| ↑ | 1 | Escritura: RAM[dir] = d\_in |
| X | X | Lectura: d\_out = RAM(dir) |

|  |  |  |
| --- | --- | --- |
| Pila | | |
| UP | **DW** | **WPC** |
| 1 | x | 1 |
| 0 | 1 | 0 |