Verification Report

AHB-LITE

# Introduction to the Device-Under-Test (DUT)

AHB-Lite is a subset of the full AHB specification for use in designs where only a single bus master is used. This can either be a simple single-master system, or a multi-layer AHB-Lite system where there is only one AHB master per layer.

AHB-Lite addresses the requirements of high-performance synthesizable  
designs. It is a bus interface that supports a single bus master and provides  
high-bandwidth operation

Masters designed to the AHB-Lite interface specification are significantly simpler in terms of interface design, than a full AHB master. AHB-Lite enables faster design and verification of these masters, and you can add a standard off-the-shelf bus mastering wrapper to convert an AHB-Lite master for use in a full AHB system.

Any master that is already designed to the full AHB specification can be used in an AHB-Lite system with no modification. The majority of AHB slaves can be used interchangeably in either an AHB or AHB-Lite system. This is because AHB slaves that do not use either the Split or Retry response are automatically compatible with both the full AHB and the AHB-Lite specification. It is only existing AHB slaves that do use Split or Retry responses that require you to use an additional standard off-the-shelf wrapper in your AHB-Lite system.

Any slave designed for use in an AHB-Lite system works in both a full AHB and an AHB-Lite design.

# Verification Plan

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| **No.** | **Feature** | **Test Description** | **Ref.** | **Expected outcome** | **Type** | **Result** | **Comments** |
| 1 | Send a low HRESET and read and write data | Send  Low HRESET and generate a 32 bit HADDR to read from memory | AMBA AHB-LITE.pdf/Sec.1 | RESET is active low so there will be no operation performed on DUT | TR |  |  |
| 2 | Keep HSEL low and send a transfer | Generate a transfer and give to AHB Lite memory while keeping HSEL low. | AMBA AHB-LITE.pdf/Sec.1 | Slave is not selected so there will be no output | TR |  |  |
| 3 | Send high HWRITE | Generate 32 bit HADDR and 32 bit HWDATA with high HWRITE signal | AMBA AHB-LITE.pdf/Sec.1 | Data should be written on HADDR | TR |  |  |
| 4 | Send Low HWRITE | Send the same HADDR with the low HWRITE signal. | AMBA AHB-LITE.pdf/Sec.2 | Same data should be read | TR |  |  |
| 5 | Send Low HREADY for 1 clock cycle | Send low HREADY with low HWRITE signal. | AMBA AHB-LITE.pdf/Sec.2 | Data should appear on HRDATA after 1 clock cycle wait | A | Pass |  |
| 6 | Send low HREADY for 2 clock cycle | Send low HREADY with low HWRITE signal. | AMBA AHB-LITE.pdf/Sec.1 | Data should appear on HRDATA after 2 clock cycle wait | A | Pass |  |
| 7 | Send 00 value of HTRANS | Send a transfer with HTRANS value set to 00 | AMBA AHB-LITE.pdf/Sec.3 | . Slave should ignore transfer and set HRESP = 0(okay) within next 2 cycles | TR |  |  |
| 8 | Send 01 value of HTRANS | Send a transfer with HTRANS value set to 01. | AMBA AHB-LITE.pdf/Sec.3 | Slave should ignore transfer and set HRESP = 0(okay) within next 2 cycles | TR |  |  |
| 9 | Send HSIZE signal with HBURST 000 | Generate 3 bit HBURST signal of value 000 with constant HSIZE and send through AHB-lite interface with a transfer | AMBA AHB-LITE.pdf/Sec.3 | Single burst should be written on memory | TR |  |  |
| 10 | Send HSIZE signal with HBURST 001 | Generate 3 bit HBURST signal of value 001 with constant HSIZE and send through AHB-lite interface with a transfer | AMBA AHB-LITE.pdf/Sec.3 | Long undefined increment should be written to the memory | TR |  |  |
| 11 | Send HSIZE signal with HBURST 010 | Generate 3 bit HBURST signal of value 010 with constant HSIZE and send through AHB-lite interface with a transfer | AMBA AHB-LITE.pdf/Sec.3 | Wrap4 burst should be written to the memory | TR |  |  |
| 12 | Send HSIZE signal with HBURST 011 | Generate 3 bit HBURST signal of value 011 with constant HSIZE and send through AHB-lite interface with a transfer | AMBA AHB-LITE.pdf/Sec.3 | Increment 4 burst should be written to the memory | TR |  |  |
| 13 | Send HSIZE signal with HBURST 100 | Generate 3 bit HBURST signal of value 100 with constant HSIZE and send through AHB-lite interface with a transfer | AMBA AHB-LITE.pdf/Sec.3 | Wrap 8 burst should be written to the memory | TR |  |  |
| 14 | Send HSIZE signal with HBURST 101 | Generate 3 bit HBURST signal of value 101 with constant HSIZE and send through AHB-lite interface with a transfer | AMBA AHB-LITE.pdf/Sec.3 | Increment 8 burst should be written to the memory | TR |  |  |
| 15 | Send HSIZE signal with HBURST 110 | Generate 3 bit HBURST signal of value 110 with constant HSIZE and send through AHB-lite interface with a transfer | AMBA AHB-LITE.pdf/Sec.3 | Wrap 16 burst should be written to the memory | TR |  |  |
| 16 | Send HSIZE signal with HBURST 111 | Generate 3 bit HBURST signal of value of 111 with constant HSIZE and send through AHB-lite interface with a transfer | AMBA AHB-LITE.pdf/Sec.3 | Increment 16 burst should be written to the memory | TR |  |  |
| 17 | Read after write transfer | Send Multiple HBURST of different HSIZES. Perform read and write operation setting HWRITE low and high consecutively. | AMBA AHB-LITE.pdf/Sec.3 | The memory should read the data written on the same address before | TR |  |  |
| 18 | Send Low HREADY signal during a burst | Generate a HBURST of size HSIZE and insert HREADY low during bead transfer. | AMBA AHB-LITE.pdf/Sec.3 | Operation should terminate and no data should be written | TR |  |  |
|  | Set HTRANS 00 and send a burst. | HTRANS 00 represents an idle state. A burst of any size should be generated and try to write or read to memory | AMBA AHB-LITE.pdf/Sec.3 | There shouldn’t be any data on read or write bus in next clock cycle. HRESP should signal okay(zero) within next 2 cycles | A | Pass |  |
| 19 | Change HTRANS type by keeping HREADY low | Add idle state between two non-sequential states and keep HREADY low for transfer. Address must remain constant for non-sequential type until HREADY is high | AMBA AHB-LITE.pdf/Sec.3 | HRESP should signal okay within next 2 cycles | A | Pass |  |
| 20 | Send non-sequential transfer to a non-existent address | Generate an address that is not present in the memory. Send non seq. transfer to that address. | AMBA AHB-LITE.pdf/Sec.4 | HRESP should become high for such transfer within next 2 cycles | A | Pass |  |
| 21 | Send sequential transfer to a non-existent address | Generate an address that is not present in the memory. Send seq. transfer to that address. HRESP should become high for such transfer | AMBA AHB-LITE.pdf/Sec.4 | HRESP should become high for such transfer within next 2 cycles | A | Pass |  |
|  | Send single burst to the memory | Generate a single burst and send to random address in the memory | AMBA AHB-LITE.pdf/Sec.5 | HRESP should be zero and HREADY should be 1 in next cycle which signals a successful transfer | A | Pass |  |