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**COURSE/YR:** BSCpE – 3A
**SUBJECT:** CPE 366 – INTRO TO HDL

# SYNCHRONOUS BINARY UP COUNTER

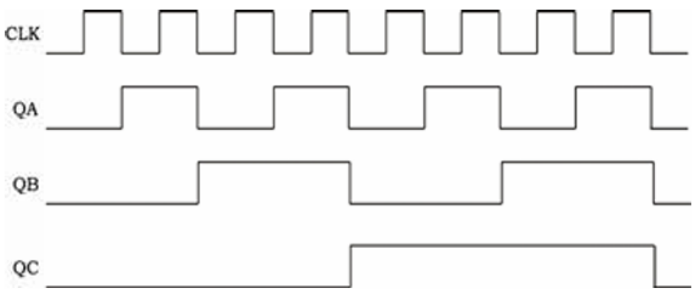
**VHDL CODE FOR SYNCHRONOUS BINARY UP COUNTER:**

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;
entity synbicount is
Port (rs,clk: in STD_LOGIC;
q: inout STD_LOGIC_VECTOR (3 downto 0));
end synbicount;
architecture Behavioral of synbicount is
signal div:std_logic_vector(22 downto 0);
signal temp:STD_LOGIC_VECTOR (3 downto 0);
signal clkd:std_logic;
begin
process(clk)
begin
if rising_edge(clk)then
div<= div+1;
end if;
end process;
clkd<=div(22);
process(clkd)
begin
```

```
if(clkd='1' and clkd'event) then
if(rs='1') then temp<=(others=>'0');
else temp<=temp+1;
end if;
q<= temp;
end if;
end process;
end Behavioral;
```

**TRUTH TABLE:**

| 3-bit Asynchronous up counter | | | |
|---|---|---|---|
| Clock | QC | QB | QA |
| 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 |
| 2 | 0 | 1 | 0 |
| 3 | 0 | 1 | 1 |
| 4 | 1 | 0 | 0 |
| 5 | 1 | 0 | 1 |
| 6 | 1 | 1 | 0 |
| 7 | 1 | 1 | 1 |
| 8 | 0 | 0 | 0 |
| 9 | 0 | 0 | 1 |




**RTL VIEWER:**