NAME: GIELO MAR R. BANDOY
COURSE/YR: BSCpE – 3A
SUBJECT: CPE 366 – INTRO TO HDL

T FLIP FLOP

12. VHDL CODE T FLIP FLOP:

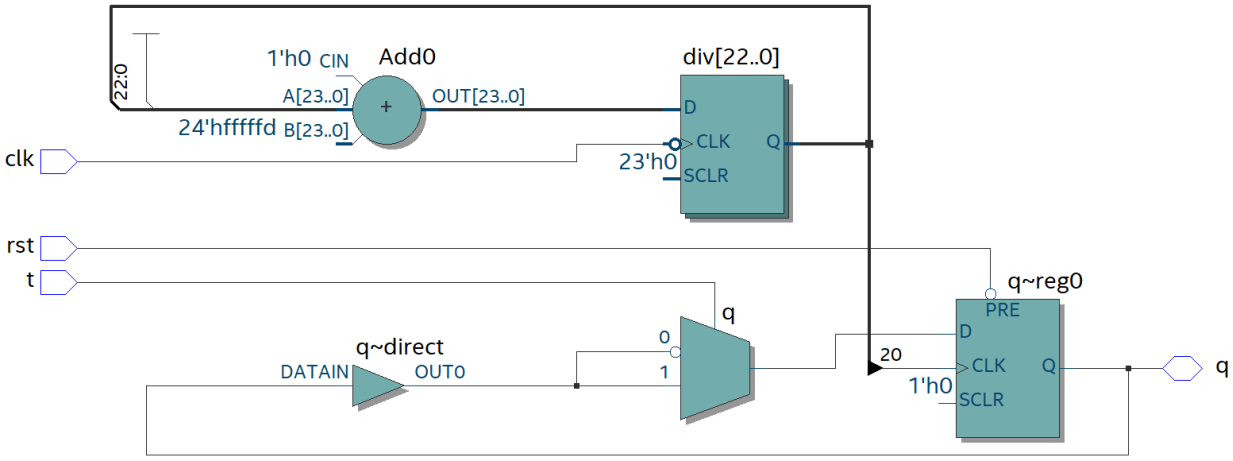
```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;

entity TFlipFlop is
   Port (
      t   : in  STD_LOGIC;
      clk : in  STD_LOGIC;
      rst : in  STD_LOGIC;
      q   : inout  STD_LOGIC
   );
end TFlipFlop;

architecture Behavioral of TFlipFlop is
   signal div  : std_logic_vector(22 downto 0);
   signal clkd : std_logic;
begin

   -- Falling edge instead of rising edge
   process(clk)
   begin
      if falling_edge(clk) then
         div <= div - 1;  -- reverse addition
```

```
    end if;
  end process;

  clkd <= not div(20);  -- reverse signal logic

  process(clkd, rst)
  begin
    if (rst = '0') then   -- reverse active-high reset to active-low
      q <= '1';        -- reverse reset value
    elsif (clkd'event and clkd = '0' and t = '0') then  -- reverse clock and T logic
      q <= not q;
    else
      q <= q;
    end if;
  end process;

end Behavioral;
```

TRUTH TABLE OF T FLIP FLOP:

Clear	T	Clock	Qn+1	$\overline{Qn+1}$
1	0	0	0	$\overline{Qn}$
0	1	⎍	$\overline{Qn}$	Qn

RTL VIEWER:


22:0
1'h0 CIN
Add0
A[23..0]
OUT[23..0]
24'hfffffd B[23..0]
+
div[22..0]
D
CLK
Q
23'h0
SCLR
clk
rst
t
q
0
1
q~direct
DATAIN
OUT0
q~reg0
PRE
D
20
CLK
Q
1'h0
SCLR
q