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COURSE/YR: BSCpE – 3A
SUBJECT: CPE 366 – INTRO TO HDL

BCD UP COUNTER

VHDL CODE OF BCD UP COUNTER:

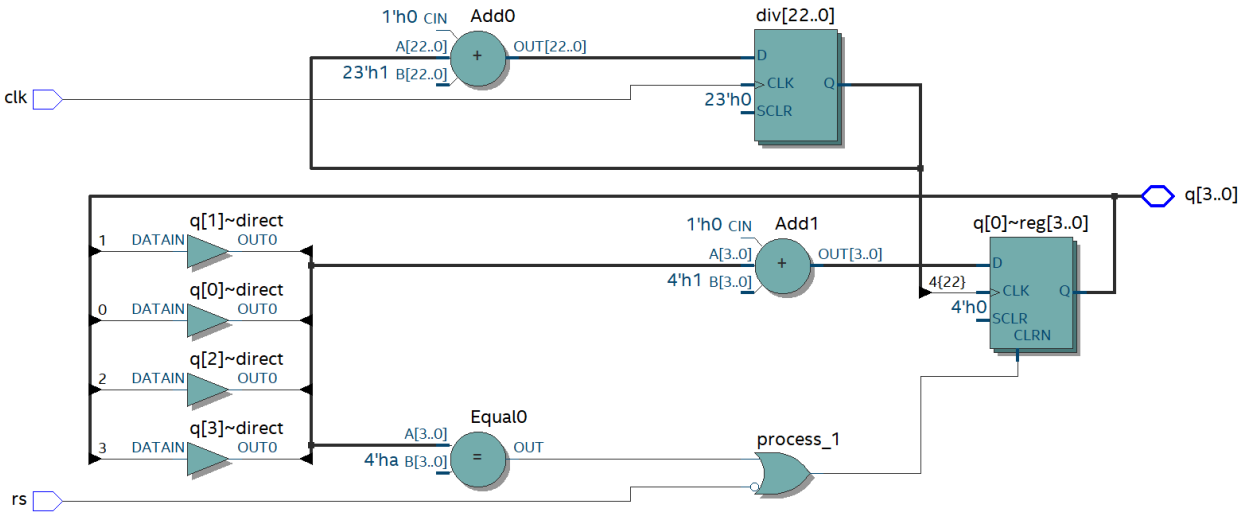
```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;
entity bcdupcount is
Port ( clk,rs : in  STD_LOGIC;
q : inout  STD_LOGIC_VECTOR (3 downto 0));
end bcdupcount;
architecture Behavioral of bcdupcount is
signal div:std_logic_vector(22 downto 0);
signal clkd:std_logic;
begin
process(clkd)
begin
if rising_edge(clk)then
div<= div+1;
end if;
end process;
clkd<=div(22);
process(clkd,rs)
begin
if rs='0' or q="1010" then
q<="0000";
```

```
elsif clkd'event and clkd='1' then
q<=q+1;
end if;
end process;
 q<=q;
 end Behavioral;
```

TRUTH TABLE OF BCD UP COUNTER:

Clock	QD	QC	QB	QA
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	0	0	0	0

NETLIST VIEWER:


1'h0 CIN
Add0
A[22..0]
23'h1 B[22..0]
+
OUT[22..0]
div[22..0]
D
CLK
Q
23'h0
SCLR
clk
q[3..0]
q[1]~direct
1
DATAIN
OUT0
q[0]~direct
0
q[2]~direct
2
q[3]~direct
3
1'h0 CIN
Add1
A[3..0]
4'h1 B[3..0]
OUT[3..0]
q[0]~reg[3..0]
4{22}
4'h0
CLRN
Equal0
4'ha B[3..0]
=
OUT
process_1
rs