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COURSE/YR: BSCpE – 3A  
SUBJECT: CPE 366 – INTRO TO HDL**

**T FLIP FLOP**

**12. VHDL CODE T FLIP FLOP:**

**library IEEE;**

**use IEEE.STD\_LOGIC\_1164.ALL;**

**use IEEE.STD\_LOGIC\_ARITH.ALL;**

**use IEEE.STD\_LOGIC\_UNSIGNED.ALL;**

**entity TFlipFlop is**

**Port (**

**t : in STD\_LOGIC;**

**clk : in STD\_LOGIC;**

**rst : in STD\_LOGIC;**

**q : inout STD\_LOGIC**

**);**

**end TFlipFlop;**

**architecture Behavioral of TFlipFlop is**

**signal div : std\_logic\_vector(22 downto 0);**

**signal clkd : std\_logic;**

**begin**

**-- Falling edge instead of rising edge**

**process(clk)**

**begin**

**if falling\_edge(clk) then**

**div <= div - 1; -- reverse addition**

**end if;**

**end process;**

**clkd <= not div(20); -- reverse signal logic**

**process(clkd, rst)**

**begin**

**if (rst = '0') then -- reverse active-high reset to active-low**

**q <= '1'; -- reverse reset value**

**elsif (clkd'event and clkd = '0' and t = '0') then -- reverse clock and T logic**

**q <= not q;**

**else**

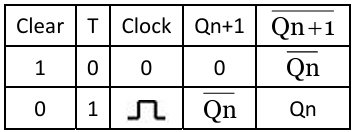
**q <= q;**

**end if;**

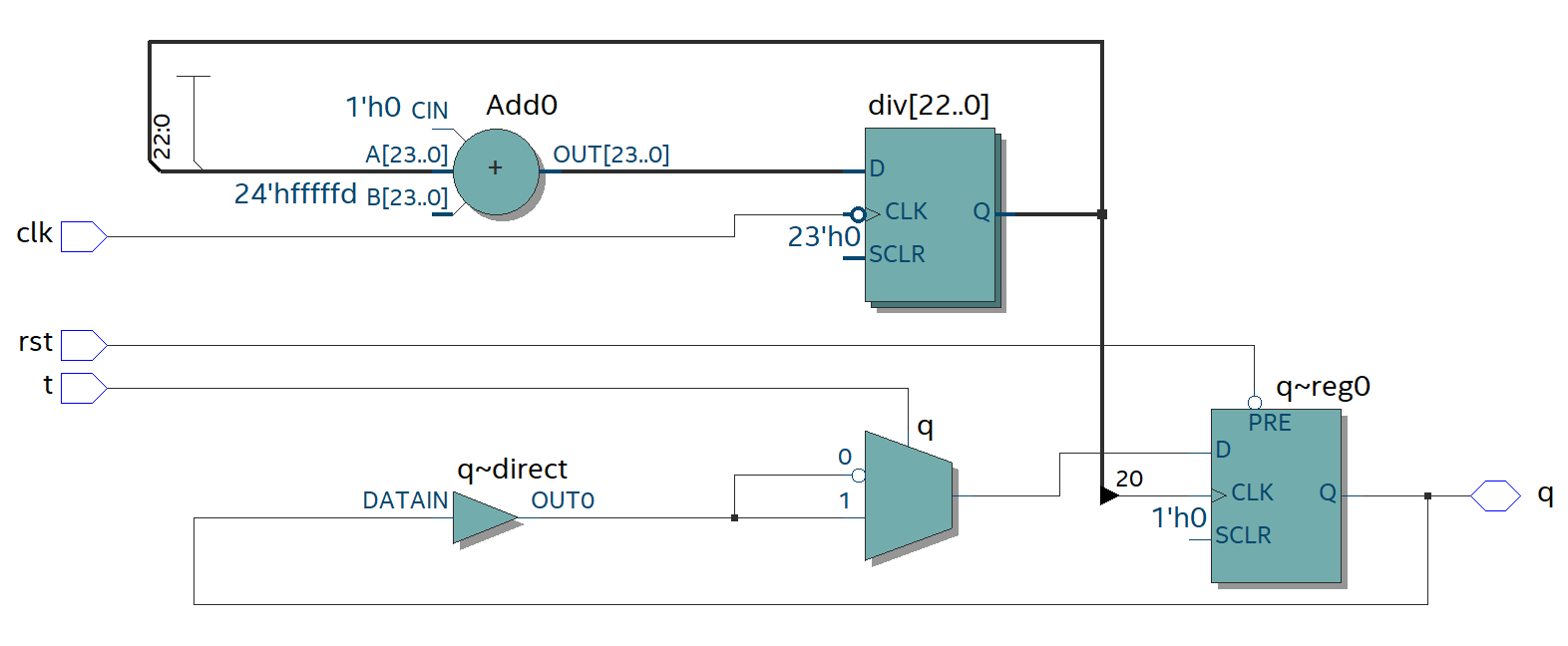
**end process;**

**end Behavioral;**

**TRUTH TABLE OF T FLIP FLOP:**

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**RTL VIEWER:**

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