Modern Scientific Computing

HW 1

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Due: Feb. 14

Answer 1:

Computing power of my computer is

$$2 \times 3.34 \times 16 = 106.88 \ \ GFLOPS$$

```
onworks@onworks-Standard-PC-i440FX-PIIX-1996:~/Desktop$ lsmem
RANGE                                  SIZE  STATE REMOVABLE BLOCK
0x0000000000000000-0x00000000bfffffff   3G online       yes  0-23
```

Fig1. lsmem

```
onworks@onworks-Standard-PC-i440FX-PIIX-1996:~/Desktop$ lscpu
Architecture:                    x86_64
CPU op-mode(s):                  32-bit, 64-bit
Byte Order:                      Little Endian
Address sizes:                   40 bits physical, 48 bits virtual
CPU(s):                          2
On-line CPU(s) list:             0,1
Thread(s) per core:              1
Core(s) per socket:              1
Socket(s):                       2
NUMA node(s):                    1
Vendor ID:                       GenuineIntel
CPU family:                      15
Model:                           6
Model name:                      Common KVM processor
Stepping:                        1
CPU MHz:                         3399.994
BogoMIPS:                        6799.98
Hypervisor vendor:               KVM
Virtualization type:             full
L1d cache:                       64 KiB
L1i cache:                       64 KiB
L2 cache:                        8 MiB
L3 cache:                        32 MiB
NUMA node0 CPU(s):               0,1
Vulnerability Itlb multihit:     KVM: Vulnerable
Vulnerability L1tf:              Mitigation; PTE Inversion
Vulnerability Mds:               Vulnerable: Clear CPU buffers attempted, no microcode; SMT Host state u
                                 nknown
Vulnerability Meltdown:          Mitigation; PTI
```

Fig2. lscpu

Answer 2:

The minimum latency time is

$$\frac{1\times10^{-2}\ m}{3\times10^{8}\ m/s}\approx0.333\ ns$$

The CPU clock time of my CPU is

$$\frac{1}{3399.994\ MHz}\approx0.294\ ns$$

These two times are the same order.

Answer 3:

Google Neural Network Processing Unit (NPU), Field-Programmable Gate Array (FPGA) and Tensor Processing Unit (TPU) are three of the most advanced and powerful hardware technologies available today. They are used to accelerate the processing of large amounts of data and enable the development of complex machine learning models.

The Google Neural Network Processing Unit (NPU) is a specialized processor designed to accelerate the processing of neural networks. It is based on a custom architecture that is optimized for deep learning applications. The NPU is capable of performing up to 10 times faster than traditional CPUs and GPUs, making it ideal for applications such as image recognition, natural language processing, and autonomous driving.

The Field-Programmable Gate Array (FPGA) is a type of integrated circuit that can be programmed to perform specific tasks. It is used to accelerate the processing of large amounts of data and enable the development of complex machine learning models. FPGAs are highly efficient and can be used to create custom hardware solutions for specific applications.

The Tensor Processing Unit (TPU) is a specialized processor designed to accelerate the processing of tensor operations. It is based on a custom architecture that is optimized for deep learning applications. The TPU is capable of performing up to 30 times faster than traditional CPUs and GPUs, making it ideal for applications such as image recognition, natural language processing, and autonomous driving.

In conclusion, Google Neural Network Processing Unit (NPU), Field-Programmable Gate Array (FPGA) and Tensor Processing Unit (TPU) are three of the most advanced and powerful hardware technologies available today. They are used to accelerate the processing of large amounts of data and enable the development of complex machine learning models. They are highly efficient and can be used to create custom hardware

solutions for specific applications.

Answer 4:

Associativity of addition: No

Existence of additive identity: Yes

Existence of additive inverses: No

Commutativity of multiplication: Yes

Associativity of multiplication: No

Existence of multiplicative identity: Yes

Existence of multiplicative inverses: No, all floating points number can be given by q/p, but p/q may not be given by floating point number.

Distributive law: No, multiple is not exact for floating point numbers.

Zero-one law: No