SEM/SET for COMP1047

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COMP1047 AY2023: Final Exam Review Guideline

- NO calculator is allowed.
- We will provide you the MIPS Ref Card appended at the end of the exam paper.
- Dictionary is permitted as per usual exam rules.

- The final exam covers the three (3) aspects that have been taught in the lecture and exercised in the labs:
  - Basic Concepts and MIPS programming
  - ISA and CPU Design
  - Computer Networking

Basic concepts and MIPS programming

- Chapter 1: Introduction
  - General concepts (no need to memorize exact numbers)
  - von Neumann architecture
- Chapter 2: Computer Performance
  - Timing – Response time, CPU Timing related, relative performance, CPI related
  - Other performance metrics – power/energy, reliability, etc.
- Chapter 3: Computer Arithmetic
  - Number formats – decimal, binary, hexadecimal, and their conversion.
  - Negative numbers – sign/magnitude, 2's complement and conversion, sign extension, overflow
  - Shift operations
  - Floating point representation – all except double precision standard
- Chapters 4 & 5: MIPS programming 1 & 2
  - All concepts: registers, memory (address, data, addressing, endianness), immediate, etc.
  - and related instructions: arithmetic, memory, logical, branch/jump, etc.
  - Floating point, multiplication, division instructions will not be covered.
  - Arrays and Procedures, but no recursive procedures.
  - Syscall will not be covered.

ISA and CPU design

- Chapter 6: MIPS ISA
  - R-, I-, J-types instructions – definitions, design, and conversion. MIPS ref card will be provided for assistance.
  - Content in the handout may be included, too.

- Chapter 7: ALU Design
  - All concepts including
    - Basic hardware principles and functionalities
      - Hardware details will not be covered, such as 1-bit adder logical expression, multi-bit adders design.
    - ALU design principle, schematic, and control
    - Add, Sub, And, Or, Slt, Nor, Nand, etc.

- Chapter 8: Single-Cycle CPU design
  - All concepts including
    - Drawing the datapaths for R-type, lw, sw, beq instructions.
    - You don’t need to know how the controller is designed, but need to know what are the corresponding control signals required to make the components work properly.

CPU design

Chapter 9: Pipelined CPU Design

- Describe the pipelined behavior for instruction execution:
  - At which cycle, which instruction is executing at which stage
  - At a certain stage, which component in CPU is functioning: reading/writing registers/memories, ALU calculation, etc.
- Comprehend all types of hazards, including RAW data hazard (both for R-type and lw instructions)
- Indicate the stalling and forwarding methods applied to mitigate the data hazard.
  - Draw arrows and bubbles on the pipeline, as in the lab questions
- Know that control hazard cannot be completely removed, but can use early branching for performance improvement.
- Calculate the CPI
  - The ideal CPI for pipelined processor is 1
  - The CPI for 'lw' is dependent on whether there is data hazard.
  - The CPI for branching is dependent on whether the branch is taken.
  - Calculate the average CPI for 'lw' and 'beq' considering hazard
  - Calculate the average CPI of the overall CPU given the percentage of each kind of instruction.
- Calculate the total execution time of the pipeline
  - For a piece of assembly code, calculate the total execution time w or w/o hazard
- May need to draw the Pipelined CPU design.