计算机体系结构 Homework 07

邱一航, Yihang Qiu, 2021/12/13-12/19

1. Solution:

1) The critical path for a LC3 ADD instruction is:

Fetch Instruction	Decode Instruction	Evaluate Address	Fetch Operands	Execution	Store Results
I-MEM	Registers			ALU	Registers
400ps	$200\text{ps} \times 2 = 400\text{ps}$	/	/	100ps	200ps

(Since need to fetch two operands from two registers)

Thus, the critical path is $400 + 400 + 100 + 200 = 1100\text{ps}$. ■

2) The new critical path for a LC3 ADD instruction is:

Fetch Instruction	Decode Instruction	Evaluate Address	Fetch Operands	Execution	Store Results
I-MEM	Registers			ALU	Registers
400ps	250ps	/	/	100ps	250ps

Thus, the new critical path is $400 + 250 + 100 + 250 = 1000\text{ps}$. ■

2. Solution:

1) The cycle time is $300 + 400 + 350 + 550 + 100 = 1700\text{ps}$.

The latency of an instruction is $300 + 400 + 350 + 550 + 100 = 1700\text{ps}$.

The throughput is $1/1700$. ■

2) The cycle time is $550 + 20 = 570\text{ps}$.

The latency of an instruction is $570 \times 4 + 100 + 20 = 2400\text{ps}$.

The throughput is $1/570$. ■

3) Choose the stage with maximal latency **i.e. <u>the Memory stage</u>** to be split to 2 equal halves.

The new cycle time is $400 + 20 = 420\text{ps}$.

The new latency of an instruction is $420 \times 5 + 100 + 20 = 2200\text{ps}$.

The new throughput is $1/420$. ■

4) By the assumption, there are no stalls or hazards.

The utilization of (*)	ALU Instruction	BR Instruction	LOAD Instruction	STORE Instruction
Data Memory	0%	20%	20%	20%
Register's Write Port	20%	0%	20%	0%

Thus, the utilization of the data memory is $20\% \times 25\% + 20\% \times 15\% + 20\% \times 10\% = 10\%$ while the utilization of the data memory is $20\% \times 50\% + 0\% + 20\% \times 15\% + 0\% = 13\%$. ■

3. Solution:

1) The ideal condition is that each stage takes exactly the same time and the CPI is 1.

Thus, the best speedup is 5 since there are 5 stages. ■

2) In this case, the clock cycle should be 4ns, **i.e.** the maximal execution time among the 5 stages.

The average execution time of instructions is 4ns.

Thus, the speedup is $10/4 = 2.5$. ■

3) The ideal condition is that each stage takes exactly the same time, **i.e.** $2\text{ns} + 20\text{ps} = 2.02\text{ns}$.

Thus, the speedup is $10/2.02 = 4.95$. ■

4) In this case, the new CPI should be

$$\frac{6}{5} \times 20\% + \frac{7}{5} \times 5\% + 1 \times 75\% = 1.06.$$

The average execution time of instructions is

$$2.02\text{ns} \times 75\% + \frac{6}{5} \times 2.02\text{ns} \times 20\% + \frac{7}{5} \times 2.02\text{ns} \times 5\% = 2.14\text{ns}$$

Thus, the speedup is $10/2.14 = 4.67$. ■

4. Solution:

1) 102 depends on 101. 104 depends on 103.

2) The execution is as follows.

	0	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**
100	IF_{100}	ID_{100}	EX_{100}	MA_{100}	WB_{100}					
101		IF_{101}	ID_{101}	EX_{101}	MA_{101}	WB_{101}				
102			IF_{102}	ID_{102}	ID_{102}	ID_{102}	ID_{102}	EX_{102}	MA_{102}	WB_{102}
103				IF_{103}	IF_{103}	IF_{103}	IF_{103}	ID_{103}	EX_{103}	MA_{103}
104								IF_{104}	ID_{104}	ID_{104}
105									IF_{105}	IF_{105}
	10	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**
100										
101										
102										

103	WB_{103}									
104	ID_{104}	ID_{104}	EX_{104}	MA_{104}						
105	IF_{105}	IF_{105}	ID_{105}	EX_{105}	MA_{105}	WB_{105}				

From the analyses above, we know there are **2 stalls** with length of **3 and 3** respectively. ■

The total execution time is **16 cycles**. ■

3) After implementing full bypassing/forwarding, the execution is as follows.

	0	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**
100	IF_{100}	ID_{100}	EX_{100}	MA_{100}	WB_{100}						
101		IF_{101}	ID_{101}	EX_{101}	MA_{101}	WB_{101}					
102			IF_{102}	ID_{102}	ID_{102}	EX_{102}	MA_{102}	WB_{102}			
103				IF_{103}	IF_{103}	ID_{103}	EX_{103}	MA_{103}	WB_{103}		
104						IF_{104}	ID_{104}	EX_{104}	MA_{104}	WB_{104}	
105							IF_{105}	ID_{105}	EX_{105}	MA_{105}	WB_{105}

From the analyses above, we know there are still **1 stall**.

Rewrite the program to eliminate the hazards. The program after rewriting is as follows.

```
100 LDR R2, R1, #0
101 LDR R1, R3, #4
102 NOP
103 ADD R3, R1, R2
104 ADD R3, R2, R2
105 OR R4, R3, #0
106 STR R3, R1, #5
```
■

5. Solution:

1) The total execution time is 14ms.

After improving the execution time of some routines, the maximal routine time is still 14ms.

Thus, the total time reduced is 0. ■

2) The maximal routine time is $(1 - 10\%) \times 14 = 12.6\text{ms}$.

The total time reduced is $14 - 12.6 = 1.4\text{ms}$, **i.e.** by **10%**. ■

2) The maximal routine time is still 12.6ms.

Thus, the total time reduced is 0, **i.e.** by **0%**. ■

6. Solution:

1) $InstructionsPerSecond = \frac{1}{ExecutionTimeperInstruction} = \frac{1}{CPI} \times \frac{1}{CycleTime}$

$$= \frac{1}{CPI} \times ClockRate$$

P1: $3.0GHz/1.5 = 2.0 \times 10^9$

P2: $2.5GHz/1.0 = 2.5 \times 10^9$

P3: $4.0GHz/2.2 = 1.8 \times 10^9$

Thus, **P2** has the highest performance expressed in instructions per second. ■

2) P1: 3.0×10^9 Cycles, 2.0×10^9 instructions

P2: 2.5×10^9 Cycles, 2.5×10^9 instructions

P3: 4.0×10^9 Cycles, 1.8×10^9 instructions ■

3) $ClockRate \times (1 + 0.2) = NewClockRate \times (1 - 0.3)$

Thus, P1: $5.14GHz$, P2: $4.29GHz$, P3: $6.86GHz$. ■