计算机体系结构 Exercise 02

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3.5. Solution:

The truth table is as follows.

A	B	C	OUT
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	0

3.7. Solution:

When $A = 1, B = 0$, the high voltage is directly linked to low voltage and the voltage of OUT is ambiguous. The ambiguity of OUT under this circumstance is a fatal error.

3.21. Solution: There are 2^{14}=16384 units. Thus, memory contains 16384 Bytes = 32768 Nibbles.

3.24. Solution:

a) X acts as a control that decides whether B or C is the operand. When $X = 0$, the result is $A + B$; when $X = 1$, the result is $A + C$.

b) Let $C = \bar{B}$. Also, let X be the carry-in of the 0-th adder (shown in the following figure).

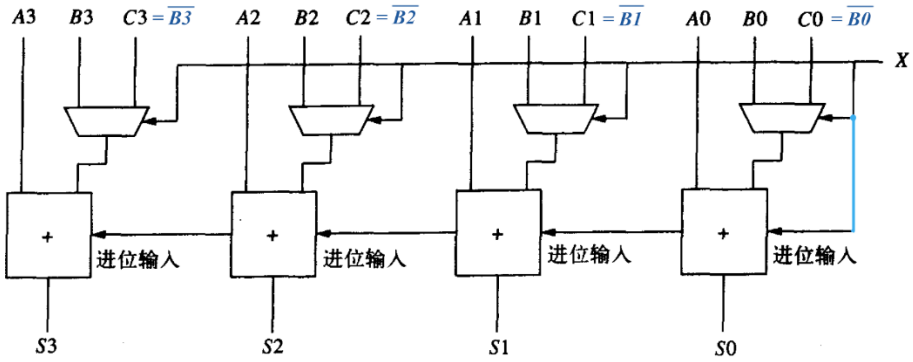
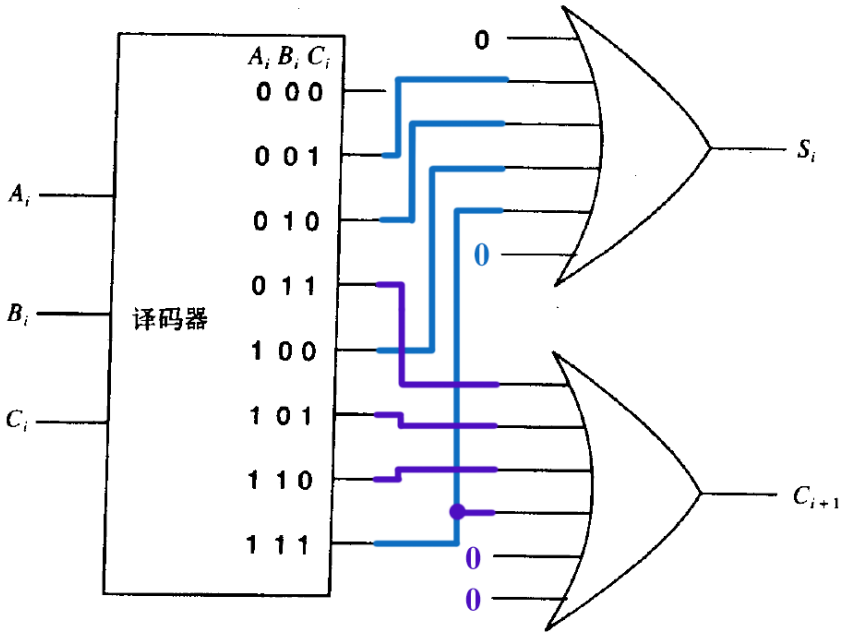


图3-39 结构框图

When $X = 0$, the circuit in the figure above acts as an adder.

When $X = 1$, the circuit acts as subtracter.

3.26. Solution:

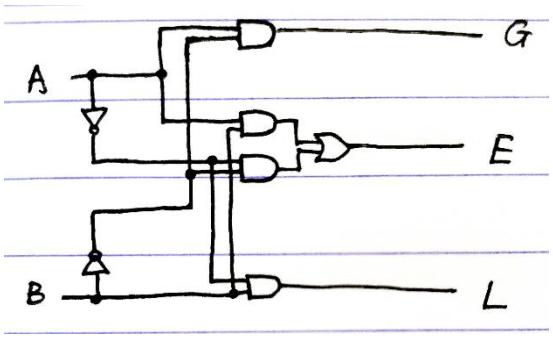


3.30. Solution:

a) The truth table is as follows.

A	B	G	E	L
0	0	0	1	0
0	1	0	0	1
1	0	1	0	0
1	1	0	1	0

b)



c)

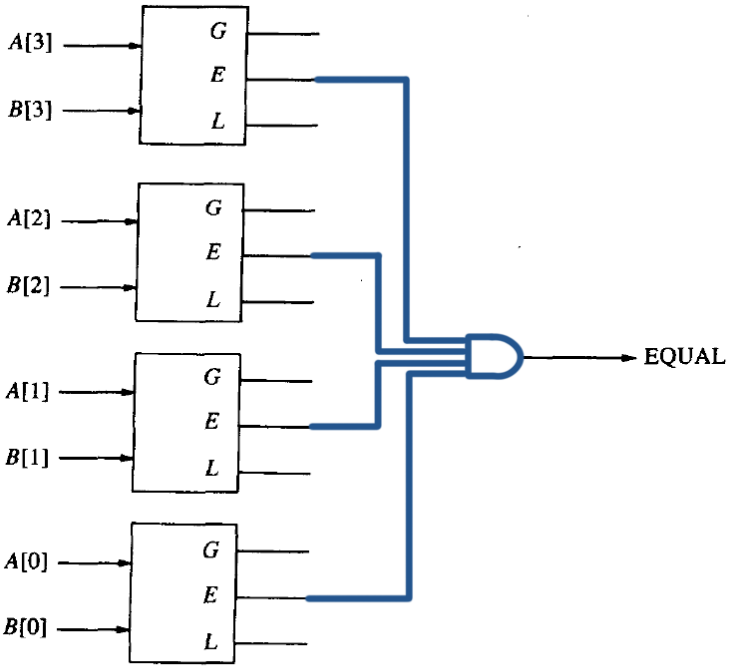


图3-41　习题3.30的结构框图

4.5 Solution:

a) 地址 3 存放的数值是 0000 0000 0000 0000；地址 6 存放的数值是 1111 1110 1101 0011。

b) (1) 地址 0 对应的补码数：$(0001\ 1110\ 0100\ 0011)_2 = 7747$；

地址 1 对应的补码数：$(1111\ 0000\ 0010\ 0101)_2 = -4059$

(2) 地址 4 对应的数值为$(0000\ 0000\ 0110\ 0101)_2 = (101)_{10}$。ASCII 码 101 对应的字符为 e。

(3) 地址 6 和 7 对应的二进制数值为 1 111 1110 1 101 0011 0000 0110 1101 1001，IEEE 标准下指数部分为+126，尾数为$(0.10100110000011011011001)_2 = (0.6486464739)_{10}$，故对应的浮点数为 $-1.6486464739 \times 10^{126}$。

(4) 地址 0 对应的无符号数：7747，地址 1 对应的无符号数为 61477。

c) 地址 0 对应的数值为 0001 111 001 000 011，对应的 LC3 标准下指令为 **R7←R1+R3**。

d) 地址 5 保存的数值为 0110，即指向的单元地址是 **6**。

该地址中存放的数值为 **1111 1110 1101 0011**。

4.7 Solution:

Since there exist 60 opcodes, we need at least 6 bits to represent these opcodes (since $2^6 = 64 > 60$).

Since there exist 32 registers, we need at least 5 bits and 5 bits to represent SR and DR respectively (since $2^5 = 32$).

Thus, in a 32-bit instruction, there are at most $32 - 6 - 5 - 5 = 16$ bits to represent immediate number.

Since the immediate number is represented as 2's complement, $-2^{16} \leq \text{IMM} \leq 2^{16} - 1$, **i.e.** the range of the immediate number is $-2^{16} \sim 2^{16} - 1$.

4.13 Solution:

1) For Intel x86 instruction "ADD [eax], edx":

FETCH – 1, DECODE – 1; EVALUATE ADDRESS – 1; FETCH OPERAND – 100; EXECUTE – 1; STORE RESULT – 100. Thus, it takes **204 periods** in total.

2) For LC-3 instruction "ADD R6,R2,R6":

FETCH – 1, DECODE – 1; FETCH OPERAND (from register files) – 1; EXECUTE – 1; STORE RESULT (into register files) – 1. Thus, it takes **5 periods** in total.