
STM32
CubeMX

1. Description

1.1. Project

Project Name	GRA_10
Board Name	custom
Generated with:	STM32CubeMX 6.0.1
Date	11/12/2020

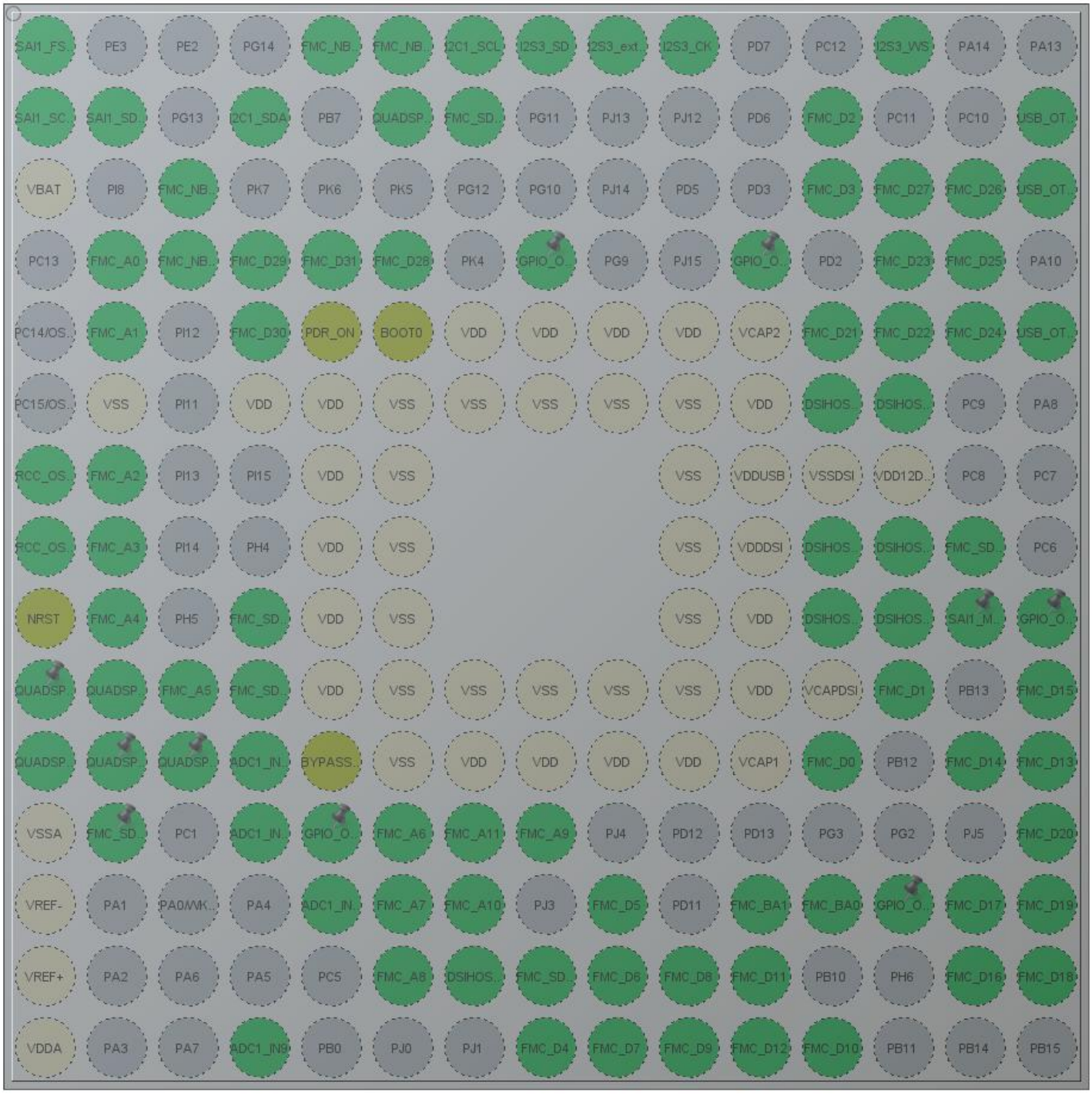
1.2. MCU

MCU Series	STM32F4
MCU Line	STM32F469/479
MCU name	STM32F469NIHx
MCU Package	TFBGA216
MCU Pin number	216

1.3. Core(s) information

Core(s)	Arm Cortex-M4

2. Pinout Configuration



TFBGA216 (Top view)

3. Pins Configuration

Pin Number TFBGA216	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
A1	PE4	I/O	SAI1_FS_A	
A5	PE1	I/O	FMC_NBL1	
A6	PE0	I/O	FMC_NBL0	
A7	PB8	I/O	I2C1_SCL	
A8	PB5	I/O	I2S3_SD	
A9	PB4	I/O	I2S3_ext_SD	
A10	PB3	I/O	I2S3_CK	
A13	PA15	I/O	I2S3_WS	
B1	PE5	I/O	SAI1_SCK_A	
B2	PE6	I/O	SAI1_SD_A	
B4	PB9	I/O	I2C1_SDA	
B6	PB6	I/O	QUADSPI_BK1_NCS	
B7	PG15	I/O	FMC_SDNCAS	
B12	PD0	I/O	FMC_D2	
B15	PA12	I/O	USB_OTG_FS_DP	
C1	VBAT	Power		
C3	PI4	I/O	FMC_NBL2	
C12	PD1	I/O	FMC_D3	
C13	PI3	I/O	FMC_D27	
C14	PI2	I/O	FMC_D26	
C15	PA11	I/O	USB_OTG_FS_DM	
D2	PF0	I/O	FMC_A0	
D3	PI5	I/O	FMC_NBL3	
D4	PI7	I/O	FMC_D29	
D5	PI10	I/O	FMC_D31	
D6	PI6	I/O	FMC_D28	
D8	PK3 *	I/O	GPIO_Output	
D11	PD4 *	I/O	GPIO_Output	
D13	PH15	I/O	FMC_D23	
D14	PI1	I/O	FMC_D25	
E2	PF1	I/O	FMC_A1	
E4	PI9	I/O	FMC_D30	
E5	PDR_ON	Reset		
E6	BOOT0	Boot		
E7	VDD	Power		
E8	VDD	Power		

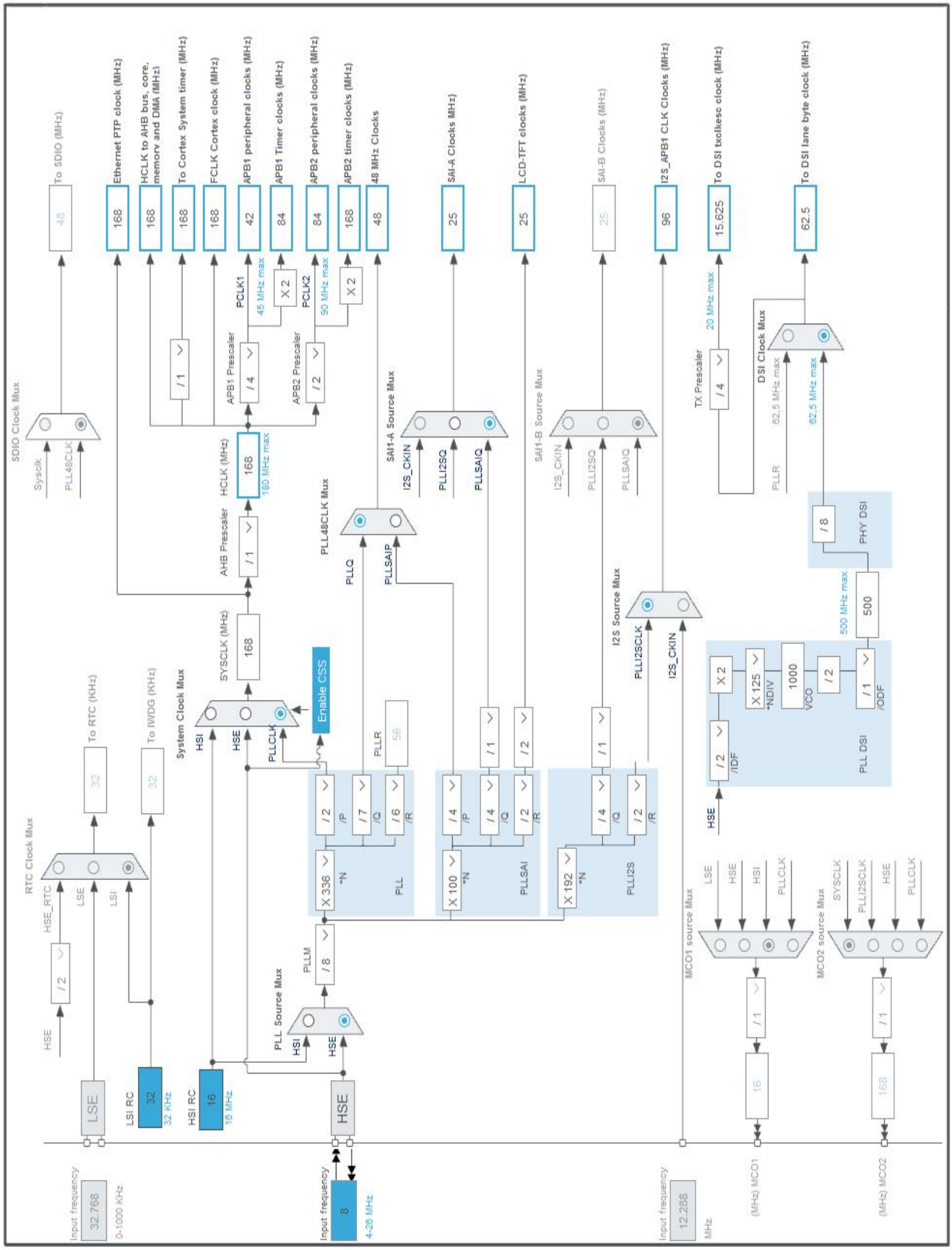
Pin Number TFBGA216	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
E9	VDD	Power		
E10	VDD	Power		
E11	VCAP2	Power		
E12	PH13	I/O	FMC_D21	
E13	PH14	I/O	FMC_D22	
E14	PI0	I/O	FMC_D24	
E15	PA9	I/O	USB_OTG_FS_VBUS	
F2	VSS	Power		
F4	VDD	Power		
F5	VDD	Power		
F6	VSS	Power		
F7	VSS	Power		
F8	VSS	Power		
F9	VSS	Power		
F10	VSS	Power		
F11	VDD	Power		
F12	DSIHOST_D1P	MonoIO	DSIHOST_D1P	
F13	DSIHOST_D1N	MonoIO	DSIHOST_D1N	
G1	PH0/OSC_IN	I/O	RCC_OSC_IN	
G2	PF2	I/O	FMC_A2	
G5	VDD	Power		
G6	VSS	Power		
G10	VSS	Power		
G11	VDDUSB	Power		
G12	VSSDSI	Power		
G13	VDD12DSI	Power		
H1	PH1/OSC_OUT	I/O	RCC_OSC_OUT	
H2	PF3	I/O	FMC_A3	
H5	VDD	Power		
H6	VSS	Power		
H10	VSS	Power		
H11	VDDDSI	Power		
H12	DSIHOST_CKP	MonoIO	DSIHOST_CKP	
H13	DSIHOST_CKN	MonoIO	DSIHOST_CKN	
H14	PG8	I/O	FMC_SDCLK	
J1	NRST	Reset		
J2	PF4	I/O	FMC_A4	
J4	PH3	I/O	FMC_SDNE0	
J5	VDD	Power		

Pin Number TFBGA216	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
J6	VSS	Power		
J10	VSS	Power		
J11	VDD	Power		
J12	DSIHOST_D0P	MonoIO	DSIHOST_D0P	
J13	DSIHOST_D0N	MonoIO	DSIHOST_D0N	
J14	PG7	I/O	SAI1_MCLK_A	
J15	PG6 *	I/O	GPIO_Output	
K1	PF7	I/O	QUADSPI_BK1_IO2	
K2	PF6	I/O	QUADSPI_BK1_IO3	
K3	PF5	I/O	FMC_A5	
K4	PH2	I/O	FMC_SDCKE0	
K5	VDD	Power		
K6	VSS	Power		
K7	VSS	Power		
K8	VSS	Power		
K9	VSS	Power		
K10	VSS	Power		
K11	VDD	Power		
K12	VCAPDSI	Power		
K13	PD15	I/O	FMC_D1	
K15	PD10	I/O	FMC_D15	
L1	PF10	I/O	QUADSPI_CLK	
L2	PF9	I/O	QUADSPI_BK1_IO1	
L3	PF8	I/O	QUADSPI_BK1_IO0	
L4	PC3	I/O	ADC1_IN13	
L5	BYPASS_REG	Reset		
L6	VSS	Power		
L7	VDD	Power		
L8	VDD	Power		
L9	VDD	Power		
L10	VDD	Power		
L11	VCAP1	Power		
L12	PD14	I/O	FMC_D0	
L14	PD9	I/O	FMC_D14	
L15	PD8	I/O	FMC_D13	
M1	VSSA	Power		
M2	PC0	I/O	FMC_SDNWE	
M4	PC2	I/O	ADC1_IN12	
M5	PB2/BOOT1 *	I/O	GPIO_Output	

Pin Number TFBGA216	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
M6	PF12	I/O	FMC_A6	
M7	PG1	I/O	FMC_A11	
M8	PF15	I/O	FMC_A9	
M15	PH12	I/O	FMC_D20	
N1	VREF-	Power		
N5	PC4	I/O	ADC1_IN14	
N6	PF13	I/O	FMC_A7	
N7	PG0	I/O	FMC_A10	
N9	PE8	I/O	FMC_D5	
N11	PG5	I/O	FMC_BA1	
N12	PG4	I/O	FMC_BA0	
N13	PH7 *	I/O	GPIO_Output	
N14	PH9	I/O	FMC_D17	
N15	PH11	I/O	FMC_D19	
P1	VREF+	Power		
P6	PF14	I/O	FMC_A8	
P7	PJ2	I/O	DSIHOST_TE	
P8	PF11	I/O	FMC_SDNRAS	
P9	PE9	I/O	FMC_D6	
P10	PE11	I/O	FMC_D8	
P11	PE14	I/O	FMC_D11	
P14	PH8	I/O	FMC_D16	
P15	PH10	I/O	FMC_D18	
R1	VDDA	Power		
R4	PB1	I/O	ADC1_IN9	
R8	PE7	I/O	FMC_D4	
R9	PE10	I/O	FMC_D7	
R10	PE12	I/O	FMC_D9	
R11	PE15	I/O	FMC_D12	
R12	PE13	I/O	FMC_D10	

* The pin is affected with an I/O function

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	GRA_10
Project Folder	C:\TouchGFXProjects\MyApplication
Toolchain / IDE	STM32CubeIDE
Firmware Package Name and Version	STM32Cube FW_F4 V1.25.2
Application Structure	Advanced
Generate Under Root	No
Do not generate the main()	No
Minimum Heap Size	0x1000
Minimum Stack Size	0x1000

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No
Enable Full Assert	No

5.3. Advanced Settings - Generated Function Calls

Rank	Function Name	IP Instance Name
1	MX_GPIO_Init	GPIO
2	MX_DMA_Init	DMA
3	SystemClock_Config	RCC
4	MX_CRC_Init	CRC
5	MX_DMA2D_Init	DMA2D
6	MX_DSIHOST_DSI_Init	DSIHOST
7	MX_FMC_Init	FMC
8	MX_LTDC_Init	LTDC
9	MX_QUADSPI_Init	QUADSPI
10	MX_I2C1_Init	I2C1
11	MX_ADC1_Init	ADC1

Rank	Function Name	IP Instance Name
12	MX_TIM2_Init	TIM2
13	MX_RNG_Init	RNG
14	MX_FATFS_Init	FATFS
15	MX_USB_HOST_Init	USB_HOST
16	MX_PDM2PCM_Init	PDM2PCM
17	MX_I2S3_Init	I2S3
18	MX_SAI1_Init	SAI1
19	MX_TouchGFX_Init	STMicroelectronics.X-CUBE-TOUCHGFX.4.15.0
20	MX_TouchGFX_Process	STMicroelectronics.X-CUBE-TOUCHGFX.4.15.0

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32F4
Line	STM32F469/479
MCU	STM32F469NIHx
Datasheet	DS11189_Rev4

6.2. Parameter Selection

Temperature	25
Vdd	3.3

6.3. Battery Selection

Battery	Li-SOCL2(A3400)
Capacity	3400.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	100.0 mA
Max Pulse Current	200.0 mA
Cells in series	1
Cells in parallel	1

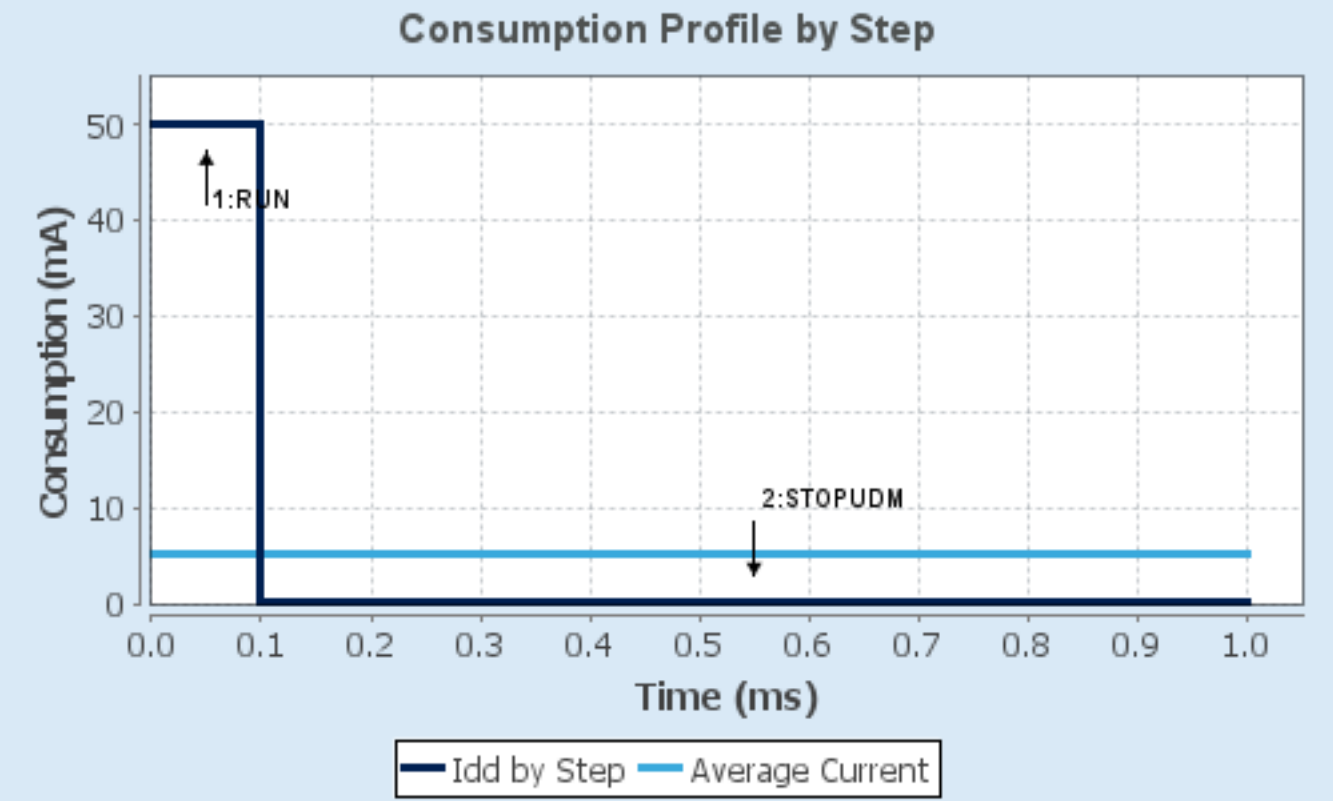
6.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP_UDM (Under Drive)
Vdd	3.3	3.3
Voltage Source	Battery	Battery
Range	Scale1-High	No Scale
Fetch Type	RAM/FLASH/ART/REGON	n/a
CPU Frequency	180 MHz	0 Hz
Clock Configuration	HSE PLL	Regulator_LP Flash-PwrDwn
Clock Source Frequency	4 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	50 mA	140 µA
Duration	0.1 ms	0.9 ms
DMIPS	225.0	0.0
Ta Max	100.21	104.99
Category	In DS Table	In DS Table

6.5. Results

Sequence Time	1 ms	Average Current	5.13 mA
Battery Life	27 days, 14 hours	Average DMIPS	225.0 DMIPS

6.6. Chart


Consumption Profile by Step
Consumption (mA)
50
40
30
20
10
0
1:RUN
2:STOPUDM
0.0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1.0
Time (ms)
Idd by Step
Average Current

7. IPs and Middleware Configuration

7.1. ADC1

mode: IN9

mode: IN12

mode: IN13

mode: IN14

7.1.1. Parameter Settings:

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Clock Prescaler	**PCLK2 divided by 8 ***
Resolution	**10 bits (13 ADC Clock cycles) ***
Data Alignment	Right alignment
Scan Conversion Mode	Enabled
Continuous Conversion Mode	**Enabled ***
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	Disabled
End Of Conversion Selection	**EOC flag at the end of all conversions ***

ADC_Regular_ConversionMode:

Number Of Conversion	**4 ***
External Trigger Conversion Source	Regular Conversion launched by software
External Trigger Conversion Edge	None
Rank	1
Channel	**Channel 12 ***
Sampling Time	**480 Cycles ***
Rank	**2 ***
Channel	**Channel 13 ***
Sampling Time	**480 Cycles ***
Rank	**3 ***
Channel	**Channel 14 ***
Sampling Time	**480 Cycles ***
Rank	**4 ***
Channel	Channel 9
Sampling Time	**480 Cycles ***

ADC_Injected_ConversionMode:

Number Of Conversions	0

WatchDog:

Enable Analog WatchDog Mode	false

7.2. CRC

mode: Activated

7.3. DMA2D

mode: Activated

7.3.1. Parameter Settings:

Basic Parameters:

Transfer Mode	Memory to Memory
Color Mode	ARGB8888
Output Offset	0
DMA2D Bytes Swap	Bytes in regular order in output FIFO
DMA2D Line Offset Mode	Line offsets expressed in pixels

Foreground layer Configuration:

DMA2D Input Color Mode	ARGB8888
DMA2D ALPHA MODE	No modification of the alpha channel value
Input Alpha	0
Input Offset	0

7.4. DSIHOST

DSIHost: Adapted Command Mode with TE Pin

7.4.1. DSI Clocks:

from PLLDSI:

Pllndiv	125
Pllodf	DSI_PLL_OUT_DIV1
Pllidf	DSI_PLL_IN_DIV2
High Speed Clock - PLLDSI Output	500000
Lane Byte Clock	62500
Tx Escape Ckdiv	4
Transmission Escape Clock	15625
Time Out Clock	62500

from PLLR:

Lane Byte Clock	56000

Transmission Escape Clock	14000
Time Out Clock	56000

7.4.2. Timeout Counters:

Time Out Clock Setting:

Time Out Clock Divider	1
Time Out Clock - from PLLDSI	62500

Contention Error Detection:

High-speed transmission time-out	0
No High-speed transmission time-out	
Low-power reception time-out	0
No Low-power reception time-out	

Peripheral Response:

High-speed read time-out	0
Resulting Timing High-speed read time-out	0
Low-power read time-out	0
Resulting Timing Low-power read time-out	0
High-speed write time-out	0
Resulting Timing High-speed write time-out	0
Low-power write time-out	0
Resulting Timing Low-power write time-out	0
BTA time-out	0
Resulting Timing for BTA time-out	0
High-speed write presp mode	Normal Behavior

7.4.3. Data and Clock Lanes:

Basic Settings:

Number of Lanes	**Two Data Lanes ***
Automatic Clock Lane Control	Clock lane is always provided
Bus Turn Around Request is	Enabled

Flow Control - Configuration:

CRC Reception	Disabled
ECC Reception	Disabled
EoTP Reception is	Disabled
EoTP Transmission is	Disabled
Acknowledge Request after Each Transmission	**Enabled ***
Tearing Effect Acknowledge Request Enable	**Enabled ***

Flow Control - Packet Analyzer Configuration:

CRC Error Interrupt	Disable
ECC Errors Interrupt	Disable
EoTP Error Interrupt	Disable
Packet Size Error Interrupt	Disable
Acknowledge Errors Interrupt	Disable
PHY related Errors Interrupt	Disable

7.4.4. PHY Timings:

LP to HS and HS to LP Transitions Timings:

Minimum wait period to request a HS transmission after the Stop state (min is 1 cycle of escape clock)	0
Resulting Minimum wait period to request a HS transmission after the Stop state (min is 1 cycle of escape clock)	0

7.4.5. Commands:

APB Interface Error Configuration:

Generic Command Error Interrupt	Disable

Transmission Mode for Commands::

Generic Short Write Zero Parameter	**Low Power Transmission ***
Generic Short Write One Parameter	**Low Power Transmission ***
Generic Short Write Two parameters	**Low Power Transmission ***
Generic Short Read Zero parameter	**Low Power Transmission ***
Generic Short Read One parameter	**Low Power Transmission ***
Generic Short Read Two parameters	**Low Power Transmission ***
Generic Long Write	**Low Power Transmission ***
DCS Short Write Zero parameter	**Low Power Transmission ***
DCS Short Write One parameter	**Low Power Transmission ***
DCS Short Read Zero parameter	**Low Power Transmission ***
DCS Long Write	**Low Power Transmission ***
Maximum Read Packet Size Command	**Low Power Transmission ***

7.4.6. Display Interface:

Basic Settings:

Display ID	0
Color Coding	RGB888 (24 bits) - DSI mode

Specific Command Mode Settings:

Maximum Command Size	448
The Refresh of the Display Frame Buffer is Triggered	**manually by Enabling the LTDC ***
Tearing Effect Source	External Source
Polarity of the External Tearing Effect Source	Rising Edge

7.4.7. LTDC Interface:

Clocking:

LTDC Pixel Clock (from Clock tree)	25

Frame Vertical Timings:

VSA: Vertical Synchronism Active duration (set in LTDC)	2
VBP: Vertical Back-Porch duration (set in LTDC)	1
VFP: Vertical Front-Porch duration (set in LTDC)	1
VACT: Vertical Active duration (set in LTDC)	480

Frame Horizontal Timings:

HSA: Horizontal Synchronism Active duration (set in LTDC)	2
HBP: Horizontal Back-Porch duration (set in LTDC)	1
HACT: Horizontal Active duration (set in LTDC)	448
HLINE: Horizontal Line duration (set in LTDC)	452

Polarity of the Control Signals:

VSYNC Polarity (set in LTDC)	DSI_VSYNC_ACTIVE_LOW
HSYNC Polarity (set in LTDC)	DSI_HSYNC_ACTIVE_LOW
Data Enable Polarity (set in LTDC)	DSI_DATA_ENABLE_ACTIVE_HIGH

Interface:

The DSI is halting the LTDC synchronously	On a Falling Edge of VSYNC

Interface Error Configuration:

LTDC FIFO Overflow Error Interrupt is	Disabled

7.5. FMC

SDRAM 1

Clock and chip enable: SDCKE0+SDNE0

Internal bank number: 4 banks

Address: 12 bits

Data: 32 bits

Byte enable: 32-bit byte enable

7.5.1. SDRAM 1:

SDRAM control:

Bank	SDRAM bank 1
Number of column address bits	8 bits
Number of row address bits	12 bits
CAS latency	**3 memory clock cycles ***
Write protection	Disabled
SDRAM common clock	Disabled
SDRAM common burst read	**Enabled ***
SDRAM common read pipe delay	**2 HCLK clock cycles ***

SDRAM timing in memory clock cycles:

Load mode register to active delay	**2 ***
Exit self-refresh delay	**7 ***
Self-refresh time	**4 ***
SDRAM common row cycle delay	**7 ***
Write recovery time	**3 ***
SDRAM common row precharge delay	**2 ***
Row to column delay	**2 ***

7.6. GPIO

7.7. I2C1

I2C: I2C

7.7.1. Parameter Settings:

Master Features:

I2C Speed Mode	**Fast Mode ***
I2C Clock Speed (Hz)	400000
Fast Mode Duty Cycle	Duty cycle Tlow/Thigh = 2

Slave Features:

Clock No Stretch Mode	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0
General Call address detection	Disabled

7.8. I2S3

Mode: Full-Duplex Master

7.8.1. Parameter Settings:

Generic Parameters:

Transmission Mode	Mode Master Transmit
Communication Standard	I2S Philips
Data and Frame Format	16 Bits Data on 16 Bits Frame
Selected Audio Frequency	8 KHz
Real Audio Frequency	**8.0 KHz ***
Error between Selected and Real	**0.0 % ***

Clock Parameters:

Clock Source	I2S PLL Clock
Clock Polarity	Low

7.9. LTDC

Display Type: RGB888 (24 bits) - DSI mode

7.9.1. Parameter Settings:

Synchronization for Width:

Horizontal Synchronization Width	**2 ***
Horizontal Back Porch	**1 ***
Active Width	**448 ***
Horizontal Front Porch	**1 ***
HSync Width	1
Accumulated Horizontal Back Porch Width	2
Accumulated Active Width	450
Total Width	451

Synchronization for Height:

Vertical Synchronization Height	**2 ***
Vertical Back Porch	**1 ***
Active Height	480
Vertical Front Porch	**1 ***
VSync Height	1
Accumulated Vertical Back Porch Height	2

Accumulated Active Height	482
Total Height	483

Signal Polarity:

Horizontal Synchronization Polarity	Active Low
Vertical Synchronization Polarity	Active Low
Not Data Enable Polarity	Active Low
Pixel Clock Polarity	Normal Input

BackGround Color:

Red	0
Green	0
Blue	0

7.9.2. Layer Settings:

BackGround Color:

Layer 0 - Blue	0
Layer 0 - Green	0
Layer 0 - Red	0

Number of Layers:

Number of Layers	**1 layer ***

Windows Position:

Layer 0 - Window Horizontal Start	0
Layer 0 - Window Horizontal Stop	**448 ***
Layer 0 - Window Vertical Start	0
Layer 0 - Window Vertical Stop	**480 ***

Pixel Parameters:

Layer 0 - Pixel Format	**RGB888 ***

Blending:

Layer 0 - Alpha constant for blending	**255 ***
Layer 0 - Default Alpha value	0
Layer 0 - Blending Factor1	Alpha constant
Layer 0 - Blending Factor2	Alpha constant

Frame Buffer:

Layer 0 - Color Frame Buffer Start Adress	**0xC0000000 ***
Layer 0 - Color Frame Buffer Line Length (Image Width)	**448 ***
Layer 0 - Color Frame Buffer Number of Lines (Image Height)	**480 ***

7.10. QUADSPI

QuadSPI Mode: Bank1 with Quad SPI Lines

7.10.1. Parameter Settings:

General Parameters:

Clock Prescaler	**1 ***
Fifo Threshold	1
Sample Shifting	**Sample Shifting Half Cycle ***
Flash Size	**27 ***
Chip Select High Time	**5 Cycles ***
Clock Mode	Low
Flash ID	Flash ID 1
Dual Flash	Disabled

7.11. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

7.11.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Instruction Cache	Enabled
Prefetch Buffer	Enabled
Data Cache	Enabled
Flash Latency(WS)	5 WS (6 CPU cycle)

RCC Parameters:

HSI Calibration Value	16
TIM Prescaler Selection	Disabled
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000

Power Parameters:

Power Regulator Voltage Scale	Power Regulator Voltage Scale 1
Power Over Drive	Disabled

7.12. RNG

mode: Activated

7.13. SAI1

Mode: Master with Master Clock Out

mode: I2S/PCM Protocol

7.13.1. Parameter Settings:

SAI A:

Synchronization Inputs	Asynchronous
Basic Parameters	
Audio Mode	Master Transmit
Output Mode	Stereo
Companding Mode	No companding mode
SAI SD Line Output Mode	Driven
Protocol Parameters	
Protocol	**I2S PCM (Pulse Code modulation) Standard ***
Data Size	16 Bits
Number of Slots	1
Clock Parameters	
Clock Source	SAI PLL Clock
Master Clock Divider	Enabled
Audio Frequency	192 KHz
Real Audio Frequency	**97.656 KHz ***
Error between Selected	**-49.13 % ***
Advanced Parameters	
Fifo Threshold	Empty
Output Drive	Disabled

7.14. SYS

Timebase Source: TIM6

7.15. TIM2

Channel1: Output Compare No Output

7.15.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**10000-1 ***
Counter Mode	Up

Counter Period (AutoReload Register - 32 bits value)	**100 ***
Internal Clock Division (CKD)	No Division
auto-reload preload	**Enable ***

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	**Update Event ***

Output Compare No Output Channel 1:

Mode	Frozen (used for Timing base)
Pulse (32 bits value)	0
Output compare preload	Disable
CH Polarity	High

7.16. USB_OTG_FS
Mode: Host_Only
mode: Activate_VBUS
7.16.1. Parameter Settings:

Speed	Full Speed 12MBit/s
Signal start of frame	Disabled

7.17. FATFS
mode: USB Disk
7.17.1. Set Defines:

Version:

FATFS version	R0.12c

Function Parameters:

FS_READONLY (Read-only mode)	Disabled
FS_MINIMIZE (Minimization level)	Disabled
USE_STRFUNC (String functions)	Enabled with LF -> CRLF conversion
USE_FIND (Find functions)	Disabled
USE_MKFS (Make filesystem function)	Enabled
USE_FASTSEEK (Fast seek function)	Enabled
USE_EXPAND (Use f_expand function)	Disabled
USE_CHMOD (Change attributes function)	Disabled
USE_LABEL (Volume label functions)	Disabled
USE_FORWARD (Forward function)	Disabled

Locale and Namespace Parameters:

CODE_PAGE (Code page on target)	Latin 1
USE_LFN (Use Long Filename)	Disabled
MAX_LFN (Max Long Filename)	255
LFN_UNICODE (Enable Unicode)	ANSI/OEM
STRF_ENCODE (Character encoding)	UTF-8
FS_RPATH (Relative Path)	Disabled

Physical Drive Parameters:

VOLUMES (Logical drives)	**4 ***
MAX_SS (Maximum Sector Size)	512
MIN_SS (Minimum Sector Size)	512
MULTI_PARTITION (Volume partitions feature)	Disabled
USE_TRIM (Erase feature)	Disabled
FS_NOFSINFO (Force full FAT scan)	0

System Parameters:

FS_TINY (Tiny mode)	Disabled
FS_EXFAT (Support of exFAT file system)	Disabled
FS_NORTC (Timestamp feature)	Dynamic timestamp
FS_REENTRANT (Re-Entrancy)	Enabled
FS_TIMEOUT (Timeout ticks)	1000
USE_MUTEX	Disabled
SYNC_t (O/S sync object)	osSemaphoreId
FS_LOCK (Number of files opened simultaneously)	2

7.17.2. Advanced Settings:

USBH:

USBH instance	USB Host MSC FS
Use dma template	Disabled

7.18. FREERTOS

Interface: CMSIS_V1

7.18.1. Config parameters:

API:

FreeRTOS API	CMSIS v1

Versions:

FreeRTOS version	10.2.1
CMSIS-RTOS version	1.02

MPU/FPU:

ENABLE_MPU	Disabled
ENABLE_FPU	Disabled

Kernel settings:

USE_PREEMPTION	Enabled
CPU_CLOCK_HZ	SystemCoreClock
TICK_RATE_HZ	1000
MAX_PRIORITIES	7
MINIMAL_STACK_SIZE	128
MAX_TASK_NAME_LEN	16
USE_16_BIT_TICKS	Disabled
IDLE_SHOULD_YIELD	Enabled
USE_MUTEXES	Enabled
USE_RECURSIVE_MUTEXES	Disabled
USE_COUNTING_SEMAPHORES	Disabled
QUEUE_REGISTRY_SIZE	8
USE_APPLICATION_TASK_TAG	**Enabled ***
ENABLE_BACKWARD_COMPATIBILITY	Enabled
USE_PORT_OPTIMISED_TASK_SELECTION	Enabled
USE_TICKLESS_IDLE	Disabled
USE_TASK_NOTIFICATIONS	Enabled
RECORD_STACK_HIGH_ADDRESS	Disabled

Memory management settings:

Memory Allocation	Dynamic / Static
TOTAL_HEAP_SIZE	**20480 ***
Memory Management scheme	heap_4

Hook function related definitions:

USE_IDLE_HOOK	**Enabled ***
USE_TICK_HOOK	Disabled
USE_MALLOC_FAILED_HOOK	**Enabled ***
USE_DAEMON_TASK_STARTUP_HOOK	Disabled
CHECK_FOR_STACK_OVERFLOW	Disabled

Run time and task stats gathering related definitions:

GENERATE_RUN_TIME_STATS	Disabled
USE_TRACE_FACILITY	**Enabled ***
USE_STATS_FORMATTING_FUNCTIONS	Disabled

Co-routine related definitions:

USE_CO_ROUTINES	Disabled
MAX_CO_ROUTINE_PRIORITIES	2

Software timer definitions:

USE_TIMERS	Disabled

Interrupt nesting behaviour configuration:

LIBRARY_LOWEST_INTERRUPT_PRIORITY	15
LIBRARY_MAX_SYSCALL_INTERRUPT_PRIORITY	5

Added with 10.2.1 support:

MESSAGE_BUFFER_LENGTH_TYPE	size_t
USE_POSIX_ERRNO	Disabled

7.18.2. Include parameters:

Include definitions:

vTaskPrioritySet	Enabled
uxTaskPriorityGet	Enabled
vTaskDelete	Enabled
vTaskCleanUpResources	Disabled
vTaskSuspend	Enabled
vTaskDelayUntil	Disabled
vTaskDelay	Enabled
xTaskGetSchedulerState	Enabled
xTaskResumeFromISR	Enabled
xQueueGetMutexHolder	Disabled
xSemaphoreGetMutexHolder	Disabled
pcTaskGetTaskName	Disabled
uxTaskGetStackHighWaterMark	Disabled
xTaskGetCurrentTaskHandle	Disabled
eTaskGetState	Disabled
xEventGroupSetBitFromISR	Disabled
xTimerPendFunctionCall	Disabled
xTaskAbortDelay	Disabled
xTaskGetHandle	Disabled
uxTaskGetStackHighWaterMark2	Disabled

7.18.3. Advanced settings:

Newlib settings (see parameter description first):

USE_NEWLIB_REENTRANT	Disabled

Project settings (see parameter description first):

Use FW pack heap file	Enabled

7.19. PDM2PCM

mode: Enabled

7.19.1. Parameter Settings:

Version:

PDM2PCM version	3.2.0

PDM2PCM:

How many channel do you use ?	1

7.19.2. CHANNEL1:

PDM2PCM_Channel:

Initialisation	
bit_order (define the bit order)	PDM_FILTER_BIT_ORDER_LSB
endianness (define the byte order)	PDM_FILTER_ENDIANNESS_BE
high_pass_tap (the high pass filter alpha)	2104533974
in_ptr_channels (the channels number in the input PDM stream)	2
out_ptr_channels (the channels number in the output PCM stream)	2
Initial Configuration	
decimation_factor (the factor to adapt PDM frequency to PCM frequency)	PDM_FILTER_DEC_FACTOR_64
output_samples_number (the number of samples by request)	16
mic_gain (the microphone gain in dB)	0

7.20. STMicroelectronics.X-CUBE-TOUCHGFX.4.15.0

mode: GraphicsJjApplication

7.20.1. TouchGFX Generator:

Display:

Interface	Custom
Framebuffer Pixel Format	**RGB888 ***
Width	**800 ***
Height	**480 ***
Framebuffer Strategy	Single Buffer
Buffer Location	**By Address ***
Start Address	**0xC0000000 ***

Driver:

Application Tick Source	Custom

Graphics Accelerator	**ChromART (DMA2D) ***
Real-Time Operating System	CMSIS_RTOS_V1

7.21. USB_HOST

Class for FS IP: Mass Storage Host Class

7.21.1. Parameter Settings:

Host Configuration:

USBH_MAX_NUM_ENDPOINTS (Maximum number of endpoints)	2
USBH_MAX_NUM_INTERFACES (Maximun number of interfaces)	2
USBH_MAX_NUM_SUPPORTED_CLASS (Maximun number of supported class)	1
USBH_MAX_NUM_CONFIGURATION (Maximun number of supported configuration)	1
USBH_KEEP_CFG_DESCRIPTOR (Keep the configuration into RAM)	Enabled
USBH_MAX_SIZE_CONFIGURATION (Maximun size in bytes for the Configuration Descriptor)	256
USBH_MAX_DATA_BUFFER (Maximun size of temporary data)	512
USBH_DEBUG_LEVEL (USBH Debug Level)	0: No debug message

CMSIS_RTOS:

USBH_USE_OS (Enable the support of an RTOS)	Enabled
USBH_PROCESS_PRIO (The CMSIS-RTOS osPriority value specifies the priority for the USB Host thread)	priority: normal (default)
USBH_PROCESS_STACK_SIZE (The CMSIS-RTOS stack size requirements in words)	**512 ***

*** User modified value**

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PC3	ADC1_IN13	Analog mode	No pull-up and no pull-down	n/a	
	PC2	ADC1_IN12	Analog mode	No pull-up and no pull-down	n/a	
	PC4	ADC1_IN14	Analog mode	No pull-up and no pull-down	n/a	
	PB1	ADC1_IN9	Analog mode	No pull-up and no pull-down	n/a	
DSIHOST	DSIHOST_D1P	DSIHOST_D1P	n/a	n/a	n/a	
	DSIHOST_D1N	DSIHOST_D1N	n/a	n/a	n/a	
	DSIHOST_CKP	DSIHOST_CKP	n/a	n/a	n/a	
	DSIHOST_CKN	DSIHOST_CKN	n/a	n/a	n/a	
	DSIHOST_D0P	DSIHOST_D0P	n/a	n/a	n/a	
	DSIHOST_D0N	DSIHOST_D0N	n/a	n/a	n/a	
	PJ2	DSIHOST_TE	Alternate Function Push Pull	No pull-up and no pull-down	Low	
FMC	PE1	FMC_NBL1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE0	FMC_NBL0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PG15	FMC_SDNCAS	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD0	FMC_D2	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PI4	FMC_NBL2	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD1	FMC_D3	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PI3	FMC_D27	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PI2	FMC_D26	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF0	FMC_A0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PI5	FMC_NBL3	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PI7	FMC_D29	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PI10	FMC_D31	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PI6	FMC_D28	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PH15	FMC_D23	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PI1	FMC_D25	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF1	FMC_A1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PI9	FMC_D30	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PH13	FMC_D21	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PH14	FMC_D22	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PI0	FMC_D24	Alternate Function Push Pull	No pull-up and no pull-down	Very High	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PF2	FMC_A2	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF3	FMC_A3	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PG8	FMC_SDCLK	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF4	FMC_A4	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PH3	FMC_SDNE0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF5	FMC_A5	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PH2	FMC_SDCKE0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD15	FMC_D1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD10	FMC_D15	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD14	FMC_D0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD9	FMC_D14	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD8	FMC_D13	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC0	FMC_SDNWE	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF12	FMC_A6	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PG1	FMC_A11	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF15	FMC_A9	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PH12	FMC_D20	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF13	FMC_A7	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PG0	FMC_A10	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE8	FMC_D5	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PG5	FMC_BA1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PG4	FMC_BA0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PH9	FMC_D17	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PH11	FMC_D19	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF14	FMC_A8	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF11	FMC_SDNRAS	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE9	FMC_D6	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE11	FMC_D8	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE14	FMC_D11	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PH8	FMC_D16	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PH10	FMC_D18	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE7	FMC_D4	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE10	FMC_D7	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE12	FMC_D9	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE15	FMC_D12	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE13	FMC_D10	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
I2C1	PB8	I2C1_SCL	Alternate Function Open Drain	Pull-up	**Very High ***	
	PB9	I2C1_SDA	Alternate Function Open Drain	Pull-up	**Very High ***	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
I2S3	PB5	I2S3_SD	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB4	I2S3_ext_SD	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB3	I2S3_CK	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA15	I2S3_WS	Alternate Function Push Pull	No pull-up and no pull-down	Low	
QUADSPI	PB6	QUADSPI_BK1_NCS	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PF7	QUADSPI_BK1_IO2	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PF6	QUADSPI_BK1_IO3	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PF10	QUADSPI_CLK	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PF9	QUADSPI_BK1_IO1	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PF8	QUADSPI_BK1_IO0	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
RCC	PH0/OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
	PH1/OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
SAI1	PE4	SAI1_FS_A	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PE5	SAI1_SCK_A	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PE6	SAI1_SD_A	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PG7	SAI1_MCLK_A	Alternate Function Push Pull	No pull-up and no pull-down	Low	
USB_OTG_FS	PA12	USB_OTG_FS_DP	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PA11	USB_OTG_FS_DM	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PA9	USB_OTG_FS_VBUS	Input mode	No pull-up and no pull-down	**n/a**	
GPIO	PK3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PD4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PG6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PB2/BOOT1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PH7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	

8.2. DMA configuration

DMA request	Stream	Direction	Priority
ADC1	DMA2_Stream0	Peripheral To Memory	Low
SAI1_A	DMA2_Stream3	Memory To Peripheral	Low

ADC1: DMA2_Stream0 DMA request Settings:

Mode:	**Circular ***
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	**Word ***
Memory Data Width:	**Word ***

SAI1_A: DMA2_Stream3 DMA request Settings:

Mode:	**Circular ***
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Word
Memory Data Width:	Word

8.3. NVIC configuration

8.3.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	15	0
System tick timer	true	15	0
TIM6 global interrupt, DAC1 and DAC2 underrun error interrupts	true	0	0
DMA2 stream0 global interrupt	true	5	0
DMA2 stream3 global interrupt	true	0	0
USB On The Go FS global interrupt	true	5	0
LTDC global interrupt	true	5	0
DMA2D global interrupt	true	5	0
DSI global interrupt	true	5	0
PVD interrupt through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
ADC1, ADC2 and ADC3 global interrupts	unused		
TIM2 global interrupt	unused		
I2C1 event interrupt	unused		
I2C1 error interrupt	unused		
FMC global interrupt	unused		
SPI3 global interrupt	unused		
HASH and RNG global interrupts	unused		
FPU global interrupt	unused		
SAI1 global interrupt	unused		
LTDC global error interrupt	unused		
QUADSPI global interrupt	unused		

8.3.2. NVIC Code generation

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	true	true	false
Hard fault interrupt	true	true	false

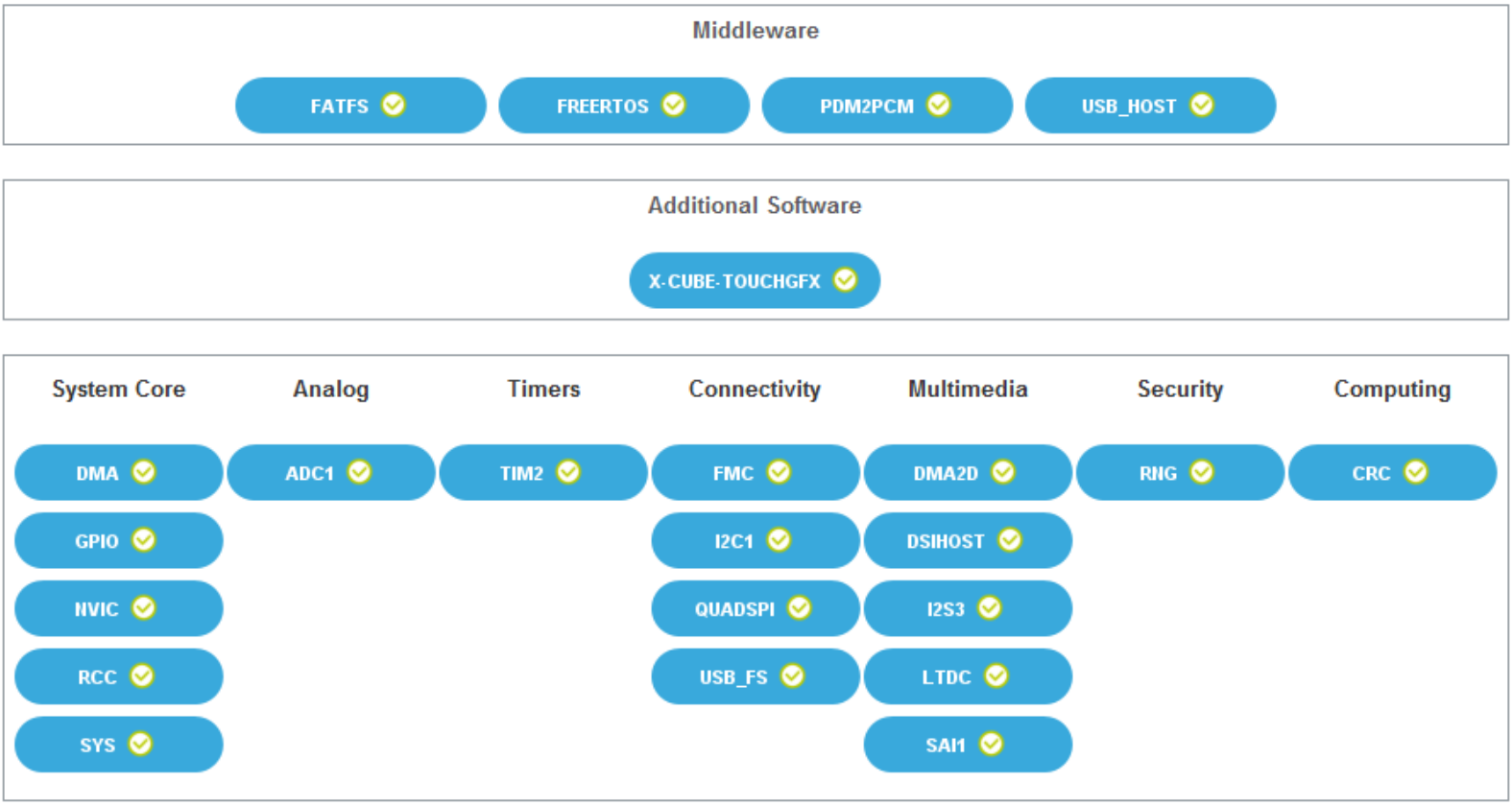
Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Memory management fault	true	true	false
Pre-fetch fault, memory access fault	true	true	false
Undefined instruction or illegal state	true	true	false
System service call via SWI instruction	true	false	false
Debug monitor	true	true	false
Pendable request for system service	true	false	false
System tick timer	true	false	false
TIM6 global interrupt, DAC1 and DAC2 underrun error interrupts	true	true	true
DMA2 stream0 global interrupt	true	true	true
DMA2 stream3 global interrupt	true	true	true
USB On The Go FS global interrupt	true	true	true
LTDC global interrupt	true	true	true
DMA2D global interrupt	true	true	true
DSI global interrupt	true	true	true

*** User modified value**

9. System Views

9.1. Category view

9.1.1. Current



10. Software Pack Report

10.1. Software Pack selected

Vendor	Name	Version	Component
STMicroelectronics	USB_HOST	1.0.0	Class : USB Group : USB Host SubGroup : MSC FS Version : 1.0
STMicroelectronics	FreeRTOS	0.0.1	Class : CMSIS Group : RTOS SubGroup : FreeRTOS Version : 10.2.0 Class : RTOS Group : Core Version : 10.2.0
STMicroelectronics	PDM2PCM	3.2.0	Class : Audio Group : Channel Version : 3.2.0
STMicroelectronics	X-CUBE-TOUCHGFX	4.15.0	Class : Graphics Group : Application Variant : TouchGFX Generator Version : 4.15.0

11. Docs & Resources

Type	Link
Datasheet	http://www.st.com/resource/en/datasheet/DM00219980.pdf
Reference manual	http://www.st.com/resource/en/reference_manual/DM00127514.pdf
Programming manual	http://www.st.com/resource/en/programming_manual/DM00046982.pdf
Errata sheet	http://www.st.com/resource/en/errata_sheet/DM00220774.pdf
Application note	http://www.st.com/resource/en/application_note/CD00167594.pdf
Application note	http://www.st.com/resource/en/application_note/CD00211314.pdf
Application note	http://www.st.com/resource/en/application_note/CD00249778.pdf
Application note	http://www.st.com/resource/en/application_note/CD00259245.pdf
Application note	http://www.st.com/resource/en/application_note/CD00264321.pdf
Application note	http://www.st.com/resource/en/application_note/CD00264342.pdf
Application note	http://www.st.com/resource/en/application_note/CD00264379.pdf
Application note	http://www.st.com/resource/en/application_note/DM00024853.pdf
Application note	http://www.st.com/resource/en/application_note/DM00040802.pdf
Application note	http://www.st.com/resource/en/application_note/DM00040808.pdf
Application note	http://www.st.com/resource/en/application_note/DM00042534.pdf
Application note	http://www.st.com/resource/en/application_note/DM00046011.pdf
Application note	http://www.st.com/resource/en/application_note/DM00072315.pdf
Application note	http://www.st.com/resource/en/application_note/DM00073742.pdf
Application note	http://www.st.com/resource/en/application_note/DM00073853.pdf
Application note	http://www.st.com/resource/en/application_note/DM00080497.pdf
Application note	http://www.st.com/resource/en/application_note/DM00081379.pdf
Application note	http://www.st.com/resource/en/application_note/DM00115714.pdf
Application note	http://www.st.com/resource/en/application_note/DM00129215.pdf
Application note	http://www.st.com/resource/en/application_note/DM00154959.pdf
Application note	http://www.st.com/resource/en/application_note/DM00160482.pdf

Application note	http://www.st.com/resource/en/application_note/DM00172465.pdf
Application note	http://www.st.com/resource/en/application_note/DM00213525.pdf
Application note	http://www.st.com/resource/en/application_note/DM00220769.pdf
Application note	http://www.st.com/resource/en/application_note/DM00227538.pdf
Application note	http://www.st.com/resource/en/application_note/DM00257177.pdf
Application note	http://www.st.com/resource/en/application_note/DM00272912.pdf
Application note	http://www.st.com/resource/en/application_note/DM00226326.pdf
Application note	http://www.st.com/resource/en/application_note/DM00236305.pdf
Application note	http://www.st.com/resource/en/application_note/DM00281138.pdf
Application note	http://www.st.com/resource/en/application_note/DM00296349.pdf
Application note	http://www.st.com/resource/en/application_note/DM00327191.pdf
Application note	http://www.st.com/resource/en/application_note/DM00287601.pdf
Application note	http://www.st.com/resource/en/application_note/DM00287603.pdf
Application note	http://www.st.com/resource/en/application_note/DM00354244.pdf
Application note	http://www.st.com/resource/en/application_note/DM00373474.pdf
Application note	http://www.st.com/resource/en/application_note/DM00315319.pdf
Application note	http://www.st.com/resource/en/application_note/DM00380469.pdf
Application note	http://www.st.com/resource/en/application_note/DM00395696.pdf
Application note	http://www.st.com/resource/en/application_note/DM00431633.pdf
Application note	http://www.st.com/resource/en/application_note/DM00493651.pdf
Application note	http://www.st.com/resource/en/application_note/DM00536349.pdf
Application note	http://www.st.com/resource/en/application_note/DM00560967.pdf