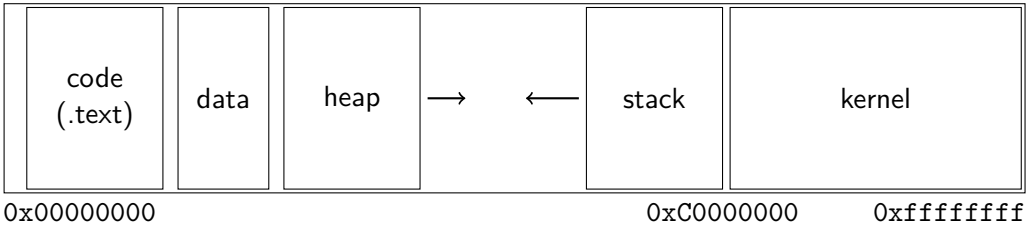
Memory

Johan Montelius

KTH

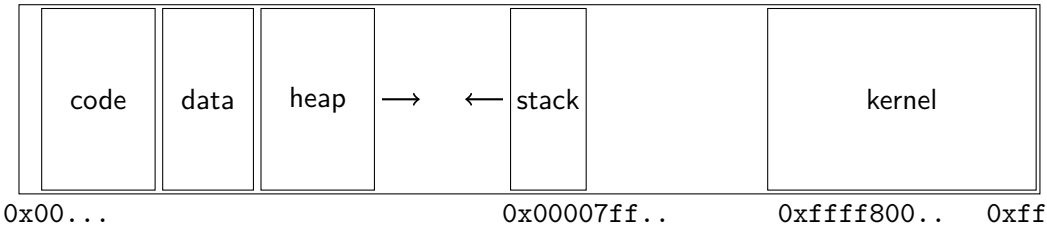
2019

The process

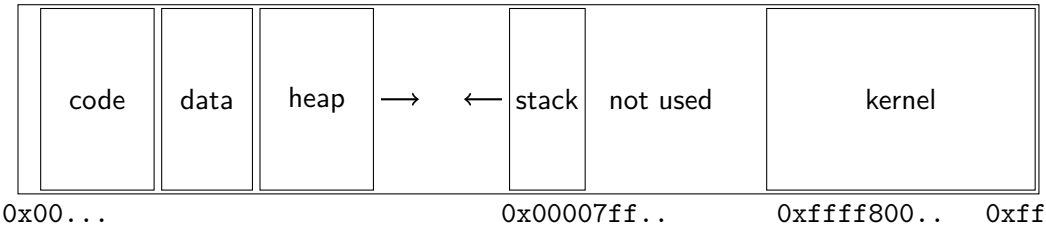


Memory layout for a 32-bit Linux process

64-bit Linux on a x86_64 architecture



64-bit Linux on a x86_64 architecture



Memory virtualization

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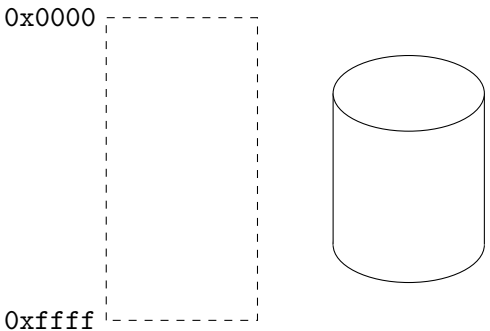
IBM System 360

Chief architect: Gene Amdahl

IBM System 360

- 1964, 8-64 Kbyte memory
- 12+12 bit address space
- batch operating system

Batch processing:



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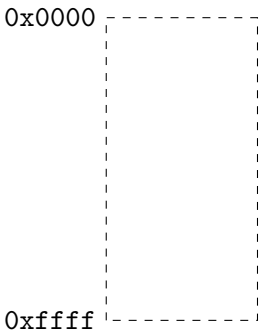

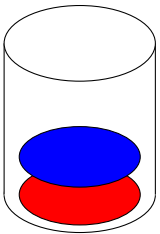

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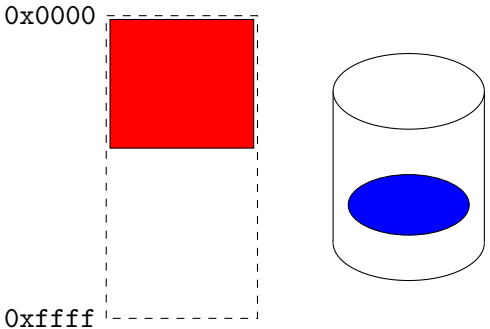

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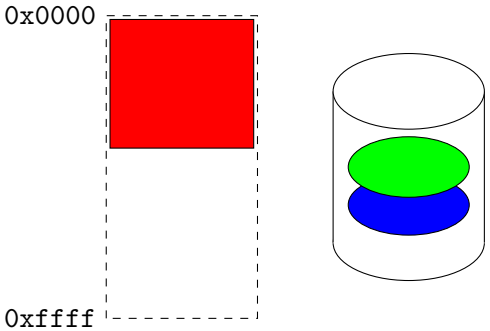

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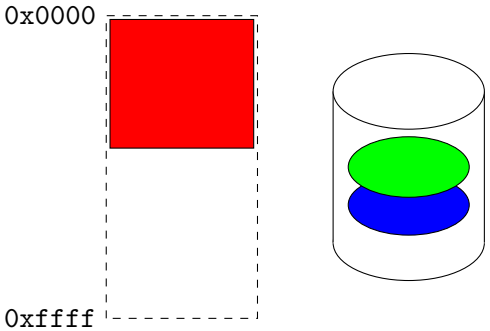

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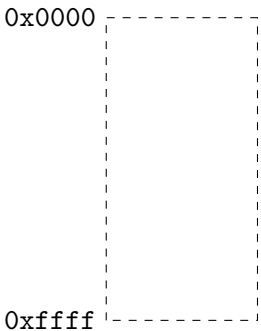

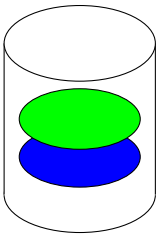

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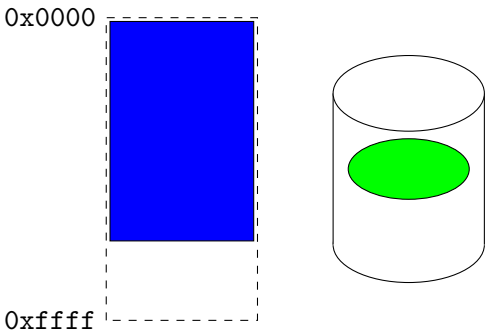

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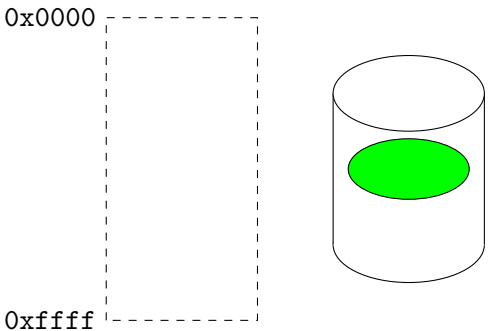

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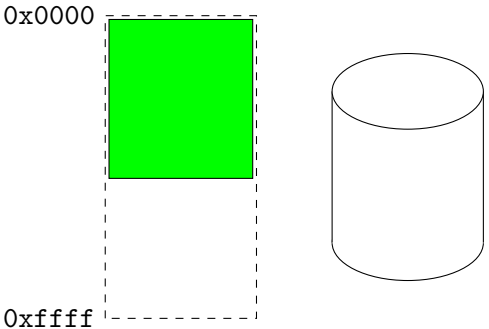
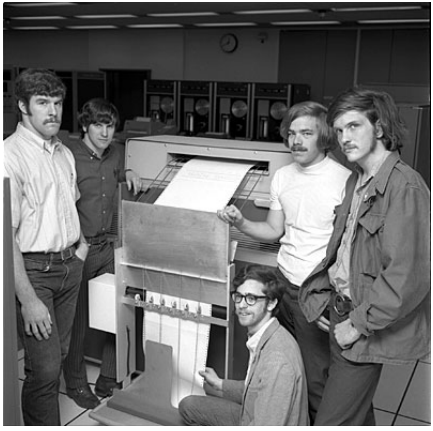


The Dartmouth Time-Sharing System

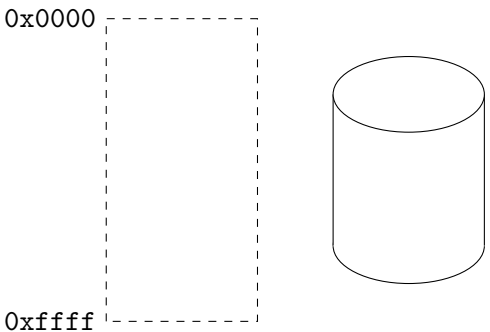


GE-235

- 1964
- 20-bit word
- 8 Kword address space

Arnold Spielberg was in the team that designed the GE-235

Time-sharing:



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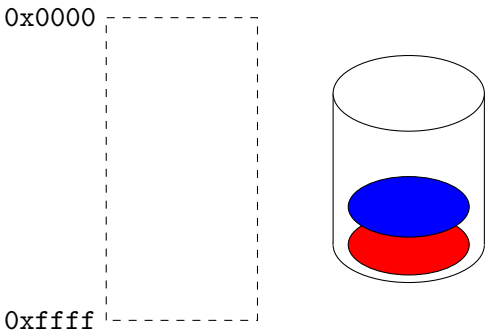

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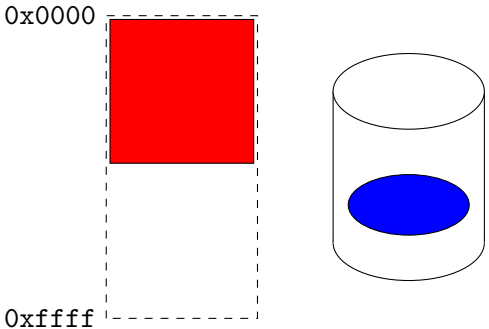

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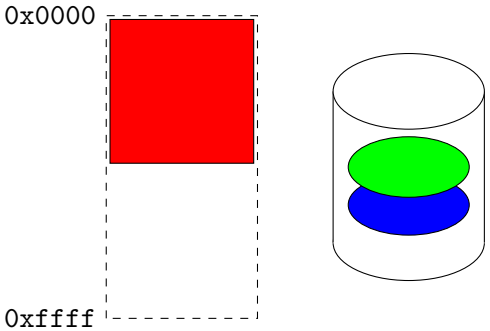

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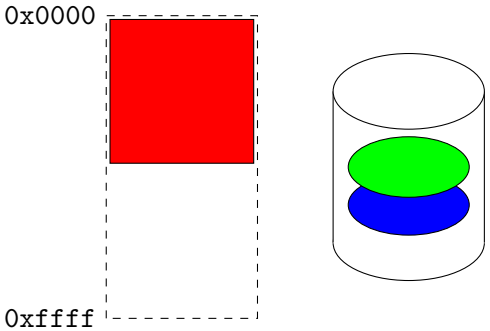

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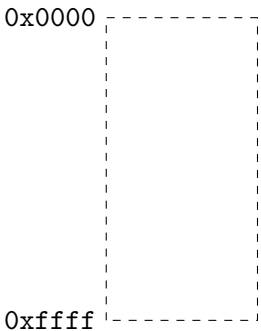

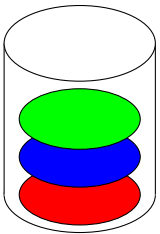

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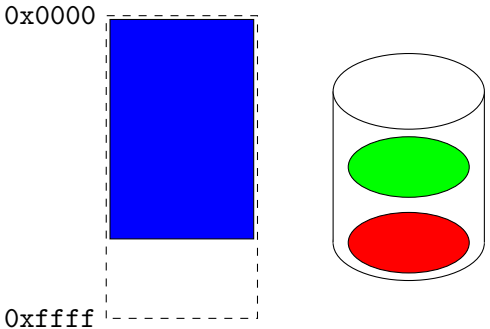

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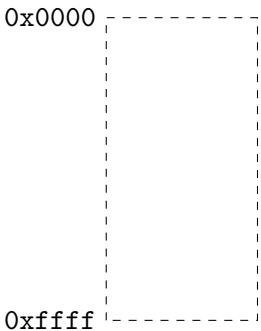

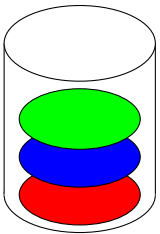

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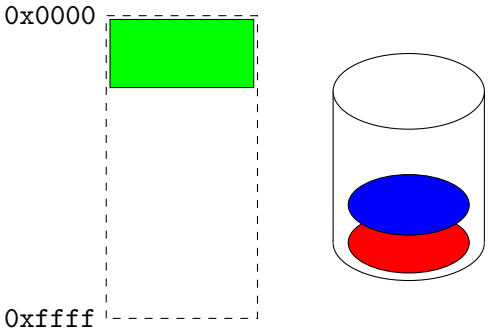

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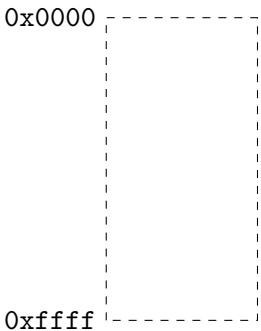

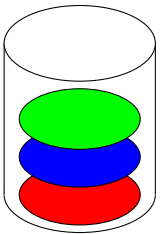

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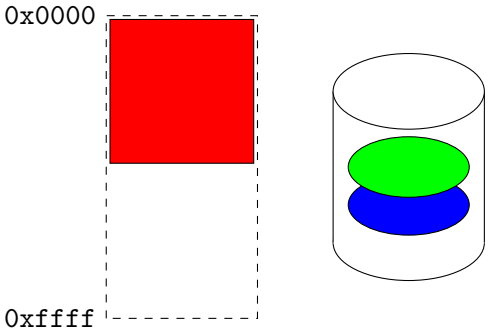
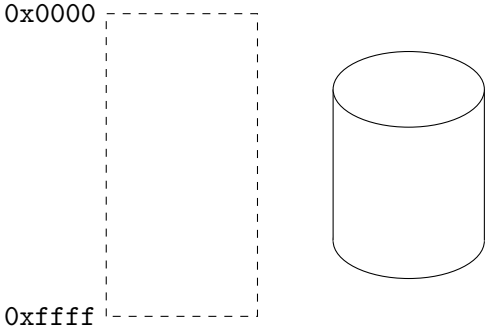


If both programs will fit in memory:



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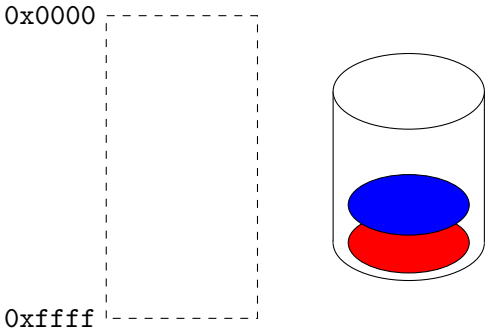

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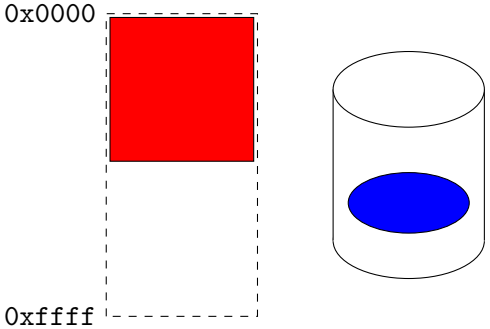

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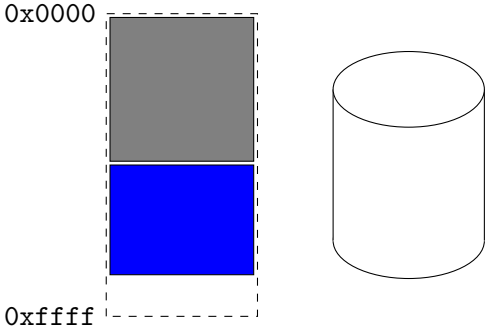
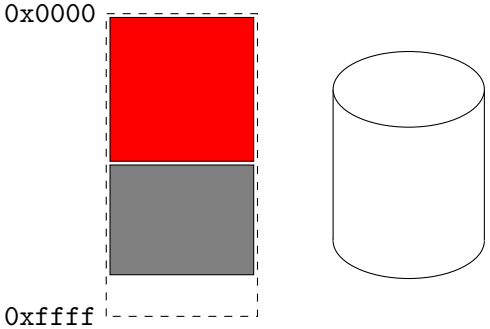


why not switch between two programs

If both programs will fit in memory:



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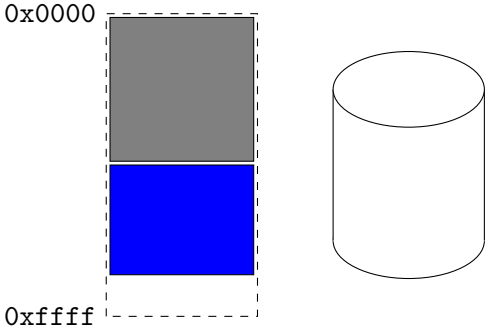

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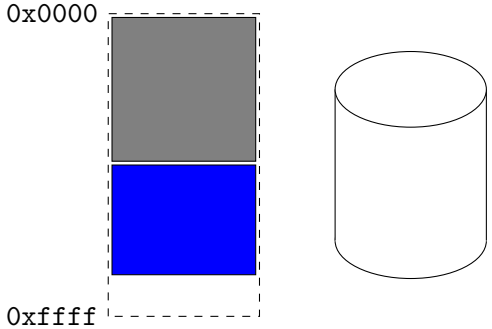
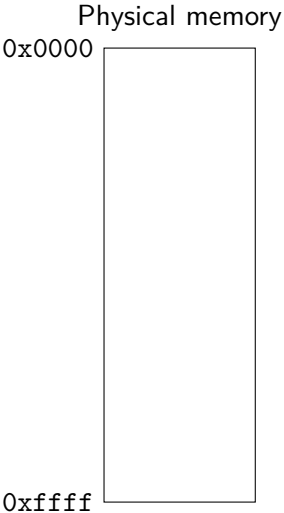


What is the problem?

Virtual memory



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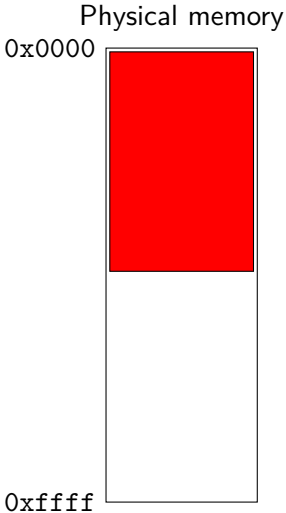

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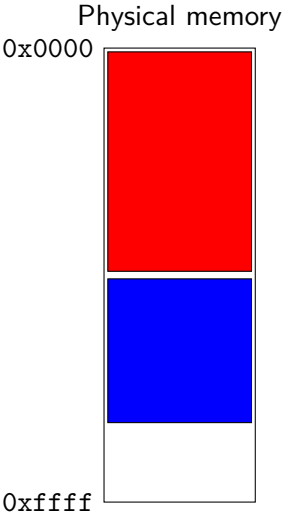

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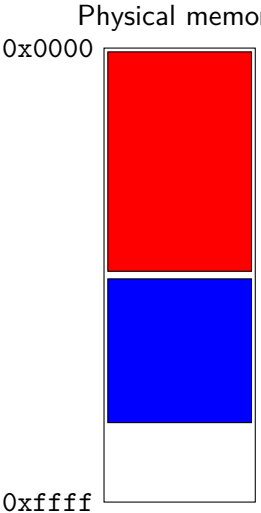
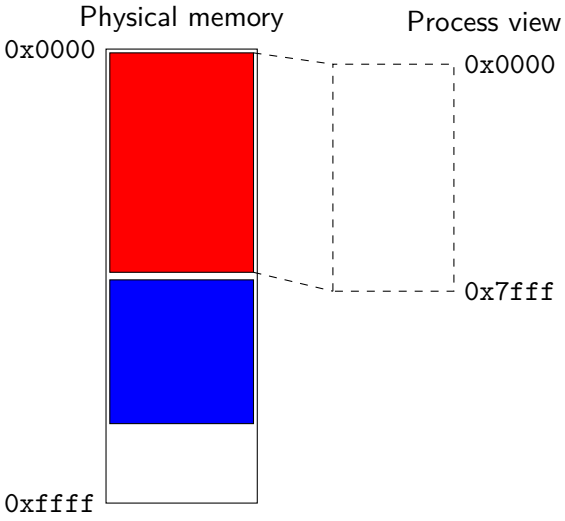


Process view

Virtual memory



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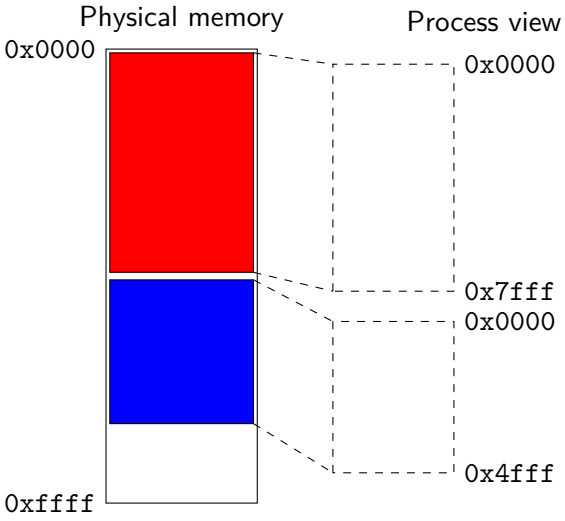

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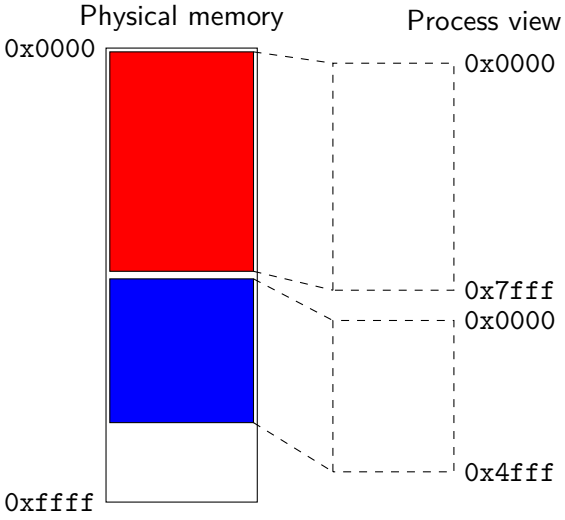
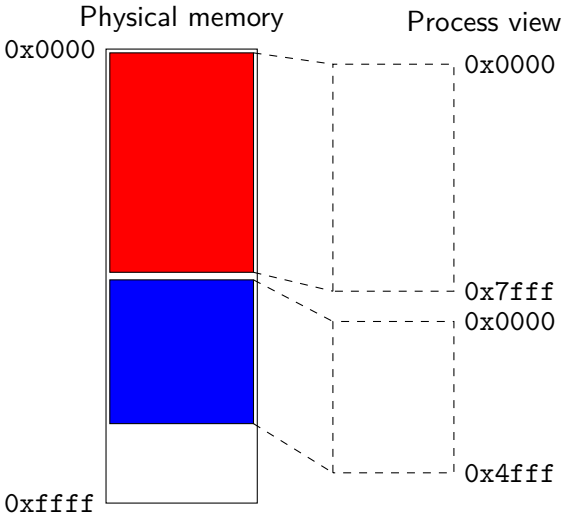


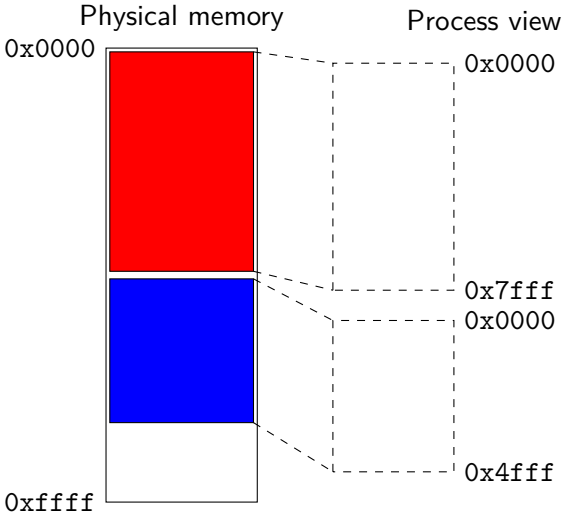
- Transparent: processes should be unaware of virtualization.

Virtual memory



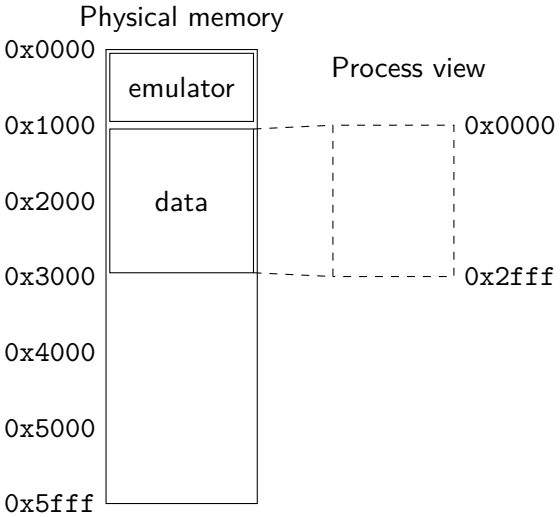
- Transparent: processes should be unaware of virtualization.
- Protection: processes should not be able to interfere with each other.

Virtual memory



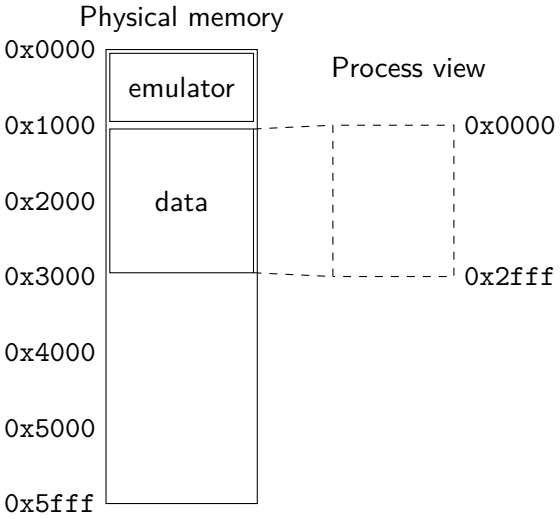
- Transparent: processes should be unaware of virtualization.
- Protection: processes should not be able to interfere with each other.
- Efficiency: execution should be as close to real execution as possible.

Emulator - simple but slow



Let the operating system run an *emulator* that interprets the operations of the process and changes the memory addresses as needed.

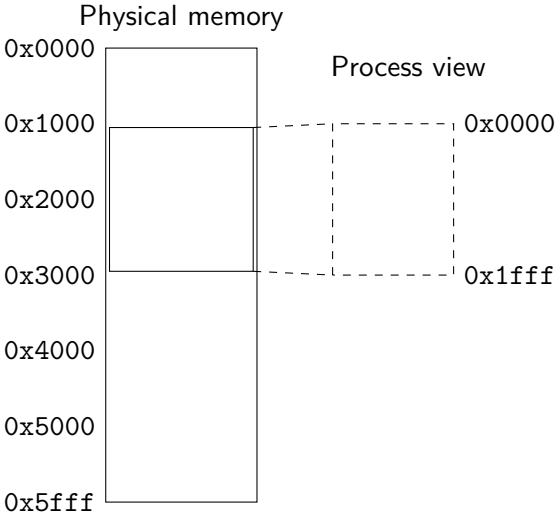
Emulator - simple but slow



This is similar to how the JVM works

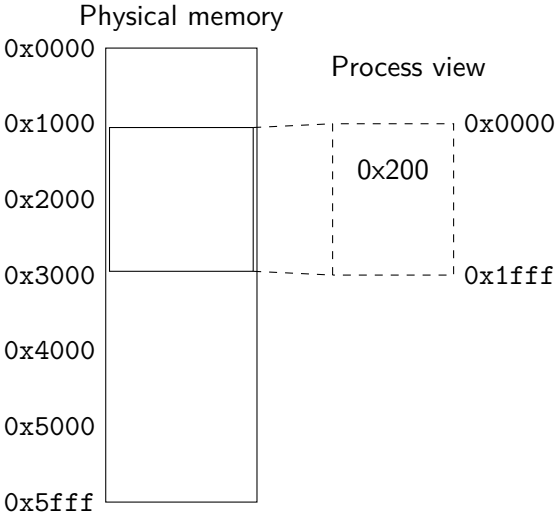
Let the operating system run an *emulator* that interprets the operations of the process and changes the memory addresses as needed.

Static relocation - ehh, static



When a program is loaded, all references to memory locations are changed so that they correspond to the actual location in RAM where the program is loaded.

Static relocation - ehh, static



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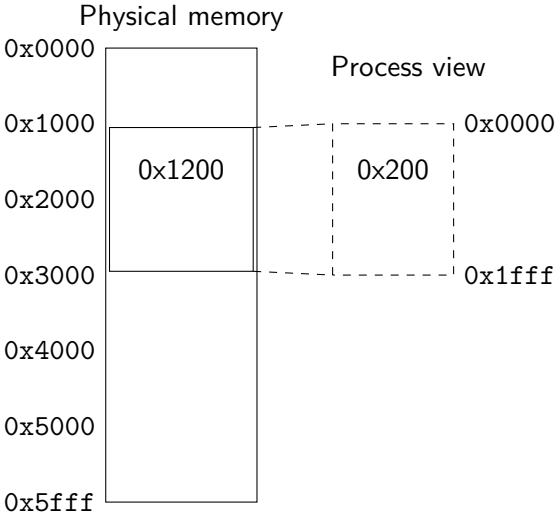

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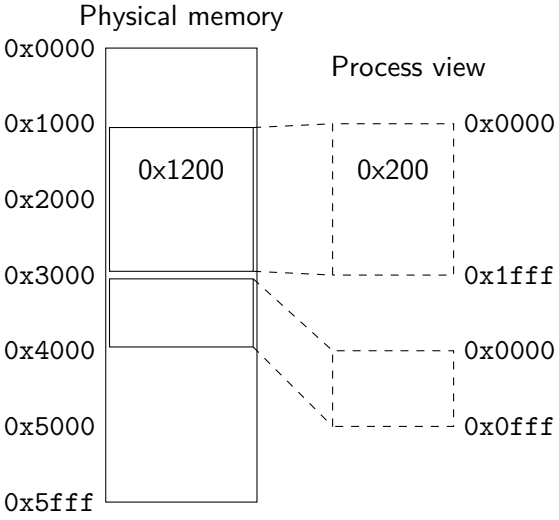

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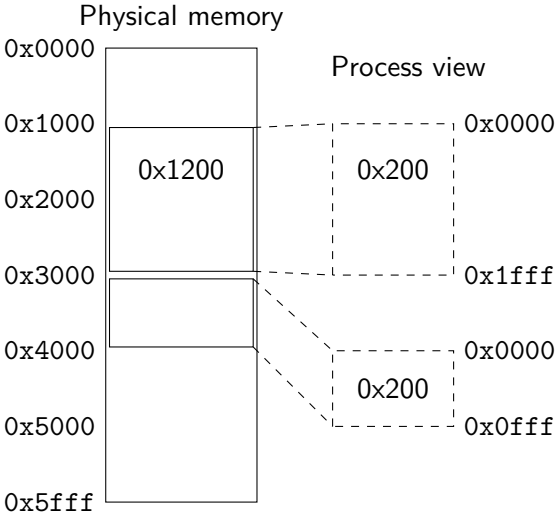

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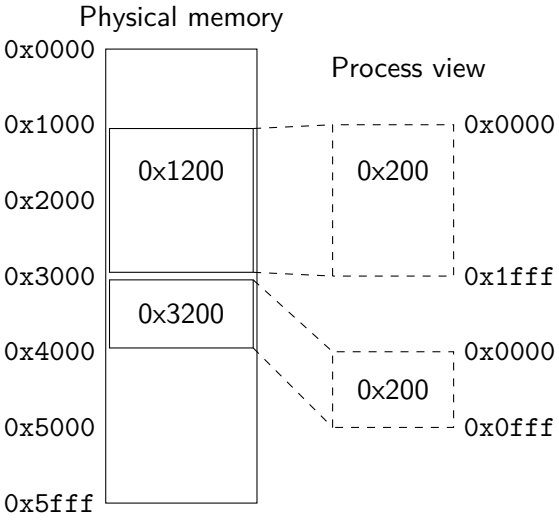

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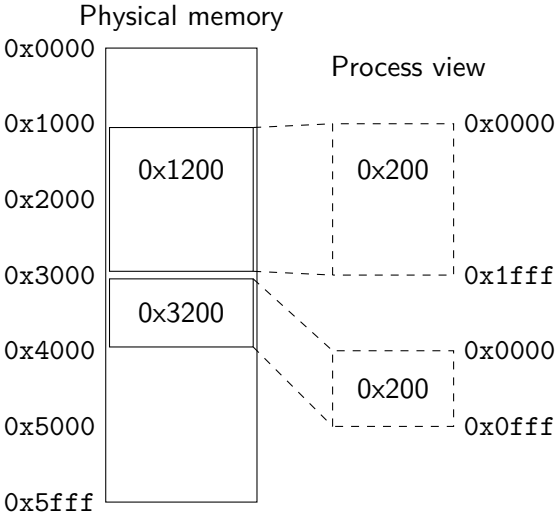

When a program is loaded, all references to memory locations are changed so that they correspond to the actual location in RAM where the program is loaded.

How do we know we have changed all addresses?

Dynamic relocation

Change every memory reference, on the fly, to a region in memory allocated for the process.

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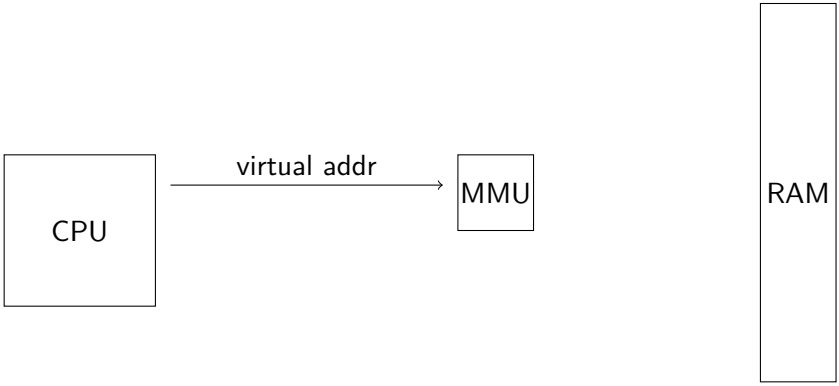

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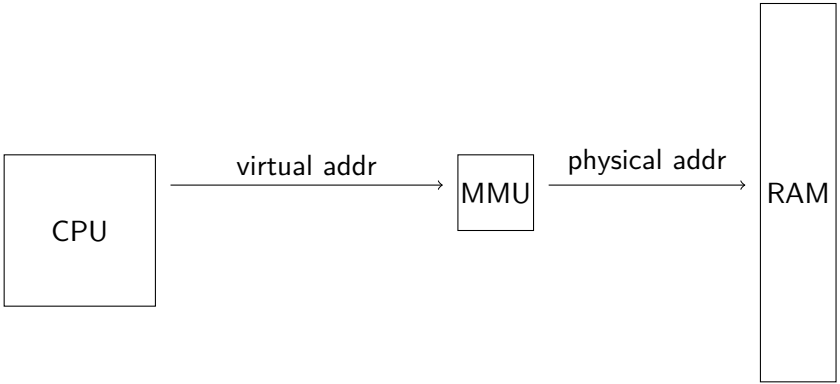

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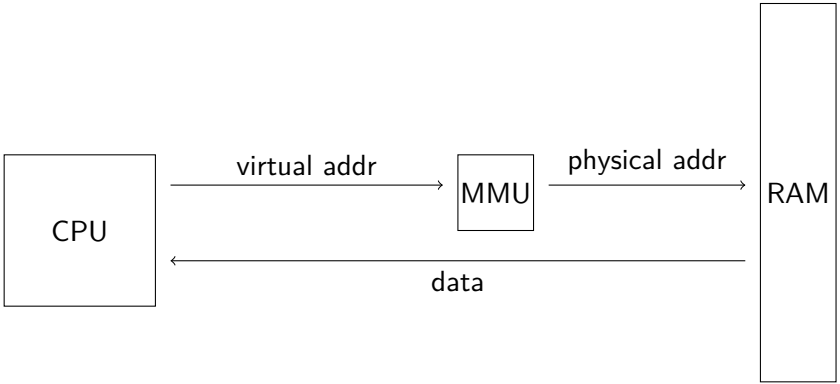
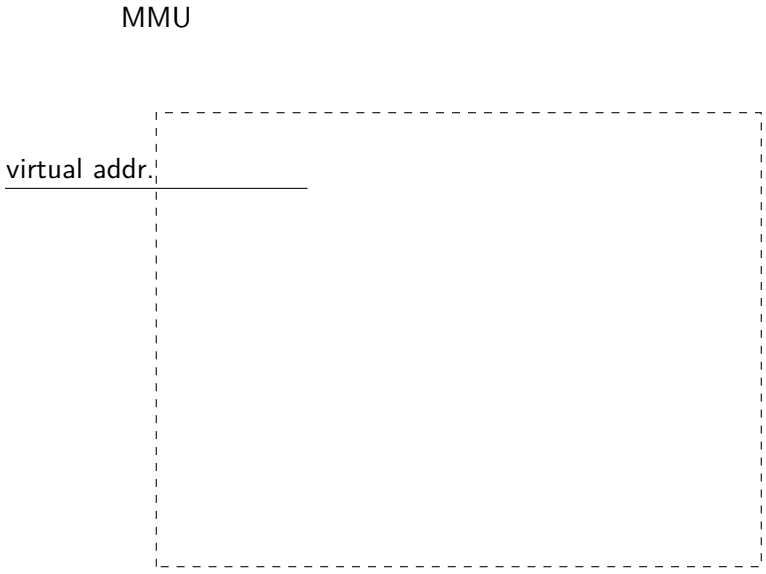


Base register



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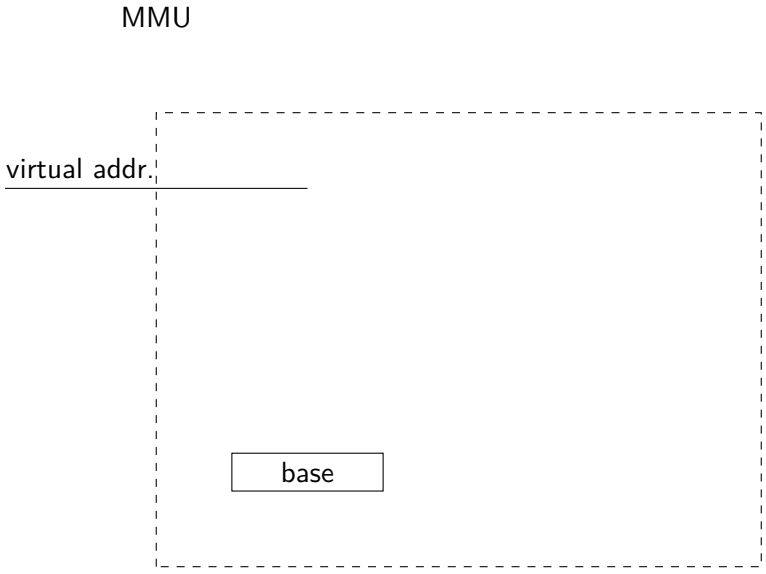

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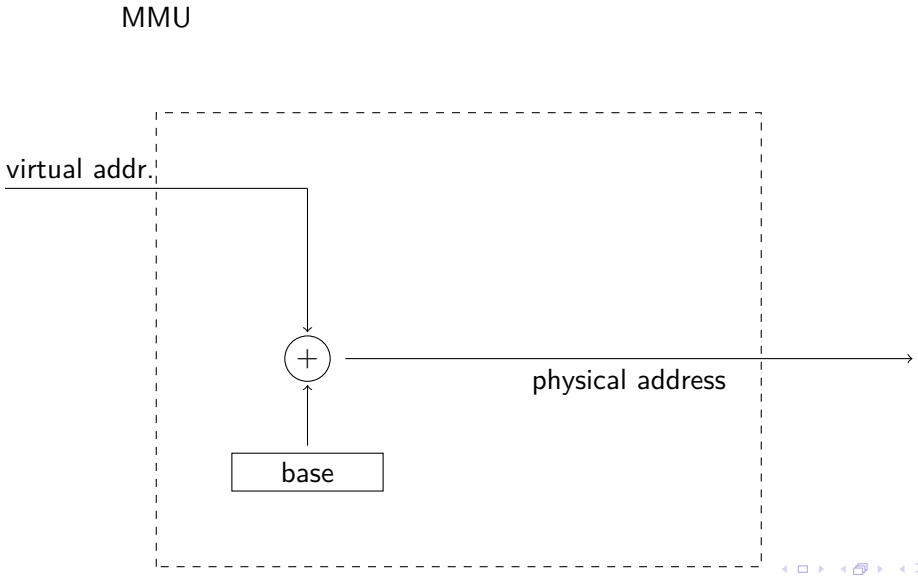

Base problem

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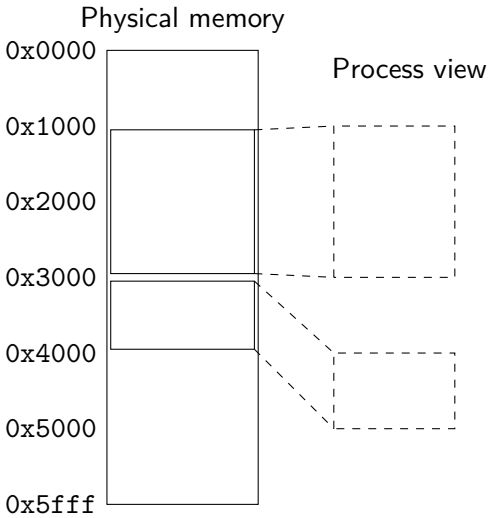

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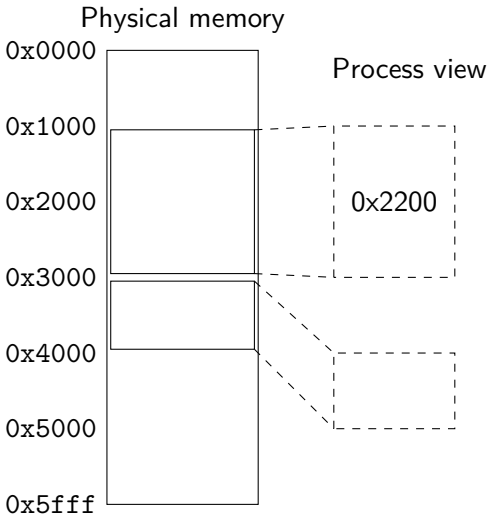

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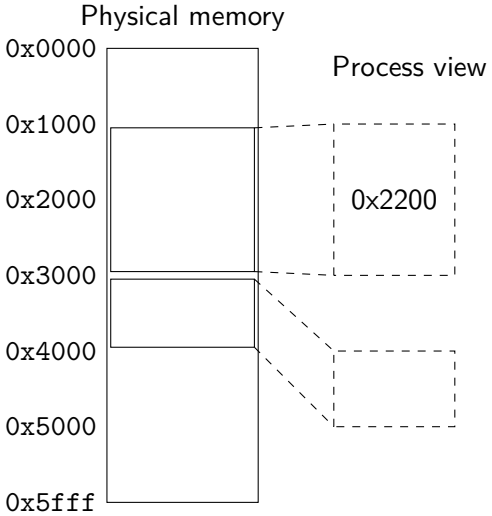
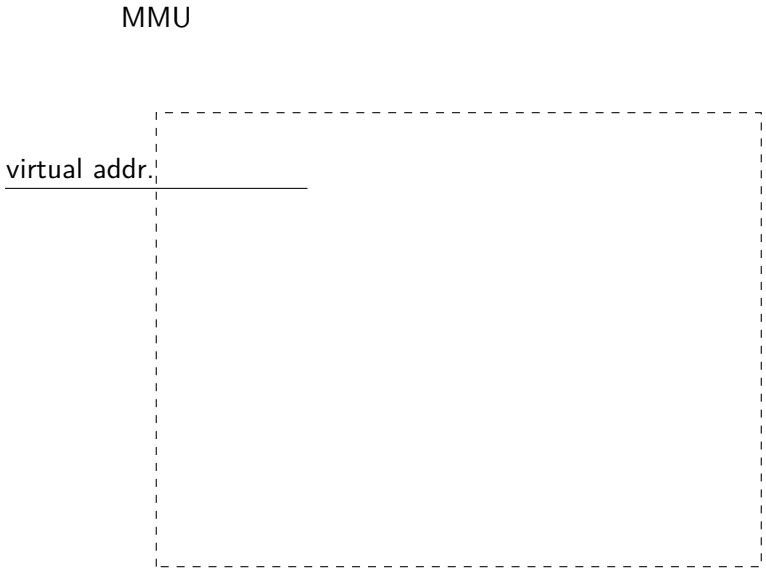


Can we prevent this at compile or load time?

Base and bound



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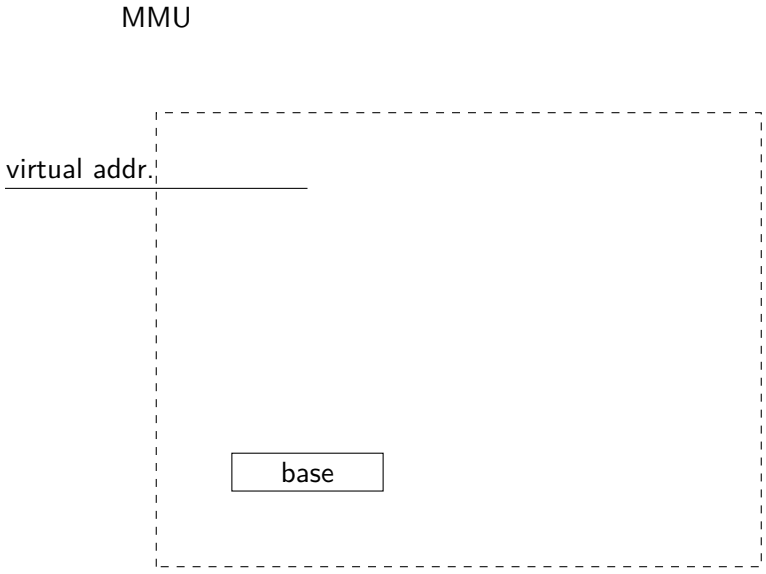

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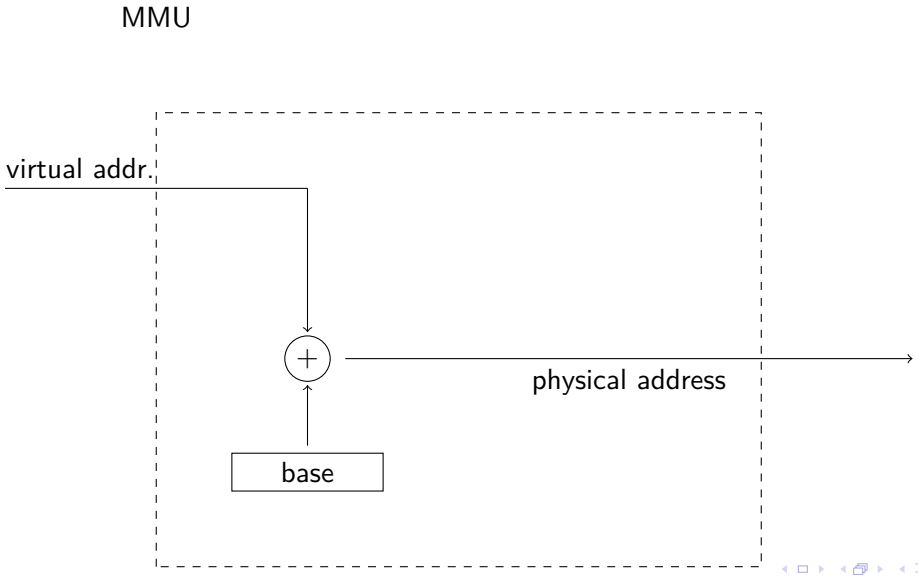

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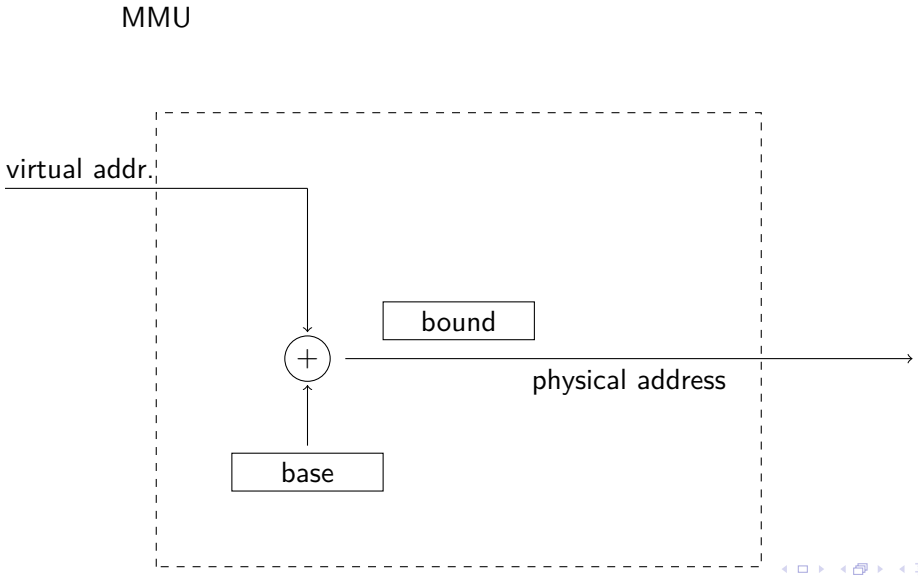

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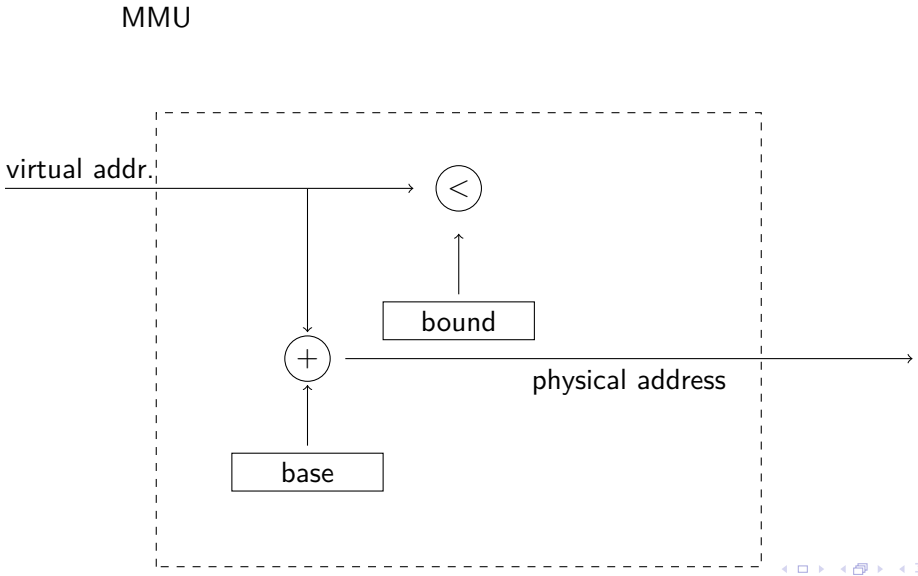

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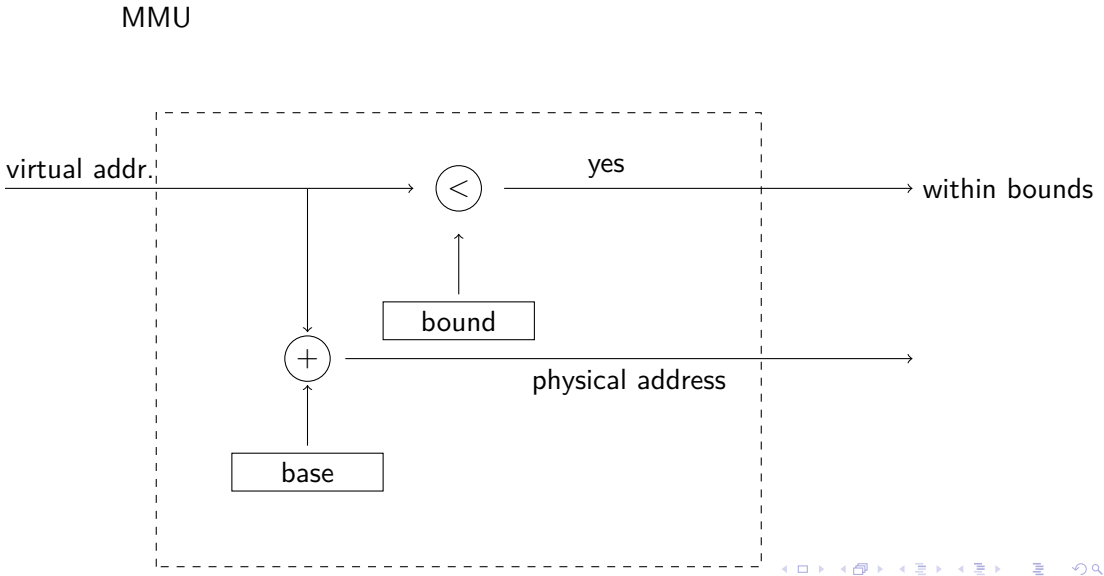

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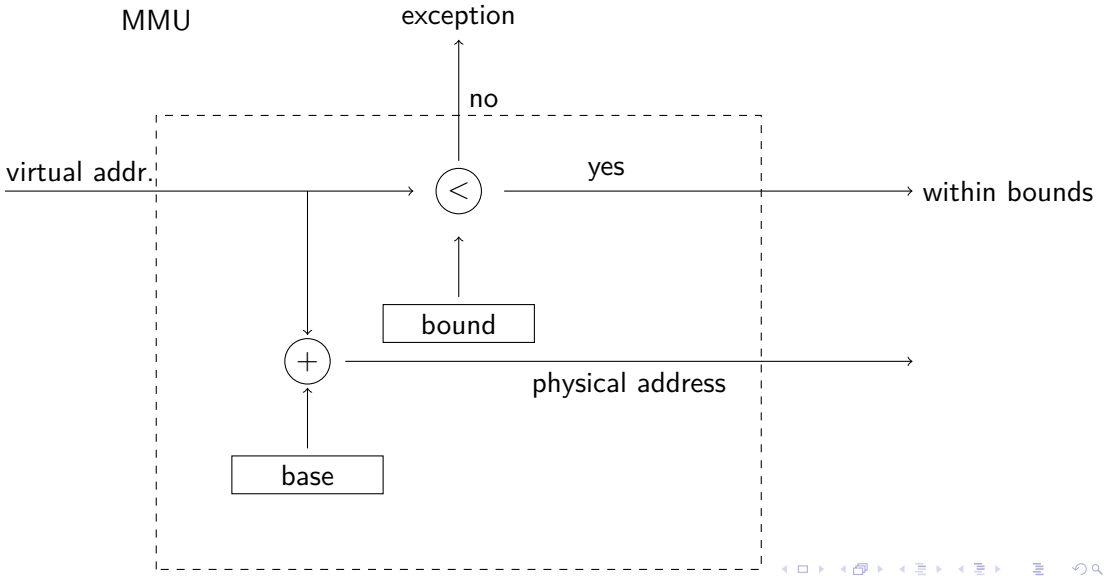

Base and bound

Pros:

- Transparent to a process.
- Simple to implement.
- Easy to change process.

Base and bound

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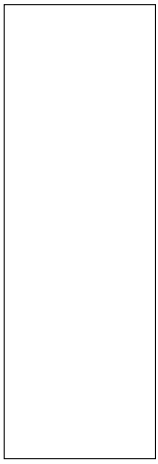
- Simple to implement.
- Easy to change process.

Cons:

- How do we share data?
- Wasted memory.

shared read-only segments

Physical memory



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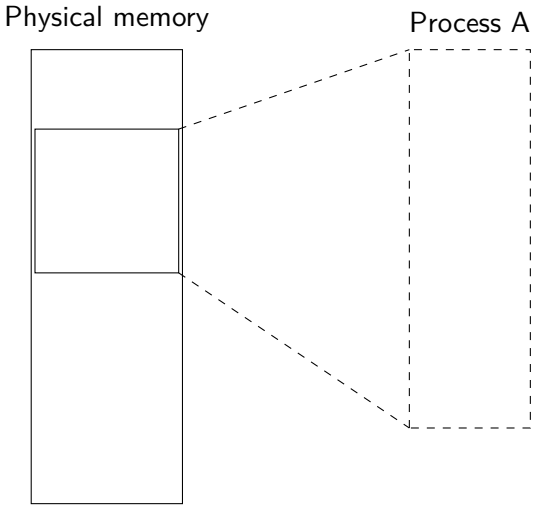

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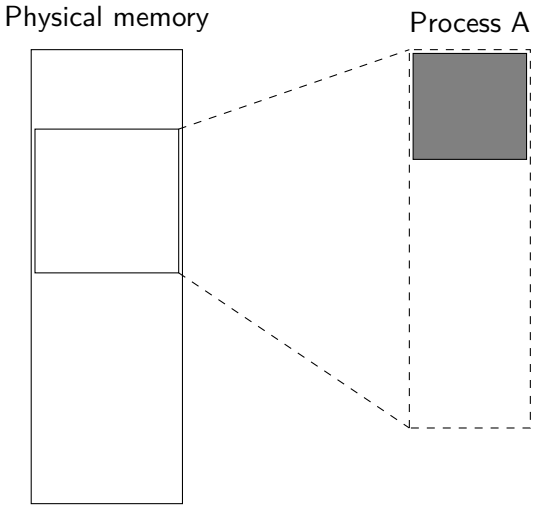

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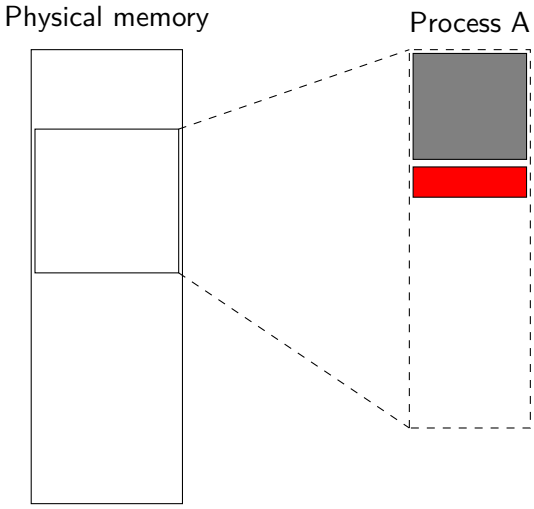

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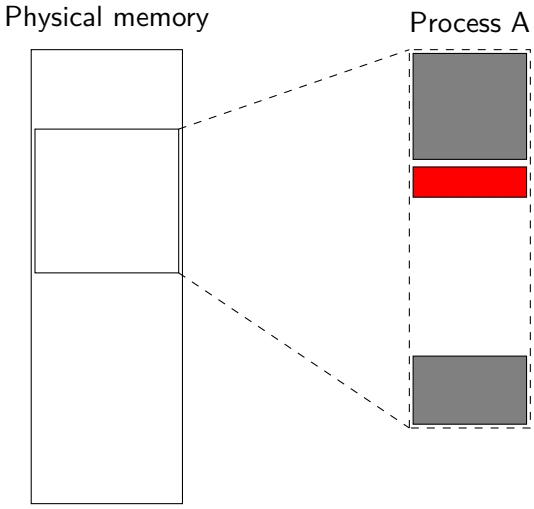

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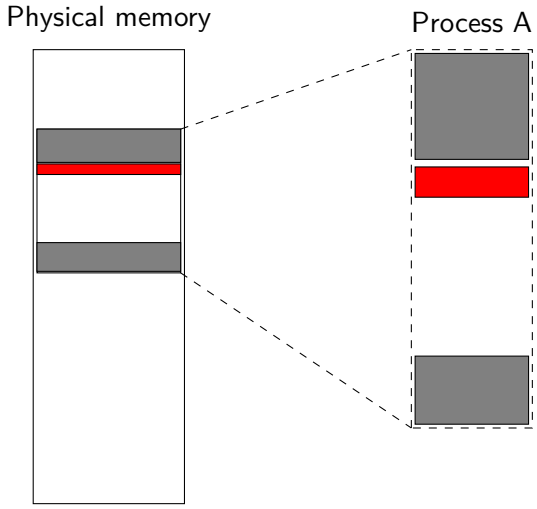

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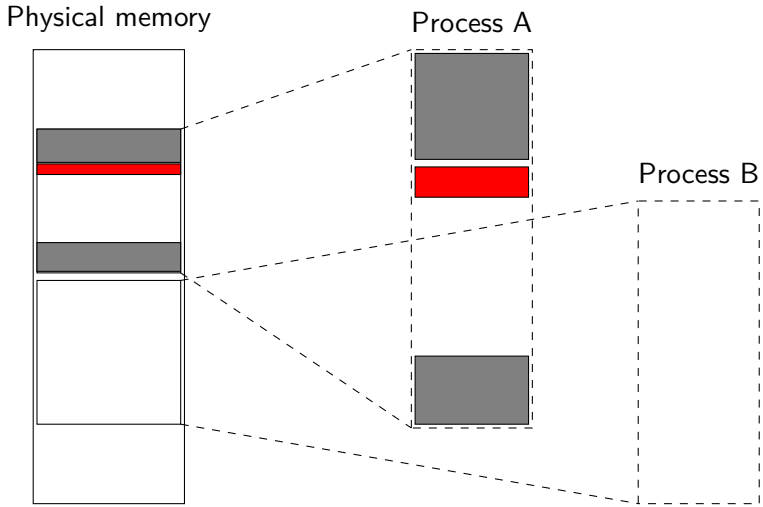

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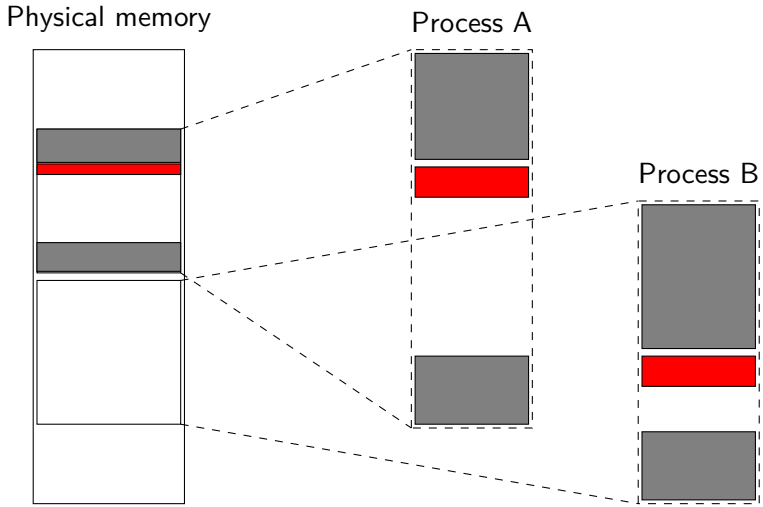

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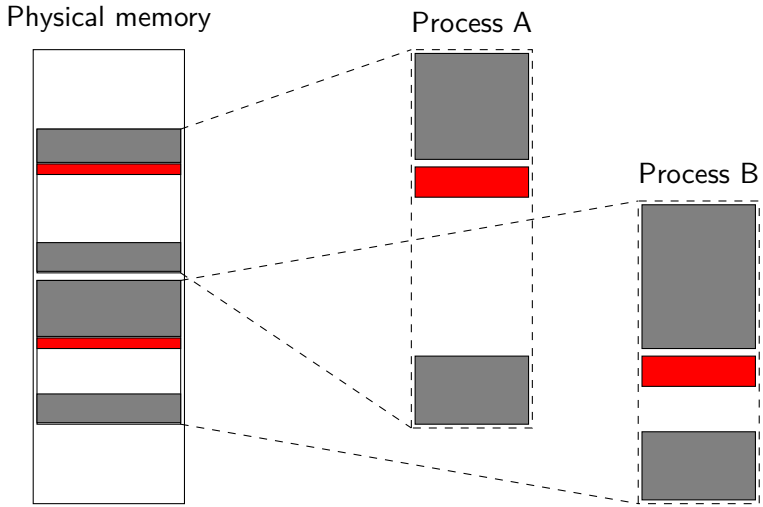

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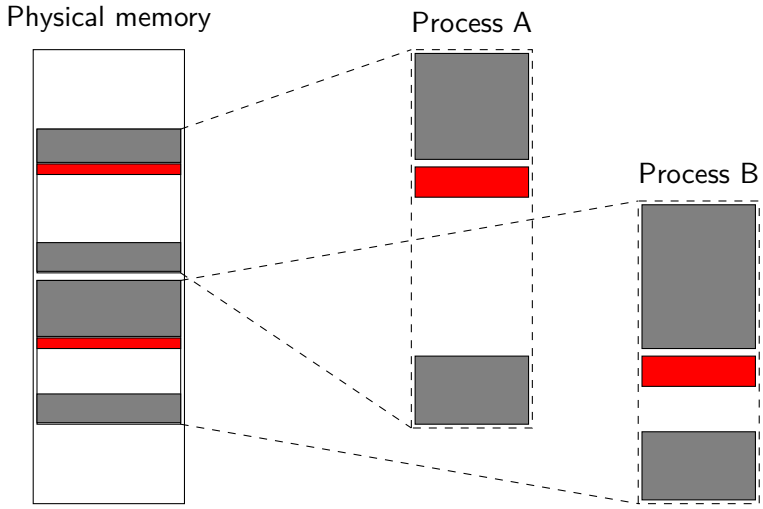
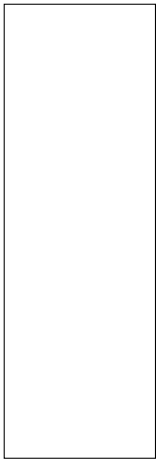


How do we write code that can be shared?

Internal fragmentation

Physical memory



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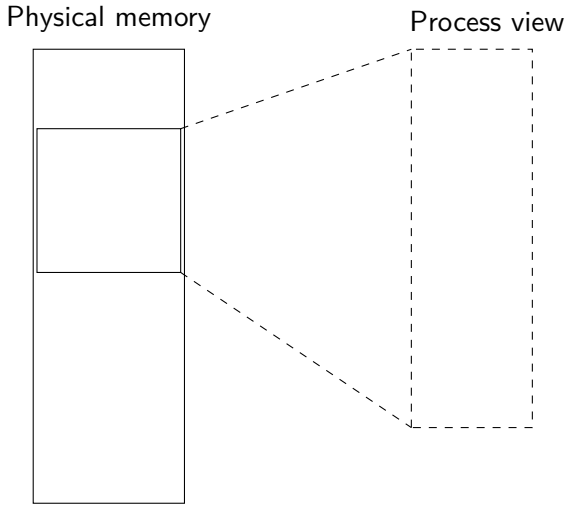

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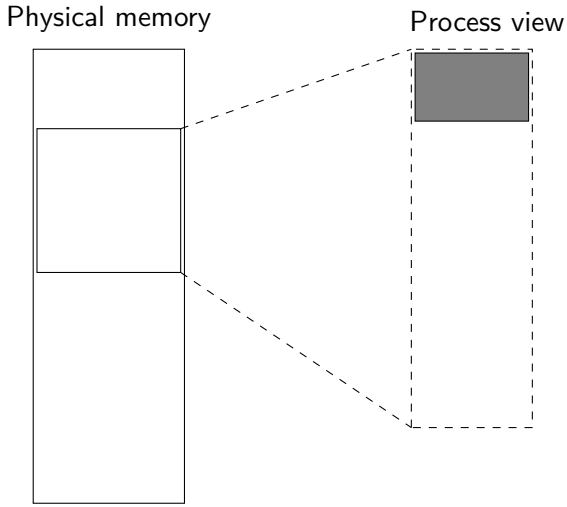

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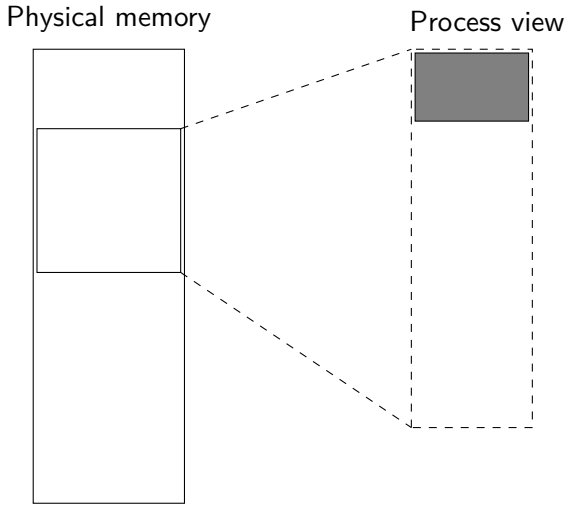

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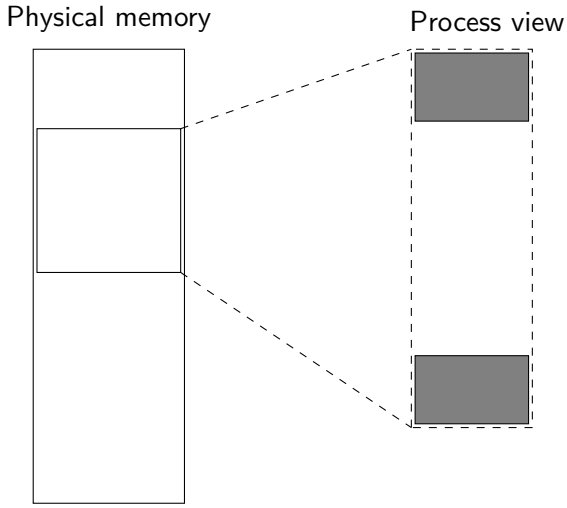

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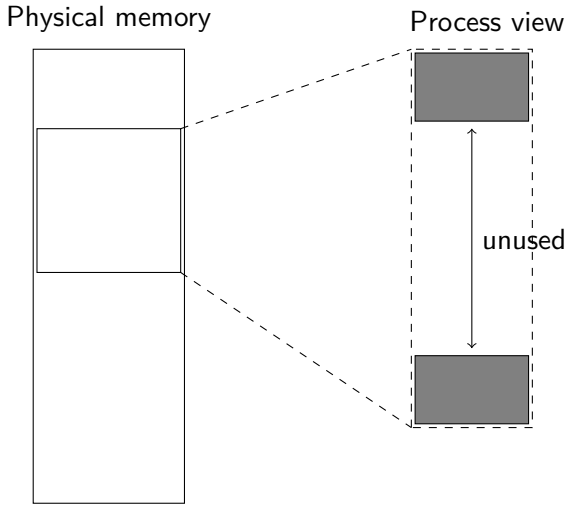

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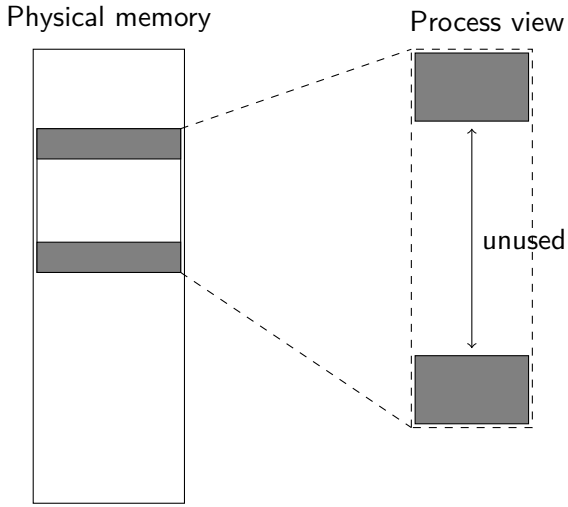

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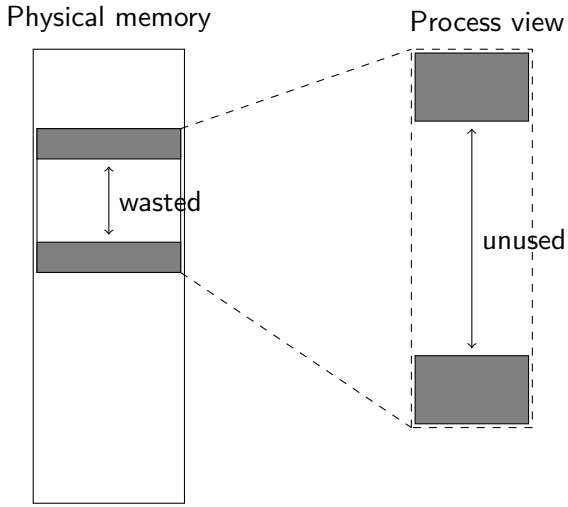

Burroughs B5000

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Burroughs B5000

Donald Knuth was part of the design team.

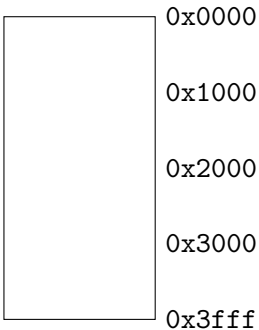
- 1961
- Designed for high-level languages: ALGOL-60
- Memory access through a set of segment *descriptors* i.e. the view of a process is not a consecutive memory rather a set of individual memory segments.

ALGOL 60

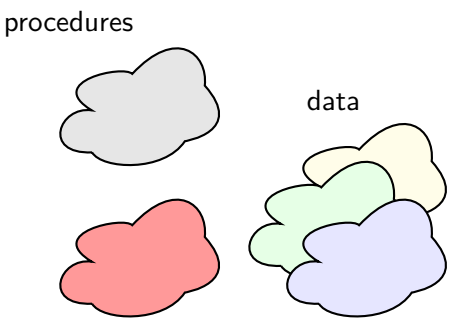
```
procedure Absmax(a) Size:(n, m) Result:(y) Subscripts:(i, k);
    value n, m; array a; integer n, m, i, k; real y;

comment The absolute greatest element of the matrix a ...

begin
    integer p, q;
    y := 0; i := k := 1;
    for p := 1 step 1 until n do
        for q := 1 step 1 until m do
            if abs(a[p, q]) > y then
                begin y := abs(a[p, q]);
                    i := p; k := q
                end
end Absmax
```

Process view

The view of the assembler programmer.

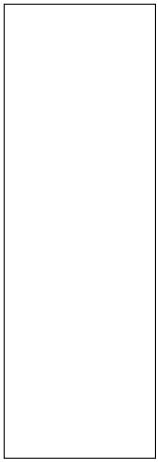


The view of the ALGOL programmer.



Segmented architecture

Physical memory



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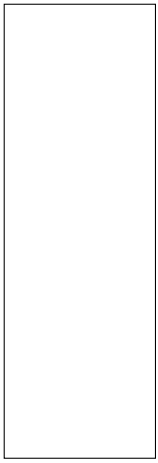

Process A

Segmented architecture

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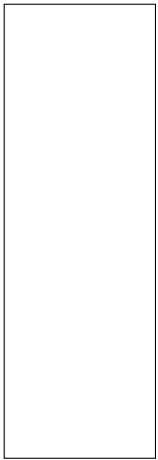

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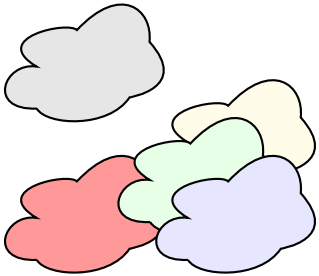

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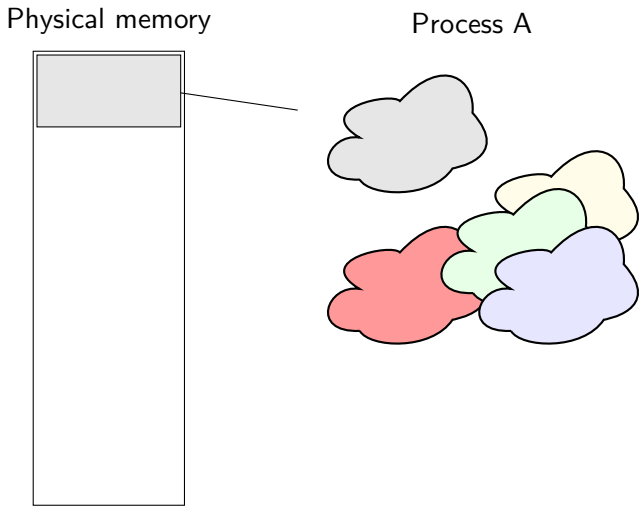

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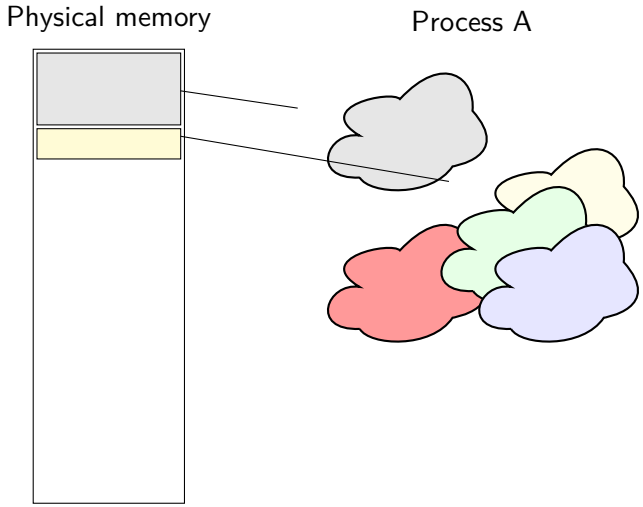

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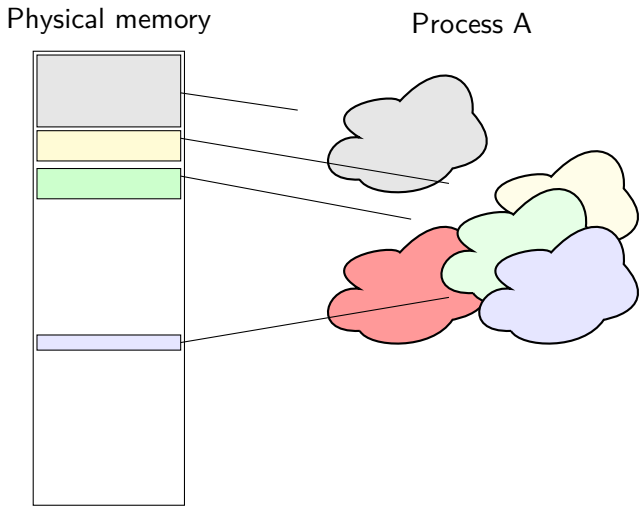

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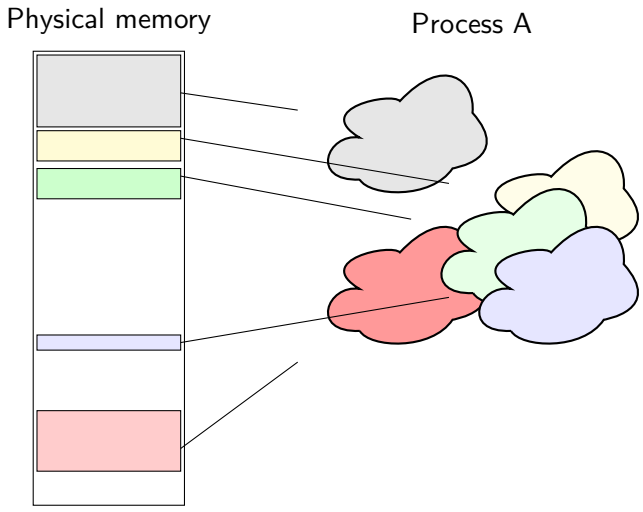

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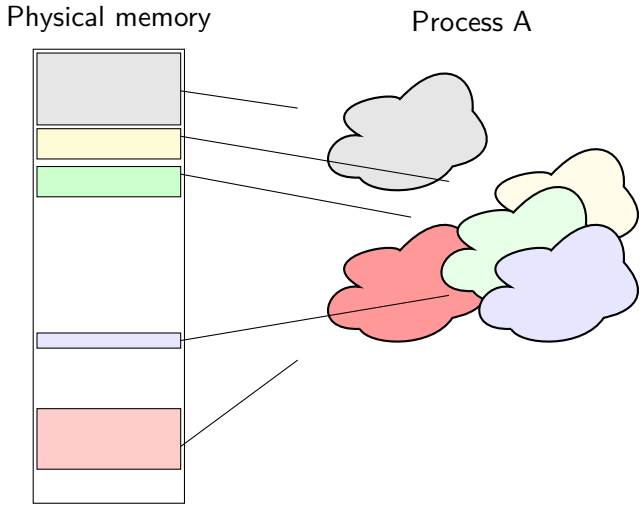

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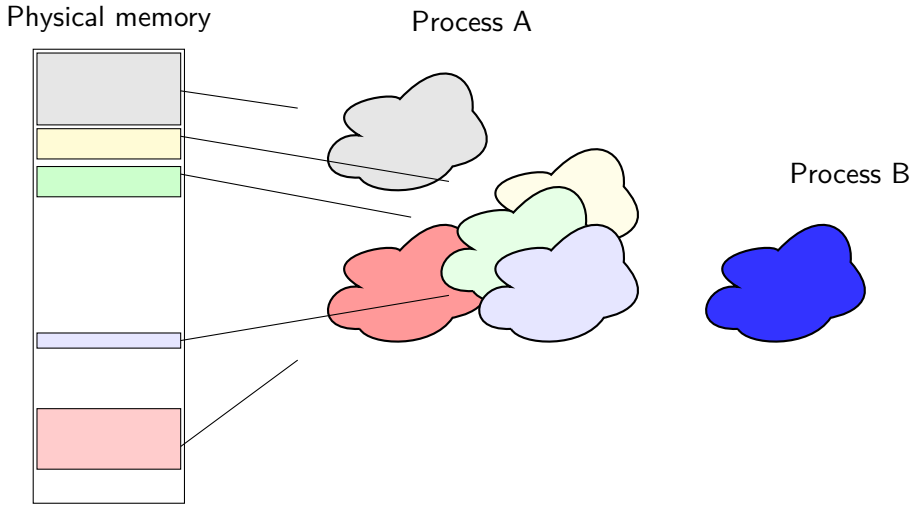

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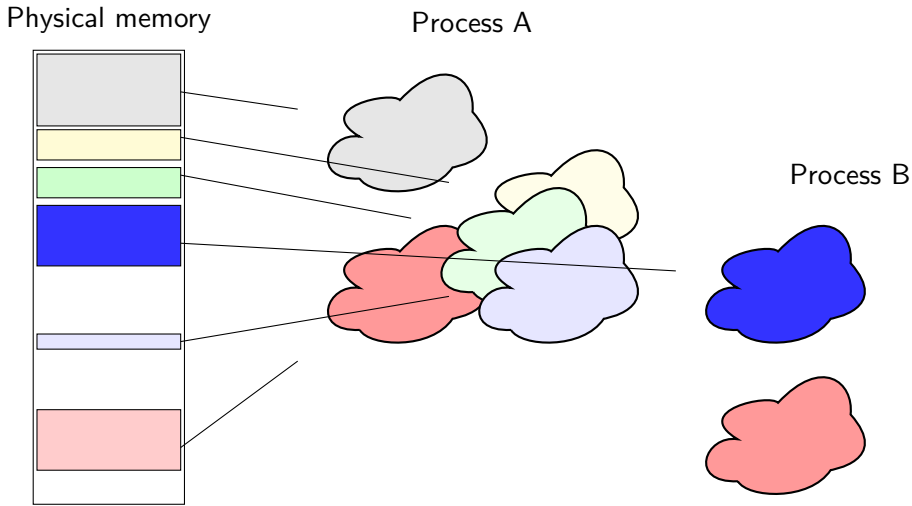
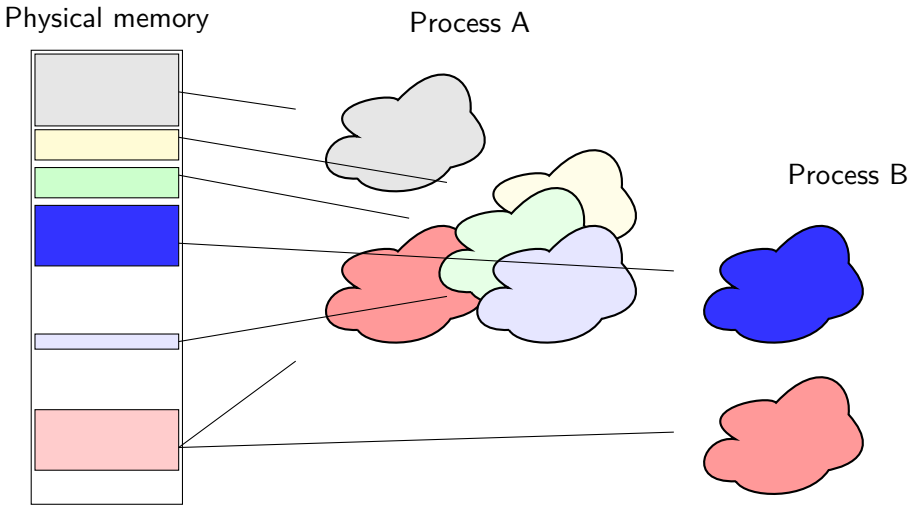


Segmented architecture



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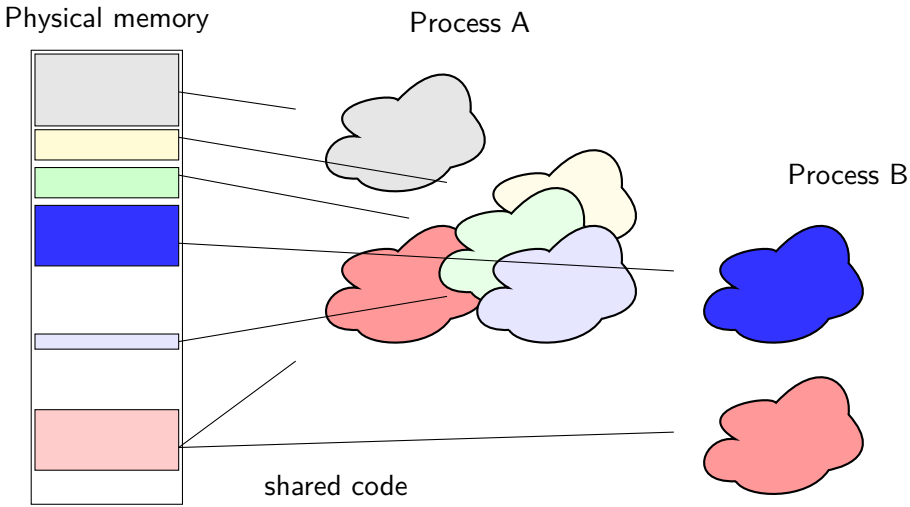
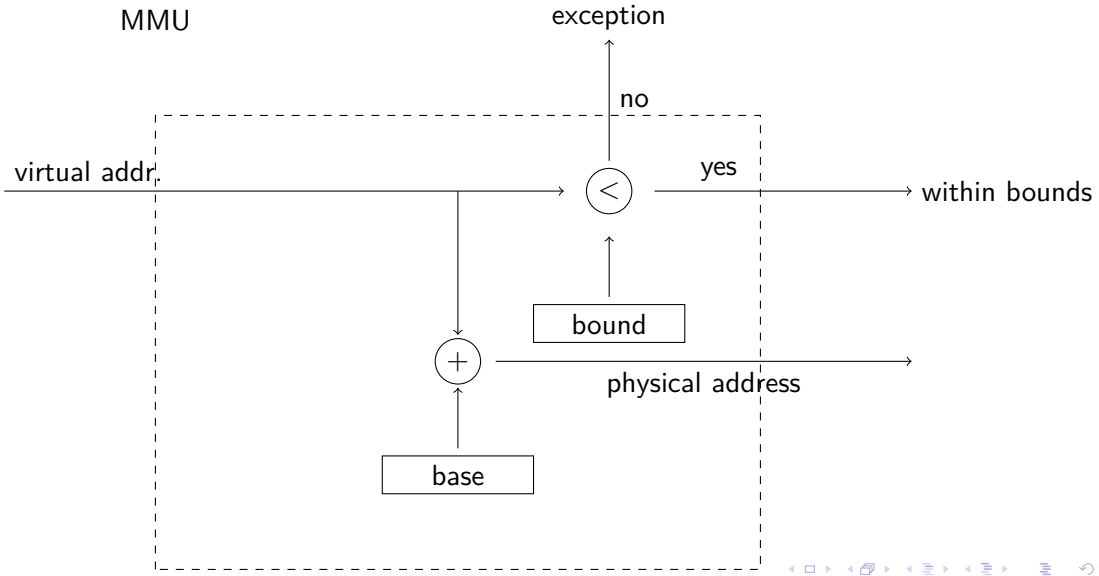


Segmented MMU



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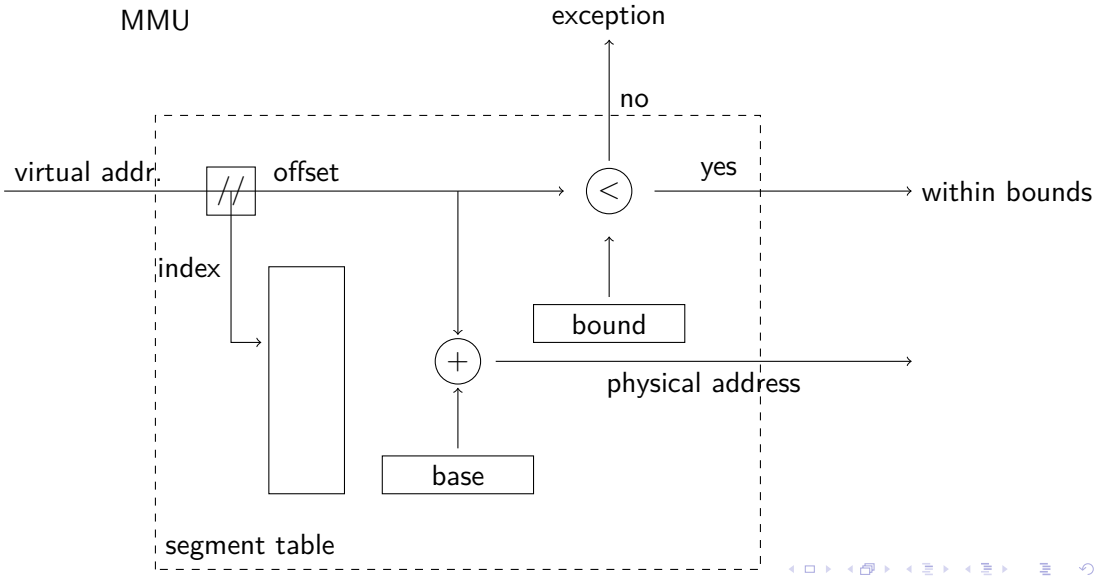

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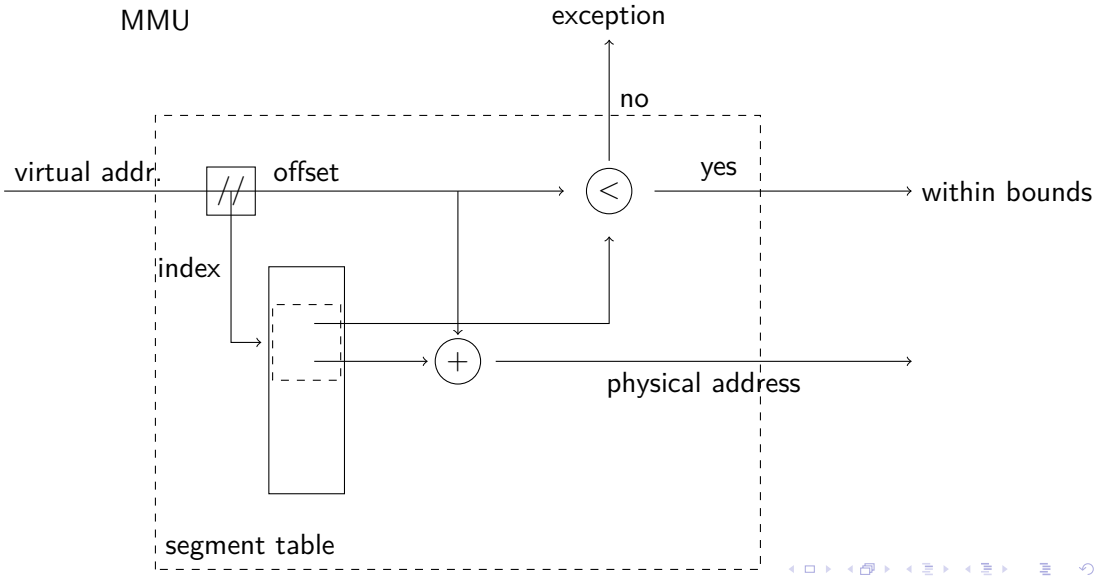
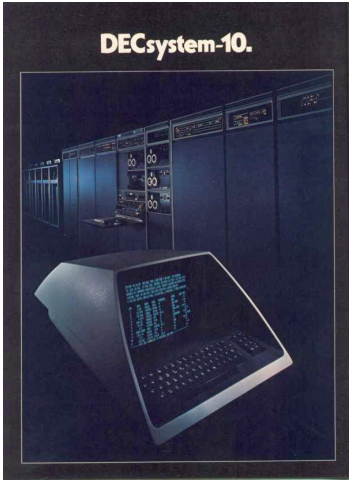


DECsystem10

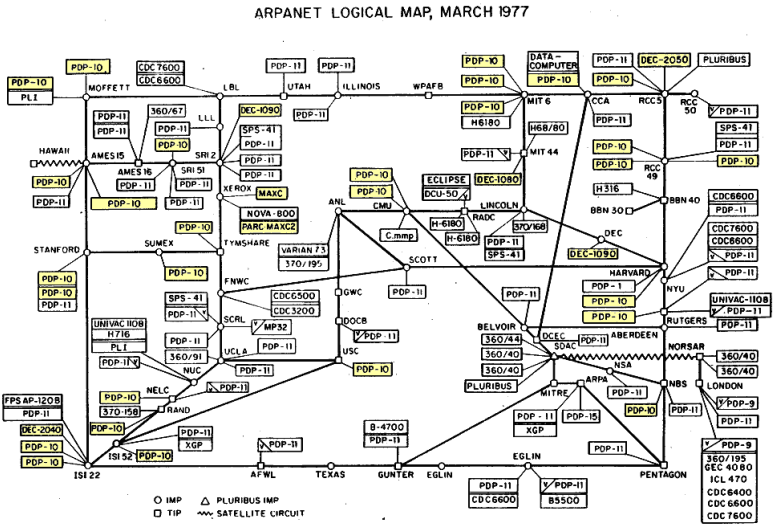


PDP-10

- 1966, 1 MHz
- 36 bit words
- 16 bit process address space (64Kword)
- 18 bit physical address (256 Kword)
- base and bound

The PDP10 had two segments per process, one read only code segment and one read/write for data.

ARPANET 1977



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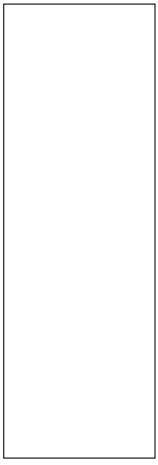

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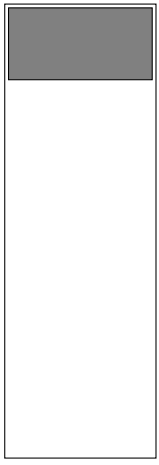

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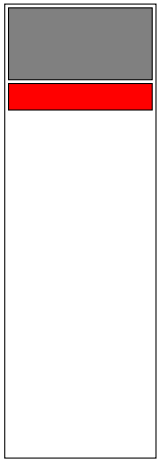

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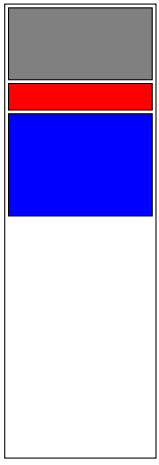

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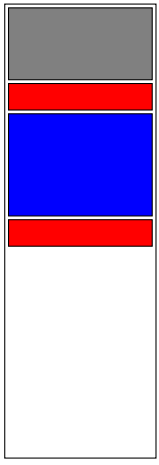

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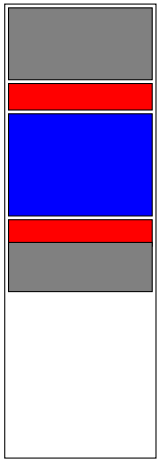

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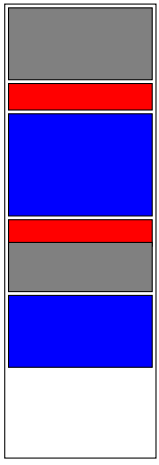

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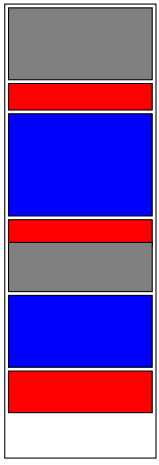

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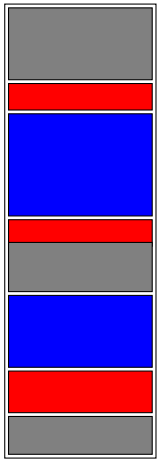

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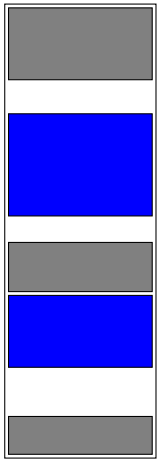

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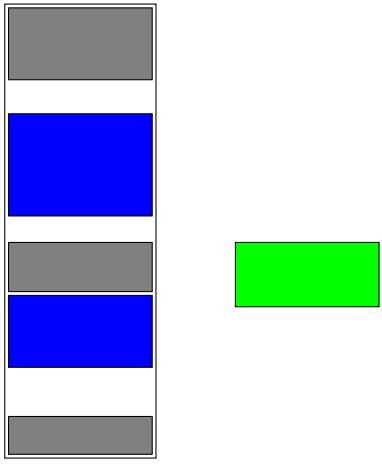

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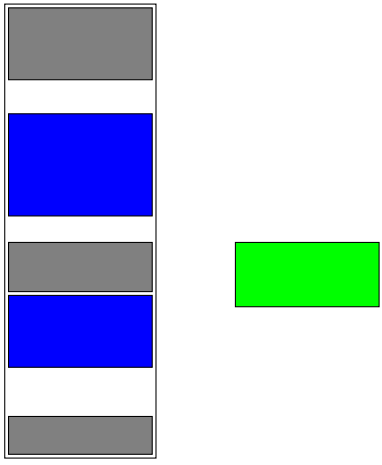

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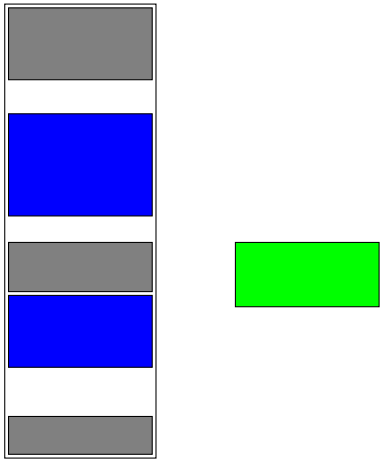

Is it possible to do compaction?

large grain vs fine grain segments

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Using few large segments is easier to implement.

large grain vs fine grain segments

Using few large segments is easier to implement.

Using many small segments would allow the compiler and operating system to do a better job.

The Altair 8800

Intel 8080

- 1972
- 2 MHz
- 16 bit address space (64 Kbyte)

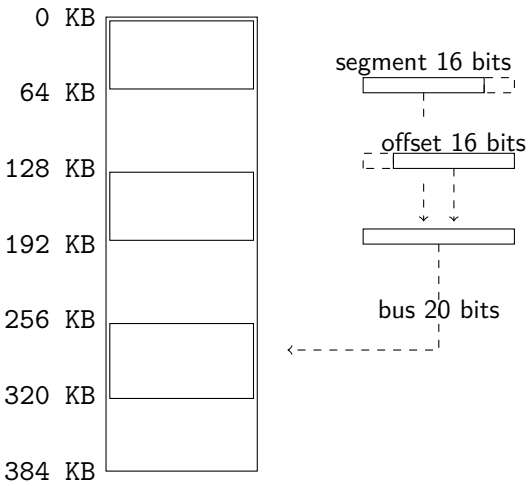
Altair 8800 would have 4 or 8 Kbytes of memory.

The workhorse: 8086

Intel 8086

- 1978, 5 MHz
- 16 bit address space (64 Kbyte)
- 20 bit memory bus (1 Mbyte)
- no protection of segments
- segments for: code, data, stack, extra

Segment addressing in 8086 - real mode



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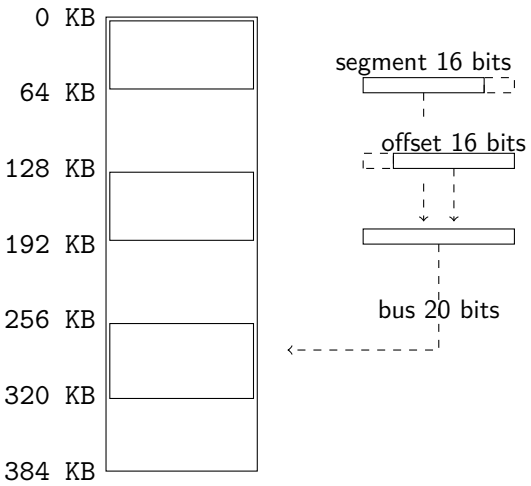

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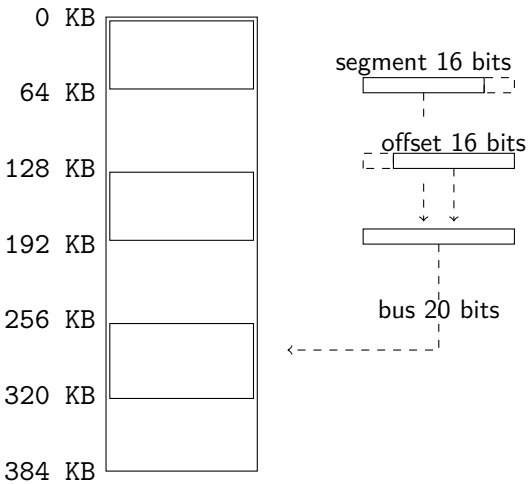
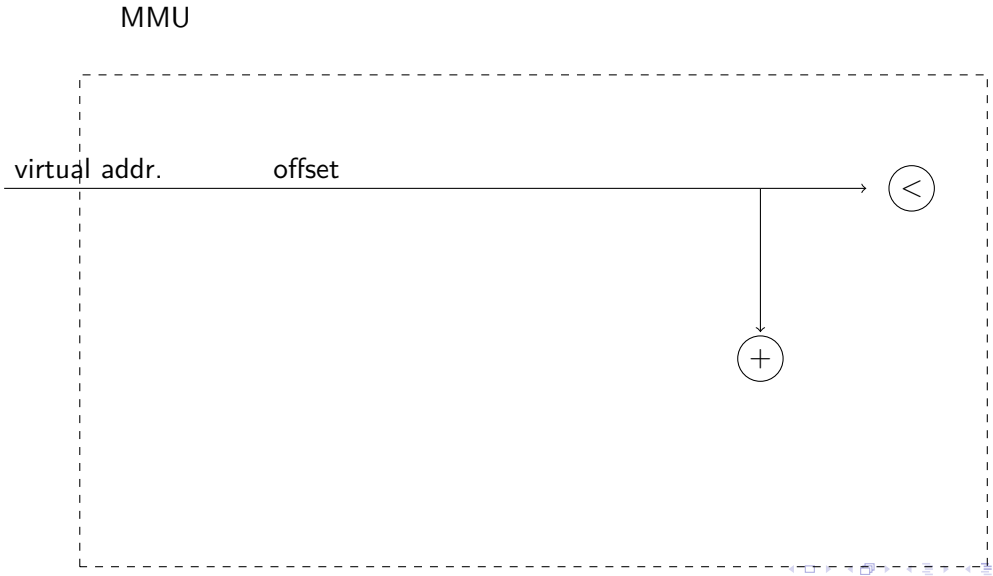


- Segment register chosen based on instruction: *code segment*, *stack segment*, *data segment* (and the *extra segment*.
- The segment architecture available still today in *real mode* i.e. the 16-bit mode that the CPU is initally in.

Segment addressing in 80386 - protected mode



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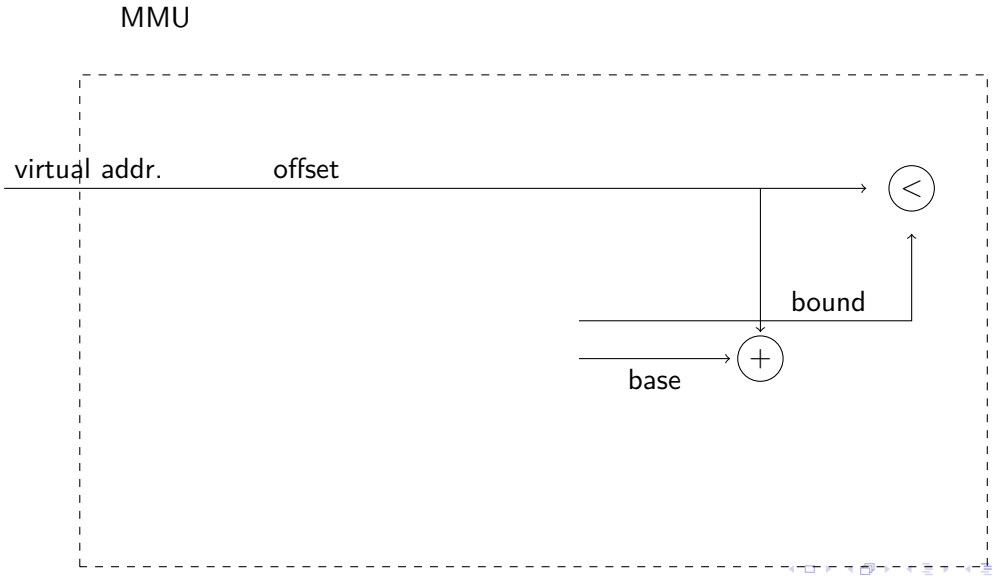

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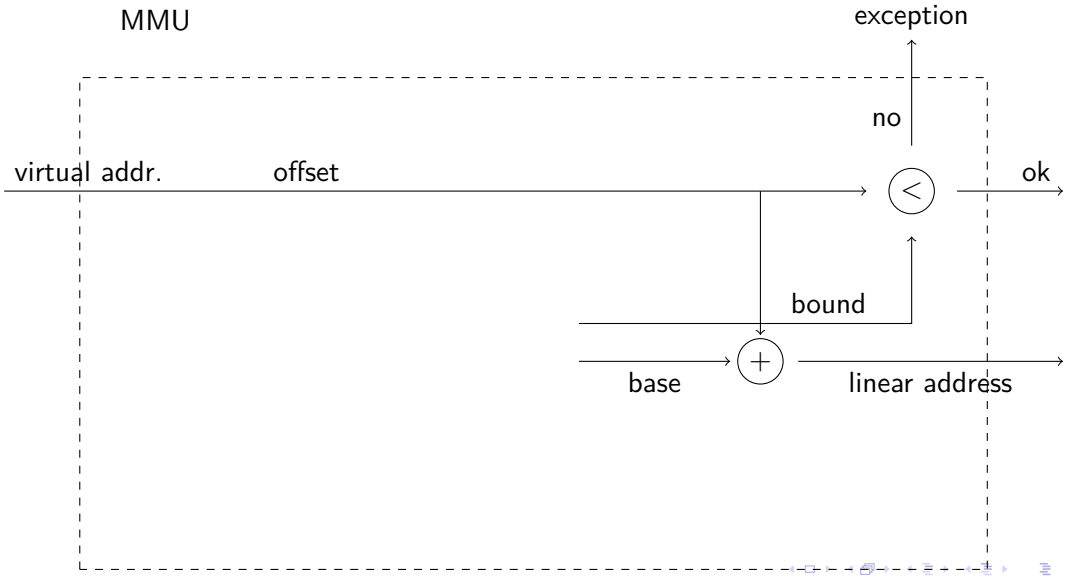

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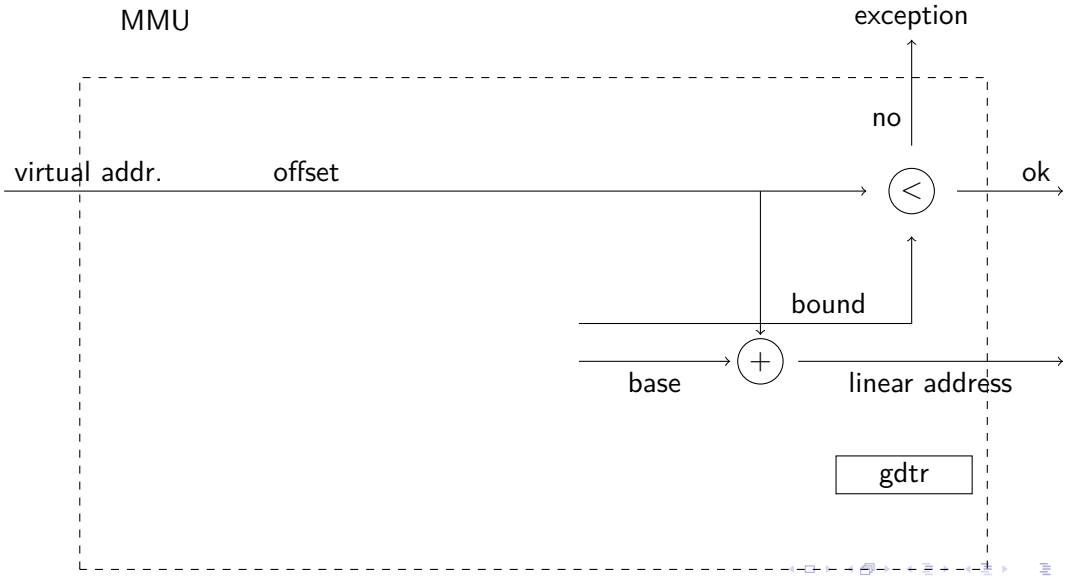

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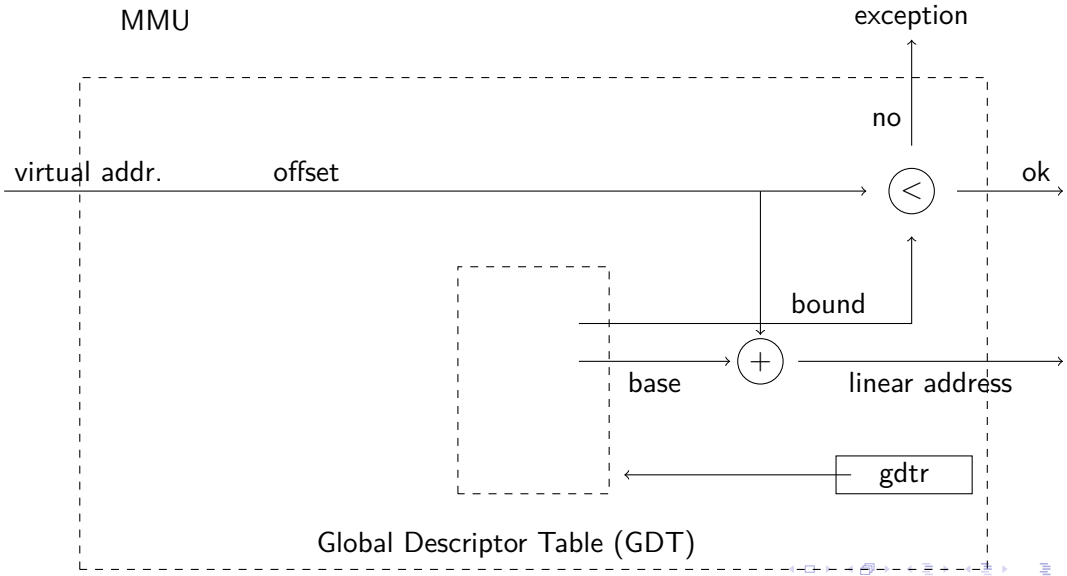

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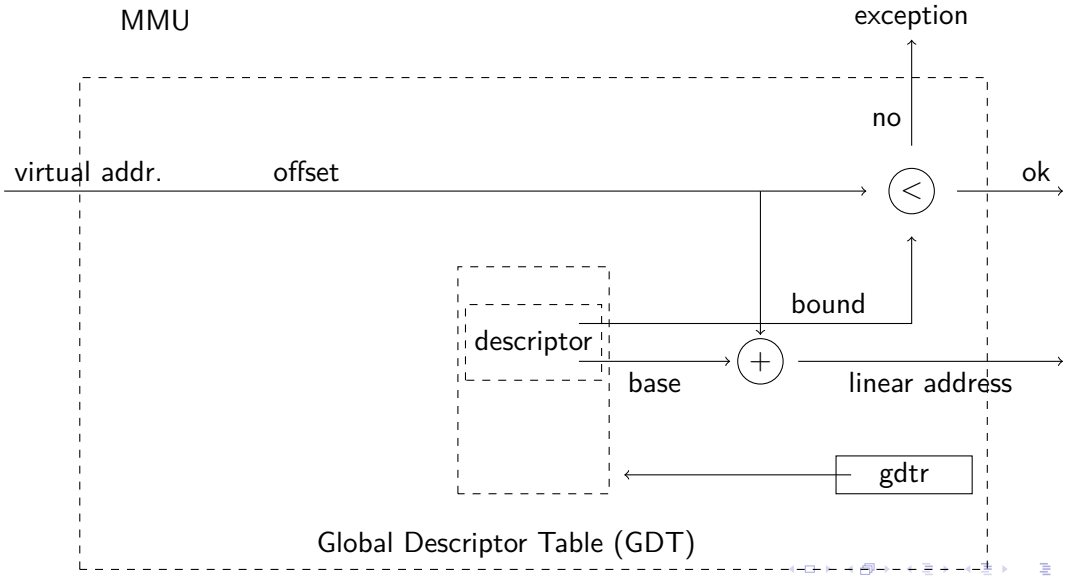

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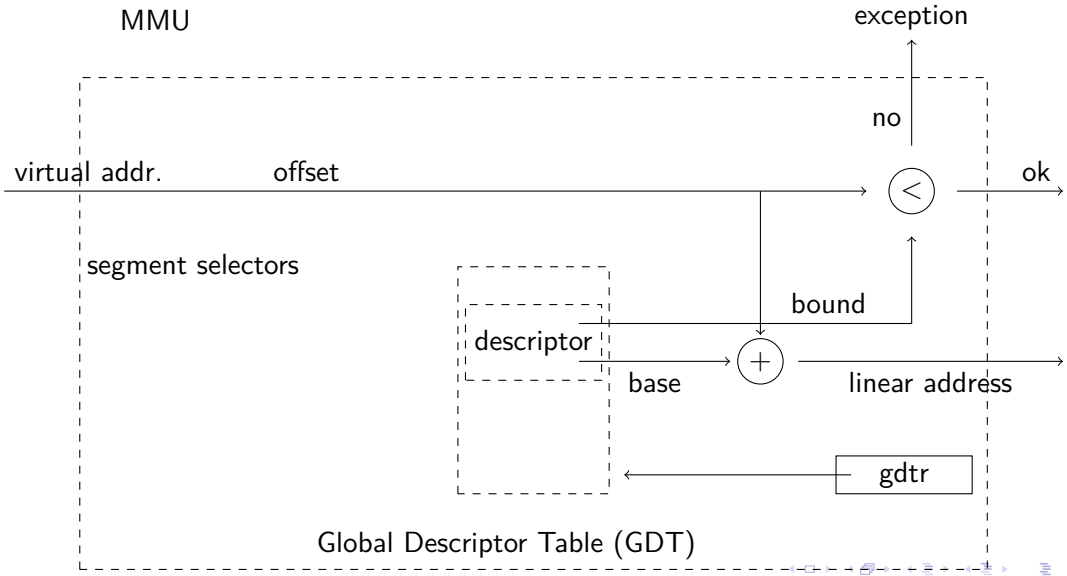

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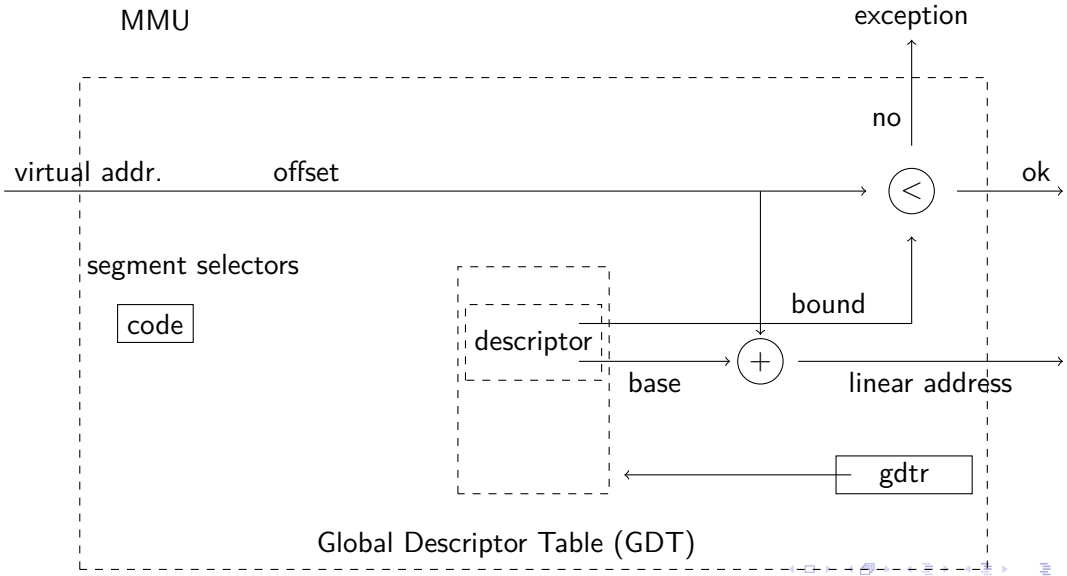

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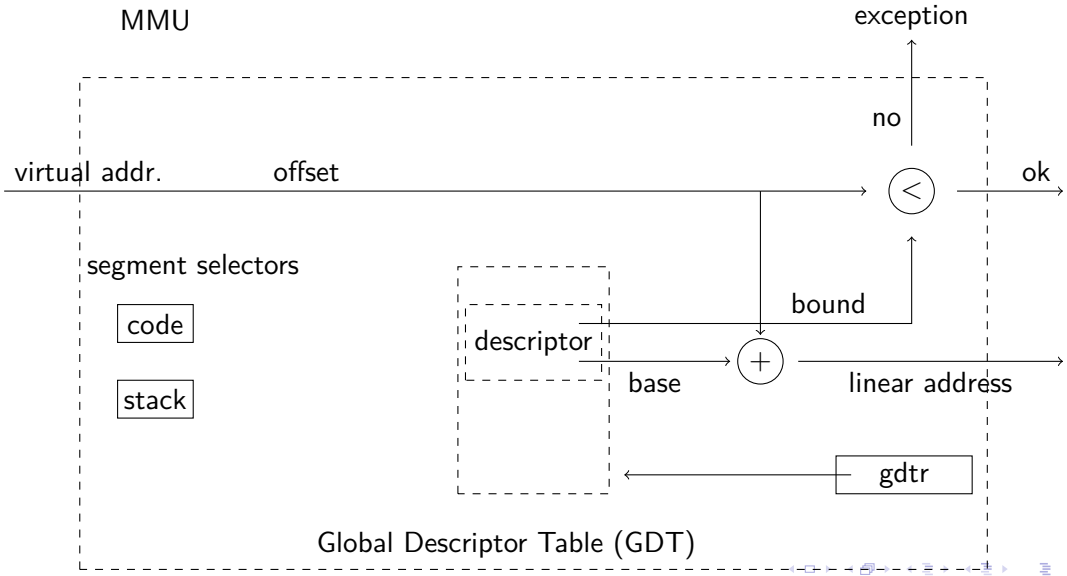

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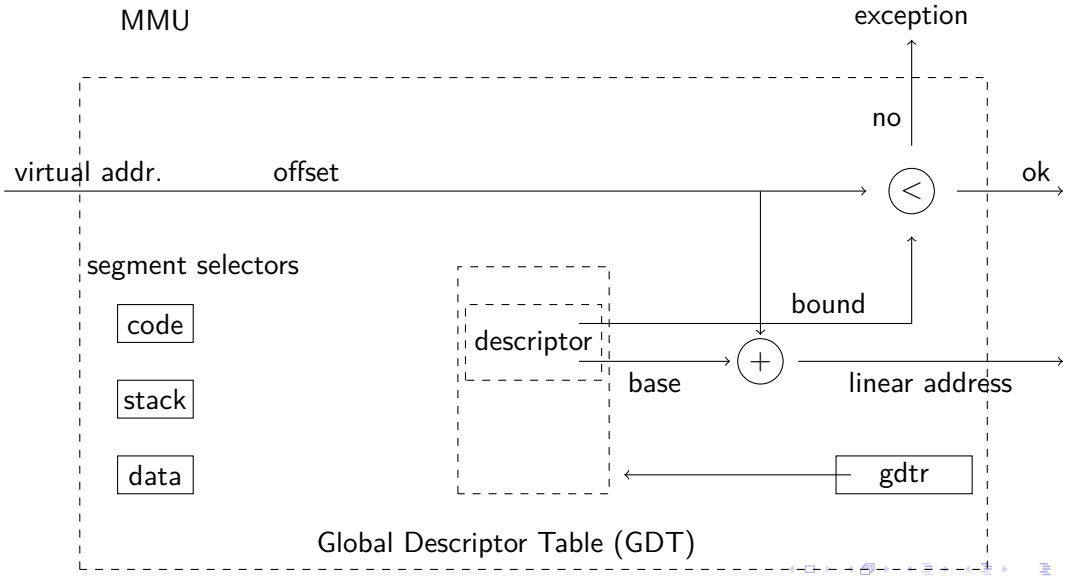

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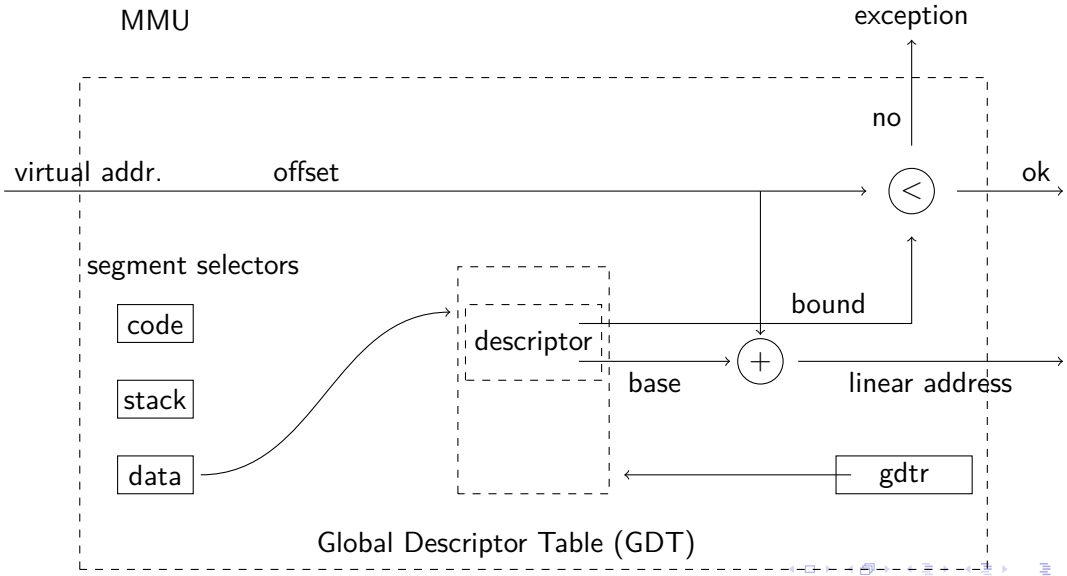

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- Segmentation is still used to refere to memory that belongs to a *specific core* or to *thread specific memory*.

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Cliffhanger - paging, the solution.