Corso di Laurea Magistrale in Ingegneria Informatica

Tesi di laurea

Implementation and synthesis of algorithms parallelization in ASIC

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In the last decades we have seen the computational time of processors been reduced more and more.
Can we do better?
The answer is ASIC. An ASIC (application-specific integrated circuit) is an integrated circuit (IC) customized for a particular use, rather than intended for general-purpose use. This thesis presents efficient implementation of various algorithms in ASIC exploiting the parallelization and computing optimization whenever possible. The goal is to compute using the ASAP (As Soon As Possible) approach and, therefore, also to present a pareto efficiency.

We have choosen a set of algorithms used for image processing, filter and image compression.

- **Summed area Table**: is an algorithm for quickly and efficiently generating the sum of values in a rectangular subset of a grid.
- **Discrete Cosine Transform**: a finite sequence of data points in terms of a sum of cosine functions oscillating at different frequencies.

- **Binomial Filter**: is a smoothing filters used to enhance noisy images (at the expense of blurring).
- **Finite impulse Response**: is a filter structure that can be used to implement almost any sort of frequency response digitally.
- **Transport equation problem**: it describes physical phenomena where particles, energy, or other physical quantities are transferred inside a physical system

This thesis work has also another funtion: been used to be compared with emergent and modern general purpose multi-core processors. In particular we will do some comparison on the Logic-In-Memory architecture and the systolic array architecture regarding the clock cycles required and the number of resources used.
The Logic-In-Memory architecture is a general purpose processor where logic and memory are embedded in a unique entity. These entities are interconnected together to allows the exchanging of data among different units. The systolic array architecture is made of arrays of processors which are connected to a small number of nearest neighbours in a mesh-like topology. Processors perform a sequence of operations on data that flows between them.

Least but not last, we will do some analysis with the experimental Thessa tool that generate a parallel code that can be used to program the LIM.