Microelectronic Systems

DLX PROJECT

2015/2016

Overview

TOP-DOWN design of DLX – RISC processor

- RTL VHDL / SIMULATION
- BENCHMARKING
- SYNTHESIS / PHYSICAL DESING
- **DOCUMENTATION**

A) Two possible versions:

- DLX-basic (max project eval 28/30)
- DLX-pro (max project eval. 33/30)

B)

C) MANDATORY: all design files + **commented** benchmark + **DETTAILED REPORT**

D)

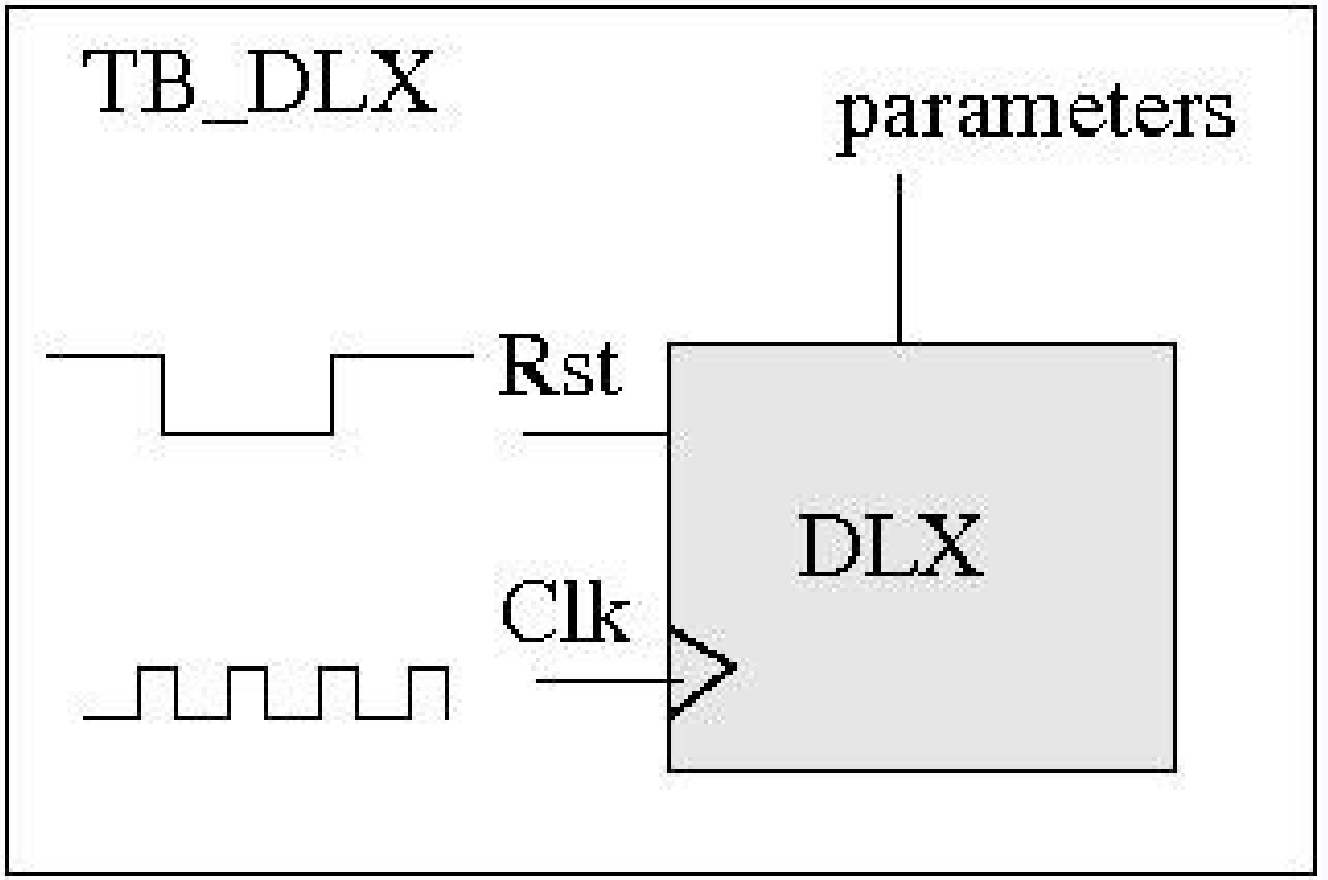
E) Deadline: suggested **July 31th**, Max: October 30th

Project setup and description

- A file will be available MS-DLX.zip containing
  1) The DLX_Project.pdf file with:
     1) Specification of DLX and Documentation
     2) Instructions on how to set-up the tools
     3) Deployment and documentation guideline
  2) This presentation: DLX_Project_15-16.pdf
  3) Some VHDL files and utilities in the folder: DLX.project/
  - A short manual on how to use the new TestBench: DLX_TestBench.pdf

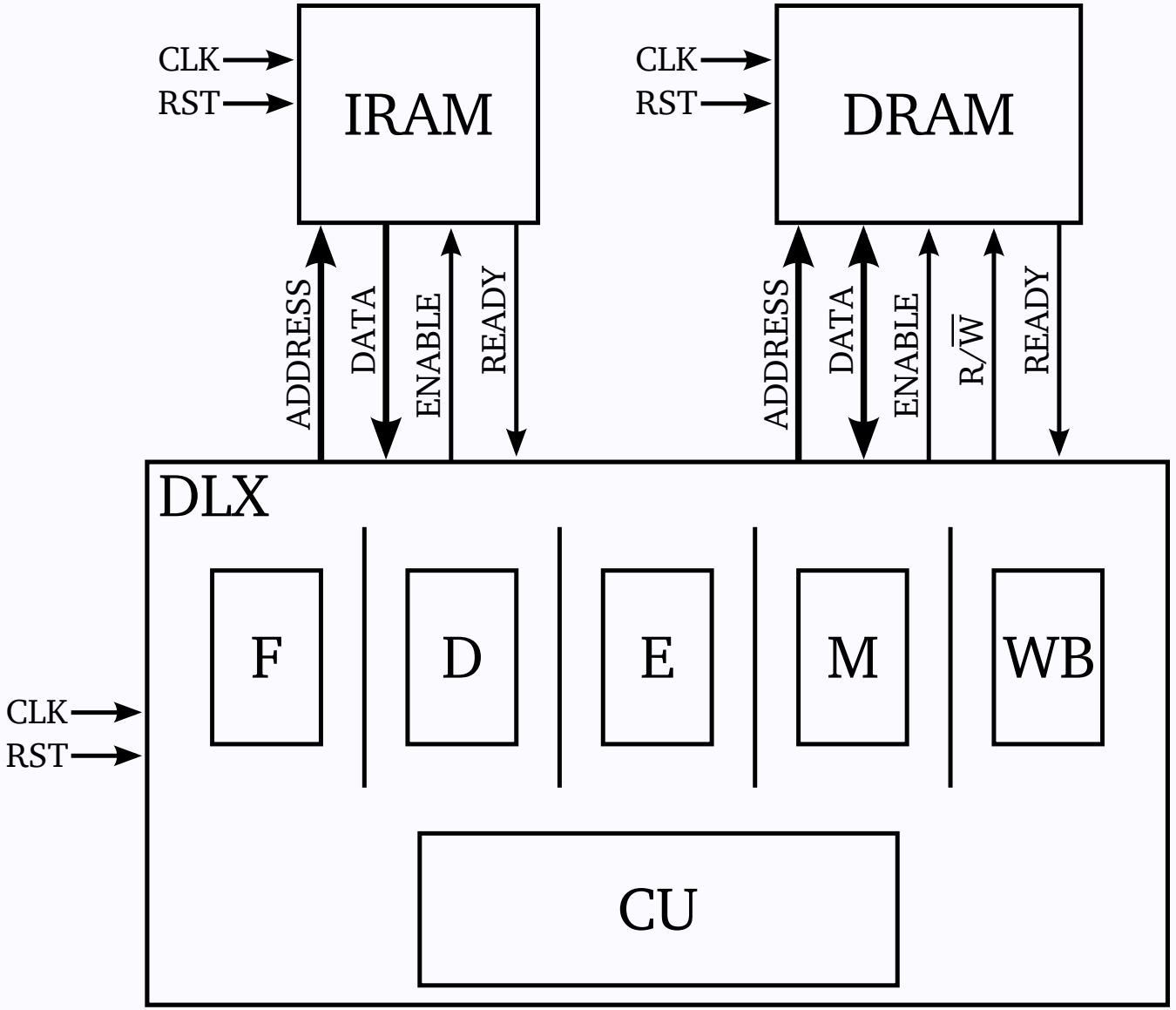
DLX PJ structure

- TEST BENCH: TB_TOP_DLX.vhd (given) OLD TestBench



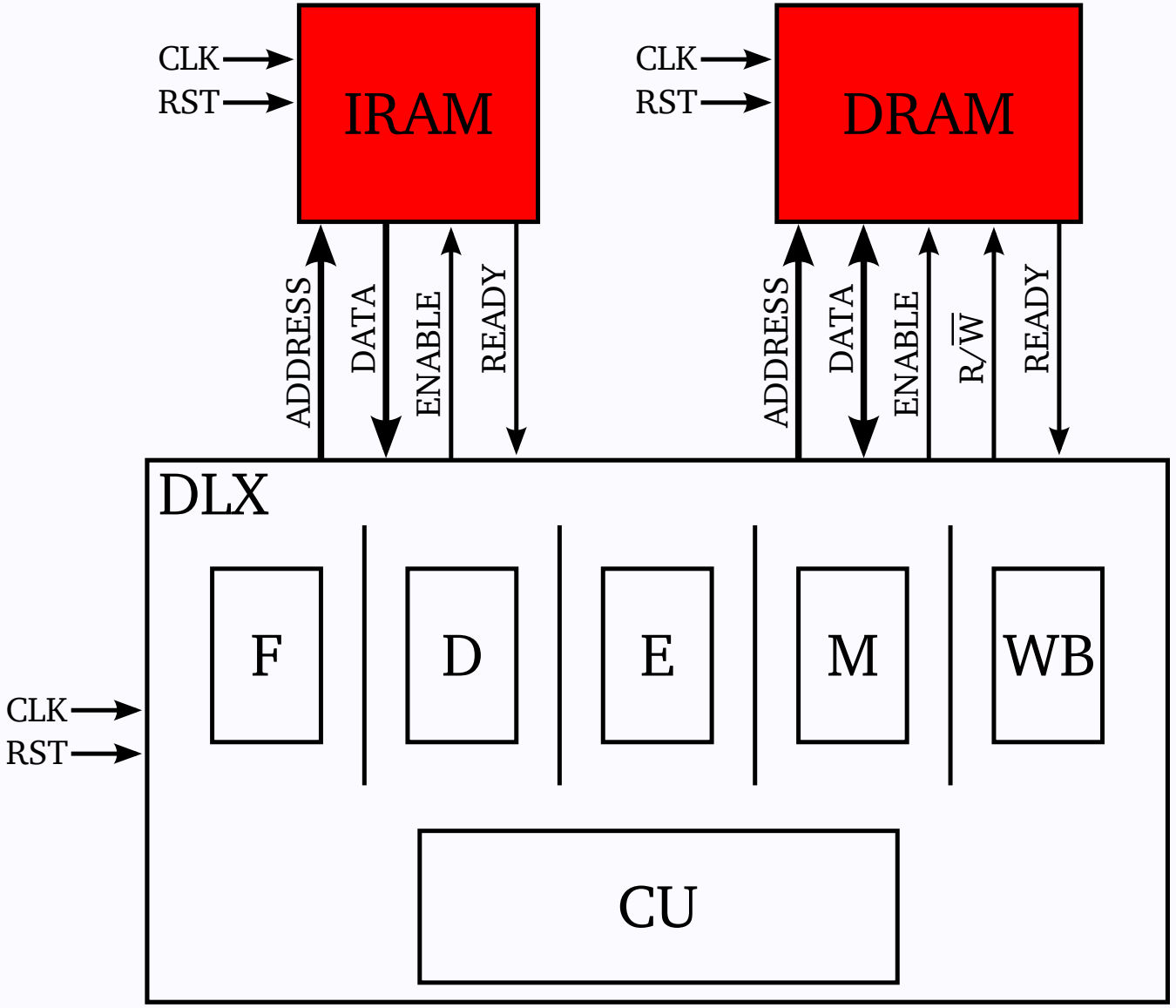
DLX PJ structure

- DLX top: DLX.vhd (given but to be completed)



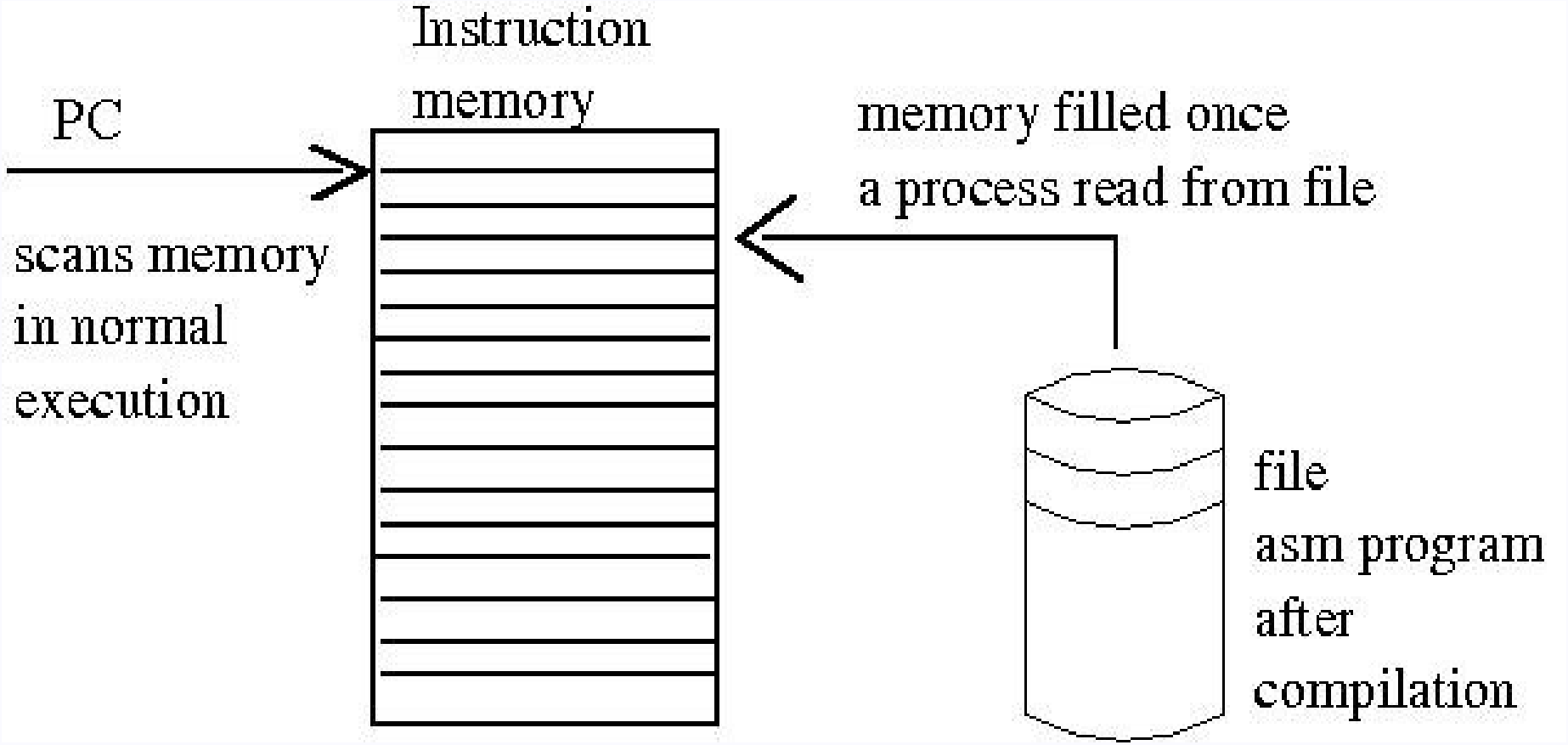
DLX PJ structure

- DLX top: DLX.vhd (given but to be completed)



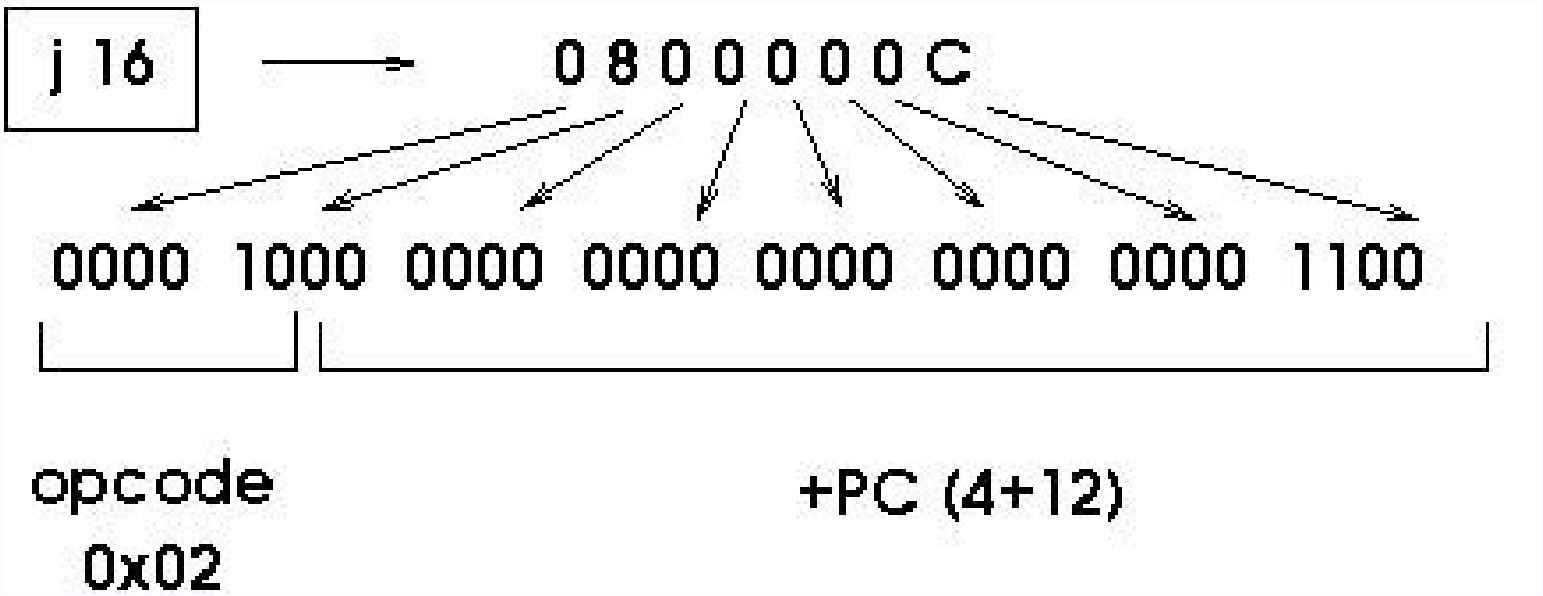
DLX PJ structure

- Input ASM programs: simple compiler given



DLX PJ ASM

Your program		for IRAM
j 16	compiler →	0800000c
add r1,r2,r3		00430820
addi r1,r2,#5		20410005
beqz 32		1040fff0



DLX Fully Synthesizable

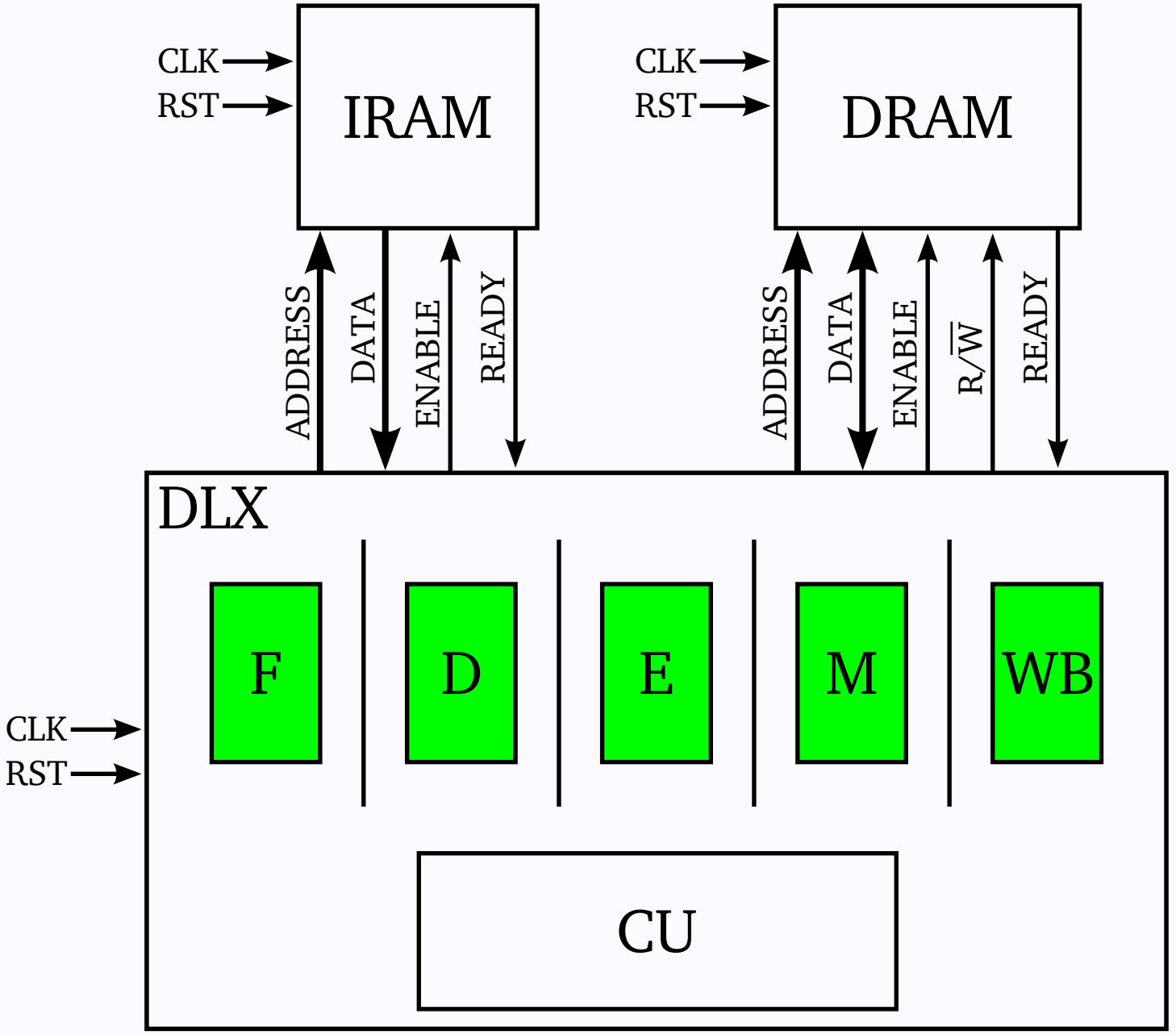
- IRAM is not synthesizable
- In order to obtain a more realistic DLX DRAM and IRAM should be moved in the testbench.
- In folder DLX_vhd_fully_synthesizable there is a complex version with the tho memory already placed in the testbench.
- The comunication protocol is summarized in DLX_TestBench.pdf

DLX ASM Instruction Set

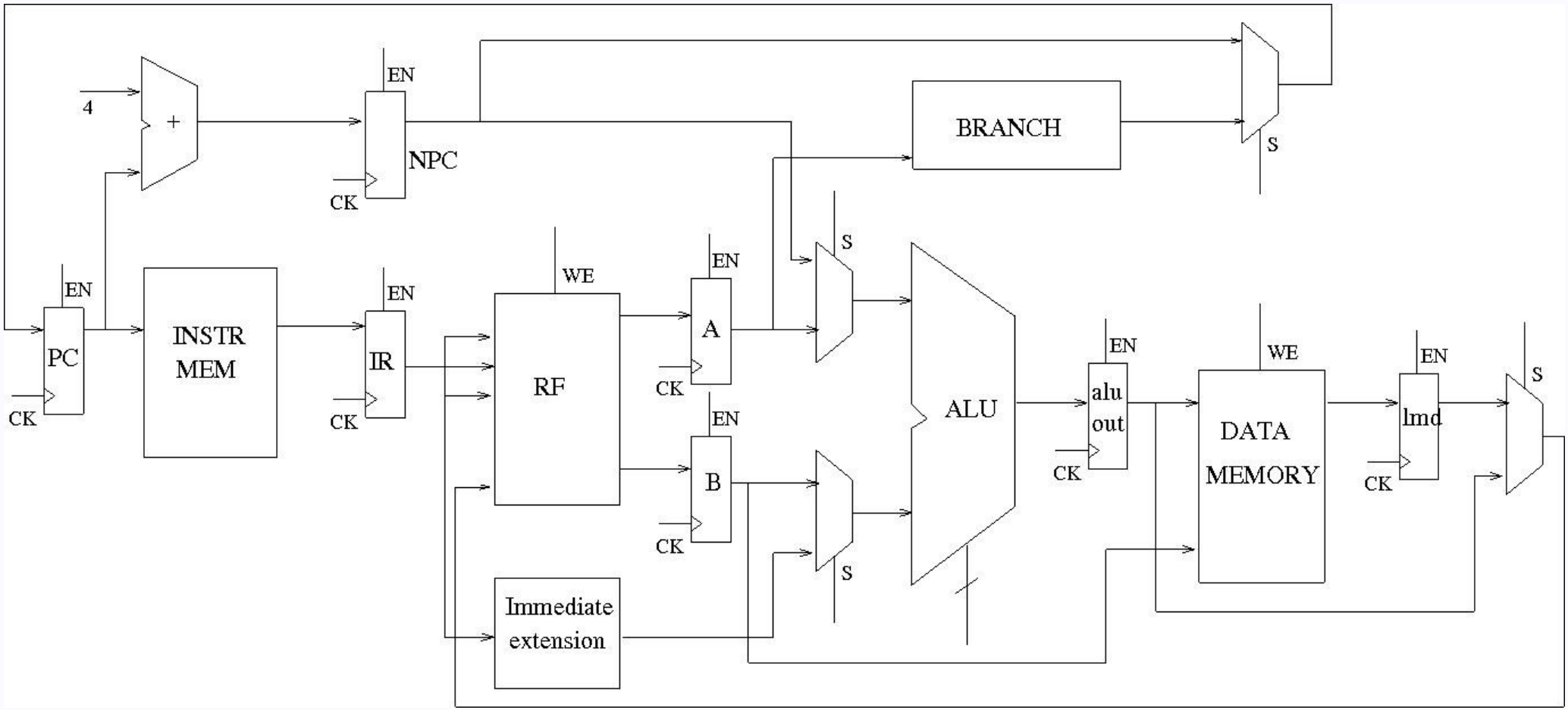
In instruction file DLX_Project.pdf are contained:

- ASM mnemonics and description
- INSTRUCTION SET coding

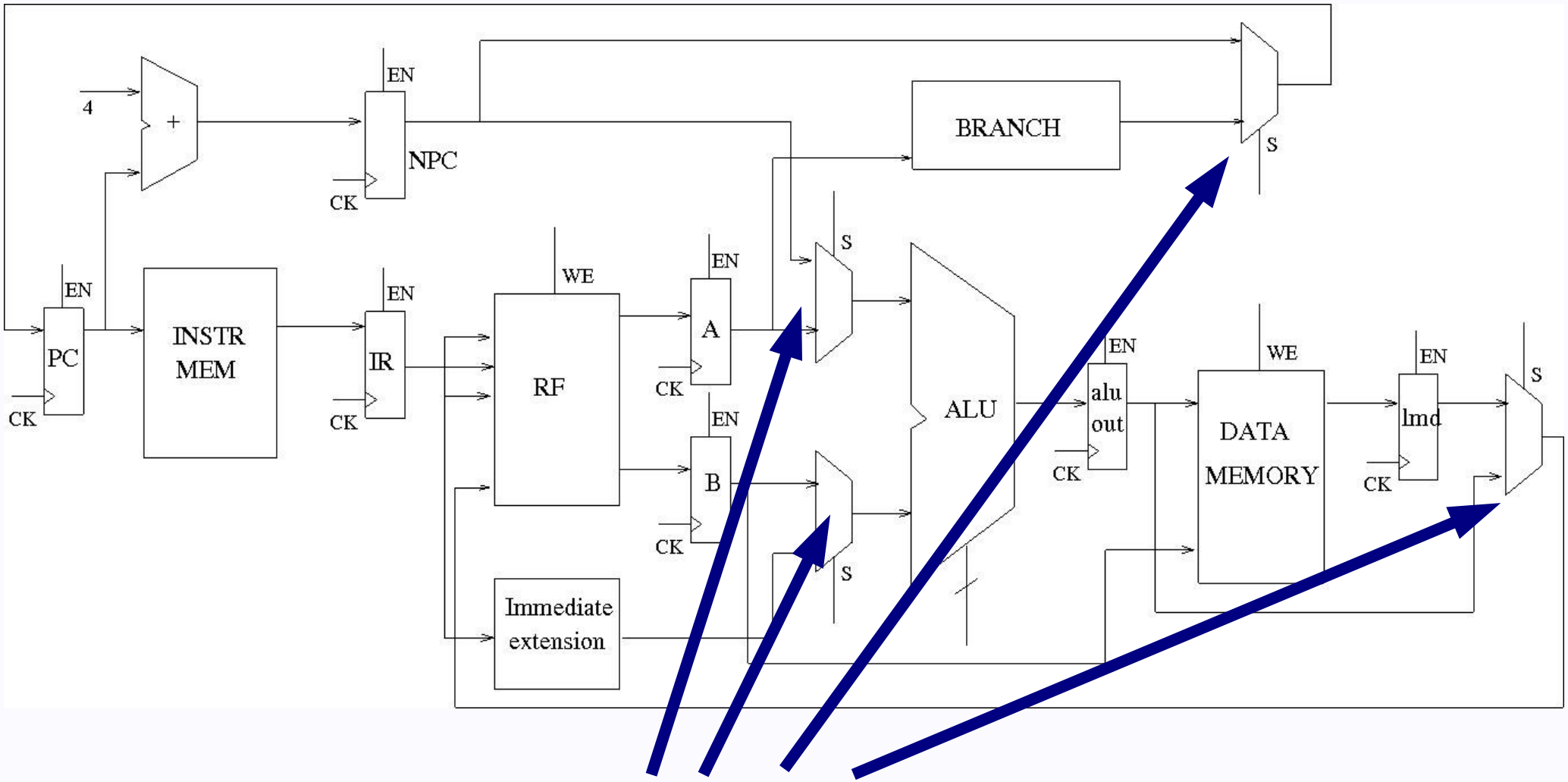
DLX PJ structure again



DLX PJ Data Path

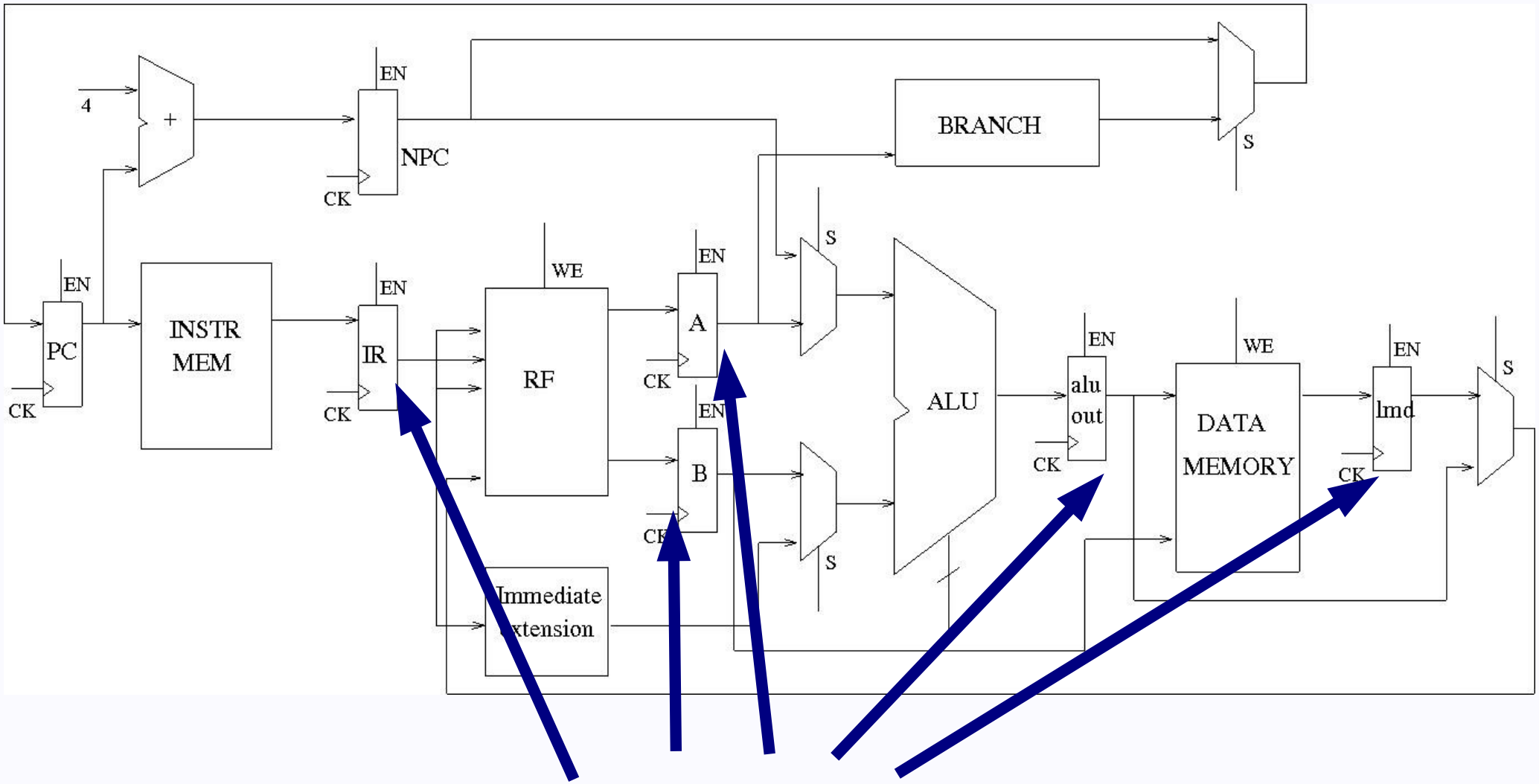


DLX PJ Data Path



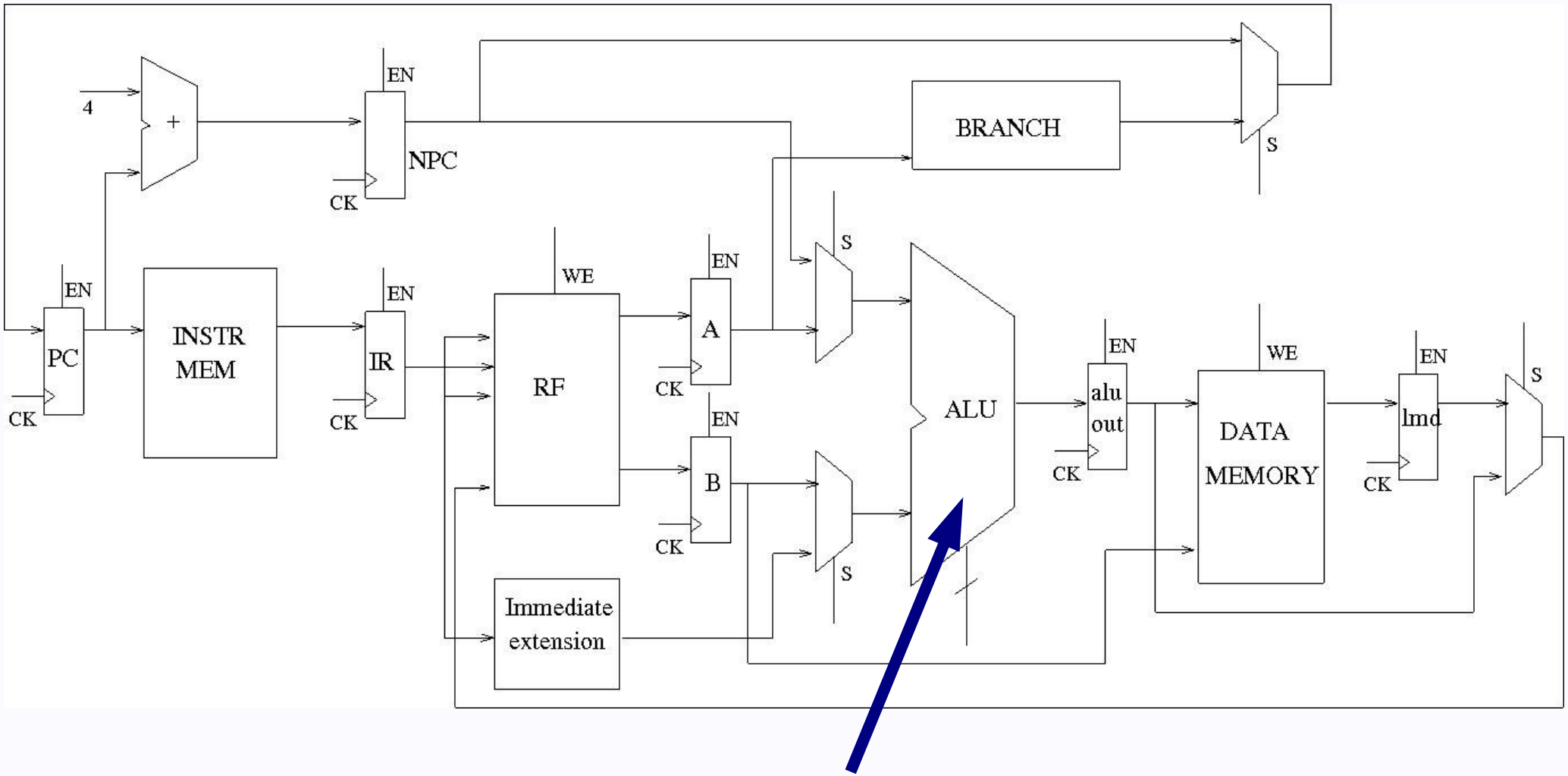
GENERIC MUXES FROM LAB1

DLX PJ Data Path



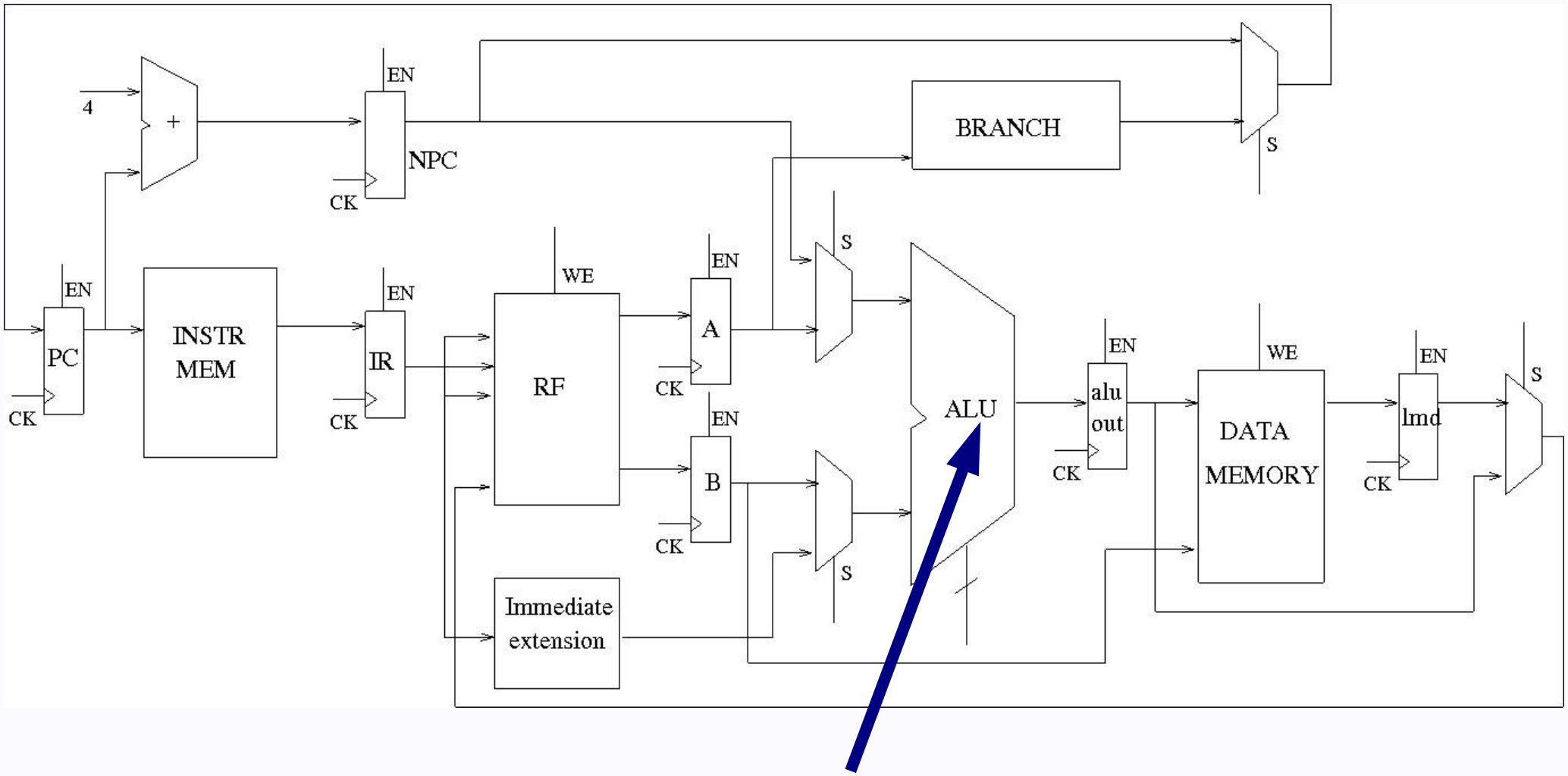
GENERIC REGS FROM LAB1

DLX PJ Data Path



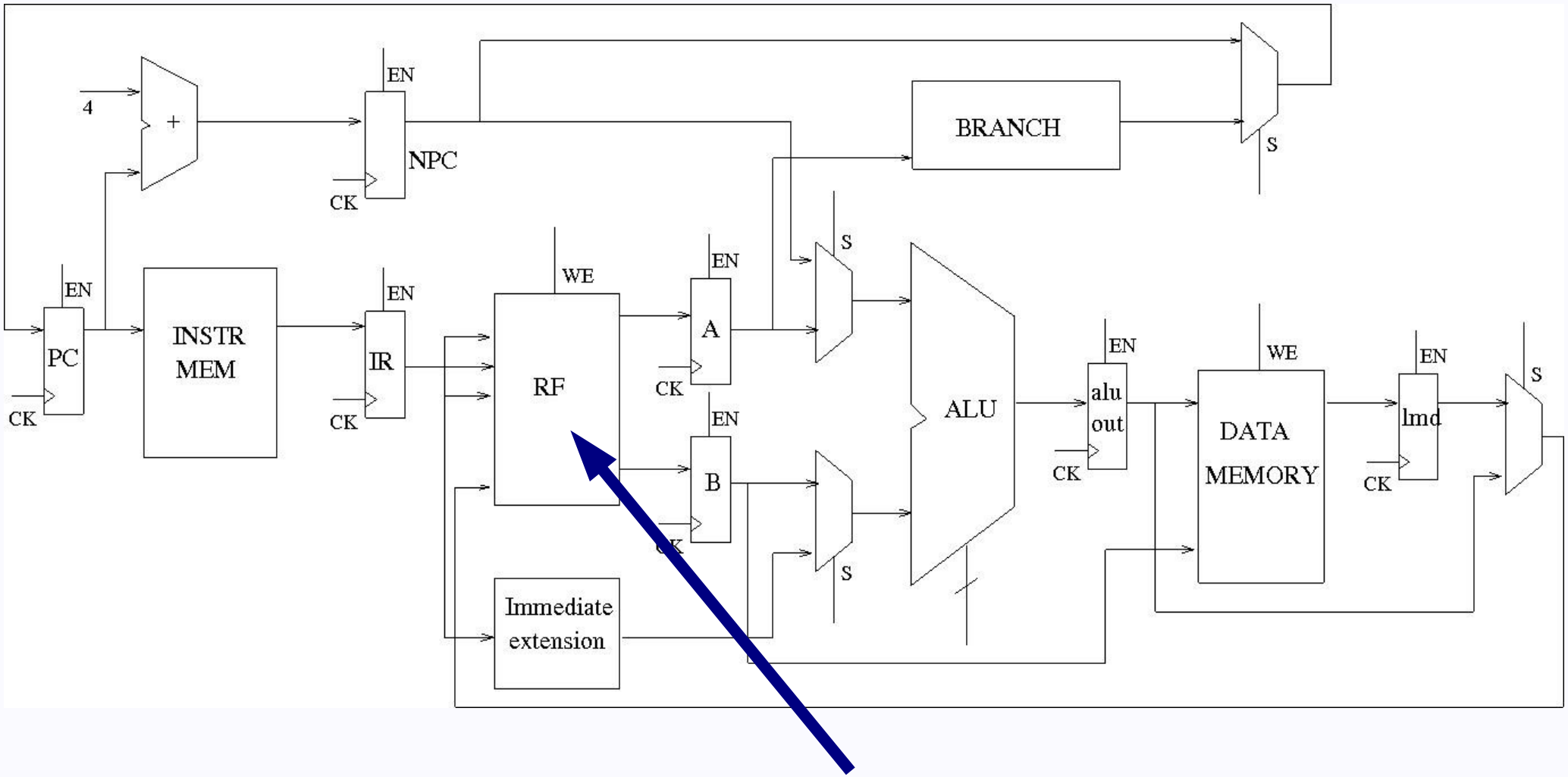
BEHAV ALU FROM LAB1

DLX PJ Data Path



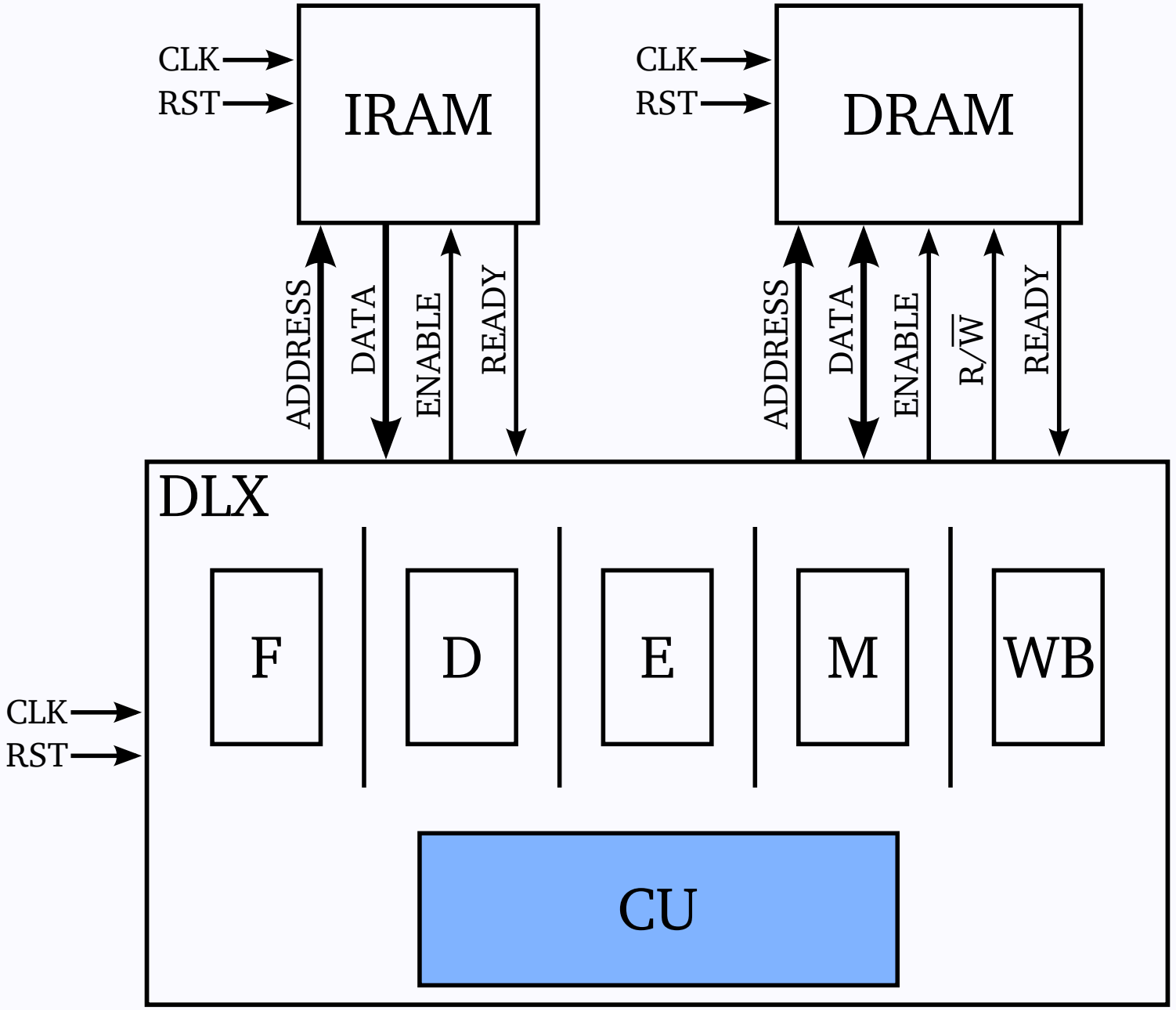
STRUCTURAL ADD, MUL FROM LAB2

DLX PJ Data Path

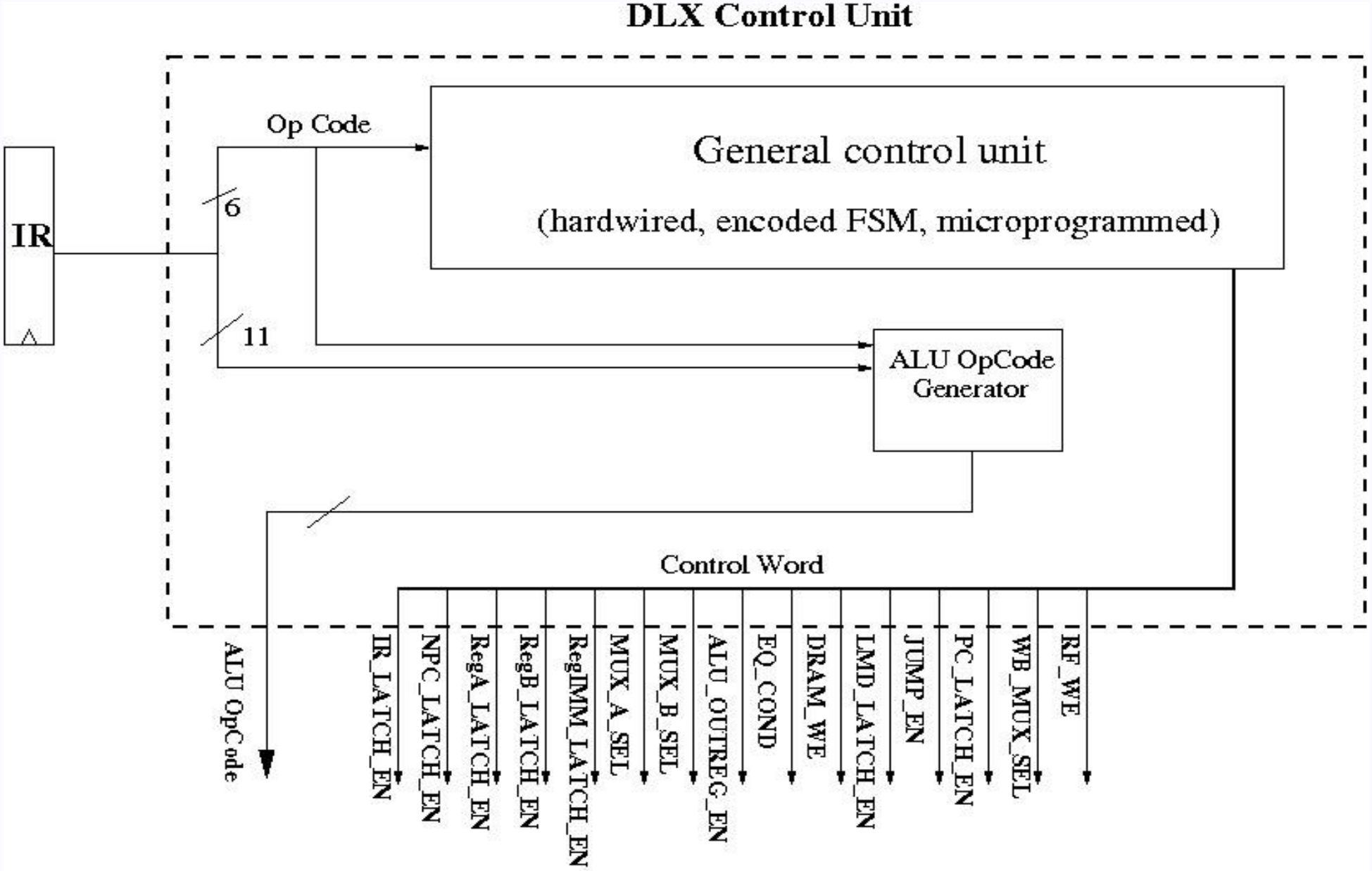


REGISTER FILE (and memory) FROM LAB3

DLX PJ structure again



DLX PJ control unit: box given CU.vhd



DLX Control Unit: implemented in CU.vhd

Can be implemented in three possible versions (you choose):

- FSM
- Microprogrammed
- Hardwired

Structures are given: File DLX_Project.pdf explain the organization DLX Control Unit (**LAB4** is organized in the same way for a simple exercise)

TEST DRIVEN DEPLOYMENT

1) **Understand** how to **generate** assembler files

2) **Run** a basic **simulation** of the given structure

3)Try to **add the management of a new ASM instruction** (follow file) of the CU

4) **Build** a very simple **DATA PATH** by connecting all the elementary blocks already used in labs 1-2-3-4

5) Connect simple **DATA PATH** to simple CU e and **check** the correct behavior

(things will be more clear along with the lab experiences!!!!)

DLX Basic requirements

- **Prepare** a few **ASM files COMMENTED** to test part of instructions.
- Organize and **fill your DP and CU** to execute an instructions subset given (DLX_Projet.pdf) essential instructions.
- **Synthesize the DLX:** synthesize first block by block (exploits scripts from previous labs).
- **Analyze timing, power, area**.
- **Execute physical design** (LAB5), report post layout timing, power, area, IR drop, EM.
- **Write the Report** (follow the guideline).

DLX Pro requirements

- As for the Basic:
  - **Prepare commented ASM files**.
  - **Fill your DP and CU**
- **ADD WHATEVER you want to your PERSONAL DLX!!!**
- **Synthesize the DLX:** synthesize first block by block (exploits scripts from previous labs).
- **Analyze timing, power, area**. (optimize synthesis by using more complex instructions)
- **Execute physical design** (LAB5), report post layout timing, power, area, IR drop, EM.
- **Write the Report** (follow the guideline).

Technical Report Structure

- First page
  - TITLE
  - Authors
  - Date of Writing
- SUMMARY
- INDEX OF CONTENTS, FIGURE and TABLE
- BODY
  - 1. **INTRODUCTION** (SPECIFICATION and FUNCTIONALITY)
  - 2. **FUNCTIONAL SCHEMA** (Block diagrams)
  - 3. **IMPLENTATION** (Technology, synthesis, optimization)
  - 4. **DISCUSSION** and **CONCLUSIONS** (Result from the BenchMark, timing, area)
- REFERENCES
- APPENDICES

Project Groups

- Lab groups and Project groups can differ
- The basic vs. pro choice is individual
- If you split and reorganize you MUST communicate the variation

Submission/evaluation/discussion

- There will be some exam sessions in July 2016 and September 2016, in which there is a possibility for final project discussion for whom submitted their final project at least "3 DAYS" before each available session
- Projects must be submitted through the course website with a clear file name.

  E.g. BLX-basic-GRXX.zip

Submission/evaluation/discussion

- The discussion is individual: each of you MUST know the project
- The discussion consists in
  - showing the structure
  - demonstrating the correct behavior using parts of asm programs execution, some of your invention and others given
  - Being ready to execute AT RUN TIME some random asm programs proposed to check the correct DECLARED behavior
  - Showing the synthesis and physical design results

HAPPY DLXING !!!!!!!