**Lockstep**

Flash

CPU 2

(checker)

Bridge

CPU 1

（master）

BUS

RAM

CPU 1 Disable

CPU 1

（master）

Receiver

Lockstep Disable

Selector

Parity Check

Outputs

Bit Compare Check

CPU 2

(checker)

CPU 2 Disable

Parity Check

Detection

& Isolation

Receiver

Reference：

《Error detection and fault isolation for lockstep processor systems》,United States Patent, US5915082.