Pulse Width Modulation Controller

Testbench Documentation

Description of module

This module is a System Verilog document which is used to test the Pulse Width Modulation Controller under simulated conditions.

Required Tests

1. Test to see that PWM is correctly working
2. Test that the PWM is correctly working at different period and duty cycle and that the duty cycle and period only update when it has finished the previously input period
3. Test that the PWMC can run anti-clockwise
4. Test that the brake function works correctly
5. Test that the PWM outputs can be turned on and off
6. Test that brake overrides the PWM output being toggled low

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How Required Tests Were Completed

1. This can be seen under the commented title “TEST 1”
2. This can be seen under the commented title “TEST 2”
3. This can be seen under the commented title “TEST 3”
4. This can be seen under the commented title “TEST 4”
5. This can be seen under the commented title “TEST 5”
6. This can be seen under the commented title “TEST 6”

Additional Information

None