Servo Control Unit Testbench Documentation

Description of module

This module is a System Verilog document which is used to test the Servo Control Unit under simulated conditions.

Required Tests

1. Test to see that the status register is output correctly
2. Test to see if you can set desired angle with bang bang control
3. Test to see if you can set desired angle with proportional control
4. Test to see that no command defaults to “brake”
5. Test to see that the reset function works correctly
6. Test to see that the brake function works correctly

How Required Tests Were Completed

1. This can be seen under the commented title “TEST 1”
2. This can be seen under the commented title “TEST 2”
3. This can be seen under the commented title “TEST 3”
4. This can be seen under the commented title “TEST 4”
5. This can be seen under the commented title “TEST 5”
6. This can be seen under the commented title “TEST 6”

Additional Information

None