Pulse Width Modulation Controller Documentation

Description of module

This module is a System Verilog document which is used to control a DC motor via a 2-wire H bridge interface. It is capable of setting a desired angle to an accuracy of <1°.

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Requirements

1. Must be possible to rotate the motor shaft both clockwise or anticlockwise
2. The motor speed must be controlled using a pulse width modulation technique
3. It must be possible to set both duty cycle and period to a resolution of 8-bits
4. It must be possible to turn the PWM outputs on and off
5. It must be possible to perform a brake

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How Requirements were met

1. This can be seen under the comment title "MOTOR DIRECTION = CLOCKWISE" and "MOTOR DIRECTION = ANTICLOCKWISE"
2. This can be seen under the comment title "COUNTER TO DETERMINE WHEN PULSE SHOULD BE HIGH"
3. This can be seen under the comment title "WAIT FOR PERIOD TO END BEFORE UPDATE"
4. This can be seen under the comment title "PWM OUTPUT TOGGLE"
5. This can be seen under the comment title "BRAKE FUCNTION"

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Inputs

- clk_50 – 50MHz clock input
- direction – when direction = 1 the PWMC will move the motor clockwise, when direction = 0 the PWMC will move the motor anticlockwise
- pwmOutEnable = when pwmOutEnable is high PWM outputs are turned on, when pwmOutEnable is low PWM outputs are turned off
- brake = when brake is high the PWMC will perform a brake
- dutyCycle = 8 bit input to set the duty cycle
- period = 8 bit input to set the period

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Outputs

- motor_1 = when motor_1 is high the DC motor will rotate anticlockwise
- motor_2 = when motor_2 is high the DC motor will rotate clockwise

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<u>Additional Information</u>

Should the duty cycle or period be updated while the motor is moving, the PWMC will update after its current period has ended. This is because when the SCU is set to proportional control mode, should the duty cycle and period be changed too quickly it would never reach the negative part of the PWM output. This would not be effective proportional control.