Display Controller Testbench Documentation

Description of module

This module is a System Verilog document which is used to test the Display Controller under simulated conditions.

Required Tests

1. Test to see that the angle is being read at fixed rate
2. Test to see that the LCD has been cleared
3. Test to see that data is being written correctly
4. Second test to see that the angle is being read at fixed rate with new angle
5. Second test to see that the LCD has been cleared with new angle
6. Second test to see that data is being written correctly with new angle

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How Required Tests Were Completed

1. This can be seen under the commented title “TEST 1”
2. This can be seen under the commented title “TEST 2”
3. This can be seen under the commented title “TEST 3”
4. This can be seen under the commented title “TEST 4”
5. This can be seen under the commented title “TEST 5”
6. This can be seen under the commented title “TEST 6”

Additional Information

None