ESP32-C5-MINI-1

Datasheet Version 1.0

Module that supports 2.4 and 5 GHz dual-band Wi-Fi 6 (802.11ax), Bluetooth® 5 (LE), Zigbee, and Thread (802.15.4)
Built around ESP32-C5 series of SoCs, 32-bit RISC-V single-core microprocessor
Flash up to 4 MB
22 GPIOs, rich set of peripherals
On-board PCB antenna

ESP32-C5-MINI-1

ESPRESSIF

1 Module Overview

1.1 Features

CPU and On-Chip Memory

- ESP32-C5 embedded, 32-bit RISC-V single-core microprocessor, up to 240 MHz
- ROM: 320 KB
- HP SRAM: 384 KB
- LP SRAM: 16 KB

Wi-Fi

- 1T1R in 2.4 and 5 GHz dual band
- Operating frequency: 2412 ~ 2484 MHz, 5180 ~ 5885 MHz
- IEEE 802.11ax-compliant
  - 20 MHz-only non-AP mode
  - Uplink and downlink OFDMA to enhance connectivity and performance in congested environments for IoT applications
  - Downlink MU-MIMO (multi-user, multiple input, multiple output) to increase network capacity
  - Beamformee that improves signal quality
  - Spatial reuse to maximize parallel transmissions
  - Target wake time (TWT) that optimizes power saving mechanisms
- IEEE 802.11ac-compliant
  - 20 MHz bandwidth
  - Downlink fullband MU-MIMO
- Fully compatible with IEEE 802.11b/g/n protocol
  - 20 MHz and 40 MHz bandwidth
  - Data rate up to 150 Mbps
  - Wi-Fi Multimedia (WMM)
  - TX/RX A-MPDU, TX/RX A-MSDU
  - Immediate Block ACK
  - Fragmentation and defragmentation
  - Transmit opportunity (TXOP)
  - Automatic Beacon monitoring (hardware TSF)
  - Four virtual Wi-Fi interfaces
  - Simultaneous support for Infrastructure BSS in Station mode, SoftAP mode, Station + SoftAP mode, and promiscuous mode
    Note that when ESP32-C5 scans in Station mode, the SoftAP channel will change along with the Station channel
  - Antenna diversity
  - 802.11mc FTM

Bluetooth®

- Bluetooth LE: Bluetooth Core 6.0 certified
- Bluetooth mesh 1.1
- High power mode (20 dBm)
- Direction finding (AoA/AoD)
- Periodic advertising with responses (PAwR)
- LE connection subrating
- LE power control
- Speed: 125 Kbps, 500 Kbps, 1 Mbps, 2 Mbps
- LE advertising extensions and multiple advertising sets
- Allow devices to operate in Broadcaster, Observer, Central, and Peripheral roles concurrently

IEEE 802.15.4

- Compliant with IEEE 802.15.4-2015 protocol
- OQPSK PHY in 2.4 GHz band
- Data rate: 250 Kbps
- Thread 1.4
- Zigbee 3.0

Peripherals

- GPIO, SPI, parallel IO interface, UART, I2C, I2S, RMT (TX/RX), pulse counter, LED PWM, USB Serial/JTAG controller, MCPWM, GDMA, CAN FD controller, SDIO slave controller, BitScrambler, event task matrix, ADC, temperature sensor, brownout detector, analog voltage comparator, system timer, general-purpose timers, RTC timer, watchdog timers, etc.

Integrated Components on Module

- 48 MHz crystal oscillator
- SPI flash

Antenna Options

- On-board PCB antenna

Operating Conditions

- Operating voltage/Power supply: 3.0 ~ 3.6 V
- Operating ambient temperature: −40 ~ 85 °C

Certification

- RF certification: See certificates
- Green certification: RoHS/REACH

Test

- HTOL/HTSL/uHAST/TCT/ESD

1.2 Series Comparison

ESP32-C5-MINI-1 modules are powerful, generic Wi-Fi MCUs that have a rich set of peripherals. They are an ideal choice for a wide variety of application scenarios related to Internet of Things (IoT), such as embedded systems, smart home, wearable electronics, etc.

ESP32-C5-MINI-1 comes with a PCB antenna.

The ordering information for the modules is as follows:

Table 1-1. ESP32-C5-MINI-1 (ANT) Series Comparison

Part Number	Flash[1,2]	Ambient Temp.[3] (°C)	Embedded Chip	Size[4] (mm)
ESP32-C5-MINI-1-N4	4 MB (Quad SPI)	−40 ~ 85	ESP32-C5NF4	15.4 × 21.3 × 2.4

[1] For specifications, refer to Section 6.5 *Memory Specifications*.

[2] By default, the SPI flash on the module operates at a maximum clock frequency of 80 MHz and does not support the auto suspend feature. If you have a requirement for a higher flash clock frequency of 120 MHz or if you need the flash auto suspend feature, please contact us.

[3] Ambient temperature specifies the recommended temperature range of the environment immediately outside the Espressif module.

[4] For details, refer to Section 10 *Module Dimensions*.

At the core of the modules is ESP32-C5 *, an Xtensa® 32-bit LX7 CPU that operates at up to 240 MHz. You can power off the CPU and make use of the low-power coprocessor to constantly monitor the peripherals for changes or crossing of thresholds.

Note:
For more information on ESP32-C5, please refer to *ESP32-C5 Series Datasheet*.

1.3 Applications

- Smart Home
- Industrial Automation
- Health Care
- Consumer Electronics
- Smart Agriculture
- POS Machines
- Service Robot
- Audio Devices
- Generic Low-power IoT Sensor Hubs
- Generic Low-power IoT Data Loggers
- Wi-Fi + Bluetooth Networking Card

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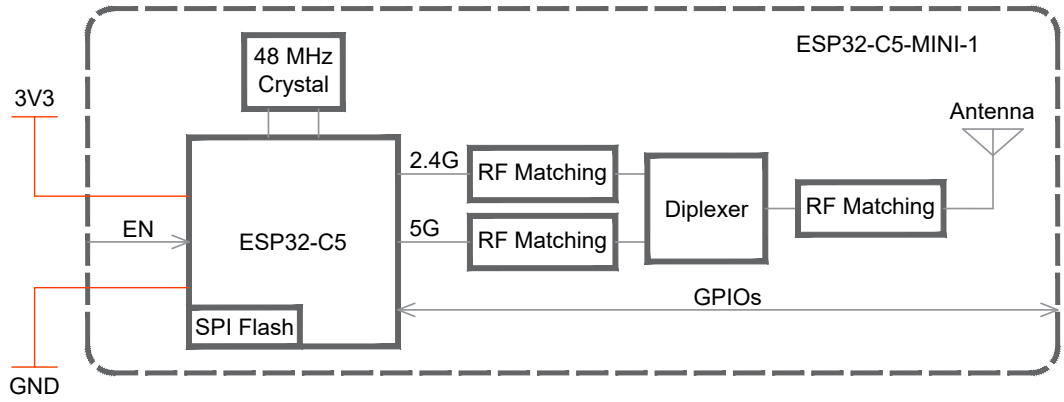

Figure 2-1. ESP32-C5-MINI-1 Block Diagram

Note:

For the pin mapping between the chip and the in-package flash/PSRAM, please refer to *ESP32-C5 Series Datasheet* > Table *Pin Mapping Between Chip and In-package Flash/PSRAM*.

3 Pin Definitions

3.1 Pin Layout

The pin diagram below shows the approximate location of pins on the module. For the actual diagram drawn to scale, please refer to Figure 10 *Module Dimensions*.

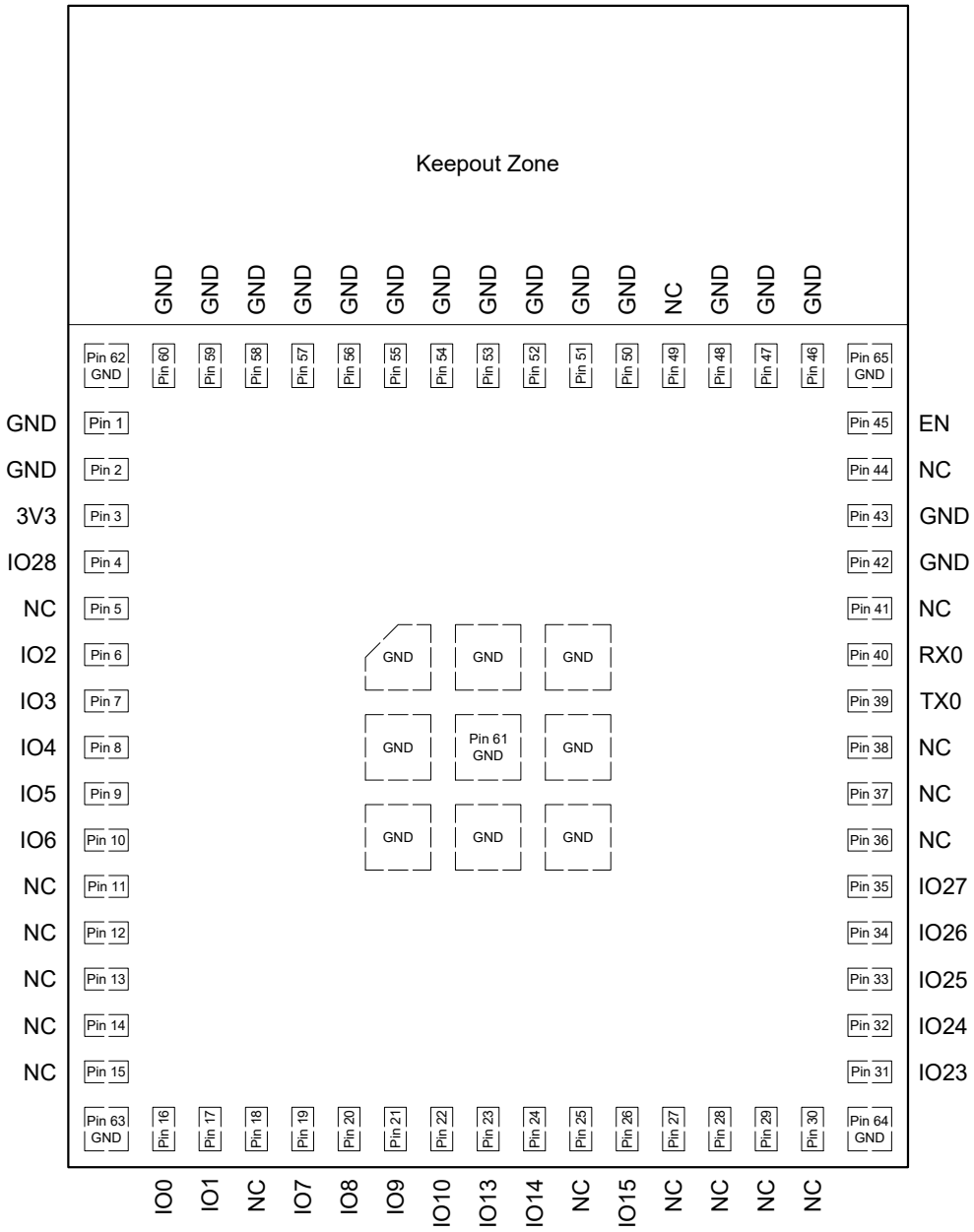

Figure 3-1. ESP32-C5-MINI-1 Pin Layout (Top View)

Note:

To learn more about the keepout zone for module's antenna on the base board, please refer to *ESP32-C5 Hardware Design Guidelines* > Section *General Principles of PCB Layout for Modules*.

3.2 Pin Description

The module has 65 pins. See pin definitions in Table 3-1 *Pin Definitions*.

For peripheral pin configurations, please refer to Section 5.2 *Peripheral Description*.

Table 3-1. Pin Definitions

Name	No.	Type[1]	Function
GND	1, 2, 42, 43, 46-48, 50-65	P	Ground
3V3	3	P	Power supply
IO28	4	I/O/T	GPIO28
NC	5, 11-15, 18, 25, 27-30, 36-38, 41, 44, 49	-	NC
IO2	6	I/O/T	MTMS, GPIO2, LP_GPIO2, LP_UART_RTSN, LP_I2C_SDA, ADC1_CH1, FSPIQ
IO3	7	I/O/T	MTDI, GPIO3, LP_GPIO3, LP_UART_CTSN, LP_I2C_SCL, ADC1_CH2
IO4	8	I/O/T	MTCK, GPIO4, LP_GPIO4, LP_UART_RXD, ADC1_CH3, FSPIHD
IO5	9	I/O/T	MTDO, GPIO5, LP_GPIO5, LP_UART_TXD, ADC1_CH4, FSPIWP
IO6	10	I/O/T	GPIO6, LP_GPIO6, ADC1_CH5, FSPICLK
IO0	16	I/O/T	GPIO0, XTAL_32K_P, LP_GPIO0, LP_UART_DTRN
IO1	17	I/O/T	GPIO1, XTAL_32K_N, LP_GPIO1, LP_UART_DSRN, ADC1_CH0
IO7	19	I/O/T	GPIO7, FSPID, SDIO_DATA1
IO8	20	I/O/T	GPIO8, PAD_COMP0, SDIO_DATA0
IO9	21	I/O/T	GPIO9, PAD_COMP1, SDIO_CLK
IO10	22	I/O/T	GPIO10, FSPICS0, SDIO_CMD
IO13	23	I/O/T	GPIO13, USB_D-, SDIO_DATA3
IO14	24	I/O/T	GPIO14, USB_D+, SDIO_DATA2
IO15	26	I/O/T	SPICS1, GPIO15
IO23	31	I/O/T	GPIO23
IO24	32	I/O/T	GPIO24
IO25	33	I/O/T	GPIO25
IO26	34	I/O/T	GPIO26
IO27	35	I/O/T	GPIO27
TX0	39	I/O/T	U0TXD, GPIO11
RX0	40	I/O/T	U0RXD, GPIO12
EN	45	I	High: on, enables the chip. Low: off, the chip powers off. Note: Do not leave the EN pin floating.

[1] P: power supply; I: input; O: output; T: high impedance.

4 Boot Configurations

Note:
The content below is excerpted from *ESP32-C5 Series Datasheet* > Section *Boot Configurations*. For the strapping pin mapping between the chip and modules, please refer to Chapter 8 *Module Schematics*.

The chip allows for configuring the following boot parameters through strapping pins and eFuse parameters at power-up or a hardware reset, without microcontroller interaction.

- **Chip boot mode**
  - Strapping pin: GPIO26, GPIO27, and GPIO28
- **SDIO sampling and driving clock edge**
  - Strapping pin: GPIO25 and MTDI
- **ROM message printing**
  - Strapping pin: GPIO27
  - eFuse parameter: EFUSE_UART_PRINT_CONTROL and EFUSE_DIS_USB_SERIAL_JTAG_ROM_PRINT
- **JTAG signal source**
  - Strapping pin: GPIO7
  - eFuse parameter: EFUSE_DIS_PAD_JTAG, EFUSE_DIS_USB_JTAG, and EFUSE_JTAG_SEL_ENABLE

The default values of all the above eFuse parameters are 0, which means that they are not burnt. Given that eFuse is one-time programmable, once programmed to 1, it can never be reverted to 0. For how to program eFuse parameters, please refer to *ESP32-C5 Technical Reference Manual* > Chapter *eFuse Controller*.

The default values of the strapping pins, namely the logic levels, are determined by pins' internal weak pull-up/pull-down resistors at reset if the pins are not connected to any circuit, or connected to an external high-impedance circuit.

Table 4-1. Default Configuration of Strapping Pins

Strapping Pin	Default Configuration	Bit Value
GPIO25	Floating	–
GPIO26	Floating	–
GPIO27	Pull-up	1
GPIO28	Pull-up	1
GPIO7	Floating	–
MTMS	Floating	–
MTDI	Floating	–

To change the bit values, the strapping pins should be connected to external pull-down/pull-up resistances.

All strapping pins have latches. At Chip Reset, the latches sample the bit values of their respective strapping pins and store them until the chip is powered down or shut down. The states of latches cannot be changed in any other way. It makes the strapping pin values available during the entire chip operation, and the pins are freed up to be used as regular IO pins after reset. For details on Chip Reset, see *ESP32-C5 Technical Reference Manual* > Chapter *Reset and Clock*.

The timing of signals connected to the strapping pins should adhere to the *setup time* and *hold time* specifications in Table 4-2 and Figure 4-1.

Table 4-2. Description of Timing Parameters for the Strapping Pins

Parameter	Description	Min (ms)
t_{SU}	*Setup time* is the time reserved for the power rails to stabilize before the CHIP_PU pin is pulled high to activate the chip.	0
t_{H}	*Hold time* is the time reserved for the chip to read the strapping pin values after CHIP_PU is already high and before these pins start operating as regular IO pins.	3

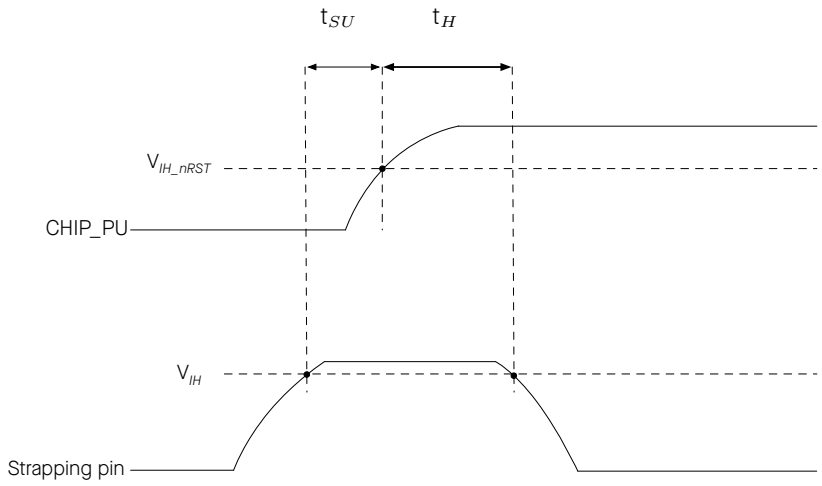

Figure 4-1. Visualization of Timing Parameters for the Strapping Pins

4.1 Chip Boot Mode Control

GPIO26, GPIO27 and GPIO28 control the boot mode after the reset is released. See Table 4-3 *Boot Mode Control*.

Table 4-3. Boot Mode Control

Boot Mode	GPIO26	GPIO27	GPIO28
SPI Boot[1]	Any value	Any value	**1**[1]
Joint Download Boot 0[2]	Any value	1	0
Joint Download Boot 1[3]	0	0	0

[1] **Bold** marks the default value and configuration.

[2] Joint Download Boot 0 mode supports the following download methods:

- USB-Serial-JTAG Download Boot
- UART Download Boot
- SPI Slave Download Boot (chip revision v0.1 only)

[3] Joint Download Boot 1 mode supports the following download methods:

- UART Download Boot
- SDIO Download Boot

In SPI Boot mode, the ROM bootloader loads and executes the program from SPI flash to boot the system.

In Joint Download Boot 0 mode, users can download binary files into flash using UART0, USB, or SPI Slave interfaces. It is also possible to download binary files into SRAM and execute it from SRAM.

In Joint Download Boot 1 mode, users can download binary files into flash using UART0 or SDIO interfaces. It is also possible to download binary files into SRAM and execute it from SRAM.

4.2 SDIO Sampling and Driving Clock Edge Control

The strapping pin GPIO25 and MTDI can be used to decide on which clock edge to sample signals and drive output lines. See Table 4-4 SDIO Input Sampling Edge/Output Driving Edge Control.

Table 4-4. SDIO Input Sampling Edge/Output Driving Edge Control

Edge behavior	GPIO25	MTDI
Falling edge sampling, falling edge output	0	0
Falling edge sampling, rising edge output	0	1
Rising edge sampling, falling edge output	1	0
Rising edge sampling, rising edge output	1	1

[1] GPIO25 and MTDI are floating by default, so above are not default configurations.

4.3 ROM Messages Printing Control

During the boot process, the messages by the ROM code can be printed to:

- (Default) UART0 and USB Serial/JTAG controller
- UART0

- USB Serial/JTAG controller

To print ROM messages to **UART0** or **USB Serial/JTAG controller**, see the description below.

EFUSE_UART_PRINT_CONTROL and GPIO27 control printing ROM messages to **UART0** as shown in Table 4-5 *UART0 ROM Message Printing Control*.

Table 4-5. UART0 ROM Message Printing Control

UART0 ROM Message Printing	Register[2]	eFuse[3]	GPIO27
ROM messages are always printed to UART0 during boot	**0**	**0 (0b00)**	x[4]
Print is enabled during boot		1 (0b01)	0
Print is disabled during boot			1
Print is disabled during boot		2 (0b10)	0
Print is enabled during boot			1
Print is disabled during boot		3 (0b11)	x
Print is disabled during boot	1	x	x

[1] **Bold** marks the default value and configuration.
[2] Register: LP_AON_STORE4_REG[0]
[3] eFuse: EFUSE_UART_PRINT_CONTROL
[4] x: x indicates that the value has no effect on the result and can be ignored.

EFUSE_DIS_USB_SERIAL_JTAG_ROM_PRINT controls the printing to **USB Serial/JTAG controller** as shown in Table 4-6 *USB Serial/JTAG ROM Message Printing Control*.

Table 4-6. USB Serial/JTAG ROM Message Printing Control

USB Serial/JTAG ROM Message Printing	EFUSE_DIS_USB_SERIAL_JTAG_ROM_PRINT
Enabled	**0**
Disabled	1
	Ignored

[1] **Bold** marks the default value and configuration.

4.4 JTAG Signal Source Control

The strapping pin GPIO7 can be used to control the source of JTAG signals during the early boot process. This pin does not have any internal pull resistors and the strapping value must be controlled by the external circuit that cannot be in a high impedance state.

As Table 4-7 shows, GPIO7 is used in combination with EFUSE_DIS_PAD_JTAG, EFUSE_DIS_USB_JTAG, and EFUSE_JTAG_SEL_ENABLE.

Table 4-7. JTAG Signal Source Control

JTAG Signal Source	eFuse 1[2]	eFuse 2[3]	eFuse 3[4]	GPIO7
USB Serial/JTAG Controller[6]	**0**	**0**	**0**	x[5]
			1	1
JTAG pins MTDI, MTCK, MTMS, and MTDO				0
		x	x	x
		1		
USB Serial/JTAG Controller[6]	1	0		
JTAG is disabled		x		
		1		

[1] **Bold** marks the default value and configuration.
[2] eFuse 1: EFUSE_DIS_PAD_JTAG
[3] eFuse 2: EFUSE_DIS_USB_JTAG
[4] eFuse 3: EFUSE_JTAG_SEL_ENABLE
[5] x: x indicates that the value has no effect on the result and can be ignored.
[6] In Joint Download Boot 1 mode, the USB Serial/JTAG controller is forcibly disabled, and the JTAG signal only comes from JTAG pins. If PAD_JTAG is also disabled, then JTAG is disabled.

4.5 Chip Power-up and Reset

Once the power is supplied to the chip, its power rails need a short time to stabilize. After that, CHIP_PU – the pin used for power-up and reset – should be pulled high to activate the chip. For information on CHIP_PU as well as power-up and reset timing, see Figure 4-2 and Table 4-8.

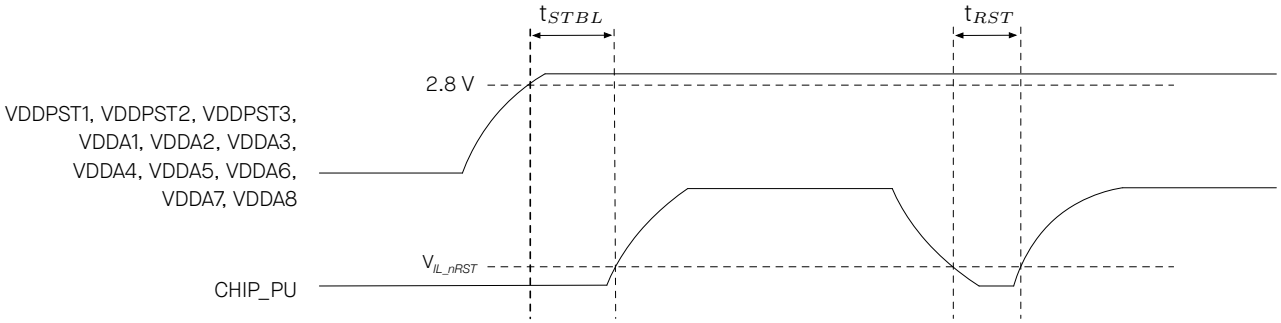

Figure 4-2. Visualization of Timing Parameters for Power-up and Reset

Table 4-8. Description of Timing Parameters for Power-up and Reset

Parameter	Description	Min (μs)
t_{STBL}	Time reserved for the power rails of VDDPST1, VDDPST2, VDDPST3, VDDA1, VDDA2, VDDA3, VDDA4, VDDA5, VDDA6, VDDA7, and VDDA8 to stabilize before the CHIP_PU pin is pulled high to activate the chip	50
t_{RST}	Time reserved for CHIP_PU to stay below V_{IL_nRST} to reset the chip (see Table 6-3)	50

5 Peripherals

5.1 Peripheral Overview

ESP32-C5 integrates a rich set of peripherals including SPI, parallel IO interface, UART, I2C, I2S, RMT (TX/RX), pulse counter, LED PWM, USB Serial/JTAG controller, MCPWM, GDMA, CAN FD controller, SDIO slave controller, BitScrambler, event task matrix, ADC, temperature sensor, brownout detector, analog voltage comparator, as well as up to 22 GPIOs, etc.

To learn more about on-chip components, please refer to *ESP32-C5 Series Datasheet* > Section *Functional Description*.

Note:
The content below is sourced from *ESP32-C5 Series Datasheet* > Section *Peripherals*. Some information may not be applicable to ESP32-C5-MINI-1 as not all the IO signals are exposed on the module.
To learn more about peripheral signals, please refer to *ESP32-C5 Technical Reference Manual* > Section *Peripheral Signal List*.

5.2 Peripheral Description

This section describes the chip's peripheral capabilities, covering connectivity interfaces and on-chip sensors that extend its functionality.

5.2.1 Connectivity Interface

This subsection describes the connectivity interfaces on the chip that enable communication and interaction with external devices and networks.

5.2.1.1 UART Controller

ESP32-C5 has three UART interfaces, i.e. UART0, UART1, and LP UART. All the three interfaces provide hardware flow control (CTS and RTS signals) and software flow control (XON and XOFF).

Feature List

- programmable baud rates up to 5 MBaud
- RAM shared by TX FIFOs and RX FIFOs
- support for various lengths of data bits and stop bits
- parity bit support
- special character AT_CMD detection
- RS485 protocol support (not supported by LP UART)
- IrDA protocol support (not supported by LP UART)
- high-speed data communication using GDMA (not supported by LP UART)
- receive timeout feature

- UART as the wake-up source
- software and hardware flow control

For details, see *ESP32-C5 Technical Reference Manual* > Chapter *UART Controller (UART)*.

Pin Assignment

The pins connected to transmit and receive signals (U0TXD and U0RXD) for **UART0** are multiplexed with GPIO11 and GPIO12 via IO MUX. Other signals can be routed to any GPIOs via the GPIO matrix.

For LP UART, the pins used are multiplexed with LP_GPIO0 ~ LP_GPIO5 via LP IO MUX.

For more information about the pin assignment, see *ESP32-C5 Series Datasheet* > Section *IO Pins* and *ESP32-C5 Technical Reference Manual* > Chapter *GPIO Matrix and IO MUX*.

5.2.1.2 SPI Controller

ESP32-C5 features three SPI interfaces (SPI0, SPI1, and SPI2). SPI0 and SPI1 can be configured to operate in SPI memory mode, while SPI2 can be configured to operate in general-purpose SPI mode.

Feature List

- **SPI Memory mode**

  In SPI memory mode, SPI0 and SPI1 interfaces are for external SPI memory. Data are transferred in unit of byte. Up to four-line STR reads and writes are supported. The clock frequency is configurable to a maximum of 120 MHz.

- **SPI2 General-purpose SPI (GP-SPI) mode**

  SPI2 can operate in master and slave modes. SPI2 supports two-line full-duplex communication and single/two/four-line half-duplex communication in both master and slave modes. The host's clock frequency is configurable. Data are transferred in unit of byte. The clock polarity (CPOL) and phase (CPHA) are also configurable. The SPI2 interface can connect to GDMA.

  - In master mode, the clock frequency is 80 MHz at most, and the four modes of SPI transfer format are supported.
  - In slave mode, the clock frequency is 40 MHz at most, and the four modes of SPI transfer format are also supported.

For details, see *ESP32-C5 Technical Reference Manual* > Chapter *SPI Controller (SPI)*.

Pin Assignment

For SPI0/1, the pins are multiplexed with GPIO15 ~ GPIO18 and GPIO20 ~ GPIO22 via the IO MUX.

For SPI2, the pins for data and clock signals are multiplexed with GPIO2 and GPIO4 ~ GPIO7 via the IO MUX. The pins for chip select signals for multiplexed with GPIO10 via the IO MUX. SPI2 signals can also be routed to any GPIOs via the GPIO matrix.

For more information about the pin assignment, see *ESP32-C5 Series Datasheet* > Section *IO Pins* and *ESP32-C5 Technical Reference Manual* > Chapter *GPIO Matrix and IO MUX*.

5.2.1.3 I2C Controller

ESP32-C5 has an I2C and an LP I2C bus interface. I2C is used for I2C master mode or slave mode, depending on your configuration, while LP I2C is always in master mode.

Feature List

- standard mode (100 Kbit/s)
- fast mode (400 Kbit/s)
- up to 800 Kbit/s (constrained by SCL and SDA pull-up strength)
- 7-bit and 10-bit addressing mode
- double addressing mode
- 7-bit broadcast address

For details, see *ESP32-C5 Technical Reference Manual* > Chapter *I2C Controller (I2C)*.

Pin Assignment

For regular I2C, the pins used can be chosen from any GPIOs via the GPIO Matrix.

For LP I2C, the pins used are multiplexed with LP_GPIO2 and LP_GPIO3 via LP IO MUX.

For more information about the pin assignment, see *ESP32-C5 Series Datasheet* > Section *IO Pins* and *ESP32-C5 Technical Reference Manual* > Chapter *GPIO Matrix and IO MUX*.

5.2.1.4 I2S Controller

ESP32-C5 includes a standard I2S interface. This interface can operate as a master or a slave in full-duplex mode or half-duplex mode, and supports 8-bit, 16-bit, 24-bit, or 32-bit serial communication. BCK clock frequency, from 10 kHz up to 40 MHz, is supported.

The I2S interface supports TDM Philips, TDM MSB alignment, TDM PCM standard, PDM standard, and PCM-to-PDM TX interface. It connects to the GDMA controller.

Feature List

- master mode and slave mode
- full-duplex and half-duplex communications
- separate TX and RX units that can work independently or simultaneously
- a variety of audio standards supported:
  - TDM Philips standard
  - TDM MSB alignment standard
  - TDM PCM standard
  - PDM standard
- various TX/RX modes

  - TDM TX mode, up to 16 channels supported
  - TDM RX mode, up to 16 channels supported
  - PDM TX mode
    * raw PDM data transmission
    * PCM-to-PDM data format conversion, up to 2 channels supported
  - PDM RX mode
    * raw PDM data reception
- configurable clock source with frequency up to 240 MHz
- configurable high-precision sample clock with a variety of sampling frequencies supported
- 8/16/24/32-bit data width
- synchronous counter in TX mode
- ETM feature
- direct memory access
- standard I2S interface interrupts

For details, see *ESP32-C5 Technical Reference Manual* > Chapter *I2S Controller (I2S)*.

Pin Assignment

The pins for the I2S controller can be chosen from any GPIOs via the GPIO Matrix.

For more information about the pin assignment, see *ESP32-C5 Series Datasheet* > Section *IO Pins* and *ESP32-C5 Technical Reference Manual* > Chapter *GPIO Matrix and IO MUX*.

5.2.1.5 USB Serial/JTAG Controller

ESP32-C5 contains a USB Serial/JTAG controller. This unit can be used to program the SoC's flash, read program output, as well as attach a debugger to the running program. All of these are possible for any computer with a USB host without any active external components.

Feature List

- USB 2.0 full speed compliant, capable of up to 12 Mbit/s transfer speed (note that this controller does not support the faster 480 Mbit/s high-speed transfer mode)
- CDC-ACM virtual serial port and JTAG adapter functionality
- programming the chip's flash
- CPU debugging with compact JTAG instructions
- a full-speed USB PHY integrated in the chip

For details, see *ESP32-C5 Technical Reference Manual* > Chapter *USB Serial/JTAG Controller (USB_SERIAL_JTAG)*.

Pin Assignment

The pins for the USB Serial/JTAG controller are multiplexed with GPIO13 ~ GPIO14 via IO MUX. GPIO13 ~ GPIO14 are also multiplexed with the pins for the SDIO Slave controller. The SDIO Slave controller can be used together with the USB Serial/JTAG controller in single SPI mode, but not in quad SPI mode.

For more information about the pin assignment, see *ESP32-C5 Series Datasheet* > Section *IO Pins* and *ESP32-C5 Technical Reference Manual* > Chapter *GPIO Matrix and IO MUX*.

5.2.1.6 CAN FD Controller

The Controller Area Network Flexible Data-Rate (CAN FD) is a multi-master, multi-cast communication protocol designed for automotive applications. The CAN FD controller facilitates the communication based on this protocol.

Feature List

- compliant with ISO11898-1:2015
- RX buffer FIFO with 32 - 4096 words (1 - 204 CAN FD frames with 64 byte of data)
- 2 - 8 TXT buffers (1 CAN FD frame in each TXT buffer)
- 32-bit slave memory interface (APB, AHB, RAM-like interface)
- support of ISO and non-ISO CAN FD protocol
- timestamping and time triggered transmission
- support interrupts
- loopback mode, bus monitoring mode, ACK forbidden mode, self-test mode, and restricted operation mode

For details, see *ESP32-C5 Technical Reference Manual* > Chapter *Controller Area Network Flexible Data-Rate*.

Pin Assignment

The pins for the CAN FD Controller can be chosen from any GPIOs via the GPIO Matrix.

For more information about the pin assignment, see *ESP32-C5 Series Datasheet* > Section *IO Pins* and *ESP32-C5 Technical Reference Manual* > Chapter *GPIO Matrix and IO MUX*.

5.2.1.7 LED PWM Controller

The LED PWM controller can generate independent digital waveform on six channels.

Feature List

- generating digital waveform with configurable periods and duty cycle. The resolution of duty cycle can be up to 20 bits
- multiple clock sources, including 80 MHz PLL clock, external main crystal clock, and internal fast RC oscillator

- operation when the CPU is in Light-sleep mode
- gradual increase or decrease of duty cycle, which is useful for the LED RGB color-gradient generator
- up to 16 duty cycle ranges for gamma curve generation, each can be independently configured in terms of duty cycle direction (increase or decrease), step size, the number of steps, and step frequency

For details, see *ESP32-C5 Technical Reference Manual* > Chapter *LED PWM Controller*.

Pin Assignment

The pins for the LED PWM controller can be chosen from any GPIOs via the GPIO Matrix.

For more information about the pin assignment, see *ESP32-C5 Series Datasheet* > Section *IO Pins* and *ESP32-C5 Technical Reference Manual* > Chapter *GPIO Matrix and IO MUX*.

5.2.1.8 Pulse Count Controller

The Pulse Count controller (PCNT) in ESP32-C5 captures pulses and counts pulse edges in seven modes.

Feature List

- four independent pulse counters (units) that count from 1 to 65535
- each unit consists of two independent channels sharing one pulse counter
- all channels have input pulse signals (e.g. sig_ch0_u*n*) with their corresponding control signals (e.g. ctrl_ch0_u*n*)
- independently filter glitches of input pulse signals (sig_ch0_u*n* and sig_ch1_u*n*) and control signals (ctrl_ch0_u*n* and ctrl_ch1_u*n*) on each unit
- each channel has the following parameters:
  1. selection between counting on positive or negative edges of the input pulse signal
  2. configuration to Increment, Decrement, or Disable counter mode for control of signal's high and low states
- support step counting
- maximum frequency of pulses: 40 MHz

For details, see *ESP32-C5 Technical Reference Manual* > Chapter *Pulse Count Controller*.

Pin Assignment

The pins for the Pulse Count controller can be chosen from any GPIOs via the GPIO Matrix.

For more information about the pin assignment, see *ESP32-C5 Series Datasheet* > Section *IO Pins* and *ESP32-C5 Technical Reference Manual* > Chapter *GPIO Matrix and IO MUX*.

5.2.1.9 Motor Control PWM

ESP32-C5 integrates an MCPWM that can be used to drive digital motors and smart light.

Feature List

- a clock divider (prescaler), three PWM timers, three PWM operators, and a dedicated capture submodule. PWM timers are used to generate timing references. PWM operators generate desired waveform based on the timing references
- a PWM operator can use the timing reference of any PWM timer
- a PWM operator can use the same timing reference with other PWM operators
- PWM operators can use different PWM timers' values to produce independent PWM signals
- PWM timers can be synchronized

For details, see *ESP32-C5 Technical Reference Manual* > Chapter *Motor Control PWM (MCPWM)*.

Pin Assignment

The pins for the Motor Control PWM can be chosen from any GPIOs via the GPIO Matrix.

For more information about the pin assignment, see *ESP32-C5 Series Datasheet* > Section *IO Pins* and *ESP32-C5 Technical Reference Manual* > Chapter *GPIO Matrix and IO MUX*.

5.2.1.10 Remote Control Peripheral

The Remote Control Peripheral (RMT) supports two channels of infrared remote transmission and two channels of infrared remote reception. By controlling pulse waveform through software, it supports various infrared and other single wire protocols.

Feature List

- four channels:
  - TX channels 0 ~ 1
  - RX channels 2 ~ 3
  - four channels share a 192 x 32-bit RAM
- the transmitter supports:
  - normal TX mode
  - wrap TX mode
  - modulation on TX pulses
  - continuous TX mode
  - multiple channels (programmable) transmitting data simultaneously
- the receiver supports:
  - normal RX mode
  - wrap RX mode
  - RX filtering
  - demodulation on RX pulses

For more details, see *ESP32-C5 Technical Reference Manual* > Chapter *Remote Control Peripheral (RMT)*.

Pin Assignment

The pins for the Remote Control Peripheral can be chosen from any GPIOs via the GPIO Matrix.

For more information about the pin assignment, see *ESP32-C5 Series Datasheet* > Section *IO Pins* and *ESP32-C5 Technical Reference Manual* > Chapter *GPIO Matrix and IO MUX*.

5.2.1.11 Parallel IO Controller

ESP32-C5 integrates a PARLIO controller for parallel data transfer. It has a transmitter and a receiver, connected with the GDMA controller. In full-duplex mode the PARLIO controller supports up to 4-bit parallel data transfer, while in half-duplex mode it supports up to 8-bit parallel data transfer.

Feature List

- multiple clock sources and clock division, with clock frequency up to 40 MHz
- receiver/transmitter supports input and output clock inverse
- 1/2/4/8-bit data transfer
- changeable sample sequence for data to be transmitted and received in 1-bit, 2-bit, and 4-bit mode
- support for multiple data sampling mode by the receiver
- support for multiple GDMA EOF signal generation modes by the receiver
- output external chip select signals with configurable delay cycles
- support for transmitter clock gating

For more details, see *ESP32-C5 Technical Reference Manual* > Chapter *Parallel IO Controller*.

Pin Assignment

The pins for the Parallel IO controller can be chosen from any GPIOs via the GPIO Matrix.

For more information about the pin assignment, see *ESP32-C5 Series Datasheet* > Section *IO Pins* and *ESP32-C5 Technical Reference Manual* > Chapter *GPIO Matrix and IO MUX*.

5.2.1.12 BitScrambler

The ESP32-C5 has an extensive amount of DMA-capable peripherals. These can move data from memory to an external device, and vice versa, without any interference from the CPU. This only works if the external device needs or emits the data in question in the same format as the software expects it: if not, the CPU needs to rewrite the format of the data. Examples include a need to swap bytes, reverse bytes, and shift the data left or right.

As bitwise operations tend to be fairly CPU-expensive and the purpose of DMA is to not use the CPU in the transfer, ESP32-C5 integrates one BitScrambler, which are dedicated peripherals to change the format of data in between memory and the peripheral. The RX channel is dedicated to peripheral-to-memory transfers, and the TX channel is dedicated to memory-to-peripheral transfers. The BitScrambler is capable of performing the

aforementioned operations, but as a flexible programmable state machine, it is capable of more advanced things as well.

Feature List

- one BitScrambler, one channel for RX (peripheral-to-memory), one channel for TX (memory-to-peripheral). The two channels support only half-duplex communications, and cannot work at the same time
- support for memory-to-memory transfers
- process up to 32 bits per DMA clock period
- data path controlled by a BitScrambler program stored in the instruction memory
- input registers able to read 0, 8, 16, or 32 bits per clock cycle
- output registers:
  - able to write 0, 8, 16, or 32 bits per clock cycle
  - data sources for output register bits: 64 bits of input data, two counters, LUT RAM data, data output of last cycle, comparators
  - with some restrictions, each of the 32 output register bits can come from any bit on the data sources
- 8 x 257-bit instruction memory, for storing eight instructions, controlling control flow and the data path
- 2048 bytes of lookup table (LUT) memory, configurable as various word widths

For more details, see *ESP32-C5 Technical Reference Manual* > Chapter *BitScrambler*.

Pin Assignment

The BitScrambler does not directly interact with IOs, so it has no pins assigned.

For more information about the pin assignment, see *ESP32-C5 Series Datasheet* > Section *IO Pins* and *ESP32-C5 Technical Reference Manual* > Chapter *GPIO Matrix and IO MUX*.

5.2.1.13 SDIO Slave Controller

The SDIO Slave controller in ESP32-C5 provides hardware support for the Secure Digital Input/Output (SDIO) device interface. It allows an SDIO host to access ESP32-C5 via an SDIO bus protocol.

Feature List

- compatible with SDIO Physical Layer Specification V2.00 and SDIO Specifications V2.00
- support SPI, 1-bit SDIO, and 4-bit SDIO transfer modes
- clock range of 0 ~ 50 MHz
- configurable sample and drive clock edge
- integrated and SDIO-accessible registers for information interaction
- support SDIO interrupts

- automatic padding data and discarding the padded data on the SDIO bus
- block size up to 512 bytes
- interrupt vector between the host and slave for bidirectional interrupt
- support DMA for data transfer
- support wake-up from sleep when connection is retained

For more details about the SDIO Slave controller, refer to the *ESP32-C5 Technical Reference Manual* > Chapter *SDIO Slave Controller (SDIO)*.

Pin Assignment

The pins for the SDIO Slave controller are multiplexed with GPIO7 ~ GPIO10, GPIO13, and GPIO14 via IO MUX. GPIO13 ~ GPIO14 are also multiplexed with the pins for the USB serial/JTAG controller. The SDIO Slave controller can be used together with the USB Serial/JTAG controller in single SPI mode, but not in quad SPI mode.

For more information about the pin assignment, see *ESP32-C5 Series Datasheet* > Section *IO Pins* and *ESP32-C5 Technical Reference Manual* > Chapter *IO MUX and GPIO Matrix*.

Note:
This peripheral is not supported by chip revision v0.0 and v0.1.

5.2.2 Analog Signal Processing

This subsection describes components on the chip that sense and process real-world data.

5.2.2.1 Temperature Sensor

ESP32-C5 provides a temperature sensor to monitor temperature changes inside the chip in real time. The sensor converts analog voltage to digital values and supports compensation for the temperature offset.

Feature List

- software-triggered temperature measurement. Once triggered, the sensor continuously measures temperature. Software can read the data any time.
- hardware-triggered automatic temperature monitoring
- two modes for automatic monitoring of temperature and support for triggering interrupts
- configurable temperature offset based on the application scenario for improved accuracy
- configurable temperature measurement range
- support for several Event Task Matrix (ETM) related events and tasks

For more details, see *ESP32-C5 Technical Reference Manual* > Chapter *Temperature Sensor*.

5.2.2.2 ADC Controller

ESP32-C5 integrates One 12-bit successive approximation ADC (SAR ADC) for measuring analog signals from up to six channels.

Feature List

- 12-bit resolution
- analog inputs sampling from up to six pins
- one-shot sampling mode and multi-channel sampling mode
- multi-channel sampling mode supports:
  - configurable channel sampling sequence
  - two filters whose filter coefficients are configurable
  - two threshold monitors that can trigger an interrupt when the filtered value is below a low threshold or above a high threshold
  - continuous transfer of converted data to memory via GDMA interface
- support for several Event Task Matrix (ETM) related events and tasks

For more details, see *ESP32-C5 Technical Reference Manual* > Chapter *ADC Controller*.

Pin Assignment

The pins for the ADC controller are multiplexed with GPIO1 ~ GPIO6.

For more information about the pin assignment, see *ESP32-C5 Series Datasheet* > Section *IO Pins* and *ESP32-C5 Technical Reference Manual* > Chapter *GPIO Matrix and IO MUX*.

5.2.2.3 Analog Voltage Comparator

ESP32-C5 provides an analog voltage comparator which contains two special pads. This peripheral can be used to compare the voltages of the two pads or compare the voltage of one pad with a stable internal voltage that is adjustable.

Feature List

- internal or external reference voltage
- supported internal reference voltage ranging from 0 to 0.7 * VDD_PST
- support for ETM
- interrupt triggered when the measured voltage reaches the reference voltage

For more details, see *ESP32-C5 Technical Reference Manual* > Chapter *Analog Voltage Comparator*.

Pin Assignment

The analog voltage comparator has dedicated pads, GPIO8 and GPIO9. GPIO9 is the test pad, and GPIO8 serves as the reference pad when using an external reference voltage.

For more information about the pin assignment, see *ESP32-C5 Series Datasheet* > Section *IO Pins* and *ESP32-C5 Technical Reference Manual* > Chapter *GPIO Matrix and IO MUX*.

6 Electrical Characteristics

The values presented in this section are preliminary and may change with the final release of this datasheet.

6.1 Absolute Maximum Ratings

Stresses above those listed in Table 6-1 *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under Table 6-2 *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Table 6-1. Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
VDD33	Power supply voltage	−0.3	3.6	V
T_{STORE}	Storage temperature	−40	85	°C

6.2 Recommended Operating Conditions

Table 6-2. Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
VDD33	Power supply voltage	3.0	3.3	3.6	V
I_{VDD}	Current delivered by external power supply	0.6	—	—	A
T_A	Operating ambient temperature	−40	—	85	°C

6.3 DC Characteristics (3.3 V, 25 °C)

Table 6-3. DC Characteristics (3.3 V, 25 °C)

Parameter	Description	Min	Typ	Max	Unit
C_{IN}	Pin capacitance	—	2	—	pF
V_{IH}	High-level input voltage	0.75 × VDD [1]	—	VDD [1] + 0.3	V
V_{IL}	Low-level input voltage	−0.3	—	0.25 × VDD [1]	V
I_{IH}	High-level input current	—	—	50	nA
I_{IL}	Low-level input current	—	—	50	nA
V_{OH} [2]	High-level output voltage	0.8 × VDD [1]	—	—	V
V_{OL} [2]	Low-level output voltage	—	—	0.1 × VDD [1]	V
I_{OH}	High-level source current (VDD [1] = 3.3 V, V_{OH} >= 2.64 V, PAD_DRIVER = 3)	—	40	—	mA
I_{OL}	Low-level sink current (VDD [1] = 3.3 V, V_{OL} = 0.495 V, PAD_DRIVER = 3)	—	28	—	mA
R_{PU}	Internal weak pull-up resistor	—	45	—	kΩ

Cont'd on next page

Table 6-3 – cont'd from previous page

Parameter	Description	Min	Typ	Max	Unit
R_{PD}	Internal weak pull-down resistor	—	45	—	kΩ
V_{IH_nRST}	Chip reset release voltage (CHIP_PU voltage is within the specified range)	0.75 × VDD [1]	—	VDD [1] + 0.3	V
V_{IL_nRST}	Chip reset voltage (CHIP_PU voltage is within the specified range)	−0.3	—	0.25 × VDD [1]	V

[1] VDD – voltage from a power pin of a respective power domain.

[2] V_{OH} and V_{OL} are measured using high-impedance load.

6.4 Current Consumption Characteristics

6.4.1 Current Consumption in Active Mode

The current consumption measurements are taken with a 3.3 V supply at 25 °C ambient temperature.

TX current consumption is rated at a 100% duty cycle.

RX current consumption is rated when the peripherals are disabled and the CPU idle.

Table 6-4. Current Consumption for Wi-Fi (2.4 GHz) in Active Mode

Work Mode	RF Condition	Description	Peak (mA)
Active (RF working)	TX	802.11b, 1 Mbps, DSSS @ 19.2dBm	323
		802.11g, 54 Mbps, OFDM @ 16.4dBm	271
		802.11n, HT20, MCS7 @ 16.5dBm	271
		802.11n, HT40, MCS7 @ 15.6dBm	263
		802.11ax, MCS9 @ 14.5dBm	249
	RX	802.11b/g/n, HT20	94
		802.11n, HT40	101
		802.11ax, HE20	94

Table 6-5. Current Consumption for Wi-Fi (5 GHz) in Active Mode

Work Mode	RF Condition	Description	Peak (mA)
Active (RF working)	TX	802.11a, 6 Mbps, OFDM @ 17.5dBm	395
		802.11n, HT20, MCS7 @ 15dBm	369
		802.11n, HT40, MCS7 @ 14.5dBm	354
		802.11ac, VHT20, MCS7 @ 15dBm	368
		802.11ax, HE20, MCS7 @ 15dBm	367
	RX	802.11a/n, HT20	121
		802.11n, HT40	128
		802.11ac, VHT20	120
		802.11ax, HE20	121

Table 6-6. Current Consumption for Bluetooth LE in Active Mode

Work Mode	RF Condition	Description	Peak (mA)
Active (RF working)	TX	Bluetooth LE @ 20.2dBm	362
		Bluetooth LE @ 8.7dBm	206
		Bluetooth LE @ 0dBm	168
		Bluetooth LE @ −15dBm	105
	RX	Bluetooth LE	85

Table 6-7. Current Consumption for 802.15.4 in Active Mode

Work Mode	RF Condition	Description	Peak (mA)
Active (RF working)	TX	802.15.4 @ 20.2dBm	360
		802.15.4 @ 8.2dBm	206
		802.15.4 @ −1dBm	167
		802.15.4 @ −15dBm	105
	RX	802.15.4	85

Note:
The content below is excerpted from Section *Power Consumption in Other Modes* in *ESP32-C5 Series Datasheet*.

6.4.2 Current Consumption in Other Modes

Table 6-8. Current Consumption in Modem-sleep Mode

Mode	CPU Frequency (MHz)	Description	Typ (mA)	
			All Peripherals Clocks Disabled	All Peripherals Clocks Enabled[1]
Modem-sleep[2,3]	240	WAITI	18	27
		CPU while loop	26	35
		Run CoreMark	34	43
	160	WAITI	15	27
		CPU while loop	20	32
		Run CoreMark	26	37
	80	WAITI	12	24
		CPU while loop	15	26
		Run CoreMark	18	29
	40	WAITI	8	18
		CPU while loop	10	19
		Run CoreMark	12	21

[1] In practice, the current consumption might be different depending on which peripherals are enabled.

[2] In Modem-sleep mode, Wi-Fi is clock gated.

[3] In Modem-sleep mode, the consumption might be higher when accessing flash.

Table 6-9. Current Consumption in Low-Power Modes

Mode	Description	Typ (mA)
Light-sleep	CPU and wireless communication modules are powered down, peripheral clocks are disabled, and all GPIOs are high-impedance	0.25
	CPU, wireless communication modules and peripherals are powered down, and all GPIOs are high-impedance	0.06
Deep-sleep	RTC timer and LP memory are powered on	0.012
Power off	CHIP_PU is set to low level, the chip is powered off	0.002

6.5 Memory Specifications

The data below is sourced from the memory vendor datasheet. These values are guaranteed through design and/or characterization but are not fully tested in production. Devices are shipped with the memory erased.

Table 6-10. Flash Specifications

Parameter	Description	Min	Typ	Max	Unit
VCC	Power supply voltage (1.8 V)	1.65	1.80	2.00	V
	Power supply voltage (3.3 V)	2.7	3.3	3.6	V
F_C	Maximum clock frequency	80	—	—	MHz
—	Program/erase cycles	100,000	—	—	cycles
T_{RET}	Data retention time	20	—	—	years
T_{PP}	Page program time	—	0.8	5	ms
T_{SE}	Sector erase time (4 KB)	—	70	500	ms
T_{BE1}	Block erase time (32 KB)	—	0.2	2	s
T_{BE2}	Block erase time (64 KB)	—	0.3	3	s
T_{CE}	Chip erase time (16 Mb)	—	7	20	s
	Chip erase time (32 Mb)	—	20	60	s
	Chip erase time (64 Mb)	—	25	100	s
	Chip erase time (128 Mb)	—	60	200	s
	Chip erase time (256 Mb)	—	70	300	s

Table 6-11. PSRAM Specifications

Parameter	Description	Min	Typ	Max	Unit
VCC	Power supply voltage (1.8 V)	1.62	1.80	1.98	V
	Power supply voltage (3.3 V)	2.7	3.3	3.6	V
F_C	Maximum clock frequency	80	—	—	MHz

7 RF Characteristics

This section contains tables with RF characteristics of the Espressif product.

The RF data is measured at the antenna port, where RF cable is connected, including the front-end loss.

Devices should operate in the center frequency range allocated by regional regulatory authorities. The target center frequency range and the target transmit power are configurable by software. See ESP RF Test Tool and Test Guide for instructions.

Unless otherwise stated, the RF tests are conducted with a 3.3 V (±5%) supply at 25 °C ambient temperature.

7.1 2.4 GHz Wi-Fi Radio

Table 7-1. 2.4 GHz Wi-Fi RF Characteristics

Name	Description
Center frequency range of operating channel	2412 ~ 2484 MHz
Wi-Fi wireless standard	IEEE 802.11b/g/n/ax

7.1.1 2.4 GHz Wi-Fi RF Transmitter (TX) Characteristics

Table 7-2. 2.4 GHz TX Power with Spectral Mask and EVM Meeting 802.11 Standards

Rate	Min (dBm)	Typ (dBm)	Max (dBm)
802.11b, 1 Mbps, DSSS	—	19.5	—
802.11b, 11 Mbps, CCK	—	19.5	—
802.11g, 6 Mbps, OFDM	—	18.5	—
802.11g, 54 Mbps, OFDM	—	16.5	—
802.11n, HT20, MCS0	—	18.5	—
802.11n, HT20, MCS7	—	16.5	—
802.11n, HT40, MCS0	—	17.5	—
802.11n, HT40, MCS7	—	15.5	—
802.11ax, HE20, MCS0	—	18.5	—
802.11ax, HE20, MCS9	—	14.5	—

Table 7-3. 2.4 GHz TX EVM Test[1]

Rate	Min (dB)	Typ (dB)	Limit (dB)
802.11b, 1 Mbps, DSSS	—	-25.0	-10.0
802.11b, 11 Mbps, CCK	—	-25.0	-10.0
802.11g, 6 Mbps, OFDM	—	-22.0	-5.0

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Table 7-3 – cont'd from previous page

Rate	Min (dB)	Typ (dB)	Limit (dB)
802.11g, 54 Mbps, OFDM	—	–30.0	–25.0
802.11n, HT20, MCS0	—	–22.0	–5.0
802.11n, HT20, MCS7	—	–31.5	–27.0
802.11n, HT40, MCS0	—	–22.0	–5.0
802.11n, HT40, MCS7	—	–31.5	–27.0
802.11ax, HE20, MCS0	—	–22.0	–5.0
802.11ax, HE20, MCS9	—	–34.0	–32.0

[1] EVM is measured at the corresponding typical TX power provided in Table *7-2 2.4 GHz TX Power with Spectral Mask and EVM Meeting 802.11 Standards* above.

7.1.2 2.4 GHz Wi-Fi RF Receiver (RX) Characteristics

For RX tests, the PER (packet error rate) limit is 8% for 802.11b, and 10% for 802.11g/n/ax.

Table 7-4. 2.4 GHz RX Sensitivity

Rate	Min (dBm)	Typ (dBm)	Max (dBm)
802.11b, 1 Mbps, DSSS	—	–99.5	—
802.11b, 2 Mbps, DSSS	—	–97.0	—
802.11b, 5.5 Mbps, CCK	—	–93.5	—
802.11b, 11 Mbps, CCK	—	–90.0	—
802.11g, 6 Mbps, OFDM	—	–95.0	—
802.11g, 9 Mbps, OFDM	—	–93.5	—
802.11g, 12 Mbps, OFDM	—	–92.5	—
802.11g, 18 Mbps, OFDM	—	–90.0	—
802.11g, 24 Mbps, OFDM	—	–87.0	—
802.11g, 36 Mbps, OFDM	—	–83.5	—
802.11g, 48 Mbps, OFDM	—	–79.0	—
802.11g, 54 Mbps, OFDM	—	–78.0	—
802.11n, HT20, MCS0	—	–94.5	—
802.11n, HT20, MCS1	—	–92.5	—
802.11n, HT20, MCS2	—	–90.0	—
802.11n, HT20, MCS3	—	–86.5	—
802.11n, HT20, MCS4	—	–83.5	—
802.11n, HT20, MCS5	—	–79.0	—
802.11n, HT20, MCS6	—	–77.0	—
802.11n, HT20, MCS7	—	–76.0	—
802.11n, HT40, MCS0	—	–91.5	—
802.11n, HT40, MCS1	—	–89.5	—
802.11n, HT40, MCS2	—	–87.0	—

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Table 7-4 – cont'd from previous page

Rate	Min (dBm)	Typ (dBm)	Max (dBm)
802.11n, HT40, MCS3	—	–83.0	—
802.11n, HT40, MCS4	—	–80.5	—
802.11n, HT40, MCS5	—	–76.0	—
802.11n, HT40, MCS6	—	–74.0	—
802.11n, HT40, MCS7	—	–73.0	—
802.11ax, HE20, MCS0	—	–94.0	—
802.11ax, HE20, MCS1	—	–91.0	—
802.11ax, HE20, MCS2	—	–88.5	—
802.11ax, HE20, MCS3	—	–85.5	—
802.11ax, HE20, MCS4	—	–82.5	—
802.11ax, HE20, MCS5	—	–78.5	—
802.11ax, HE20, MCS6	—	–77.0	—
802.11ax, HE20, MCS7	—	–75.5	—
802.11ax, HE20, MCS8	—	–71.5	—
802.11ax, HE20, MCS9	—	–69.5	—

Table 7-5. 2.4 GHz Maximum RX Level

Rate	Min (dBm)	Typ (dBm)	Max (dBm)
802.11b, 1 Mbps, DSSS	—	5	—
802.11b, 11 Mbps, CCK	—	5	—
802.11g, 6 Mbps, OFDM	—	5	—
802.11g, 54 Mbps, OFDM	—	0	—
802.11n, HT20, MCS0	—	5	—
802.11n, HT20, MCS7	—	0	—
802.11n, HT40, MCS0	—	5	—
802.11n, HT40, MCS7	—	0	—
802.11ax, HE20, MCS0	—	5	—
802.11ax, HE20, MCS9	—	0	—

Table 7-6. 2.4 GHz RX Adjacent Channel Rejection

Rate	Min (dB)	Typ (dB)	Max (dB)
802.11b, 1 Mbps, DSSS	—	41	—
802.11b, 11 Mbps, CCK	—	40	—
802.11g, 6 Mbps, OFDM	—	37	—
802.11g, 54 Mbps, OFDM	—	17	—
802.11n, HT20, MCS0	—	34	—

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Table 7-6 – cont'd from previous page

Rate	Min (dB)	Typ (dB)	Max (dB)
802.11n, HT20, MCS7	—	16	—
802.11n, HT40, MCS0	—	24	—
802.11n, HT40, MCS7	—	13	—
802.11ax, HE20, MCS0	—	38	—
802.11ax, HE20, MCS9	—	12	—

7.2 5 GHz Wi-Fi Radio

Table 7-7. 5 GHz Wi-Fi RF Characteristics

Name	Description
Center frequency range of operating channel	5180 ~ 5885 MHz
Wi-Fi wireless standard	IEEE 802.11a/n/ac/ax

7.2.1 5 GHz Wi-Fi RF Transmitter (TX) Characteristics

Table 7-8. 5 GHz TX Power with Spectral Mask and EVM Meeting 802.11 Standards

Rate	Min (dBm)	Typ (dBm)	Max (dBm)
802.11a, 6 Mbps, OFDM	—	18.5	—
802.11a, 54 Mbps, OFDM	—	16.5	—
802.11n, HT20, MCS0	—	18.5	—
802.11n, HT20, MCS7	—	15.5	—
802.11n, HT40, MCS0	—	17.5	—
802.11n, HT40, MCS7	—	14.5	—
802.11ac, VHT20, MCS0	—	18.5	—
802.11ac, VHT20, MCS7	—	15.5	—
802.11ax, HE20, MCS0	—	18.5	—
802.11ax, HE20, MCS7	—	15.5	—

Table 7-9. 5 GHz TX EVM Test[1]

Rate	Min (dB)	Typ (dB)	Limit (dB)
802.11a, 6 Mbps, OFDM	—	–25.0	–5.0
802.11a, 54 Mbps, OFDM	—	–29.0	–25.0
802.11n, HT20, MCS0	—	–25.0	–5.0
802.11n, HT20, MCS7	—	–31.0	–27.0
802.11n, HT40, MCS0	—	–25.0	–5.0

Cont'd on next page

Table 7-9 – cont'd from previous page

Rate	Min (dB)	Typ (dB)	Limit (dB)
802.11n, HT40, MCS7	—	–31.0	–27.0
802.11ac, VHT20, MCS0	—	–25.0	–5.0
802.11ac, VHT20, MCS7	—	–31.0	–27.0
802.11ax, HE20, MCS0	—	–25.0	–5.0
802.11ax, HE20, MCS7	—	–31.5	–27.0

[1] EVM is measured at the corresponding typical TX power provided in Table 7-8 *5 GHz TX Power with Spectral Mask and EVM Meeting 802.11 Standards* above.

7.2.2 5 GHz Wi-Fi RF Receiver (RX) Characteristics

For RX tests, the PER (packet error rate) limit is 10% for 802.11a/n/ac/ax.

Table 7-10. 5 GHz RX Sensitivity

Rate	Min (dBm)	Typ (dBm)	Max (dBm)
802.11a, 6 Mbps, OFDM	—	–94.0	—
802.11a, 9 Mbps, OFDM	—	–93.0	—
802.11a, 12 Mbps, OFDM	—	–91.5	—
802.11a, 18 Mbps, OFDM	—	–89.5	—
802.11a, 24 Mbps, OFDM	—	–86.5	—
802.11a, 36 Mbps, OFDM	—	–83.0	—
802.11a, 48 Mbps, OFDM	—	–78.5	—
802.11a, 54 Mbps, OFDM	—	–77.0	—
802.11n, HT20, MCS0	—	–93.5	—
802.11n, HT20, MCS1	—	–92.0	—
802.11n, HT20, MCS2	—	–89.5	—
802.11n, HT20, MCS3	—	–85.5	—
802.11n, HT20, MCS4	—	–82.5	—
802.11n, HT20, MCS5	—	–78.5	—
802.11n, HT20, MCS6	—	–76.5	—
802.11n, HT20, MCS7	—	–75.5	—
802.11n, HT40, MCS0	—	–90.5	—
802.11n, HT40, MCS1	—	–89.0	—
802.11n, HT40, MCS2	—	–86.5	—
802.11n, HT40, MCS3	—	–82.5	—
802.11n, HT40, MCS4	—	–79.5	—
802.11n, HT40, MCS5	—	–75.5	—
802.11n, HT40, MCS6	—	–73.5	—
802.11n, HT40, MCS7	—	–72.5	—
802.11ac, VHT20, MCS0	—	–93.5	—

Cont'd on next page

Table 7-10 – cont'd from previous page

Rate	Min (dBm)	Typ (dBm)	Max (dBm)
802.11ac, VHT20, MCS1	—	–92.0	—
802.11ac, VHT20, MCS2	—	–89.5	—
802.11ac, VHT20, MCS3	—	–85.5	—
802.11ac, VHT20, MCS4	—	–82.5	—
802.11ac, VHT20, MCS5	—	–78.0	—
802.11ac, VHT20, MCS6	—	–76.5	—
802.11ac, VHT20, MCS7	—	–75.5	—
802.11ax, HE20, MCS0	—	–93.5	—
802.11ax, HE20, MCS1	—	–90.5	—
802.11ax, HE20, MCS2	—	–88.0	—
802.11ax, HE20, MCS3	—	–85.0	—
802.11ax, HE20, MCS4	—	–81.5	—
802.11ax, HE20, MCS5	—	–77.5	—
802.11ax, HE20, MCS6	—	–76.5	—
802.11ax, HE20, MCS7	—	–74.5	—

Table 7-11. 5 GHz Maximum RX Level

Rate	Min (dBm)	Typ (dBm)	Max (dBm)
802.11a, 6 Mbps, OFDM	—	5	—
802.11a, 54 Mbps, OFDM	—	0	—
802.11n, HT20, MCS0	—	5	—
802.11n, HT20, MCS7	—	0	—
802.11n, HT40, MCS0	—	5	—
802.11n, HT40, MCS7	—	0	—
802.11ac, VHT20, MCS0	—	5	—
802.11ac, VHT20, MCS7	—	0	—
802.11ax, HE20, MCS0	—	5	—
802.11ax, HE20, MCS7	—	0	—

Table 7-12. 5 GHz RX Adjacent Channel Rejection

Rate	Min (dB)	Typ (dB)	Max (dB)
802.11a, 6 Mbps, OFDM	—	29	—
802.11a, 54 Mbps, OFDM	—	9	—
802.11n, HT20, MCS0	—	26	—
802.11n, HT20, MCS7	—	8	—
802.11n, HT40, MCS0	—	29	—

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Table 7-12 – cont'd from previous page

Rate	Min (dB)	Typ (dB)	Max (dB)
802.11n, HT40, MCS7	—	11	—
802.11ac, VHT20, MCS0	—	25	—
802.11ac, VHT20, MCS7	—	6	—
802.11ax, HE20, MCS0	—	25	—
802.11ax, HE20, MCS7	—	6	—

7.3 Bluetooth 5 (LE) Radio

Table 7-13. Bluetooth LE RF Characteristics

Name	Description
Center frequency range of operating channel	2402 ~ 2480 MHz
RF transmit power range	–15~20 dBm

7.3.1 Bluetooth LE RF Transmitter (TX) Characteristics

Table 7-14. Bluetooth LE - Transmitter Characteristics - 1 Mbps

Parameter	Description	Min	Typ	Max	Unit
Carrier frequency offset and drift	Max. $\lvert f_n \rvert_{n=0,\,1,\,2,\,3,\,\ldots k}$	—	7.0	—	kHz
	Max. $\lvert f_0 - f_n \rvert_{n=2,\,3,\,4,\,\ldots k}$	—	0.6	—	kHz
	Max. $\lvert f_n - f_{n-5} \rvert_{n=6,\,7,\,8,\,\ldots k}$	—	0.6	—	kHz
	$\lvert f_1 - f_0 \rvert$	—	0.3	—	kHz
Modulation characteristics	$\Delta\, F1_{\text{avg}}$	—	250.0	—	kHz
	Min. $\Delta\, F2_{\text{max}}$ (for at least 99.9% of all $\Delta\, F2_{\text{max}}$)	—	255.0	—	kHz
	$\Delta\, F2_{\text{avg}} / \Delta\, F1_{\text{avg}}$	—	0.98	—	—
In-band emissions	± 2 MHz offset	—	–33	—	dBm
	± 3 MHz offset	—	–40	—	dBm
	> ± 3 MHz offset	—	–45	—	dBm

Table 7-15. Bluetooth LE - Transmitter Characteristics - 2 Mbps

Parameter	Description	Min	Typ	Max	Unit
Carrier frequency offset and drift	Max. $\lvert f_n \rvert_{n=0,\,1,\,2,\,3,\,\ldots k}$	—	7.0	—	kHz
	Max. $\lvert f_0 - f_n \rvert_{n=2,\,3,\,4,\,\ldots k}$	—	0.6	—	kHz
	Max. $\lvert f_n - f_{n-5} \rvert_{n=6,\,7,\,8,\,\ldots k}$	—	0.7	—	kHz
	$\lvert f_1 - f_0 \rvert$	—	0.3	—	kHz
Modulation characteristics	$\Delta\, F1_{\text{avg}}$	—	495.1	—	kHz

Cont'd on next page

Table 7-15 – cont'd from previous page

Parameter	Description	Min	Typ	Max	Unit
	Min. $\Delta F2_{max}$ (for at least 99.9% of all $\Delta F2_{max}$)	–	515.0	–	kHz
	$\Delta F2_{avg}/\Delta F1_{avg}$	–	0.99	–	–
In-band emissions	± 4 MHz offset	–	–43	–	dBm
	± 5 MHz offset	–	–45	–	dBm
	> ± 5 MHz offset	–	–45	–	dBm

Table 7-16. Bluetooth LE - Transmitter Characteristics - 125 Kbps

Parameter	Description	Min	Typ	Max	Unit
Carrier frequency offset and drift	Max. $\lvert f_n \rvert_{n=0,\,1,\,2,\,3,\,\ldots k}$	–	7.0	–	kHz
	Max. $\lvert f_0 - f_n \rvert_{n=1,\,2,\,3,\,\ldots k}$	–	0.3	–	kHz
	$\lvert f_0 - f_3 \rvert$	–	0.3	–	kHz
	Max. $\lvert f_n - f_{n-3} \rvert_{n=7,\,8,\,9,\,\ldots k}$	–	0.4	–	kHz
Modulation characteristics	$\Delta F1_{avg}$	–	251.2	–	kHz
	Min. $\Delta F1_{max}$ (for at least 99.9% of all $\Delta F1_{max}$)	–	256.7	–	kHz
In-band emissions	± 2 MHz offset	–	–31	–	dBm
	± 3 MHz offset	–	–40	–	dBm
	> ± 3 MHz offset	–	–43	–	dBm

Table 7-17. Bluetooth LE - Transmitter Characteristics - 500 Kbps

Parameter	Description	Min	Typ	Max	Unit
Carrier frequency offset and drift	Max. $\lvert f_n \rvert_{n=0,\,1,\,2,\,3,\,\ldots k}$	–	7.0	–	kHz
	Max. $\lvert f_0 - f_n \rvert_{n=1,\,2,\,3,\,\ldots k}$	–	0.5	–	kHz
	$\lvert f_0 - f_3 \rvert$	–	0.2	–	kHz
	Max. $\lvert f_n - f_{n-3} \rvert_{n=7,\,8,\,9,\,\ldots k}$	–	0.5	–	kHz
Modulation characteristics	$\Delta F2_{avg}$	–	246.3	–	kHz
	Min. $\Delta F2_{max}$ (for at least 99.9% of all $\Delta F2_{max}$)	–	253.3	–	kHz
In-band emissions	± 2 MHz offset	–	–31	–	dBm
	± 3 MHz offset	–	–40	–	dBm
	> ± 3 MHz offset	–	–43	–	dBm

7.3.2 Bluetooth LE RF Receiver (RX) Characteristics

Table 7-18. Bluetooth LE - Receiver Characteristics - 1 Mbps

Parameter	Description	Min	Typ	Max	Unit
Sensitivity @30.8% PER	–	–	–98.0	–	dBm
Maximum received signal @30.8% PER	–	–	5	–	dBm

Cont'd on next page

Table 7-18 – cont'd from previous page

Parameter		Description	Min	Typ	Max	Unit
C/I and receiver selectivity performance	Co-channel	F = F0 MHz	—	9	—	dB
	Adjacent channel	F = F0 + 1 MHz	—	–4	—	dB
		F = F0 – 1 MHz	—	–3	—	dB
		F = F0 + 2 MHz	—	–31	—	dB
		F = F0 – 2 MHz	—	–34	—	dB
		F = F0 + 3 MHz	—	–33	—	dB
		F = F0 – 3 MHz	—	–43	—	dB
		F ≥ F0 + 4 MHz	—	–37	—	dB
		F ≤ F0 – 4 MHz	—	–50	—	dB
	Image frequency	—	—	–28	—	dB
	Adjacent channel to image frequency	F = F_{image} + 1 MHz	—	–27	—	dB
		F = F_{image} – 1 MHz	—	–30	—	dB
Out-of-band blocking performance		30 MHz ~ 2000 MHz	—	–13	—	dBm
		2003 MHz ~ 2399 MHz	—	–25	—	dBm
		2484 MHz ~ 2997 MHz	—	–20	—	dBm
		3000 MHz ~ 12.75 GHz	—	–20	—	dBm
Intermodulation		—	—	–41	—	dBm

Table 7-19. Bluetooth LE - Receiver Characteristics - 2 Mbps

Parameter		Description	Min	Typ	Max	Unit
Sensitivity @30.8% PER		—	—	–95.0	—	dBm
Maximum received signal @30.8% PER		—	—	5	—	dBm
C/I and receiver selectivity performance	Co-channel	F = F0 MHz	—	8	—	dB
	Adjacent channel	F = F0 + 2 MHz	—	–8	—	dB
		F = F0 – 2 MHz	—	–10	—	dB
		F = F0 + 4 MHz	—	–27	—	dB
		F = F0 – 4 MHz	—	–42	—	dB
		F = F0 + 6 MHz	—	–39	—	dB
		F = F0 – 6 MHz	—	–50	—	dB
		F ≥ F0 + 8 MHz	—	–48	—	dB
		F ≤ F0 – 8 MHz	—	–54	—	dB
	Image frequency	—	—	–27	—	dB
	Adjacent channel to image frequency	F = F_{image} + 2 MHz	—	–26	—	dB
		F = F_{image} – 2 MHz	—	–28	—	dB
Out-of-band blocking performance		30 MHz ~ 2000 MHz	—	–13	—	dBm
		2003 MHz ~ 2399 MHz	—	–25	—	dBm
		2484 MHz ~ 2997 MHz	—	–20	—	dBm
		3000 MHz ~ 12.75 GHz	—	–20	—	dBm
Intermodulation		—	—	–39	—	dBm

Table 7-20. Bluetooth LE - Receiver Characteristics - 125 Kbps

Parameter		Description	Min	Typ	Max	Unit
Sensitivity @30.8% PER		—	—	–106.0	—	dBm
Maximum received signal @30.8% PER		—	—	5	—	dBm
C/I and receiver selectivity performance	Co-channel	F = F0 MHz	—	3	—	dB
	Adjacent channel	F = F0 + 1 MHz	—	–6	—	dB
		F = F0 – 1 MHz	—	–7	—	dB
		F = F0 + 2 MHz	—	–34	—	dB
		F = F0 – 2 MHz	—	–39	—	dB
		F = F0 + 3 MHz	—	–30	—	dB
		F = F0 – 3 MHz	—	–47	—	dB
		F ≥ F0 + 4 MHz	—	–46	—	dB
		F ≤ F0 – 4 MHz	—	–54	—	dB
	Image frequency	—	—	–28	—	dB
	Adjacent channel to image frequency	F = F_{image} + 1 MHz	—	–34	—	dB
		F = F_{image} – 1 MHz	—	–31	—	dB

Table 7-21. Bluetooth LE - Receiver Characteristics - 500 Kbps

Parameter		Description	Min	Typ	Max	Unit
Sensitivity @30.8% PER		—	—	–102.0	—	dBm
Maximum received signal @30.8% PER		—	—	5	—	dBm
C/I and receiver selectivity performance	Co-channel	F = F0 MHz	—	3	—	dB
	Adjacent channel	F = F0 + 1 MHz	—	–6	—	dB
		F = F0 – 1 MHz	—	–7	—	dB
		F = F0 + 2 MHz	—	–33	—	dB
		F = F0 – 2 MHz	—	–38	—	dB
		F = F0 + 3 MHz	—	–38	—	dB
		F = F0 – 3 MHz	—	–47	—	dB
		F ≥ F0 + 4 MHz	—	–41	—	dB
		F ≤ F0 – 4 MHz	—	–52	—	dB
	Image frequency	—	—	–23	—	dB
	Adjacent channel to image frequency	F = F_{image} + 1 MHz	—	–29	—	dB
		F = F_{image} – 1 MHz	—	–29	—	dB

7.4 802.15.4 Radio

Table 7-22. 802.15.4 RF Characteristics

Name	Description
Center frequency range of operating channel	2405 ~ 2480 MHz

[1] Zigbee in the 2.4 GHz range supports 16 channels at 5 MHz spacing from channel 11 to channel 26.

7.4.1 802.15.4 RF Transmitter (TX) Characteristics

Table 7-23. 802.15.4 Transmitter Characteristics - 250 Kbps

Parameter	Min	Typ	Max	Unit
RF transmit power range	–15.0	—	20.0	dBm
EVM	—	4.0%	—	—

7.4.2 802.15.4 RF Receiver (RX) Characteristics

Table 7-24. 802.15.4 Receiver Characteristics - 250 Kbps

Parameter		Description	Min	Typ	Max	Unit
Sensitivity @1% PER		—	—	–103.5	—	dBm
Maximum received signal @1% PER		—	—	5	—	dBm
Relative jamming level	Adjacent channel	F = F0 + 5 MHz	—	28	—	dB
		F = F0 – 5 MHz	—	32	—	dB
	Alternate channel	F = F0 + 10 MHz	—	48	—	dB
		F = F0 – 10 MHz	—	53	—	dB

8 Module Schematics

This is the reference design of the module.

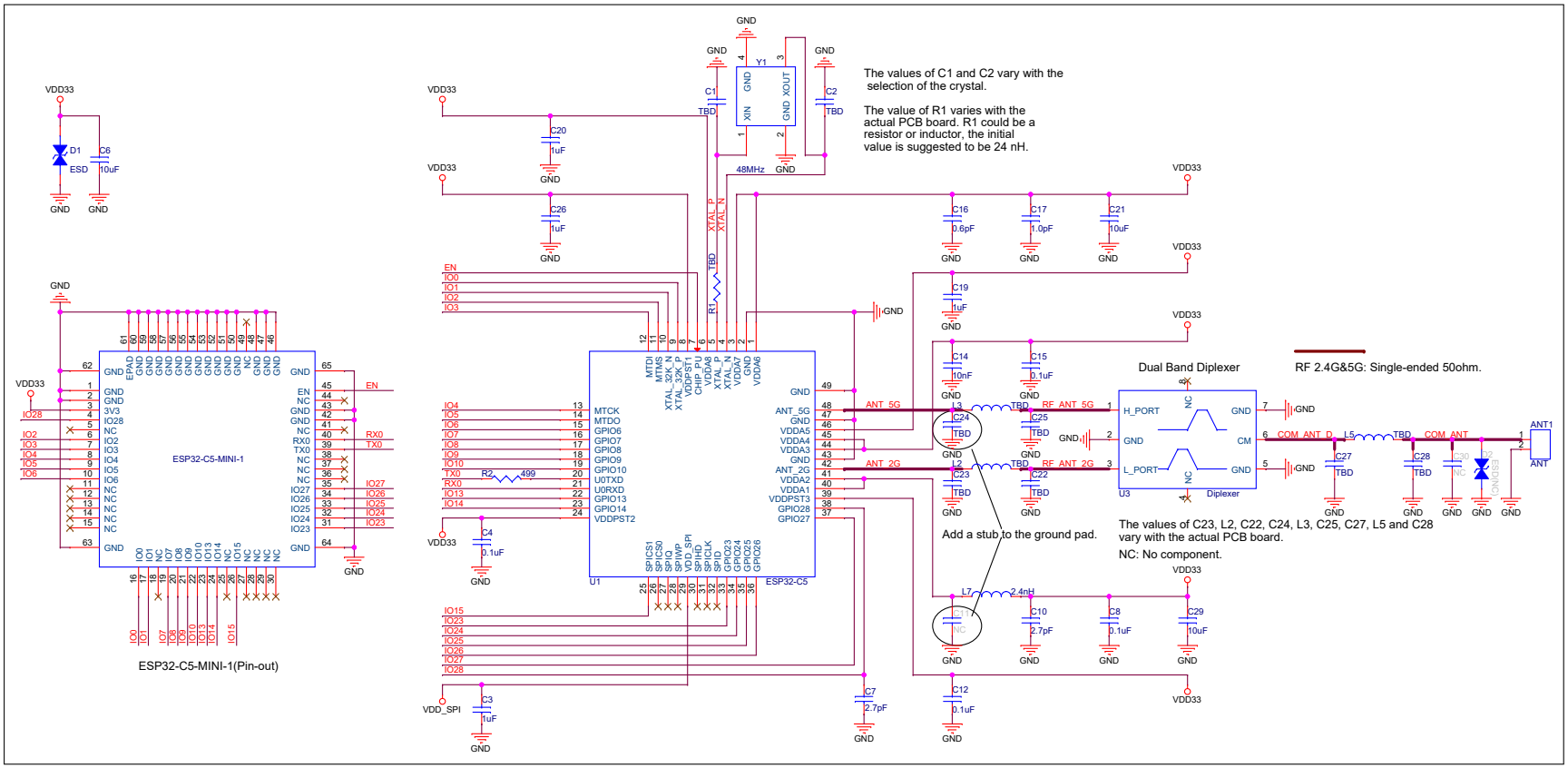

Figure 8-1. ESP32-C5-MINI-1 Schematics

9 Peripheral Schematics

This is the typical application circuit of the module connected with peripheral components (for example, power supply, antenna, reset button, JTAG interface, and UART interface).

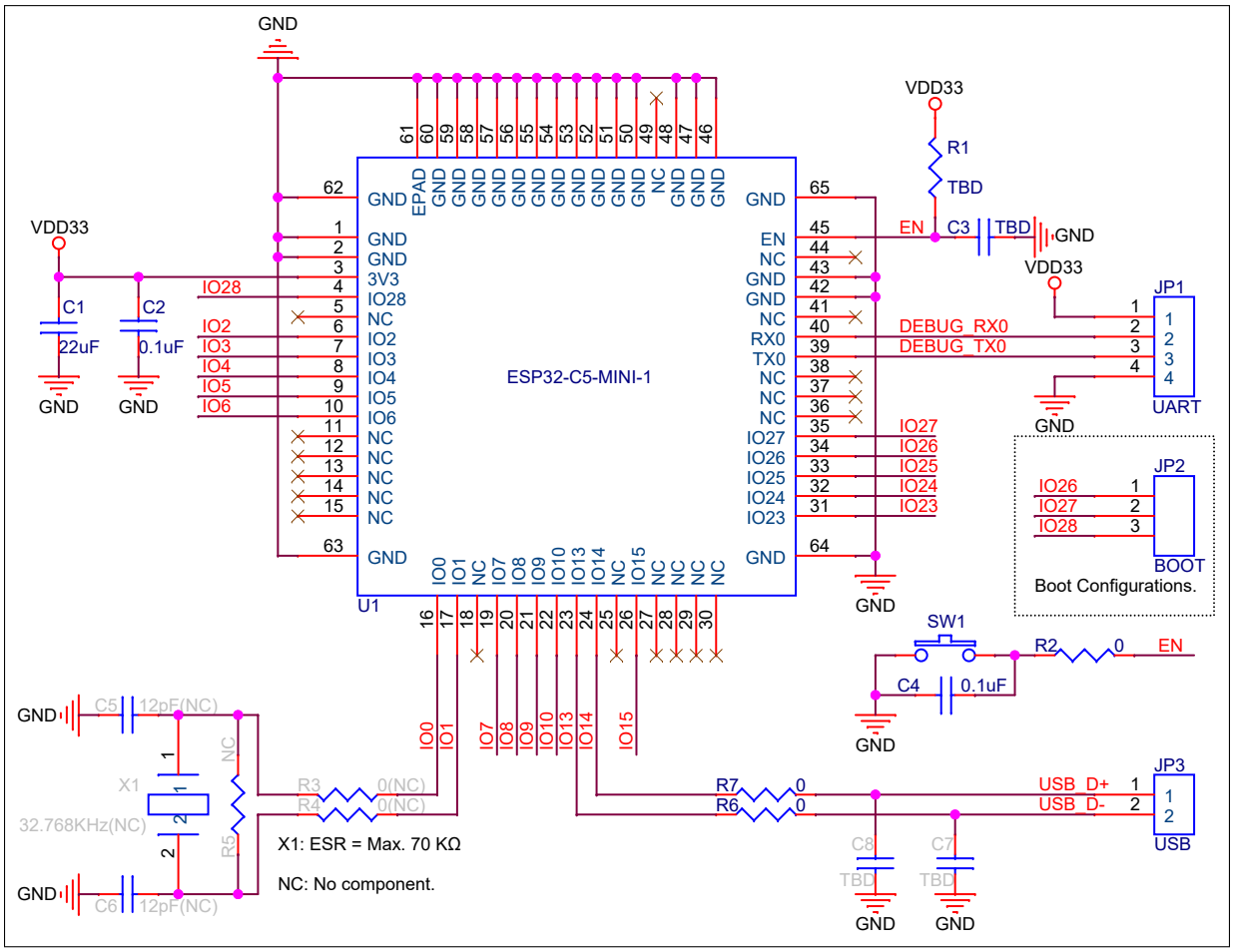

Figure 9-1. ESP32-C5-MINI-1 Peripheral Schematics

- Please control the voltage levels of strapping pins. For more details, please refer to Chapter *4 Boot Configurations*.
- Soldering the EPAD to the ground of the base board is not a must, however, it can optimize thermal performance. If you choose to solder it, please apply the correct amount of soldering paste. Too much soldering paste may increase the gap between the module and the baseboard. As a result, the adhesion between other pins and the baseboard may be poor.
- To ensure that the power supply to the ESP32-C5 chip is stable during power-up, it is advised to add an RC delay circuit at the EN pin. The recommended setting for the RC delay circuit is usually R = 10 kΩ and C = 1 μF. However, specific parameters should be adjusted based on the power-up timing of the module and the power-up and reset sequence timing of the chip. For ESP32-C5's power-up and reset sequence timing diagram, please refer Section *4.5 Chip Power-up and Reset*.

10 Module Dimensions

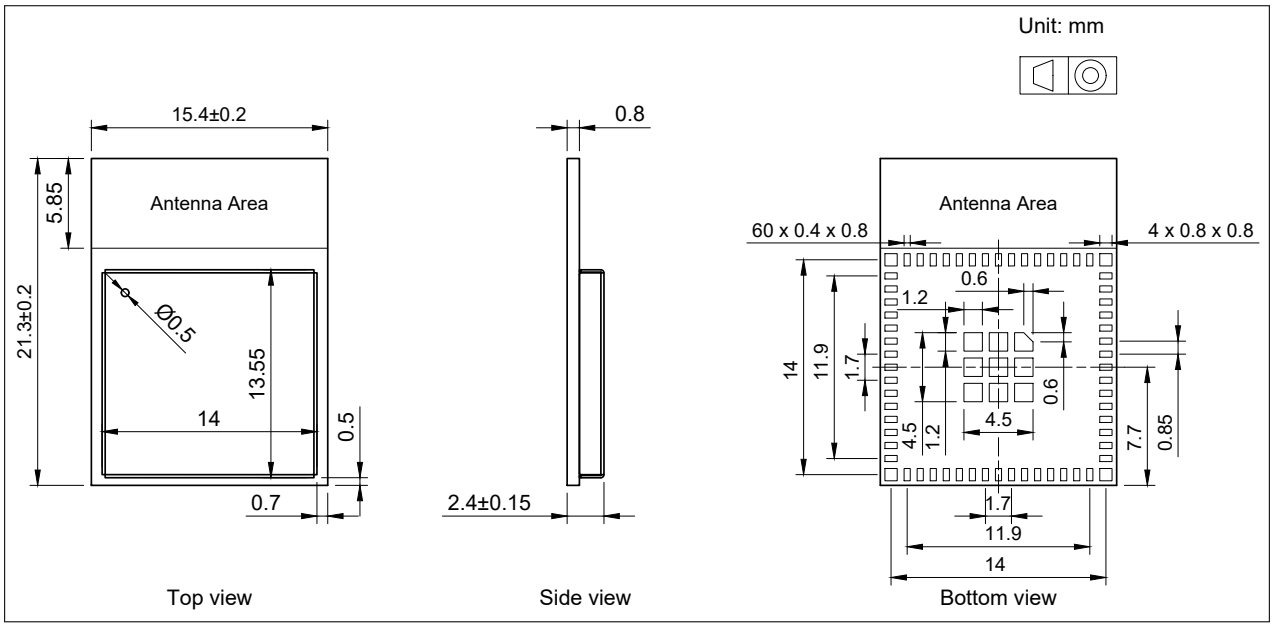

Figure 10-1. ESP32-C5-MINI-1 Physical Dimensions

Note:

For information about tape, reel, and product marking, please refer to *ESP32-C5 Module Packaging Information*.

11 PCB Layout Recommendations

11.1 PCB Land Pattern

This section provides the following resources for your reference:

- Figures for recommended PCB land patterns with all the dimensions needed for PCB design. See Figure 11-1 *ESP32-C5-MINI-1 Recommended PCB Land Pattern*.
- Source files of recommended PCB land patterns to measure dimensions not covered in Figure 11-1. You can view the source files for ESP32-C5-MINI-1 with Autodesk Viewer.

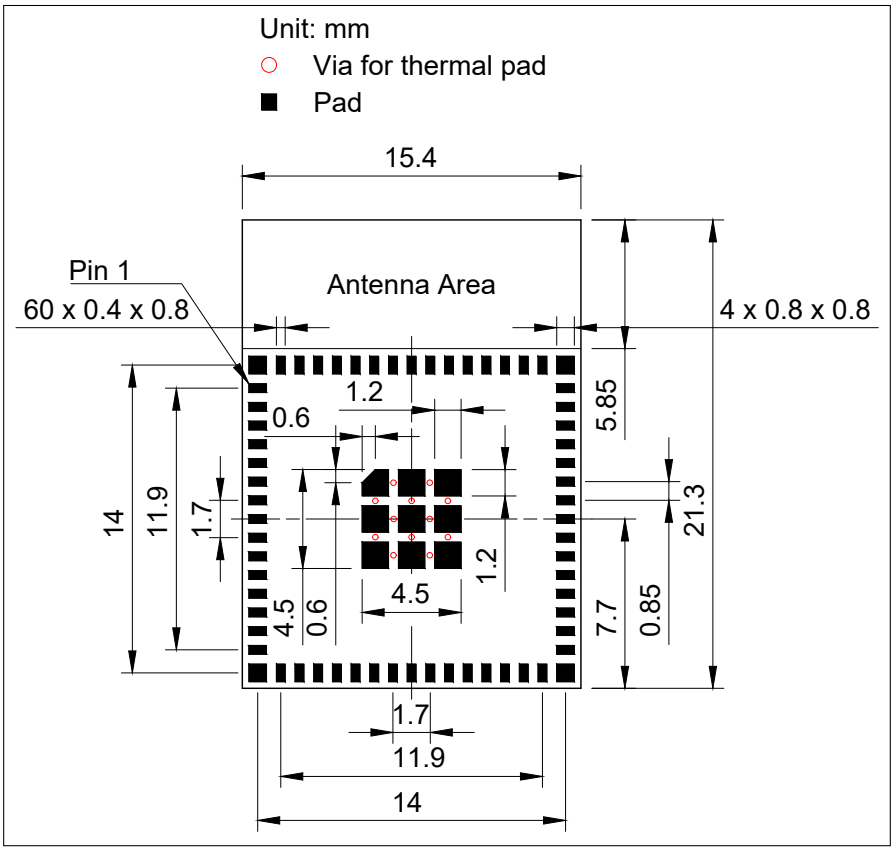

Figure 11-1. ESP32-C5-MINI-1 Recommended PCB Land Pattern

11.2 Module Placement for PCB Design

If module-on-board design is adopted, attention should be paid while positioning the module on the base board. The interference of the base board on the module's antenna performance should be minimized.

For details about module placement for PCB design, please refer to *ESP32-C5 Hardware Design Guidelines* > Section *General Principles of PCB Layout for Modules*.

12 Product Handling

12.1 Storage Conditions

The products sealed in moisture barrier bags (MBB) should be stored in a non-condensing atmospheric environment of < 40 °C and 90%RH. The module is rated at the moisture sensitivity level (MSL) of 3.

After unpacking, the module must be soldered within 168 hours with the factory conditions 25±5 °C and 60%RH. If the above conditions are not met, the module needs to be baked.

12.2 Electrostatic Discharge (ESD)

- Human body model (HBM): ±2000 V
- Charged-device model (CDM): ±500 V

12.3 Reflow Profile

Solder the module in a single reflow.

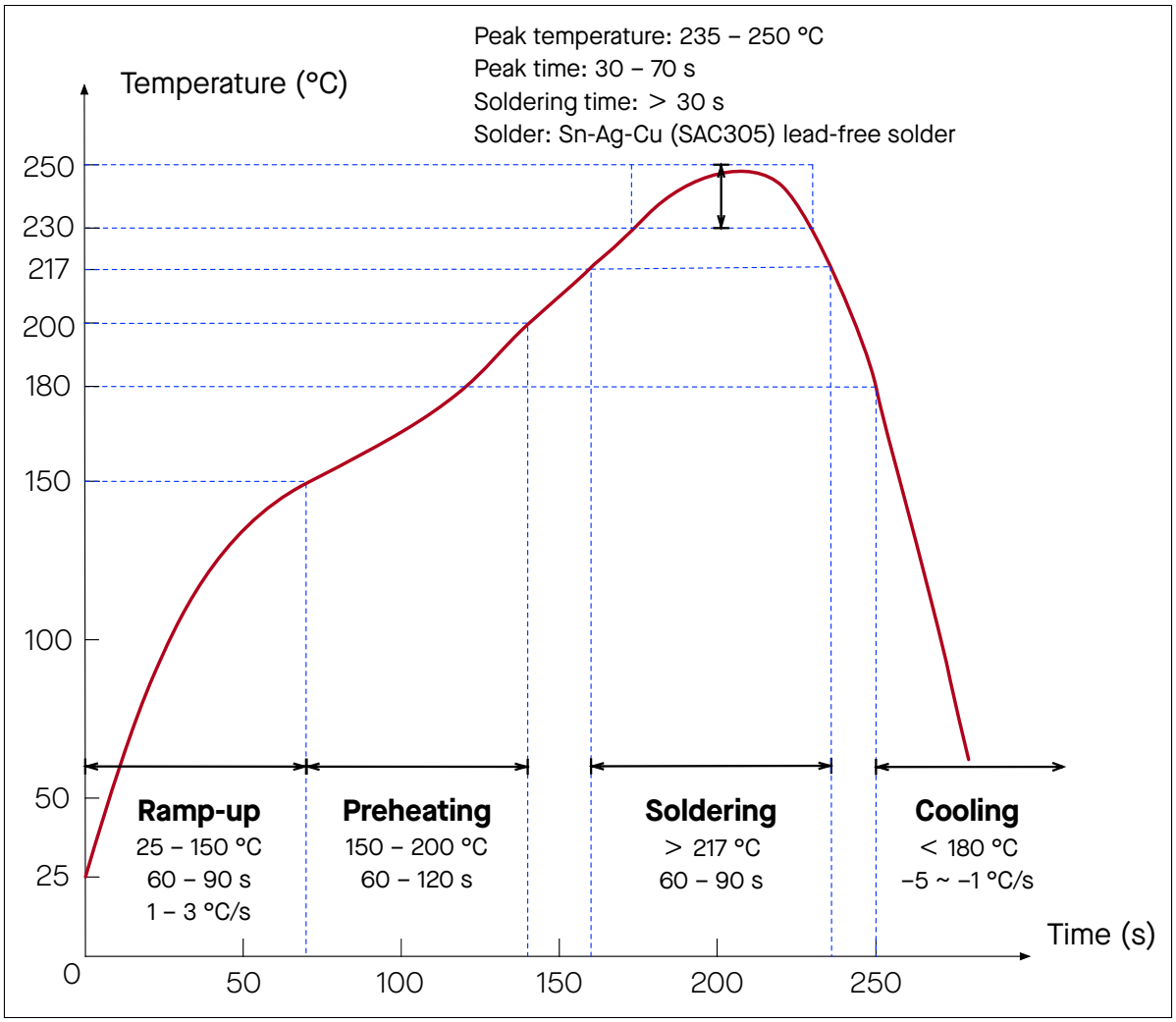

Figure 12-1. Reflow Profile

12.4 Ultrasonic Vibration

Avoid exposing Espressif modules to vibration from ultrasonic equipment, such as ultrasonic welders or ultrasonic cleaners. This vibration may induce resonance in the in-module crystal and lead to its malfunction or even failure. As a consequence, **the module may stop working or its performance may deteriorate**.

Datasheet Versioning

Datasheet Version	Status	Watermark	Definition
v0.1 ~ v0.5 (excluding v0.5)	Draft	Confidential	This datasheet is under development for products in the design stage. Specifications may change without prior notice.
v0.5 ~ v1.0 (excluding v1.0)	Preliminary release	Preliminary	This datasheet is actively updated for products in the verification stage. Specifications may change before mass production, and the changes will be documentation in the datasheet's Revision History.
v1.0 and higher	Official release	—	This datasheet is publicly released for products in mass production. Specifications are finalized, and major changes will be communicated via Product Change Notifications (PCN).
Any version	—	Not Recommended for New Design (NRND)[1]	This datasheet is updated less frequently for products not recommended for new designs.
Any version	—	End of Life (EOL)[2]	This datasheet is no longer mtained for products that have reached end of life.

[1] Watermark will be added to the datasheet title page only when all the product variants covered by this datasheet are not recommended for new designs.

[2] Watermark will be added to the datasheet title page only when all the product variants covered by this datasheet have reached end of life.

Related Documentation and Resources

Related Documentation

- *ESP32-C5 Series Datasheet* - Specifications of the ESP32-C5 hardware.
- *ESP32-C5 Technical Reference Manual* – Detailed information on how to use the ESP32-C5 memory and peripherals.
- *ESP32-C5 Hardware Design Guidelines* – Guidelines on how to integrate the ESP32-C5 into your hardware product.
- *ESP32-C5 Series SoC Errata* – Descriptions of known errors in ESP32-C5 series of SoCs.
- *Certificates*
  https://espressif.com/en/support/documents/certificates
- *ESP32-C5 Product/Process Change Notifications (PCN)*
  https://espressif.com/en/support/documents/pcns?keys=ESP32-C5
- *ESP32-C5 Advisories* – Information on security, bugs, compatibility, component reliability.
  https://espressif.com/en/support/documents/advisories?keys=ESP32-C5
- *Documentation Updates and Update Notification Subscription*
  https://espressif.com/en/support/download/documents

Developer Zone

- ESP-IDF Programming Guide for ESP32-C5 – Extensive documentation for the ESP-IDF development framework.
- *ESP-IDF* and other development frameworks on GitHub.
  https://github.com/espressif
- *ESP32 BBS Forum* – Engineer-to-Engineer (E2E) Community for Espressif products where you can post questions, share knowledge, explore ideas, and help solve problems with fellow engineers.
  https://esp32.com/
- *ESP-FAQ* – A summary document of frequently asked questions released by Espressif.
  https://espressif.com/projects/esp-faq/en/latest/index.html
- *The ESP Journal* – Best Practices, Articles, and Notes from Espressif folks.
  https://blog.espressif.com/
- See the tabs *SDKs and Demos*, *Apps*, *Tools*, *AT Firmware*.
  https://espressif.com/en/support/download/sdks-demos

Products

- *ESP32-C5 Series SoCs* – Browse through all ESP32-C5 SoCs.
  https://espressif.com/en/products/socs?id=ESP32-C5
- *ESP32-C5 Series Modules* – Browse through all ESP32-C5-based modules.
  https://espressif.com/en/products/modules?id=ESP32-C5
- *ESP32-C5 Series DevKits* – Browse through all ESP32-C5-based devkits.
  https://espressif.com/en/products/devkits?id=ESP32-C5
- *ESP Product Selector* – Find an Espressif hardware product suitable for your needs by comparing or applying filters.
  https://products.espressif.com/#/product-selector?language=en

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Revision History

Date	Version	Release notes
2025-12-04	v1.0	Official release

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