NAME: GINI CHACKO

SEMESTER: IV

CLASS: SE COMPS B

BATCH: B

ROLL: 8942

TOPIC: MP EXPERIMENT 8:

Write short note on

- **8255**
- **8237**
- **8259**

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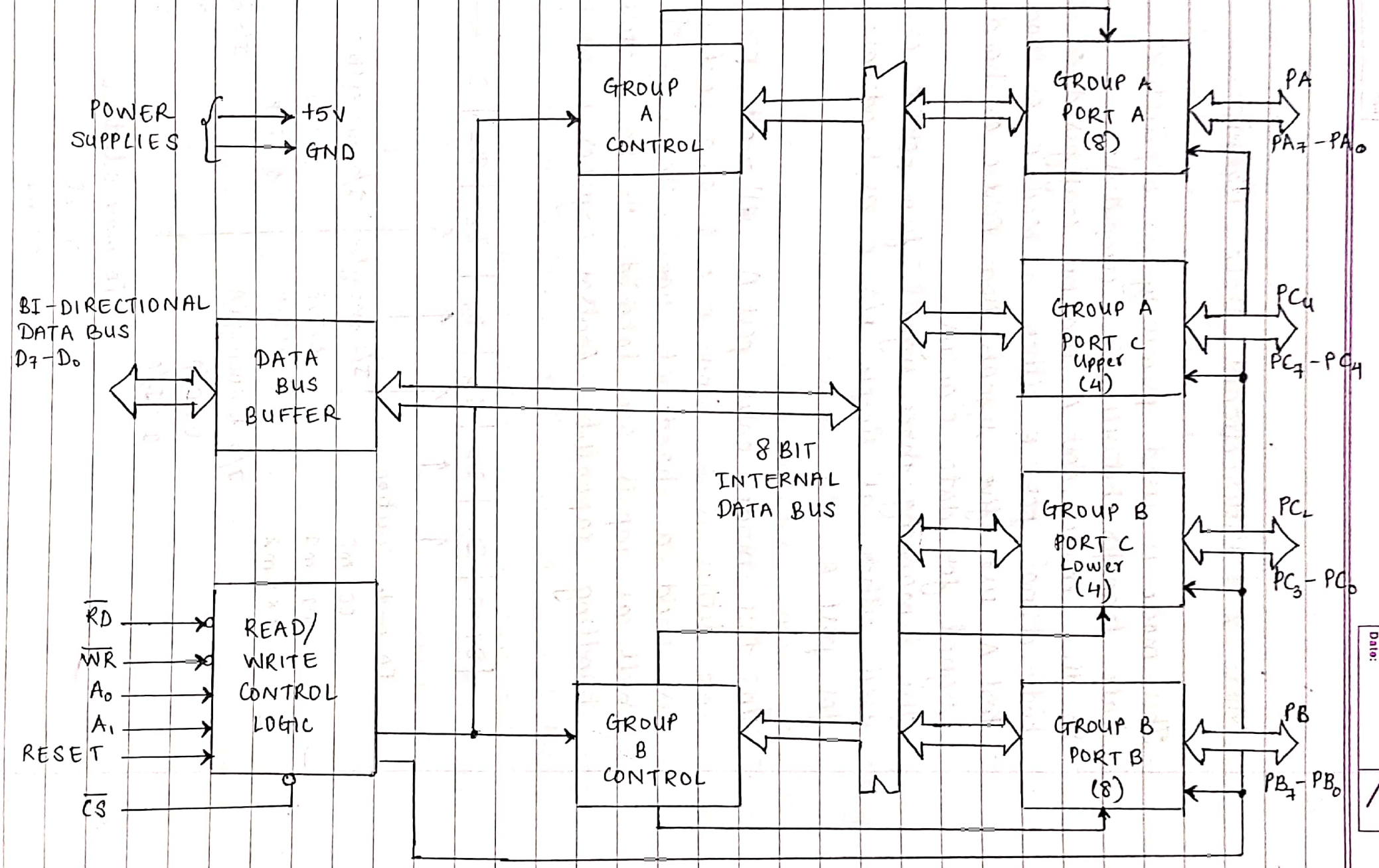
1] Short note on 8255

- PPI 8255 is a general purpose programmable I/O device designed to interface the CPU with its outside world such as ADC, DAC, keyboard, etc.
- It consists of three 8-bit bidirectional I/O ports i.e PORT A, PORT B and PORT C. We can assign different ports as input or output functions.
- It consists of 40 pins and operates in +5V regulated power supply. PORT C is further divided into two 4-bit ports i.e PORT C lower and PORT C upper and PORT C can work in either BSR (bit set rest) mode or in mode 0 of input-output mode of 8255.
- PORT B can work either mode or in mode 1 of input-output mode. PORT A can work either in mode 0, mode 1 or mode 2 of input-output mode
- It has two control groups, control group A and control group B. Control group A consist of port A and port C upper. Control group B consists of port C lower and port B.
- Depending upon the values of CS', A1 and A0 we can select different ports in different modes as input-output function or BSR. This done by writing a suitable word in control register.
- Operating modes include:
  - Bit Set Reset (BSR) mode
  - Input-Output mode
  - Mode 0
  - Mode 1
  - Mode 2

BLOCK DIAGRAM OF 8255



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2] Short note on 8237

- CAR (Current Address Register):
  - The current address register holds a 16-bit memory address used for the DMA transfer.
  - Each channel has its own current address register for this purpose.
  - When a byte of data is transferred during a DMA operation, CAR is either incremented or decremented depending on how it is programmed.

- CWCR (Current word count register):
  - The current word count register programs a channel for the number of bytes to transferred during a DMA action.

- CR (Command Register):
  - The command register programs the operation of the 8237 DMA controller.
  - Transfer mode:
    - Memory-to-memory DMA transfers use DMA channel
    - DMA channel 0 to hold the source address
    - DMA channel 1 holds the destination address.

- BA (Base Address) and BWC (Base Word Count):
  - The Base Address (BA) and Base Word Count (BWC) registers are used when auto-initialization is selected for a channel.
  - In auto-initialization mode, these registers are used to reload the CAR and CWCR after the DMA action is completed.

- MR (Mode Register):
  - The mode register programs the mode of operation for a channel.
  - Each channel has its own mode register as selected by bit positions 1 and 0.
  - Remaining bits of the mode register select operation, auto-initialization, increment/decrement, and mode for the channel.

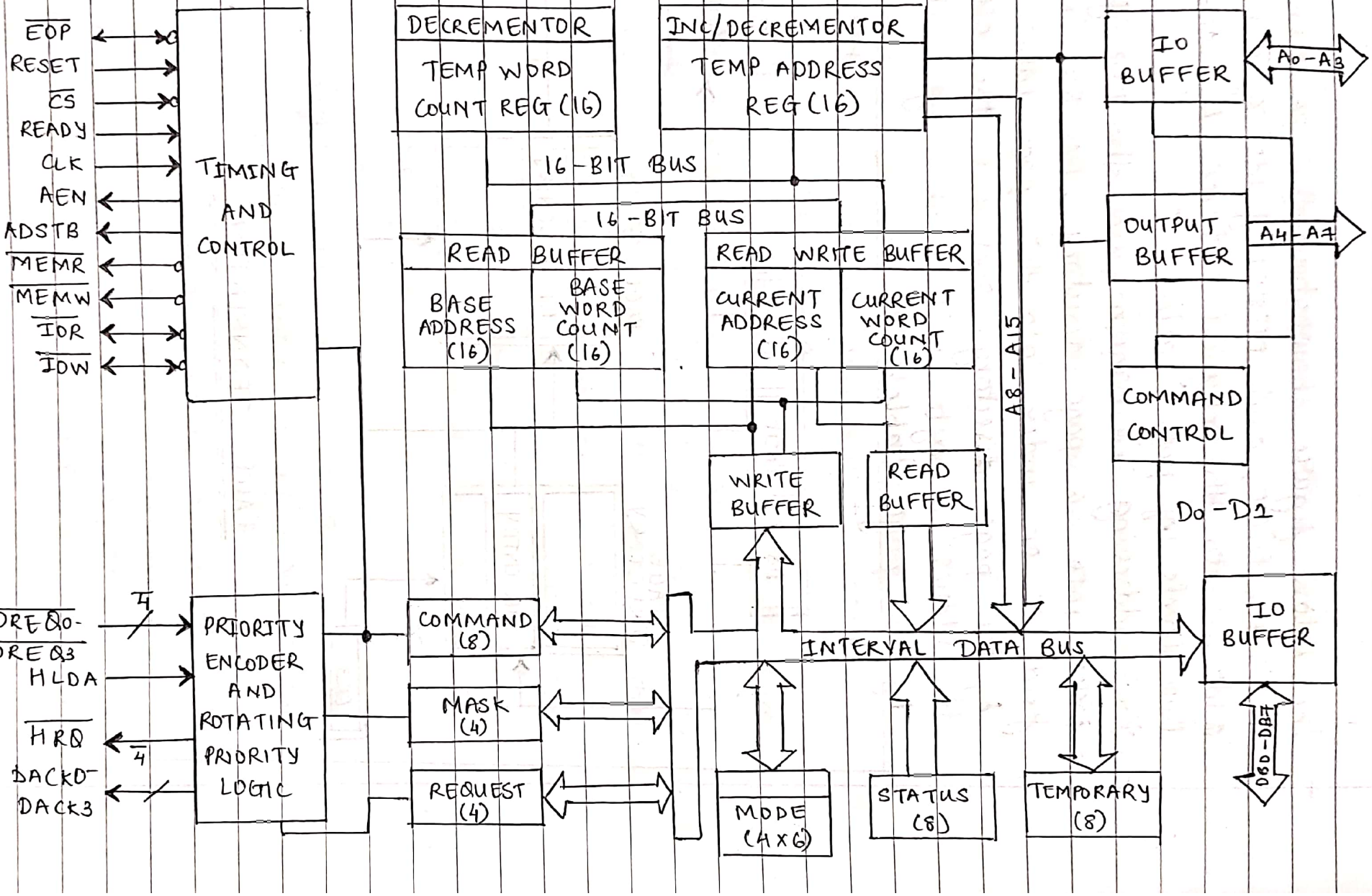
- BR (Bus request register):
  - The bus request register is used to request a DMA transfer via for software.
  - It is very useful in memory-to-memory transfers where an external signal is not available to begin the DMA transfer.

- MRSR (Mask register set/reset):
  - The mask register set/reset sets or clears the channel mask.
  - If the mask is set, the channel is disabled.
  - The RESET signal sets all channel masks to disable.

- MSR (Mask Register)
  - The mask register clears or sets all of the masks with one command instead of individual channels, as with the MRSR.

- SR (status Register)
  - The status register shows status of each DMA channel. The TC bits indicates if the channel has reached its terminal count. When the terminal count is reached, the DMA transfer is terminated for most modes of operation. The request bits indicate whether the DREQ input for a given channel is active.

BLOCK DIAGRAM OF 8237



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Q.3] Initialization sequence of 8259

The 8259 can be programmed through a sequence of simple I/O operations. It accepts 2 types of command words. They are:

1] Initialization Command Word 1 (ICW1)

It is used to program the basic operation of 8259A. To write this command word into ICW1 register A_0 pin should be at logic '0'. After accepting this command the 8259A performs the foll. internal operations:

(1) It resets edge sense circuits, hence an interrupt request must make a low to high transition to trigger IR input after initialization.
(2) It clears interupt mask register hence all interupt are unmasked.
(3) It assigns lowest priority to IR_7 and highest priority to IR_0.
(4) It sets slave identification number of slave 7 (1, 1, 1) if D_1 bit of ICW1 is '0'.
(5) It clears special mode and sets the status read to IRR, i.e microprocessor can read IRR without issuing a special command word.
(6) If D_0 bit of ICW1 is reset, then it clears all functions associated with ICW4.

2] Initialization Command Word 2 (ICW2)

The ICW2 is used to progeam 8 bit vector number of interupt type. A write command issued after ICW1 with $A_0 = 1$ is considered as ICW2. The ICW2 format can hence be represented. In 8085 mode, ICW2 bits are used to program A_8 to A_{15} address bits of ISR address. In 8086 mode, D_3 to D_7 bits are used to program T_3 to T_7 bits of 8 bit vector number. The lowest bits T_0 to T_2 are provided by 8259 depending on which interupt input is activated.

3] Initialization Command Word 3 (ICW3)

It is used in cascaded mode only. There are 2 types of ICW3's viz master ICW3 and slave ICW3. The master ICW3 is used to specify whether it has a slave 8259 connected to its interupt request interest input. The slave ICW3 is used to assign a slave identification number. Identification number is used to tell slave 8259 on which IR input it is connected to master. A write command is issued after ICW1 and ICW2 and multiple 8259 system with $A_0 = 1$ is considered as ICW3.

4] Initialization Command Word 4 (ICW4)

The ICW4 is used to initialize the 8259A in the following modes:

1) Special fully nested mode. 2) Buffered mode
3) Auto EOI mode 4) 8086/8088 mode

A write command issued after ICW3 and ICW4 bit needed bit set in ICW1 with $A_0 = 1$ is considered as ICW4.

5] Operation Command Word 1 (OCW1)

The OCW1 is used to mask unwanted interupt request inputs (IR inputs). A write command issued after intialization with $A_0 = 1$ is considered as OCW1.

6] Operation Command Word 2 (OCW2)

The OCW2 is used to perform EOI (End of Interupt), rotate priorities and combination of both. A write command issused with $A_0 = 0$ and $D_4 D_3 = 00$ is considered as OCW2.

7] Operational Command Word 3 (OCW3)

The OCW3 is used to program 1) Special mask mode 2) Polled mode 3) Read IRR and ISR. A write command issued with $A_0 = 0$ & $D_4 D_3 = 01$ is considered as OCW3.