Computer Organization
Lab 5: Advanced Pipelined CPU

Due: 2020/06/30 23:55

1. Goal

Modify your Lab 4 CPU design, implement an advanced pipelined CPU with (1) hazard detection and (2) data forwarding.

2. Homework Requirement

1. **Basic Instructions: (80%)**
    a. **Instructions**
        i. ADD
        ii. ADDI
        iii. SUB
        iv. AND
        v. OR
        vi. SLT
        vii. SLTI
        viii. LW
        ix. SW
        x. MULT
    b. You must implement (1) **Hazard Detection** and (2) **Forwarding** Unit.
    c. Your CPU need to forward data if instructions have data dependency.
    d. Your CPU need to stall pipelined CPU if it detects a load-use.
2. **Advanced Instructions (20%)**
    a. **Instructions**

Instruction	Op
BEQ	000 100
BNE	000 101
BGE	000 001
BGT	000 111

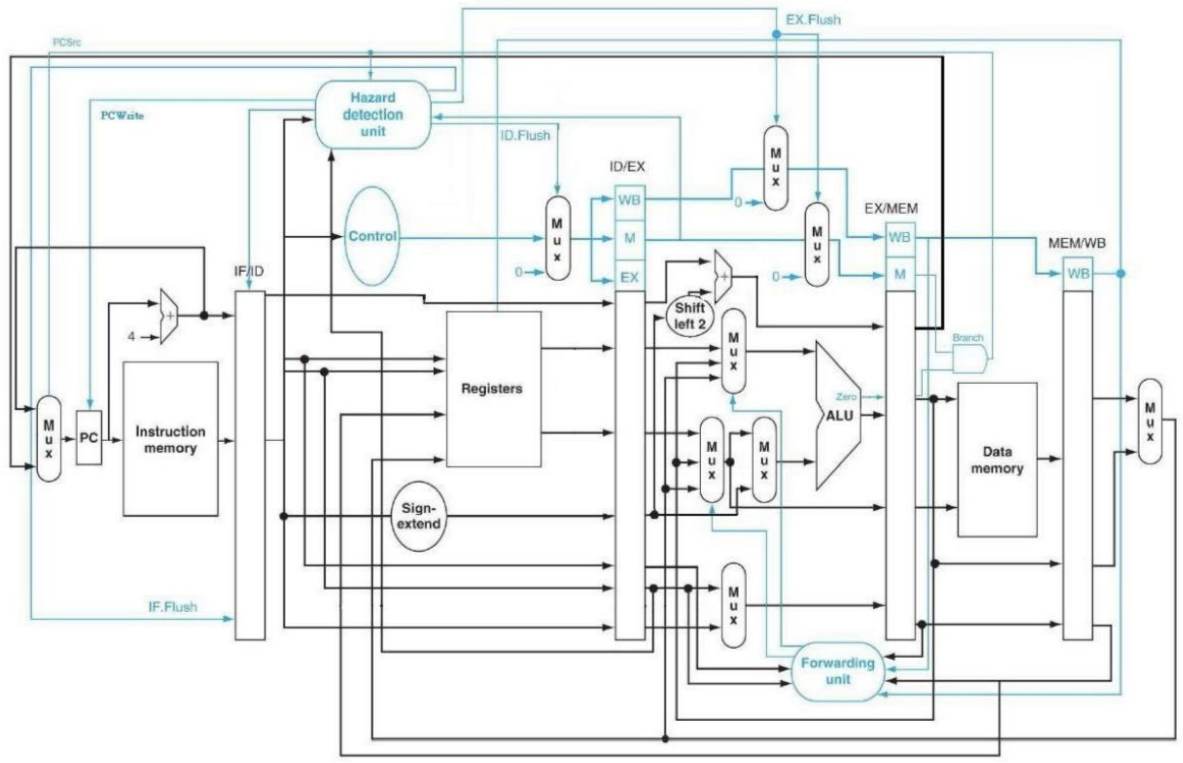
b. Modify **Hazard Detection Unit** to flush useless pipelined registers (IF/ID, ID/EX, EX/MEM) if a branch launch.

3. Testbench (“CO_P出_test_1.txt”):
   Try to solve the date hazards in I1/I2, I5/I6, I8/I9, I9/I10 by using forwarding unit and Hazard Detection Unit.

```
I1:  addi  $1,$0,16
I2:  mult  $2,$1,$1
I3:  addi  $3,$0,8
I4:  sw    $1,4($0)
I5:  lw    $4,4($0)
I6:  sub   $5,$4,$3
I7:  add   $6,$3,$1
I8:  addi  $7,$1,10
I9:  and   $8,$7,$3
I10: slt   $9,$8,$7

Result
r1 = 16;
r2 = 256;
r3 = 8;
r4 = 16;
r5 = 8;
r6 = 24;
r7 = 26;
r8 = 8;
r9 = 1;
data_mem[1] = 16;
```

3. Architecture Diagram



4. Report

a. Your Architecture
b. Hardware Module Analysis
c. Problems You Met and Solutions
d. Result
e. Summary

5. Grade

a. **Total:** 120 points (plagiarism will get 0 point)
b. **Report:** 20 points (please use **pdf format**)