Assignment 2

Task 1

2) What happens in the simulation cycle?

We assign values to signals with VHDL code. During the simulation, if the value of a signal changes, this change is registered in the event queue, and after one delta delay, the new value is assigned to the signal.

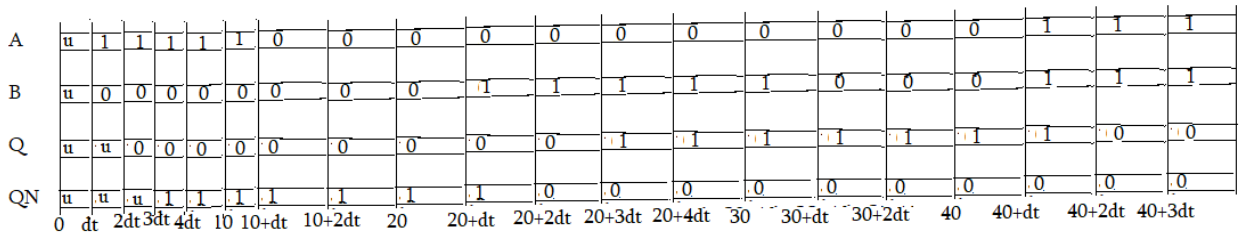
3) Explain what happens to signals that are assigned values with and without explicit delays.

Signals that are assigned without explicit delay are updated after the default delta delay (after 1fs).

Signals that are assigned with explicit delay are updated after the declared delay.

Task 2

1)



2) If these stimuli are inside a process and the process does not have a sensitivity list or wait statement, we would experience oscillations after all stimuli have been applied and the two processes Q and QN are suspended.

3) (See the next 2 pages).

```vhdl
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

entity assignment2 is
    Port ( A  : in  STD_ULOGIC;
           B  : in  STD_ULOGIC;
           Q  : out STD_ULOGIC;
           QN : out STD_ULOGIC);
end assignment2;

architecture Behavioral of assignment2 is
signal internal1, internal2 : STD_ULOGIC;
begin

    internal1 <= A nor internal2;
    internal2 <= B nor internal1;

    Q  <= internal1;
    QN <= internal2;
end Behavioral;
```

```vhdl
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

entity testbench is
end testbench;

architecture Behavioral of testbench is
    signal A, B, Q, QN : STD_ULOGIC;
begin
    DUT: entity work.assignment2(Behavioral)
        port map(A => A, B => B, Q => Q, QN => QN);
    stimuli: process is
    begin
        A <= '1' ; B <= '0' ;
        wait for 10 ns ;
        A <= '0' ;
        wait for 10 ns ;
        B <= '1' ;
        wait for 10 ns ;
        B <= '0' ;
        wait for 10 ns ;
        B <= '1' ; A <= '1' ;
    end process stimuli;
end Behavioral;
```