



UNIVERSITY OF TURIN
DEPARTMENT OF PHYSICS
SCHOOL OF SCIENCE OF NATURE
MASTER DEGREE IN PHYSICS

~ . ~

ACADEMIC YEAR 2020–2021

**Study of the performance of the
first MAPS-based tracker for
space applications**

Supervisor
Prof.ssa Stefania BEOLÈ

Co-supervisor
Prof.ssa Elena BOTTA

Graduate Student
Stefania PERCIBALLI
941212

FINAL EXAMINATION DATE: 11 April 2022

*”Alle famiglie, il posto dove
possiamo permetterci di essere fragili”*
Gio Evan

Abstract

Silicon pixel sensors are a widespread technology which has stimulated a growing interest. Some of the fields of application are cellular cameras and particle tracking in high energy physics; in particular, they could also be used for space applications.

The Limadou collaboration is implementing the first space tracker based on silicon pixel sensors aiming to include it in a detector to study ionosphere physics and to deepen the comprehension of some events which indicate a time correlation between the main earthquake shock and an increase in the electron flux in the inner Van Allen belt.

The sensor chosen for this intent is the ALPIDE (ALice PIxel DEtector), a sensor developed by the ALICE (A Large Ion Collider Experiment) collaboration at CERN for the upgraded vertex detector.

The assembly procedure together with the qualification tests that allow to select the best modules for the tracker construction are explained in this work. Furthermore, the sensor performance as a function of temperature is studied. To verify that its behaviour at different temperatures is not degraded, the ALPIDE operation was tested between -10°C and 50°C; at the same time, a calibration of the ALPIDE in-chip temperature sensor has been performed through the comparison with an external temperature reference given by Dallas sensor (DS18B20U) added to the detector unit layout. From the acquired data, a calibration of the ALPIDE temperature sensor was obtained and it was possible to verify that the sensor performance is not affected by different temperature conditions in the range under test.

Contents

Abstract	5
Contents	8
Introduction	9
1 Monolithic Pixel Detectors for tracker applications	11
1.1 Silicon Pixel Detectors	12
1.1.1 Silicon Strip Detectors for space application	12
1.1.2 Hybrid and Monolithic Pixel Sensors	13
1.1.3 Pixel Detectors for space applications	14
1.2 Structure of Monolithic Pixels Sensors	15
1.3 Early developments and R&D	17
1.3.1 The MIMOSA series	17
1.3.2 The ALPIDE and MISTRAL sensors	19
1.3.3 Ongoing Developments	22
2 The Limadou Collaboration	23
2.1 HEPD-02 tracker	25
3 ALPIDE Sensors	29
3.1 Signal formation	30
3.1.1 In-pixel signal processing	30
3.1.2 Matrix Readout	31
3.2 Analogue in-pixel front-end electronics	32
4 Tracker Assembly Procedure	33
4.1 HIC Assembly	35
4.2 Stave Assembly	38
5 Qualification Procedure	41
5.1 Set-up	42
5.2 Tests	43
5.3 Threshold Tuning	47
6 Temperature performance dependence studies	51
6.1 Set-up	52
6.2 Dallas Sensors	53
6.3 Threshold as a function of temperature	56
6.4 Noise as a function of temperature	59
6.5 ALPIDE temperature sensor calibration	61

7 Future Developments of MAPS	63
7.1 Set-up	64
7.2 Parameters	66
7.3 Preliminary results	67
7.3.1 Jitter measurements	68
7.3.2 Parameter optimization	68
7.3.3 Reverse bias current	72
7.3.4 Future steps of the characterization process	72
Conclusion	73
List of Figures	75
List of Tables	77
References	79
Acknowledgements	83

Introduction

This thesis focuses on the assembly, quality assurance and temperature topical study of the detectors that will form the HEPD-02 (High Energy Particle Detector) tracker. HEPD-02 is a particle detector that will be launched on board the CSES-02 (China Seismo-Electromagnetic Satellite) whose launch is scheduled for mid 2023. The CSES-02 mission is the second sample of a satellite constellation aimed at further investigating some phenomena which showed a time correlation between earthquakes and an increase in the electron flux in the inner Van Allen radiation belt.

The HEPD-02 detector is of vital importance to the mission because it is designed to detect electrons and protons or light nuclei respectively in the energy range 3-100 MeV and 30-200 MeV/Z. For this purpose, HEPD-02 is composed by a trigger system, a silicon sensor tracker, a calorimeter and a veto system. The HEPD-02 core is the tracker, devoted to particle tracking; the tracker is based on Monolithic Active Pixels Sensors (MAPS) technology, never used so far in space applications.

Chapter 1 describes the previously used technologies in space environment, the advantages of MAPS, together with the sensors development process. A particular attention is given to the ALPIDE (ALice PIxel DEtector) sensor which is based on CMOS commercial 180 nm technology and was designed and optimised by the ALICE (A Large Ion Collider Experiment) collaboration to equip the experiment upgraded Inner Tracking System (ITS2).

Chapter 2 is dedicated to the detailed description of the CSES missions and of the HEPD-02 tracker, as well as the challenges of designing and operating the MAPS in the space environment. The sensor chosen for the construction of the HEPD-02 tracker is the ALPIDE, whose layout, working principle and main parameters are explained in Chapter 3.

During the thesis project, a great effort was devoted to the assembly of the modules that will constitutes the HEPD-02 tracker. Chapter 4 is completely dedicated to the assembly strategy which was carefully studied in order to maximise the mechanical quality and minimise any possible damage occurred during each step of the process.

For this purpose, in chapter 5, a description of the electrical qualification test that are used to determine if the modules are suitable to be used for the final tracking system, is reported.

In particular, section 5.3 reports the study on the ALPIDE parameters which was performed to obtain an equalize response on a single tracker module. As a result the author describes the choice of the parameters for the tests that will be performed on the tracker modules.

The following chapter is dedicated to the topical study of the temperature

performance of the ALPIDE detector; the effort was motivated by the presence of a temperature gradient along the tracker modules and it was necessary to verify if a punctual parameter choice was needed. Chapter 6, reports the set-up and the temperature characterization of the ALPIDE performance between -10°C and 50°C . Furthermore, the ALICE collaboration needed the calibration of the ALPIDE temperature sensor but did not have a temperature reference to perform such a calibration. The HEPD-02 modules have included a temperature sensor which can give the external temperature reference. Section 6.5, describes the temperature sensor behavior as function of the power supply voltage and of the working temperature.

Finally chapter 7, describes one ongoing development of MAPS based sensors, showing the first obtained results and the main innovation that characterize the detectors, which could revolutionize the silicon pixel sensor technology for every application.

Chapter 1

Monolithic Pixel Detectors for tracker applications

1.1 Silicon Pixel Detectors

Detectors, and in particular silicon sensors, are widely employed and of growing importance in measuring physical quantities: adaptability and performances are two of the main qualities among the reasons for their widespread use [1]. The main field of application is accelerator physics in which silicon detectors are devoted to particle tracking and vertices reconstruction.

A great R&D effort has led to the production of many different silicon detector technologies: silicon strip detectors, silicon pixel detectors and silicon drift detectors are just some of them.

The choice of the employed technology depends mainly on the application requirements: granularity, power consumption, readout speed and radiation hardness are some parameters to be considered.

This work will be focused on Monolithic Active Pixel Sensors (MAPS) and more specifically, on their use as tracking devices in space experiments. Before going into details, a more general overview is needed, to recall the current state of silicon sensors in accelerator and space applications, starting by distinguishing between the two main categories of silicon detectors: strip and pixel sensors.

1.1.1 Silicon Strip Detectors for space application

Silicon strip detectors were developed for many applications including several trackers in accelerator and space experiments such as ATLAS, ALICE, AMS, FERMI.

Silicon strip are designed exploiting the p-n junction behaviour to detect the point in which a particle crossed the detector, by measuring the charge released by ionization.

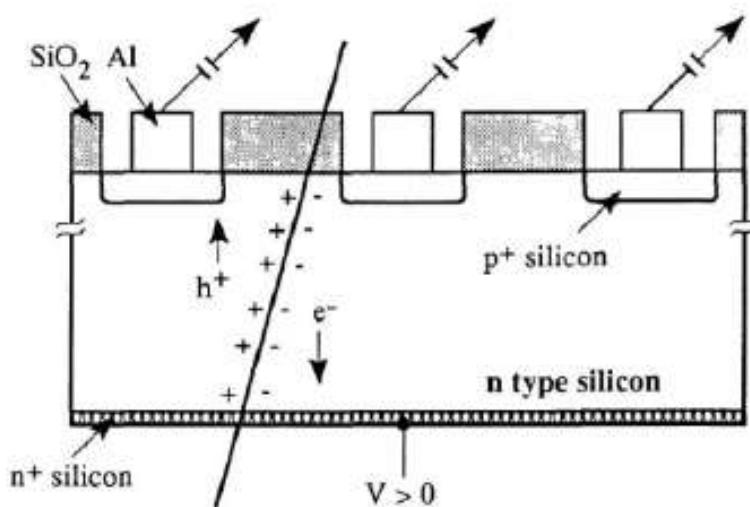


Figure 1.1: Example of the schematic of a silicon strip detector [2]

A series of p+ doped collecting strips is implanted on n doped silicon substrate: this configuration produces a strong electric field due to the different

charge densities and originates a depletion region which can be widened by applying a positive voltage to the n+ substrate (figure 1.1).

The electron hole pairs generating by the particle crossing the detector will drift towards the corresponding electrode, p+ for holes and n+ for electrons, generating a measurable signal on the p+ collection diode [2].

By segmenting the n+ electrode in the opposite direction, it is possible to obtain the particle interacting point by using a single silicon layer. Placing several detector layers one over the other, the particle track can be reconstructed. Spatial resolution of each interaction point is one of the most important detector quality, and it is defined by:

$$\sigma_{x,y} = \frac{pitch_{x,y}}{\sqrt{12}}$$

if the charge is collected by a single strip.

Many space detectors have used silicon strip sensors to build their trackers, for example PAMELA [3] and afterwards AMS exploited the high spatial resolution to reconstruct particle momentum. For this purpose, the tracker was placed inside a magnetic field and the charged particle sign and momentum were detected by measuring the track curvature [4]. The main aim of these two experiments is antimatter measurements and the search of dark matter by monitoring charged cosmic rays. Currently AMS hosts the larger microstrips tracker in space.

Another example of silicon strip technology in space experiments is represented by FERMI-LAT and DAMPE, in which calorimeter layers alternate with silicon microstrip layers to allow γ -ray conversion in the calorimeter and electron-hole pairs detection in silicon microstrip. FERMI-LAT main purpose is the detection of Gamma Ray Burst (GRB) to discover their sources [5] while DAMPE studies electron and positron fluxes in the hope of discovering dark matter signs [6].

1.1.2 Hybrid and Monolithic Pixel Sensors

On the other side, there are silicon pixel sensors, that instead of measuring one coordinate at a time, measure both coordinates by segmenting the collecting diode along the x and y direction. [7]

They are divided in two categories depending on the way they are connected to the in-pixel readout electronics or Application Specific Integrated Circuit (ASIC).

Hybrid Pixel sensor have two separated silicon wafer for the sensor and the ASIC [8]: when the particle crosses the detector it generates a charge in the active area that is collected by the n+ electrode. To read out the signal, the collection electrode is connected to electronics by a technique called bump bonding.

On the other hand, Monolithic Active Pixel detector have the electronics and the sensor implanted on the same silicon substrate [9], thus reducing connection issues due to the deposit of the bump bond which sometimes can cause short circuits. In standard MAPS the fact that complex readout electronics

needs both NMOS and PMOS processes can cause a problem in the charge collection efficiency, because the implant of the n-well can be seen as an alternative collecting electrode. To avoid this issue in the last MAPS generations an additional deep p-well is implanted under the PMOS n-wells to shield it (figure 1.2).

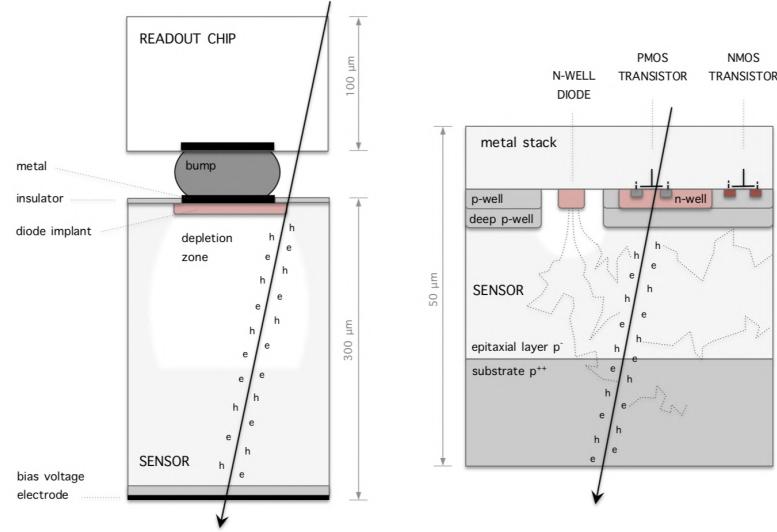


Figure 1.2: On the left: schematic section of a hybrid pixel sensor. On the right: schematic section of a monolithic active pixel detector [13].

The main benefits of hybrid detectors are the possibility to optimize sensor and ASIC separately, the possibility of applying a high reverse bias voltage. However, the material budget is higher due to the use of two silicon wafer. Monolithic pixel sensors, instead, are composed of a single silicon chip containing both front-end electronics and the sensor active area. This choice eliminates bump bonding yield problem and reduces the material budget. Furthermore, the sensor can be produced in commercial CMOS imaging processes reducing the cost, and avoiding the need of dedicated production lines [10].

Hybrid pixel sensor were used in the ALICE[8], CMS[11], ATLAS [12] inner tracking system (ITS): ALICE upgraded the inner tracking system in 2021 and substituted hybrid pixels with MAPS [14], building the largest scale application of MAPS in a high-energy physics experiment.

1.1.3 Pixel Detectors for space applications

Silicon Strip sensors have numerous advantages in being used for space application, the most important being the fact that they can guarantee a low power consumption and a small number of readout channels.

However, they have some limits: only a small number of foundries has expertise in microstrip sensors production, and since the sensor must be specifically designed for each application the cost is high. Moreover also the ASIC must be specifically designed and has a large cost. For these reasons, the possibility of using a MAPS silicon pixel detector was investigated. [15]

Silicon pixel detector have been used in space application for dosimetry purpose, on board ISS, but they have never yet been used for particle tracking aims [15].

MAPS were chosen for space application because they are produced with a commercial CMOS imaging processes that reduces costs of a factor $\frac{1}{5}$ and with respect to hybrid pixels. In addition the assembly procedure is much simpler because bump-bonding is no longer required [15].

In digital response pixel sensors, the in-pixel front-end electronics amplifies and discriminate the signals, giving a logic 1 if the pixel is hit, otherwise having a logic 0 as output. By implementing an algorithm of zero-suppression it is possible to read only hit pixels reducing the data budget. Moreover track reconstruction on board is feasible by applying a cluster recognition strategy, with the goal of sending the already processed data down to Earth.

The main issue in using silicon pixel detectors is the high power consumption, that must be carefully studied to respect the strict satellite requirements [15].

1.2 Structure of Monolithic Pixels Sensors

Monolithic pixel detectors may differ between different applications, but they have common elements, shown in figure 1.3, that are described below, from bottom to top.

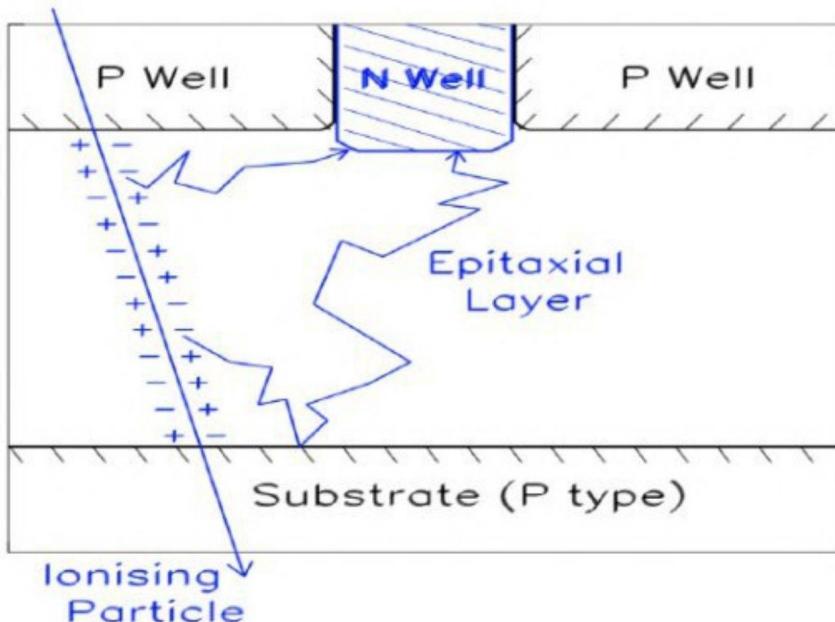


Figure 1.3: Structure of Monolithic Active Pixel Detectors (MAPS), example of the MIMOSA sensor [16]

- the substrate: a region heavily doped p++ with low resistivity that can be as thin as $10\text{ }\mu\text{m}$
- the epitaxial layer: a region slightly p doped grown on the substrate, it can have high or low resistivity, depending on the application. The

epitaxial layer represents the sensor active area in which electron-holes pair are generated and charge can be collected by drift or diffusion.

- the wells: region p or n doped that constitutes the substrate over which transistors are implanted. P substrate host NMOS transistors while n substrate corresponds to PMOS.
- n-type and p-type diffusion implantation: they are more doped than the wells and form the electrodes of PMOS (p implantation over n-well) and NMOS (n implantation over p-well) transistors.
- n-type collection diode: heavily doped n++ region that is used to collect the generated charge inside the epitaxial layer and from which the signal is read by in-pixel electronics.
- metal connection are deposited over to realize the connection between transistors and the collecting diode. They are usually made of aluminium (Al) or copper (Cu). To isolate different lines and avoid short circuits, a silicon oxide layer is deposited over the connections.

After their creation, the electrons diffuse in the epitaxial layer, where they are confined by the very different concentration between the epitaxial layer and the substrate. If they reach the depletion region, they are collected by the collecting diode.

To help the collection procedure and cope with the radiation damage, it is possible to apply a reverse bias to the substrate thus creating a wider depletion region in which the electrons move by drift [17] (figure 1.4).

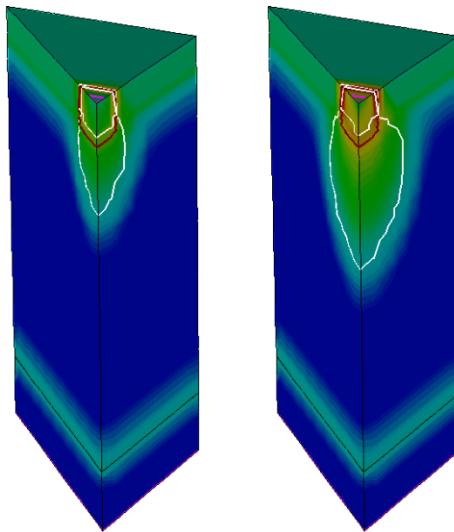


Figure 1.4: MAPS depletion region simulation in the case of reverse bias voltage -1 V (on the left) and -6 V (on the right) with a epitaxial layer doping of $1 \times 10^{13}\text{ cm}^{-3}$, and collecting diode dimensions of $3\text{ }\mu\text{m} \times 3\text{ }\mu\text{m}$. The colour code shows the logarithm of the electrical field. [10]

The pixels are arranged to form a matrix of dimensions of about $1 \times 1\text{ cm}^2$, the whole matrix is called chip, and contains also a peripheral zone for the signal processing electronics.

1.3 Early developments and R&D

CMOS sensors for particle detection have been developed starting from imaging sensors: since 1960's many groups were working on the development of a solid state imaging sensor, but until 1990's not much interest was expressed for CMOS technologies.

The research underwent significant acceleration in 1990's with the necessity to create a highly functional single-chip imaging system and NASA's need for a highly miniaturized, low-power, instrument for next-generation spacecraft. These two motivations pulled in two different directions: the first on a low cost device, while the second on its high performance.

A strong effort led to the development of the first CMOS pixel imaging sensors, that quickly became competitive with the existing charge-coupled devices (CCD) [18]. Still in 1987 CCD were proposed for the detection of minimum ionising particles, and in 1999 the suggestion was extended to CMOS pixel sensors [9].

For the last two decades, an ongoing research effort has been carried out to pull even further the device performances, leading to the construction of the first large area MAPS-based tracker; in the next section an overview of the MAPS evolution is presented.

1.3.1 The MIMOSA series

In 1999-2000 the first CMOS sensors for particle detection were developed: the main contribution to the effort was given by the Institut Pluridisciplinaire Hubert Curien (IPHC, Strasbourg, France), the Rutherford Appleton Laboratory (RAL, Chilton, UK) and CERN (Geneva, Switzerland).

An example of the first developed detectors is MIMOSA (acronym of Minimum Ionizing MOS Active pixel sensor). It's important to underline that MIMOSA sensors were designed with n-mos only electronics, because of technology limitations.

The first prototypes tested were MIMOSA-1 and MIMOSA-2, which were followed by many other sensors with different layouts, investigating various pixel and diode sizes, epitaxial layer thicknesses and resistivity, electronics integration processes (with different transistor feature sizes) and design choices [17]. In 2007-2008, MIMOSA-22 sensor was realized in AMS (Austria Mikro Systeme) $0.35\text{ }\mu\text{m}^1$ process with a pixel pitch of $18.4\text{ }\mu\text{m}$, after the characterization and test phase, it was selected as the sensor technology for the first EUDET telescope, subsequently tested both at the DESY and CERN test beam facilities [19].

Rolling Shutter

In the MIMOSA series MAPS sensors, the in-pixel electronic included only analogue front-end electronic: in particular only the signal amplification stage.

¹This number indicates the minimum channel length of the transistors front-end electronics. The transistor channel is defined as the distance between the two electrodes

Analogue signals must then be read from the pixel matrix and discriminated elsewhere.

The chip is organized in rows and columns and the rolling shutter readout method allows scanning the matrix row by row reading all the analogue pixel signals [20] (figure 1.5).

When read, the pixels of the same row send their signals in parallel to the end-of-column logic where signals are discriminated and zero suppression logic is applied [21].

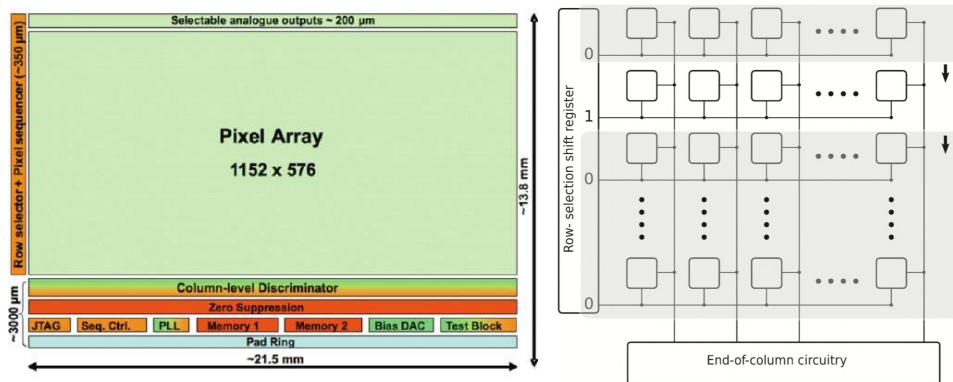


Figure 1.5: On the left: schematic view of MIMOSA-26 chip [21]. On the right: rolling shutter readout mode [10]

When all the pixels of the row are read, the shutter (row selector) can switch to the following row. The time needed to complete all the matrix readout is called the integration time.

The main advantage in using the rolling shutter readout is the low number of transistors needed for each pixel while most of the front-end electronics is moved to the chip periphery.

The main drawbacks are the fact that clock must be spread to all the pixels in the matrix and the necessity of propagating the analogue signals to the end-of-column logic. This readout mode increases the power consumption (connected to the rolling shutter frequency) and forces the clock to be permanently active on all the matrix.

MIMOSA-26 and MIMOSA-28

The MIMOSA-26 sensor played an important role in the process towards the production of a sensor for collider experiments: it is fabricated in the $0.36 \mu\text{m}^2$ OPTO (Optical Semiconductor Manufacturing Process) process and consists of a 1152×576 pixels array with pitch $18.4 \mu\text{m}$.

A EUDET telescope was also built with this sensor for use in test beam facilities [22] and MIMOSA-26 became also the direct predecessor of the ULTIMATE sensor designed and built for the STAR silicon pixel tracker (PXL), the first large area MAPS-based vertex tracker system ever used in a collider experiment [23].

ULTIMATE-2 (MIMOSA-28) is an optimization of MIMOSA-26 and was designed at Institut Pluridisciplinaire Hubert Curien (IPHC, Strasbourg, France) in order to meet the STAR PXL detector requirements [24]. MIMOSA-28 has

a higher resistivity of the epitaxial layer in comparison to MIMOSA-26, providing an increased depletion depth and, as a consequence, an increased radiation hardness and signal to noise ratio [20].

MIMOSA-28 has still rolling shutter readout and the possibility of implanting only NMOS transistor since only p-wells are available.

However, the characteristics of MIMOSA-28 were not suitable for ALICE Inner Tracking System (ITS) upgrade requirements in terms of radiation hardness, integration time and power consumption [10, 23].

1.3.2 The ALPIDE and MISTRAL sensors

To reach the ALICE requirements, two path were followed leading to the development of the MISTRAL (MImosa Sensor for the inner TRacker of Alice) and the ALPIDE (ALice Pixel Detector) sensors [10].

They were both built in TowerJazz 0.18 μm^2 CMOS imaging process, and the sensor design overcome many of the issues carried by the first generation of MAPS, such as the MIMOSA-series [25, 26].

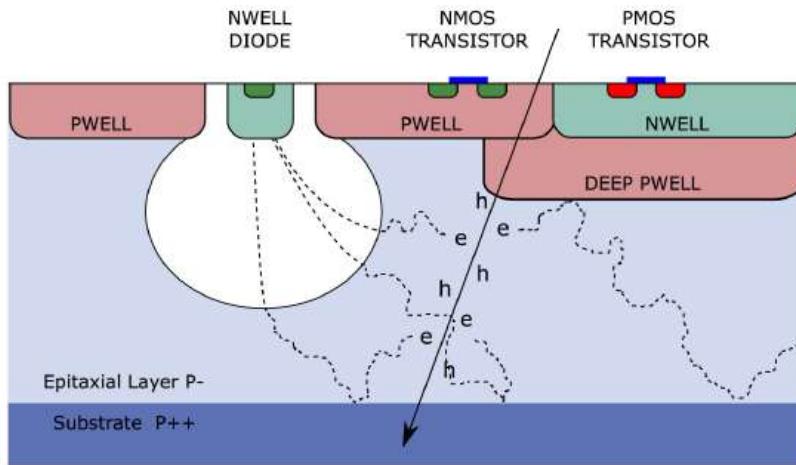


Figure 1.6: Vertical section of the ALPIDE sensor realized in the 180 nm TowerJazz CMOS imaging process [10].

The main improvements are listed below:

- the substrate is implemented in a low resistivity (about 10Ω), heavily-doped p-type silicon, over which a lightly doped p-type epitaxial layer is grown by chemical vapor deposition. The high epitaxial resistivity allows for a larger depleted volume, improving the signal to noise ratio and the radiation hardness;
- charge collection can be optimised by increasing the depletion region obtained when a moderate reverse substrate bias is applied;
- TowerJazz imaging process allows for a stack-up of up to 6 metal layers, which, besides with the small (180 nm) size, enables to insert high-density, low-power circuitry in each pixel;
- higher radiation tolerance is achieved through the reduction of the gate-oxide thickness to 3 nm and the decrease of transistor feature size (180 nm);

- TowerJazz imaging process also grants the possibility to design a fully CMOS in-pixel front-end circuitry. The main problem is the realization of the n-well for PMOS transistors, which could compete with the n-type collection diode by absorbing part of the released charge. To overcome this issue, a deeper p-well is implanted in order to shield the PMOS n-wells: the adopted solution generates also a potential barrier that contributes to the charge confinement in the epitaxial layer [27];
- more elements can be implanted in the same space, leading to an increase of the number of in-pixel front-end elements thanks to the choice of a fully CMOS logic.

In figure 1.6, the ALPIDE pixel section is depicted.

MISTRAL sensor

MISTRAL (MImosa Sensor for the inner TRacker of ALice) sensors were developed at IPHC (Strasburg) as an evolution of the MIMOSA series with the aim of producing a sensor for the ALICE ITS upgrade [28].

Similarly to the MIMOSA series, the MISTRAL sensor presents only in-pixel amplification, the analogue signal is then propagated to the end-of-column peripheral circuitry. The novelty is the double-row rolling shutter readout: two rows are read simultaneously and the signals are sent to the periphery (figure 1.7).

The double-row rolling shutter achieves a halving of the integration time, thus doubling the readout speed: this is possible thanks to the small transistors size obtained thanks to the 180 nm process. A typical integration time of 20 μ s and a power consumption of 97 mW/cm² is obtained [28, 29].

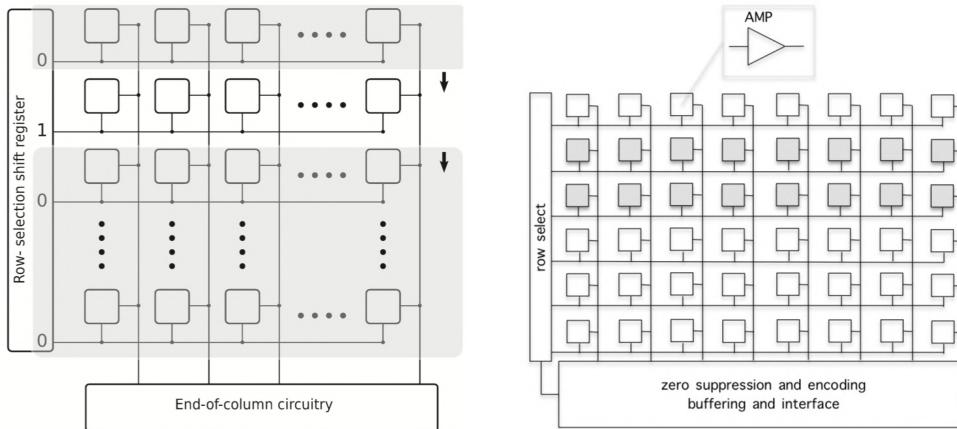


Figure 1.7: MIMOSA readout mode [10] (On the left) compared to MISTRAL double-row rolling shutter readout [13] (On the right)

ALPIDE sensor

The ALPIDE (ALice PIxel DEtector) sensor consists of a pixel matrix of 1024 column and 512 rows and has a more complex in-pixel circuitry; in fact each pixel contains:

- a n-type octagonal collecting diode with a diameter of $2\text{ }\mu\text{m}$ and a spacing between n-well and p-well equal to $3\text{ }\mu\text{m}$;
- an analogue front-end consisting of an amplifier and a shaper;
- a comparator that permits in pixel discrimination and performs analogue to digital conversion;
- a digital front-end which contains a digital buffer that can store up to three hits, a pixel masking register and a pulsing logic;

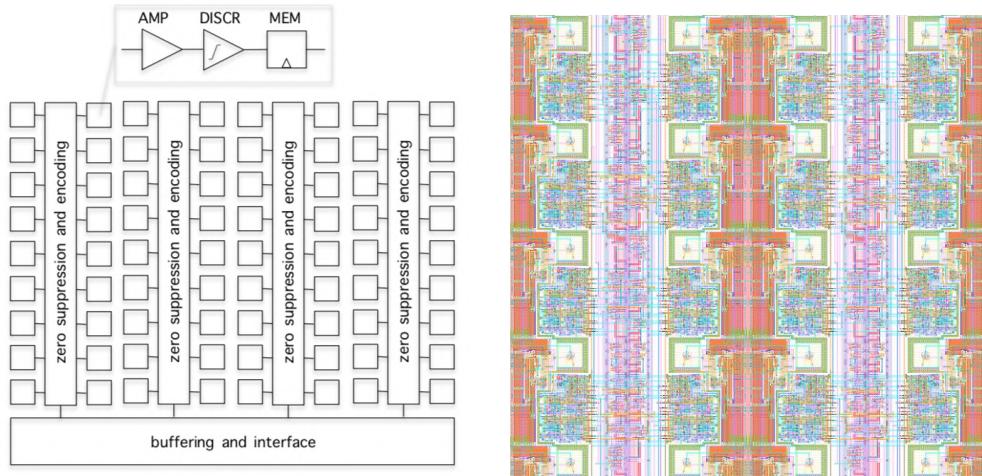


Figure 1.8: ALPIDE readout schematic using the priority encoder mode (on the left) [30]; on the right, microscope view, it is possible to see the collecting diode as octagons inside the green square [32]

In contrast to MISTRAL sensor, a sparsified readout is implemented: a global strobe signal is generated, while the strobe is active, the discriminator output is stored in the buffer.

When the strobe deactivates, the matrix readout begins [13]. This is possible thanks to the availability of fully CMOS logic and to the small transistor size that permits a high in-pixel transistors integration.

The pixels readout is managed by the priority encoder which is data driven and is based on Address-Encoder Reset-Decoder (AERD)[30]. The AERD receives a digital input only from the hit pixels, generates their address and resets their memory buffers. The address are then propagated to the end-of-column peripheral circuitry (figure 1.8).

Zero suppression is automatically achieved as only the hit pixels send their signals to the AERD while non-hit pixels are ignored.

ALPIDE pixel matrix is organized in double columns sharing the same priority encoder circuit: since only hit pixel generates a digital output, the clock does not need to be propagated in the matrix and the power consumption is limited to the hit pixels, moreover, only digital signals are propagated across the matrix [31].

The final result is an integration time of about $5\text{-}10\text{ }\mu\text{s}$ and a power consumption of 35 mW/cm^2 .

Other improvements are the reduction of dead area (achieved by moving the

discriminator and the zero suppression logic to the in-pixel circuitry) and the increase of the radiation hardness, from $1.5 \times 10^{12} \text{ MeVn}_{\text{eq}}/\text{cm}^2$ MISTRAL to $1.7 \times 10^{13} \text{ MeVn}_{\text{eq}}/\text{cm}^2$ ALPIDE [14].

1.3.3 Ongoing Developments

Another ALICE upgrade is in program for the next years to make the experiment compliant to the next High Luminosity Large Hadron Collider (HL-LHC) phase.

The project main innovation is the idea of building the first truly cylindrical tracker for collider experiments by implementing every tracker layers with a single silicon wafer. Another aim is the elimination of the mechanical support structure of the layers thus achieving a further reduction of the material budget, which can be as low as $0.05\%X_0$ per layer.

The sensor chosen for the next upgrade, is a MAPS sensor which is being developed by the collaboration. The technology chosen is TowerJazz 65 nm CMOS process which allows:

- the use of 300 mm wafer that allows the implementation of half-cylindrical layer with a single silicon chip;
- the reduction of the pixel pitch by a factor grater than two that grants a better spatial resolution and the decrease of the sensor thickness to $20 \mu\text{m}$, which allows a greater flexibility. The decrease of the sensor thickness could allows also the complete depletion of the sensor active area that grants the charge collection only by drift, and a significant reduction of the collection time.

The development process has started and the collaboration has obtained the first preliminary results, for a more detailed explanation see chapter 7. However further studies are needed on the sensor performance and the radiation hardness.

This future development will be of great interest and importance for different application and could transform the silicon technology for tracking purposes [33].

Chapter 2

The Limadou Collaboration

The China Seismo-Electromagnetic Satellites (CSES) are the most advanced missions for the investigation of the lithosphere-ionosphere coupling from space.

This is a complex topic due to the number of physical effects that act between Earth and magnetosphere: tropospheric activities (i.e. lightning and volcanoes) and anthropogenic electromagnetic emissions can cause some interactions. Moreover also seismic events can induce ionosphere perturbation and particle precipitation from the inner Van Allen Belts.

Furthermore, the Sun causes perturbation of the geomagnetic structure caused by coronal mass ejection and solar flares and modulates the cosmic-ray flux [34, 35].

CSES-2 is the second satellite that will be launched and will join the CSES-01 satellite to proceed the investigation of the near-Earth electromagnetic environment and of some phenomena of solar-terrestrial interactions.

The satellite is designed to take advantage of a multi-instruments payload composed of nine detectors for the measurement of electromagnetic field components, plasma parameters, and energetic particles as well as X-ray flux.

The Italian contribution to the CSES missions is the design and operation of the High-Energy Particle Detector (HEPD) which main aim is to increase our knowledge of cosmic rays and of some magnetic processes, investigate the spatial and temporal stability of the inner Van Allen belts and the impact of natural electromagnetic emissions on the iono-magnetosphere transition zone. The Limadou Collaboration has developed an improved version of the HEPD detector for electrons in the 3-100 MeV energy window and for proton and light nuclei in the 30-200 MeV/Z energy range [36].

HEPD-02 is the detector designed by the Limadou collaboration for the CSES-02 satellite, which will be launched as second element of satellites constellation.

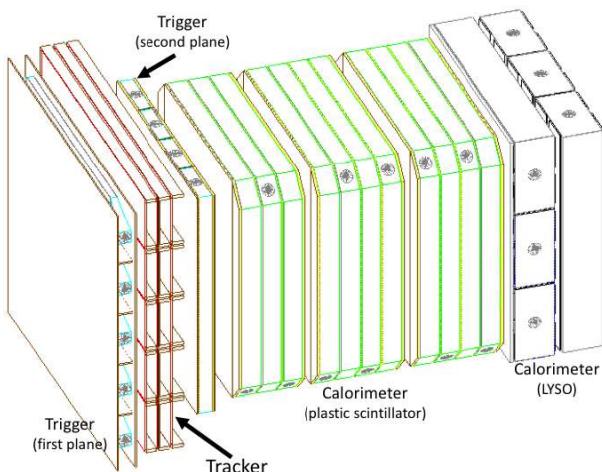


Figure 2.1: Schematic of the HEPD-02 detector. The veto system is not represented in the figure [15]

The detector is composed by two trigger planes, a silicon MAPS tracker, a calorimeter and a veto system.

The first trigger plane is placed over the tracker and is formed by a plastic scintillator segmented in five parts while the second plane is placed under the

tracker and it is arranged as a plastic scintillator divided in four parts. The tracker is composed by five turrets each one containing three staves consisting of the active sensor and a carbon fiber cold plate. Between the staves in the same turret there is a space of 8.6 mm. Each stave contains ten ALPIDE chips disposed in two lines of five detectors and glued to the cold plate. The tracker components and final structure is sketched in figure 2.2.

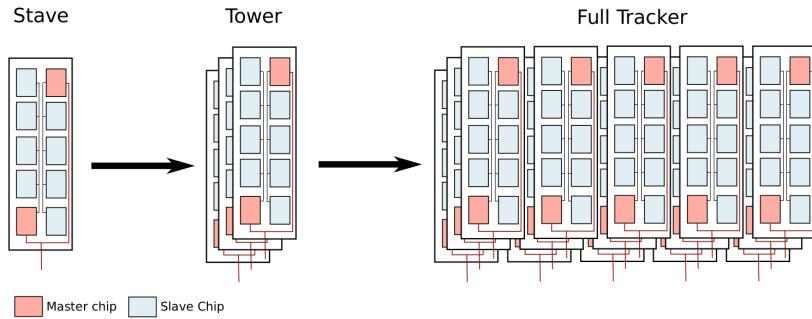


Figure 2.2: HEPD-02 tracker structure: master-slave and turrets arrangement are sketched [15]

The trigger and the tracker are placed over the calorimeter, that is divided in two part: the first is composed of twelve layers of plastic scintillators and the second consists of two layers of three LYSO bars disposed orthogonally one another (figure 2.1).

The veto system is composed by plastic scintillators that are placed along the lateral and bottom side of the detector.

HEPD-02 main innovation is the tracker that will be the first silicon MAPS tracker for space application [37]. A more detailed description of the tracker will be given in the next section.

2.1 HEPD-02 tracker

All space particle trackers built so far rely on hybrid micro-strip silicon sensors, and their readout is made by custom ASICs implementing shaping and amplification stages. However strip sensors are an uncommon technology in modern application causing a slower sensor development and an higher cost [37].

MAPS, instead, provide a more compact solution, since sensor and front-end electronics are embedded in the same silicon substrate. Furthermore they offer a higher granularity, lower noise, the need of much fewer bonding interconnection and last but not least the production costs are lower. On the other hand they are still available only with small areas and relatively high power consuming for space application.

For the HEPD-02 tracker, the only MAPS sensor with adequate requirements was the ALPIDE sensor that will be further described in chapter 3. The ALPIDE chip was chosen as the solution for the construction of the HEPD-02 tracker, although an optimization procedure had to be carried out to adapt the mechanics and power consumption to space requirements.

Parameters	HEPD-01 silicon strip	HEPD-02 MAPS
Tracker dimension	$20 \times 21 \text{ cm}^2$	$15 \times 15 \text{ cm}^2$
Chip dimension	$7 \times 7 \text{ cm}^2$	$3.0 \times 1.5 \text{ cm}^2$
Chip thickness	$300 \mu\text{m}$	$50 \mu\text{m}$
Spatial resolution	$50 \mu\text{m}$	$5 \mu\text{m}$
Power Consumption	8 mW/cm^2	$<19 \text{ mW/cm}^2$

Table 2.1: Comparison between HEPD-01 double sided silicon micro-strip and HEPD-02 MAPS sensor [15, 37]

The main challenges in using ALPIDE for space application are the mechanical stress due to the satellite launch, the thermal stress because of prolonged in-orbit operation and the overall tracker power consumption ($\sim 16 \text{ W}$ for the whole tracker including readout electronics).

The first two critical issue were investigated by several thermal and vibrational test, that did not produce damages or alteration in the performance of the tested prototypes. Thermal issue are solved by using the carbon fiber to dissipate heat, since the only way to realize a cooling system in space is by thermal conduction.

The satellites provides a radiator plane at about 35°C , at the opposite side from the readout electronics, to which the cold plate is thermally and mechanically connected [15]. The thermal gradient along the stave is expected to be lower than 5°C (figure 2.3).

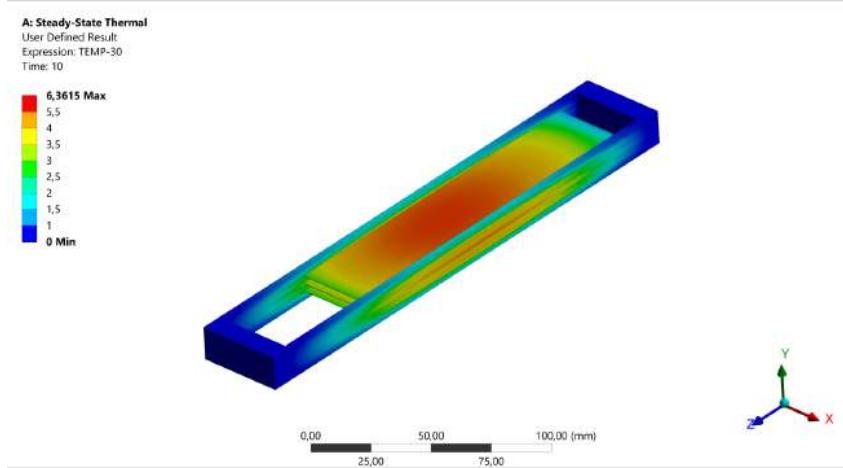


Figure 2.3: Thermal dissipation of a single turret during detector operation [15]

The third issue was solved by choosing a master-slave architecture and by implementing the slave readout through the master local bus at 80 Mbps, while the ALPIDE build-in fast data transmission unit (DTU) is kept permanently switched off. The maximum ALPIDE chip power consumption in this configuration is equal to 55 mW compared to 150 mW in the ALICE ITS [38].

As a consequence, the dead time is increased, but it is still acceptable for the HEPD-02 application given the low trigger rate of the whole system, up to few kHz.

Moreover the ALPIDE clock is normally switched off and it is turned on only

in response to a particle trigger in the first trigger plane.

The first trigger plane is segmented in 5 parts each one corresponding to a tracker turret in order to turn on the clock on the under-laying turret, avoiding the readout of the other turrets.

Furthermore, the segmentation of the tracker in five small sub-unit allows, in case of failure, the loss of only 1/5 of the tracker and also an easier optimization in terms of mechanical and thermal requirements [15].

Chapter 3

ALPIDE Sensors

As briefly explained in section 1.3.2, the ALPIDE is a monolithic active pixel sensor build in TowerJazz 180 μm CMOS imaging process consisting of a pixel matrix of 1024 columns and 512 rows. The sensor thickness is 50 μm . Each pixel has a front-end electronics composed of an amplifier, a shaper, a discriminator and also an event buffer with maximum memory of three events (figure 1.8). All the front-end electronics is embedded in the same silicon substrate as the sensor.

A small depletion region is created by applying a minimum potential of 1 V to the collecting diode, that can be expanded by adding a reverse bias tension to the p-well and to the substrate (max 6V).

The main reference in this chapter is [30].

3.1 Signal formation

When a charged particle crosses the detector, produces electron-hole pairs by ionization. The ALPIDE structure is designed to trap the electrons in the epitaxial layer where they move by diffusion.

When they reach the depletion region, electrons start moving also by drift until they are collected by the collecting diode.

3.1.1 In-pixel signal processing

Each pixel contains some front-end electronics to process and digitize the signal. For the ALPIDE sensor, the in-pixel electronics is given by an amplifier, a shaper, a discriminator and a three element memory buffer.

The signal is collected, amplified, and if it is greater than the imposed threshold, the discriminator gives an high output that is memorized in the event buffer.

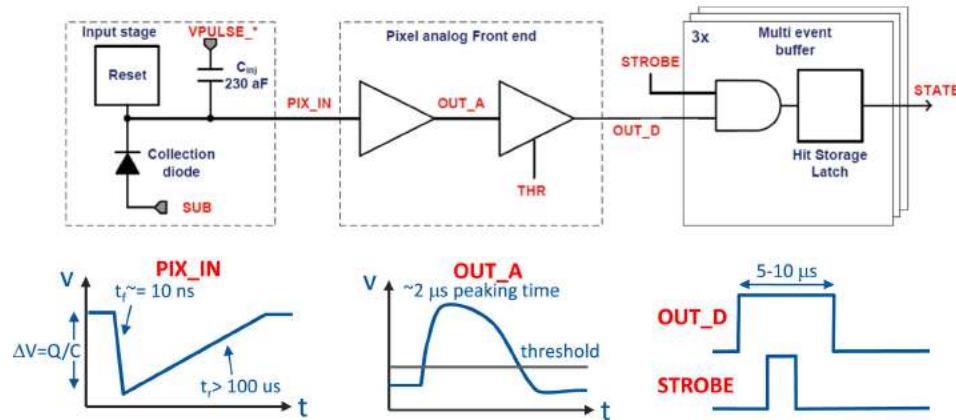


Figure 3.1: Block diagram of the ALPIDE pixel [30].

The front-end electronics is also composed of an injecting capacitor that can simulate the sensor charge collection signal and it is used to test the front-end electronics.

The threshold calibration can be done by injecting different charge values in the capacitor to find the best discriminator parameters for each application expected signal (figure 3.1). Zero suppression is automatically obtained from the in-pixel discriminator output.

3.1.2 Matrix Readout

The matrix is divided in 32 regions of 16 double columns each and it is read with a sparsified approach.

A STROBE signal is generated, and while the STROBE is high, the pixel output is stored in the memory buffer. When the STROBE is deactivated, the matrix readout starts.

Each double column has a priority encoder circuitry that generates the hit pixels addresses and sends them to the peripheral circuitry (figure 3.2).

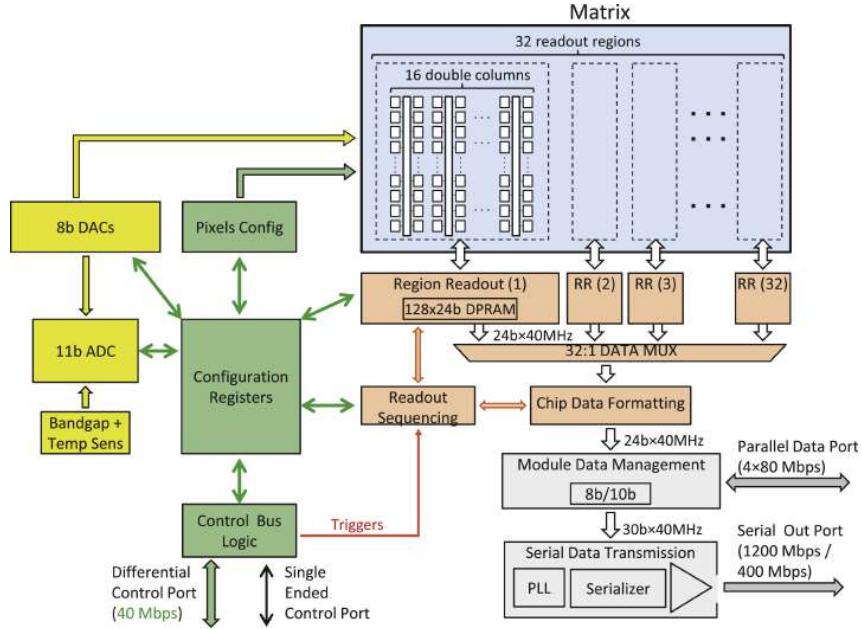


Figure 3.2: ALPIDE block diagram [30].

The periphery includes also a DAC to convert the configuration registers values in tension values and an ADC to convert tension into DAC units.

Every ALPIDE chip has a temperature sensor and when the ADC is properly configured, it is possible to obtain a temperature measurement.

The ALPIDE temperature sensor consist in the measure of a voltage value which depends on the working temperature and is then converted in DAC units by the ADC. A careful calibration must be carried out to obtain the temperature measurements: the two parameters that can affect the ADC value are the power supply voltage received by the chip and the ALPIDE working temperature.

There are two ways in which the matrix can be readout:

- *Continuous mode*: it is designed to sample the matrix status between two subsequent trigger events: the STROBE duration is equal to the inverse of the trigger frequency.
- *Trigger mode*: it is designed to sample the pixel status over short periods of time: the STROBE duration it is usually equal to some hundreds of ns.

The peripheral circuitry can be properly operated by setting the correct value to the periphery configuration registers: they define the ALPIDE readout mode and contain the chip set-up for the current working conditions.

3.2 Analogue in-pixel front-end electronics

When a particle crosses the sensor, it produces electron-hole pairs in the pixels active area; the electrons are collected by the collecting electrode and generate the signal on the *pix_in* node in figure 3.3.

The signal is amplified by the first stage, and then discriminated in the second phase. The discrimination is done by imposing a voltage value and determine if the signal overcomes it or not.

The voltage that is used to discriminate the signal is called threshold and its effect is to control the pixels output. If the signal overcomes the threshold, the pixels output is a logic 1 otherwise a logic 0 is obtained.

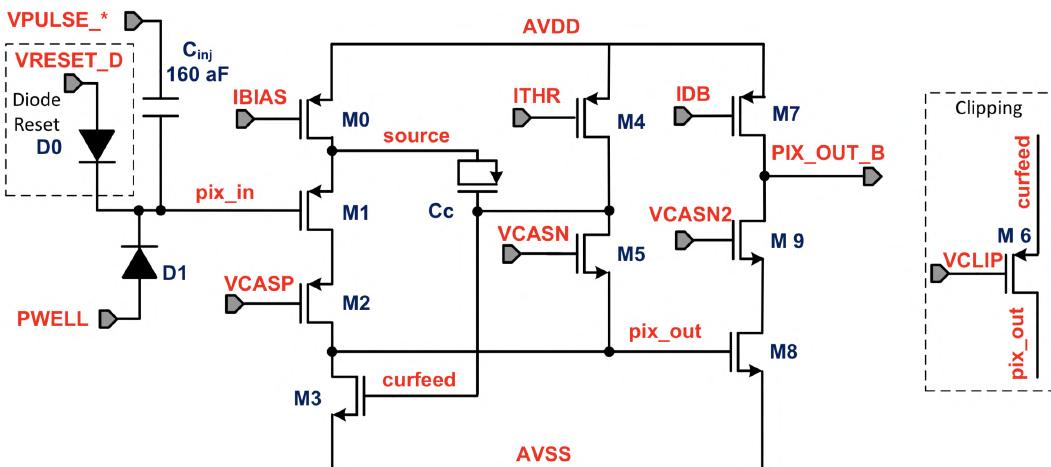


Figure 3.3: Analogue front-end in-pixel circuitry schematic [30].

The most important parameters to determine the ALPIDE in-pixel threshold are:

- **VCASN:** is a voltage parameter that acts as a baseline over which the analogue input signal is superimposed: threshold decreases when increasing VCASN.
- **ITHR:** is a current parameter that determines the pulse shape: the higher is ITHR the higher becomes the threshold.
- **VCASN2:** defines the transistor M9 operating region: must be always set to VCASN + 12.
- **VCLIP:** controls the gate of the clipping transistor, it is important to set VCLIP when applying a back bias voltage different from zero.

To find the correct parameters for having a certain threshold a calibration must be carried out: the VCASN values must be all carefully studied because the threshold has not a linear relation to VCASN. Instead, the threshold has a linear dependence with ITHR, that can be exploited to reduced the ITHR tested values thanks to the use of a linear fit.

Chapter 4

Tracker Assembly Procedure

The Turin Limadou group is responsible for the assembly and test of the modules that will be installed on the detector. For space experiments it is necessary to build two copies of the detector that must then be tested on beam and by applying different accelerations to evaluate the resistance of the system to the flight.

The two detectors constitutes the Qualification Model (QM) and the Flight Model (FM).

The assembly procedure reported in figure 4.1, can be divided in two parts:

- The Hybrid Integrated Circuit (HIC) Assembly: this stage is composed of the ten ALPIDE chip aligned in their final position, they are glued to the Flexible Printed Circuit (FPC) and then electrically connected by wire bond to the FPC.
- The Stave Assembly: this stage is composed in various parts, the assembly of the mechanical stave (carbon fiber U-structure for mechanical stability), the cut of the FPC extension on the sides (TAB and wings), and the gluing of the HIC on the cold plate.

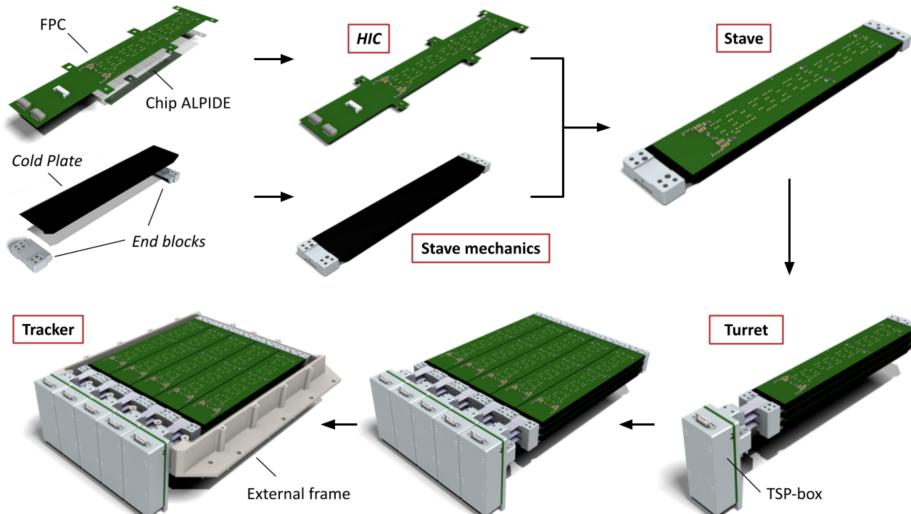
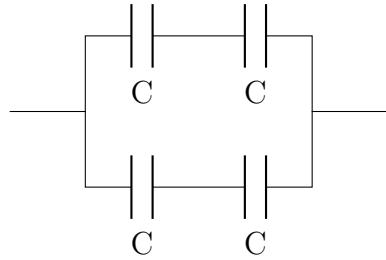


Figure 4.1: HEPD-02 tracker: assembly schematic [37]

Before describing in detail the assembly process, a brief explanation of the FPC is outlined. The FPC is the structure that carries the power from the power supply to the sensors and the signals from the ALPIDE to the acquisition system.

The main differences between the FPC designed for the ALICE experiment and the one for the Limadou project are the presence of a greater number of capacitors and the addition of DS18B20U temperature sensors, hereafter called Dallas sensors.

The capacitors are a critical element in space environment because they store a lot of energy and are very small. For this reason, a redundancy policy is applied and, to give a capacitor C, four capacitors of equal capacitance C are disposed as sketched in the following scheme.



In this way, the total capacitance is maintained, while if a damage occurs during the flight or the operation, the other capacitors keep working.

The other addition is the presence of six temperature sensor (DS18B20U) along the entire FPC length, which give the temperature measurement with respect to their position.

The following part of this chapter is dedicated to the tracker modules assembly procedure.

4.1 HIC Assembly

Since the collaboration forecast an assembly of about 30 modules, a manual alignment procedure was chosen: the ALPIDE chips are positioned by an operator in a position identified by a Coordinate Measuring Machine (CMM). The CMM is a machine that, thanks to the definition of a reference frame (figure 4.2), is able to measure positions with a resolution of about 1 micrometer, whenever a reference system is set at the beginning of each operation. In this specific case the CMM is used to guide the operator during the chip positioning phase, by offering a visual reference point on the field of view, given by a cross.

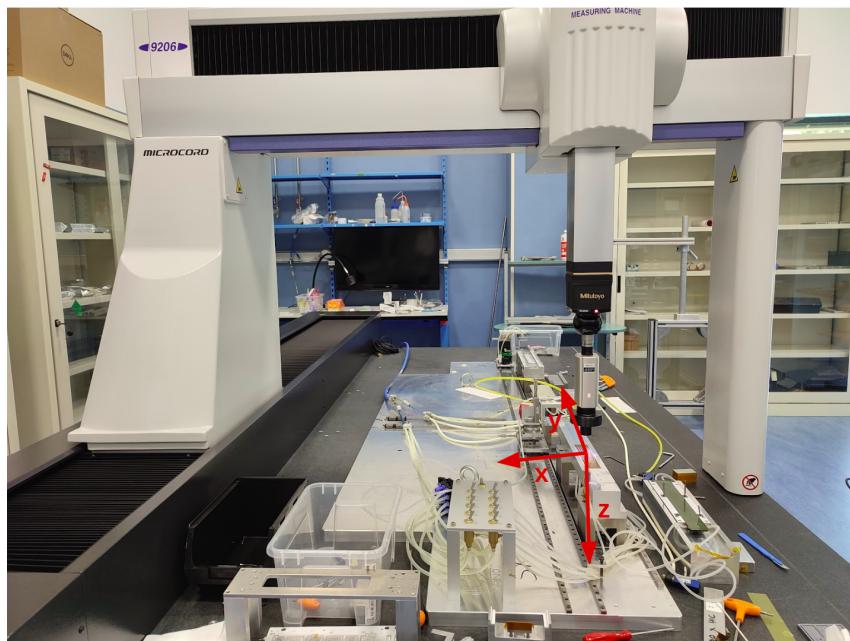


Figure 4.2: CMM reference frame for the ALPIDE alignment

To align the sensors, each chip is taken from the box using an alignment station that exploits the vacuum to keep the ALPIDE fixed to the support.

Then the chips are placed close to their final position, and the alignment procedure starts.

On the ALPIDE top side, there are four markers, each one consisting in a cross, placed near the corners, in a position known with a precision below the micrometer.

The alignment procedure is guided by the CMM which measures the markers positions and guides the operator until the center of the reference marker is in the expected position defined by the cross in the field of view (figure 4.3).

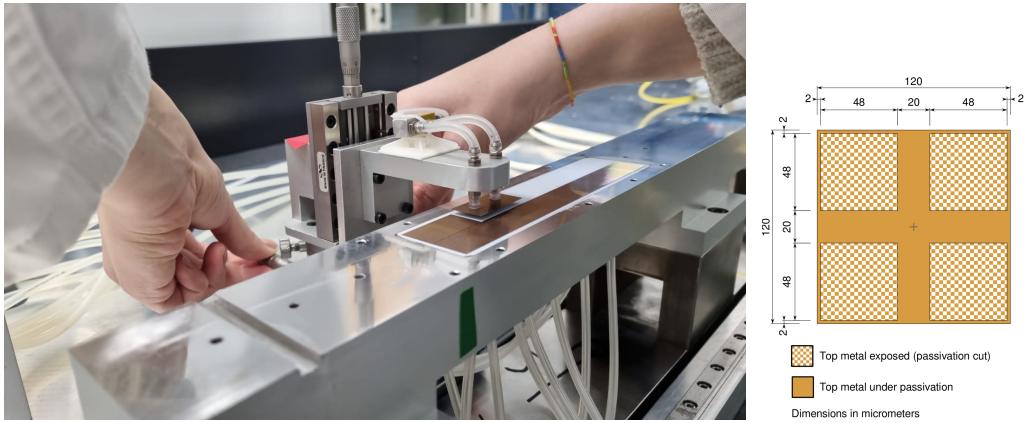


Figure 4.3: On the left: operator positioning the chip in the correct position. On the right: alignment marker on the ALPIDE back side

The alignment is divided in three steps: the first is the rotation, then there is the shift and at the end, the chip is lowered to the final position.

The rotation phase is used to correct the chip orientation with respect to the exact position, in this part only the angle and the y coordinate are involved. This procedure is very delicate, because the alignment station rotates around its axis, which is not the chip one. If a big rotation angle is present, a repetition of the rotation phase is needed.

The shift procedure is used to correct the x and y position of the chip with respect to the nominal position. At the end of this phase, if the chip is in the exact position, it is possible to lower it down on the base, otherwise a repetition of the whole process is needed.

The third step is the most delicate one, because it is possible that when the chip is close to the base, the chip is forced to rotate due to the friction with the base. If the chip moves in this phase, a repetition of the whole alignment is needed.

When the chip is on the plane, the CMM measures the distance between the expected position and the marker position: the difference must be lower than $15 \mu\text{m}$ to be accepted, otherwise a repetition of the entire sequence is needed. Then the vacuum of the alignment station is released and the one on the base is switched on, and it is possible to move to the next chip.

When all the ten chip are aligned, it is necessary to verify that the chips lay on a plane: this is done by measuring the markers position on each chip and finding the distance from the plane where they lay. The alignment is validated if the maximum distance along z from the ideal position is less than $50 \mu\text{m}$.

At this point, the FPC is prepared: it must be carefully cleaned to avoid

dust presence that can cause scratches on the chip surface or compromise the feasibility of wire bonds. Then it is placed in a proper holder, called module gripper, which has a vacuum system to keep the FPC during the operation of glue deposition and positioning it over the ALPIDE chips.

To place the glue, an adhesive mask is positioned on bottom of the FPC and an operator uses the CMM to check if the mask holes are not superimposed to the connection pads that must be clean to allow a correct electrical connection. The glue, a bi-component epoxy adhesive, is then spread over the mask and distributed by means of a spatula (figure 4.4).

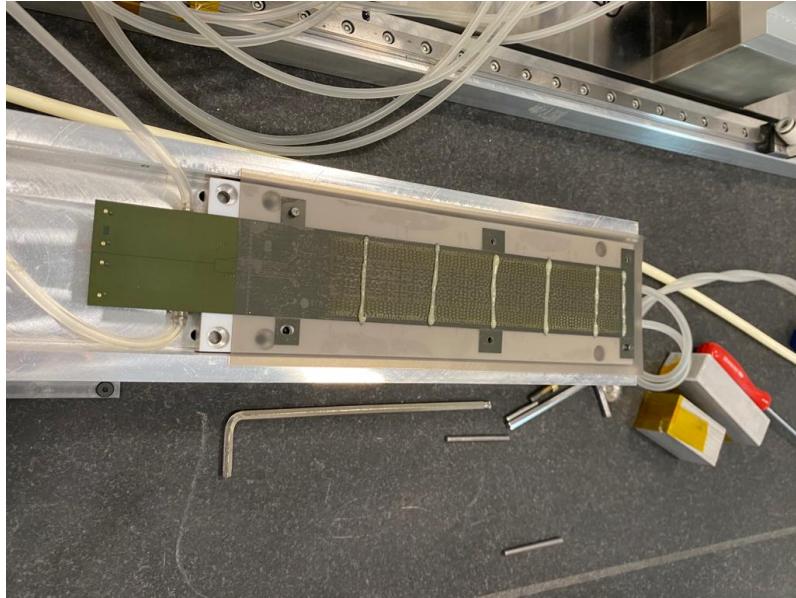


Figure 4.4: FPC kept with the module gripper, covered by the mask and the glue

At this point, the mask is carefully removed and another check is performed to see if the glue drops are evenly distributed and are not too close to the pads area.

At the end, the FPC is placed on top of the previously aligned ALPIDE chips: to check if the position is right, there are four holes on the module gripper allowing to verify the centering of the ALPIDE on the FPC pads.

Once the FPC is in position a weight is placed on top of the FPC gripper and the assembly is kept in position until the glue has polymerized.

After 24 hours, the glue has polymerized and the quality assurance procedure foresees to check whether any glue drop has covered the chip pads. In this case the glue must be removed to allow the wire bonding between the sensors and the FPC. Furthermore, a visual inspection of the HIC back side is performed to control that no damage was done to the ALPIDE chips during the alignment.

At this point, the wire bond between the ALPIDE pads and the FPC can be done and this process is performed by the Bari group. Each sensor pad is connected to the FPC by three wire bonds, moreover, the bond strength is tested by means of an automatic pull test machine, which pulls a subset of

wire bonds until they break and the breaking force is then measured. Once the wire bond procedure is finished, the resistance between the power supplies and the ground pads on the FPC are measured to check the presence of short circuit.

The HIC are then sent back to Turin for the first qualification test, explained in chapter 5, and the subsequent assembly procedure.

4.2 Stave Assembly

The stave assembly is divided in four phases: after each step the stave is tested to check if it is still working properly.

TAB and WING cut Procedure

The first step in the stave assembly is the removal of the FPC extension that allowed the connections during the HIC qualification test (TAB) and the wings used during the FPC and HIC manipulations (WING).

This operation is very delicate, because the wings are very close to the copper lines that lead the power supply to the ALPIDE chips, furthermore a very linear and precise cut is needed.

For this purpose the HIC is placed on a special base and it is steadily fixed to it during the cut. A scalpel is used to cut the TAB and WINGs (figure 4.5). Once the cut is done, the HIC is placed on the HIC testing base and tested.

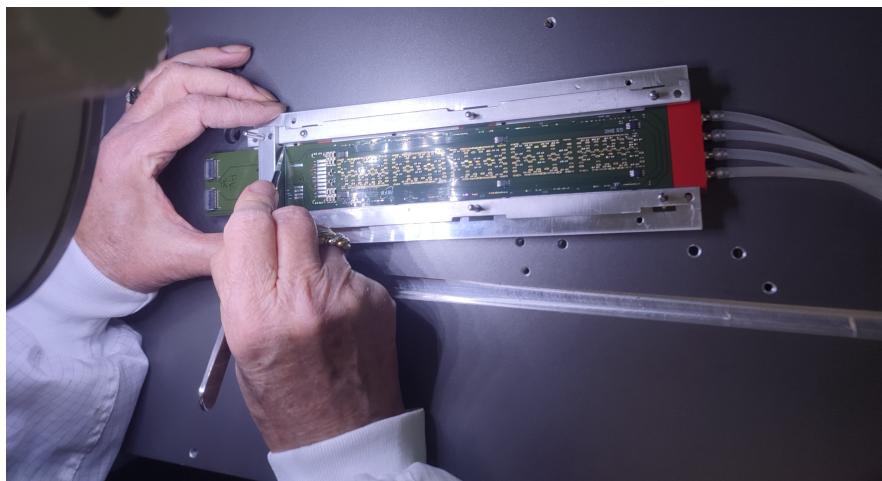


Figure 4.5: Tab and wing cut operation

Mechanical Support Assembly

Before gluing the HIC to the carbon fiber, a previous step is needed: the assembly of the mechanical support to keep the modules in place. The mechanical support is composed by the cold plate glued to a lateral structure called end blocks in which pins and screws can be fixed to then assembly the staves into a turret.

The cold plate is made by three layers of carbon fibers, disposed perpendicularly one another. The carbon fiber is already shaped in a U-structure, that

will give the spacing of 8.6 mm between the three HICs in each turret. First of all, the carbon fiber is conductive so it must be isolated in order not to have conduction between the ALPIDE chips. The carbon fiber is covered with a 100 μm thick glue layer which grants the isolation. The next step is the positioning and gluing of the end blocks at the sides of the carbon fiber cold plate. The positions of the end block with respect to the cold plate is controlled and measured by means of the CMM. When the glue is dried, the height of the cold plate is measured, and if the measurements are acceptable, a mechanical support is considered ready to be used to support a stave.

STAVE Alignment

At this point, it is possible to glue the HIC on the mechanical support. For this process, the CMM is needed and another reference frame must be used (figure 4.6).

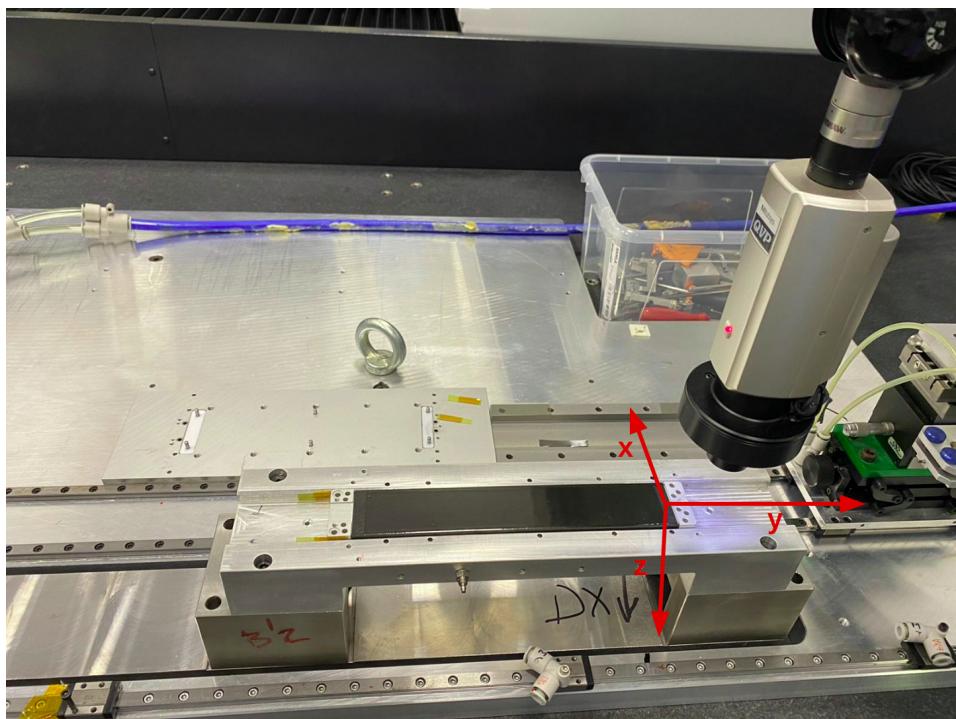


Figure 4.6: CMM reference frame for the stave assembly

The mechanical support is covered with a proper mask and the glue is distributed on the whole cold plate.(figure 4.7).

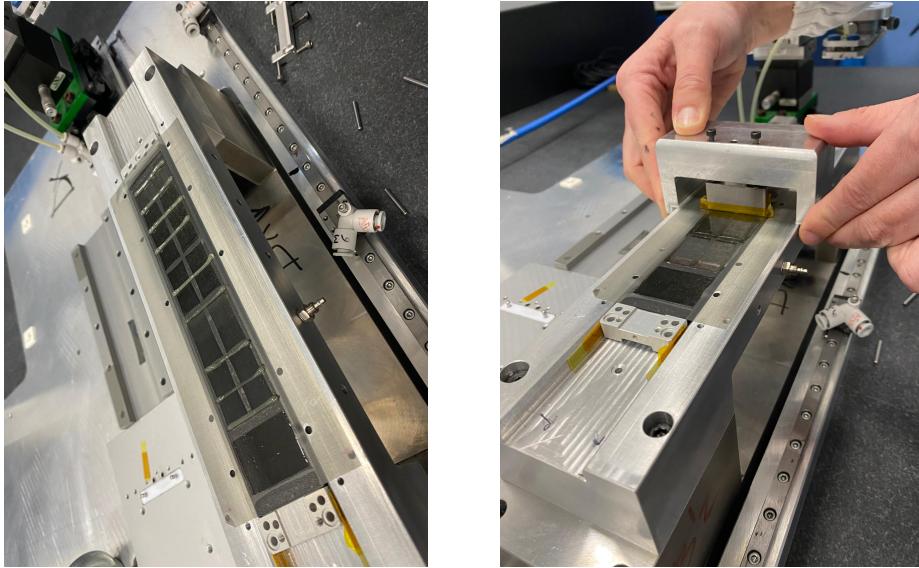


Figure 4.7: On the left: mask for gluing the ALPIDE on the mechanical support. On the right: glue distribution thanks to a spatula.

The HIC can now be taken with the module gripper and placed on top the cold plate. Few pins are used to fix the HIC gripper and the CMM is used to guide the positioning of the HIC with respect to the mechanical support, using the chip corners as a reference.

Thanks to a micrometric screwing system, the module gripper is moved until the alignment markers are in the right position. The stave is then left in position for 24 hours.

STAVE Soldering and Turret assembly

The staves are then sent to Trento, where the local Limadou group is responsible for the soldering of the cables (figure 4.8) that will be used on the satellite to power the staves and of the subsequent step: the assembly of three staves in a turret with the corresponding readout electronics.



Figure 4.8: Wire soldering on the FPC pads: the stave can now be connected to the final powering and readout system

Chapter 5

Qualification Procedure

After the HIC is assembled and the chips are bonded to the FPC, the system can be tested. At the end of every step of the assembly, the detectors are tested to check if any damage occurred during the procedure. The systems on which the test can be performed are the HIC, the HIC after the TAB and WING cut, the stave, and the stave after the wire soldering.

After the TAB is cut, the only way to test the detector is using a special tool which allows contacting the pads on the FPC, the same where the wires will be then soldered.

In this chapter, a description of the qualification tests and the expected output is carried out: the results are presented for a single HIC, but every module produced must satisfy the minimum requirements set for each test step. If the requirements are not satisfied the HIC is excluded from the choice of modules for the tracker construction.

5.1 Set-up

The HICs were tested in the dark by placing the aluminium cover superimposed to the FPC, leaving some free space in order not to damage wire bonds. The dark condition must be used to keep the leakage current as low as possible.

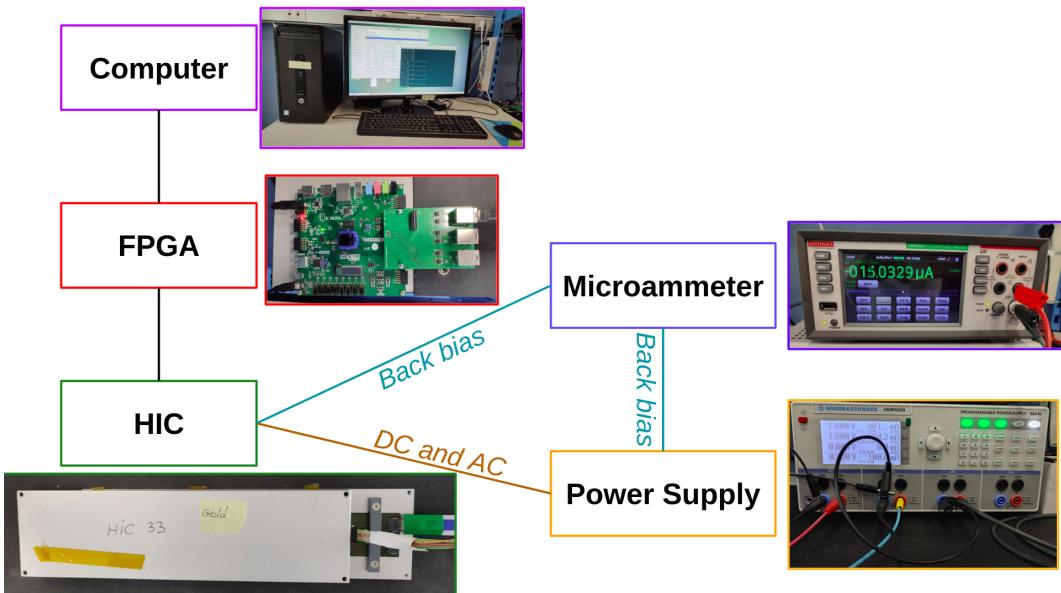


Figure 5.1: Set up used for qualification tests: the HIC is powered by a power supply and connected to an FPGA that sends the readout commands from the computer to the device under test (DUT)

The power is given to the ALPIDE via the FPC that is connected with a Rohde&Schwarz HMP4040 power supply: the channels give the digital (channel 1), the analogue (channel 2) and the back bias (channel 3) voltages to the HIC. Digital and analogue tensions are set to 1.8 V and are separately given to the ALPIDE chips.

On the other hand, the back bias voltage is kept at 0 V in the first tests, when the correct working of the module is established, a back bias voltage is applied and the currents are measured by a micro-ammeter. The ammeter used is a Keithley DMM6500.

The tests are managed by an FPGA that is controlled by a computer: the computer sends commands to the FPGA that sends them to the ALPIDE chips. The answer is generated and the information goes the other way round. The setup is shown in figure 5.1.

The HIC are probed using the connectors on the TAB, but after the cut, the tests are performed by electrical connection with the pads on the FPC thanks to an specific tool that carries the connectors and allows the proper powering and communication of the sensor.

The programs and the FPGA firmware are developed by the Trento group that is also in charge of the readout system of the full detector. The ALPIDE readout is based on the read and write of end-of-region registers present in the periphery, as described in chapter 3.

In the next section, the results obtained testing HIC 033 are presented. HIC 033 is chosen as reference sample for explaining the procedure and showing reference plots.

5.2 Tests

To access the quality assurance for each HIC a set of fundamental tests was defined.

- base electrical tests to verify the absence of damages:
 - currents measurements in the idle condition and when the clock is distributed to the ALPIDE chips;
 - photo taken with a thermal camera;
 - Back bias current curve as function of the applied back bias voltage;
- qualification tests on whose output the selection cuts are applied:
 - chip scan;
 - digital;
 - threshold scan;

In the next paragraphs a more detailed description of each test and the expected output is outlined. The chosen order is the one used during the qualification procedure.

Currents in idle and clock on

The first important check is that the currents at power-on are within the expected limits: each ALPIDE chip, working as slave, consumes about 12 mA on the digital and 10 mA on the analogue channel. Due to the presence of two master chips, the total current will be about 20 mA higher, because each master drains approximately twice as much as a slave chip.

Once current values in idle state (no clock) are stored, the clock can be spread to the whole matrix: the expectation is an increase in the digital current, while the analogue must remain constant.

In table 5.1, the measured currents for HIC 033 are presented: the colored cells refer to the expected value.

	Digital	Analogue
Idle	142 mA (143 ± 7) mA	124 mA (125 ± 3) mA
Clock on	452 mA (453 ± 9) mA	123 mA (124 ± 3) mA

Table 5.1: Currents in idle and clock on for a sample: in the colored cells the reference current value is reported

Thermal camera photo

The second test is the verification of the working temperature of the HIC to check the presence of hotter points that could be sign of a mechanical damage. To do this test, a photo with a infrared camera is taken and the color uniformity as well as the maximum measured temperature is controlled. An example of the expected thermal camera photo is shown in figure 5.2.

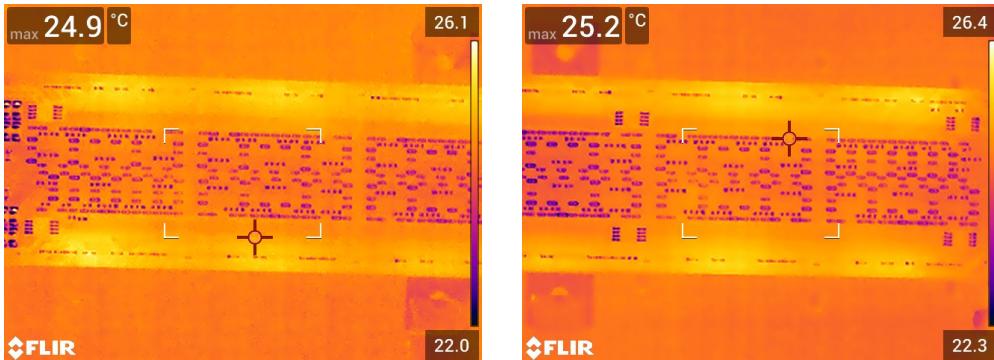


Figure 5.2: Thermal camera photo in the clock on condition

Chip scan

The third step is checking if all the chips communicate correctly with the acquisition system. For this purpose, a set of known words is written on and consequently read out of each chip memory register. The outcome of the test consists in the chip ID (chip identification address) which is printed on the output data stream if the chip responded correctly. In figure 5.3, the ALPIDE addresses and positions along the FPC are shown.

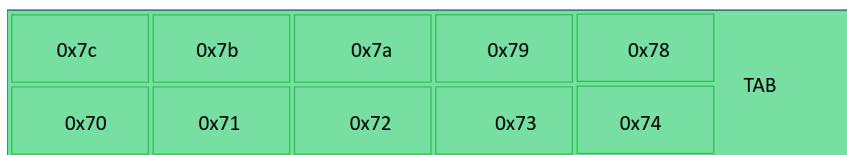


Figure 5.3: Address of the chips located in their positions along the FPC

Digital scan & White scan

Another test is the digital scan, to test the digital response of the chip. It consist in injecting ten times a fixed amount of charge in each pixel and then

try to read it. For each pixel a charge injection circuit is present before the amplification and shaping stages of the front end. If the pixel reacts positively to the injection, the hit is stored 10 times: the number of times a pixel reacts to the injection is plotted in a map with the row number on the x axis and the column number on the y axis; the test output is reported in figure 5.4.

The following test is the white scan, which is complementary to the digital scan and aims to find the pixels that cannot be masked during the readout process. All the pixels are masked and then charge is injected, as for the digital scan. The expected output is zero for every pixel in the matrix, if correctly masked. When a masked pixel reacts positively to the injection we can say that the masking procedure did not work. The pixel is tagged as unmaskable in the matrix. Nevertheless such pixels can be excluded from the data taking via software masking in the read-out phase.

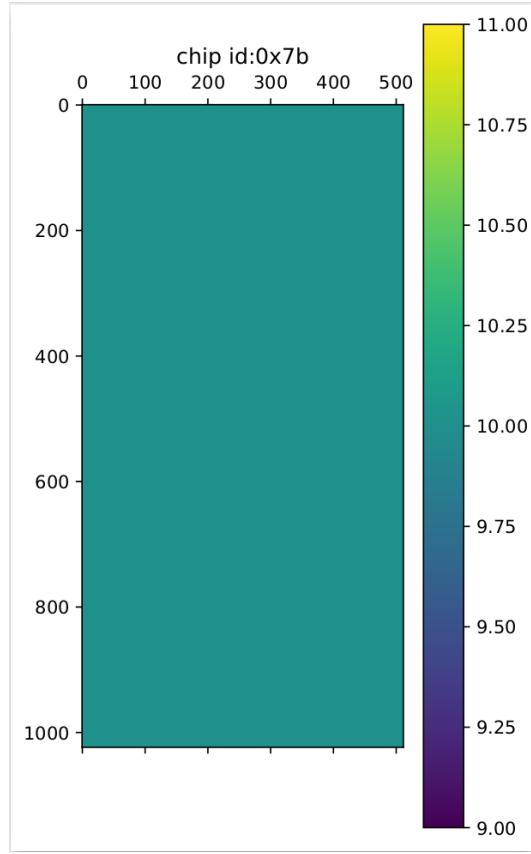


Figure 5.4: Digital scan output for a chip

Threshold scan

This test is devoted to determine the threshold of the front end discriminator, for each pixel in the matrix. Thirty different charge values, ranging from 0 to 300 equivalent electrons, are injected in every pixel, each one for 20 times. The signals are processed by the front-end electronics that is supposed to give a binary output equal 1 whether the signal has overcome the threshold or equal 0 if not.

To check the threshold, the histogram of the binary output as a function of injection charge is fitted with a s-curve. Then, the derivative is taken: the

average value correspond to the pixel threshold, while the width represents the pixel electronic noise.

The output is a map in which the x and y are the coordinates of the pixel and the z axis represent the pixel threshold, measured in equivalent electrons.

The map in figure 5.5 is generated by injecting charge between 10 to 300 equivalent electron spaced by step of 10 electrons repeating each value for 20 times.

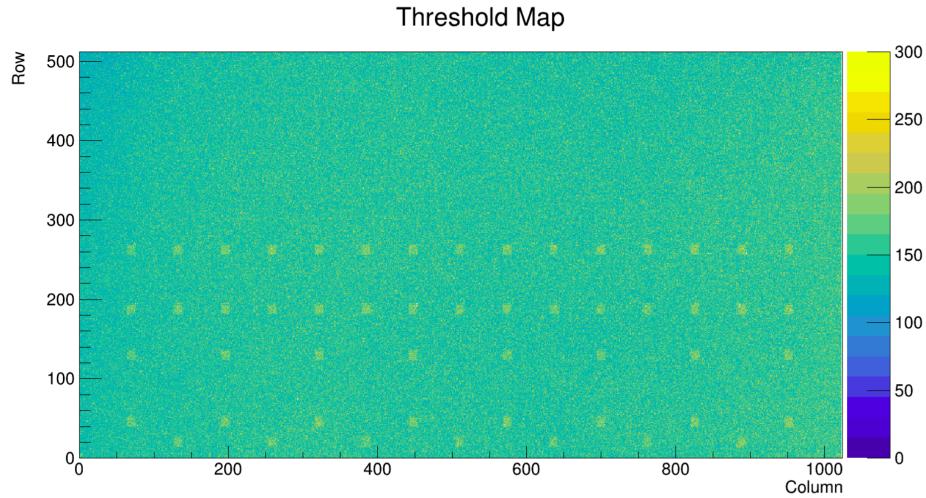


Figure 5.5: Map of the ALPIDE with the pixel threshold on the z axis

The uniformity of the threshold is very important to permit a uniform performance of the sensor. From the threshold scan it is possible to obtain also the noise distribution on the chip which must also be as uniform as possible. For the pixels under the connection pads, the threshold and noise is higher, see figure 5.5 and 5.6: this effect is probably due to a change in the pulsing capacitance C_{inj} ; parasitic capacitance might be induced by the metal of the pads deposited over the pixels [13].

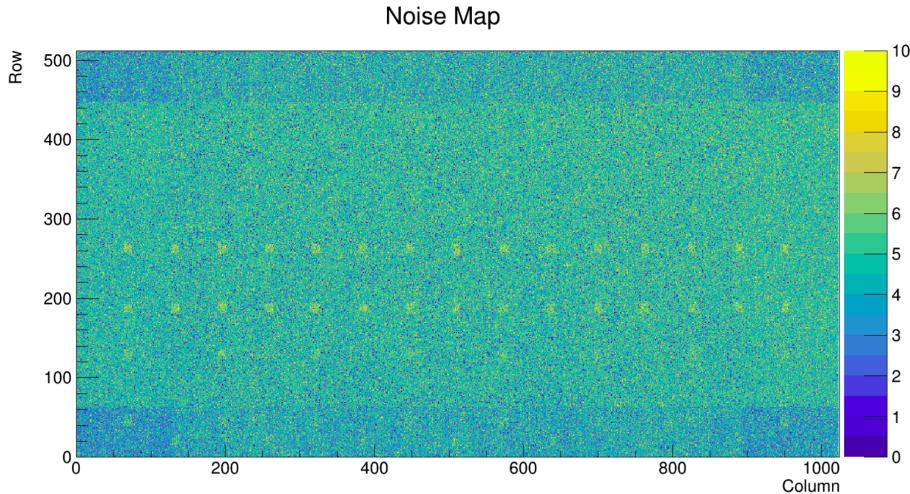


Figure 5.6: Map of the ALPIDE with the pixel noise on the z axis

Back bias curve

To evaluate the possibility of applying a reverse bias voltage to the sensor substrate the current versus reverse bias voltage is measured. The reverse bias tension is gradually given to the ALPIDE chips always verifying that the current stays lower than a certain limit. If the reverse bias current is always smaller than 10 mA for a voltage lower or equal to -3 V, reverse bias can be applied to this HIC.

In figure 5.7, a sample curve is shown.

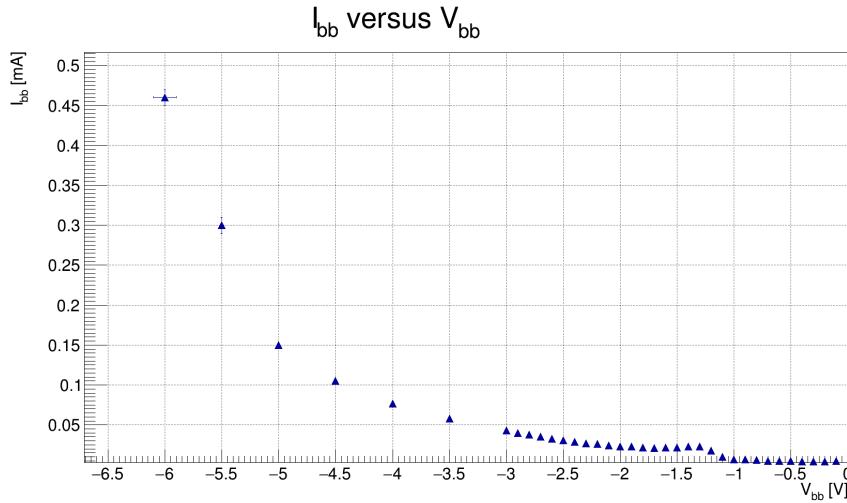


Figure 5.7: Back bias curve for a HIC, to which back bias is applicable

5.3 Threshold Tuning

Each HIC has ten ALPIDE chips that can have different average thresholds. For this reason a tuning process must be done to obtain the parameters to set the same average threshold on every chip.

This procedure will be done on the final system. However it was carried out on a sample HIC (HIC 033) to understand how the parameters affect the threshold and to develop a code for this process. Another difference is that the threshold tuning will be done on a subset of pixel to reduce the time needed for the test, while the test described here is done on all the matrix.

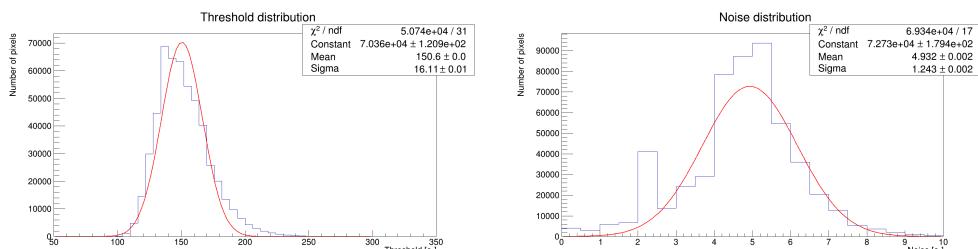


Figure 5.8: On the left: threshold cumulative distribution on a chip, on the right: noise cumulative distribution on a chip, both distribution are obtained with VCASN = 50 and ITHR = 50

For every parameter choice, the average threshold on the chip is calculated by a gaussian fit on the threshold distribution: the mean value gives the threshold and the width gives the dispersion of the threshold values on the chip.

The same procedure is done for the noise distribution. In figure 5.8, the threshold and noise cumulative distribution for a chip are shown.

The threshold scan is repeated with different parameter configuration. For back bias voltage of 0V the tested values, in DAC units, were:

- VCASN: 50, 52, 53, 56, 60;
- ITHR: 50, 60, 80;

and the average threshold as function of ITHR and VCASN are plotted in figure 5.9.

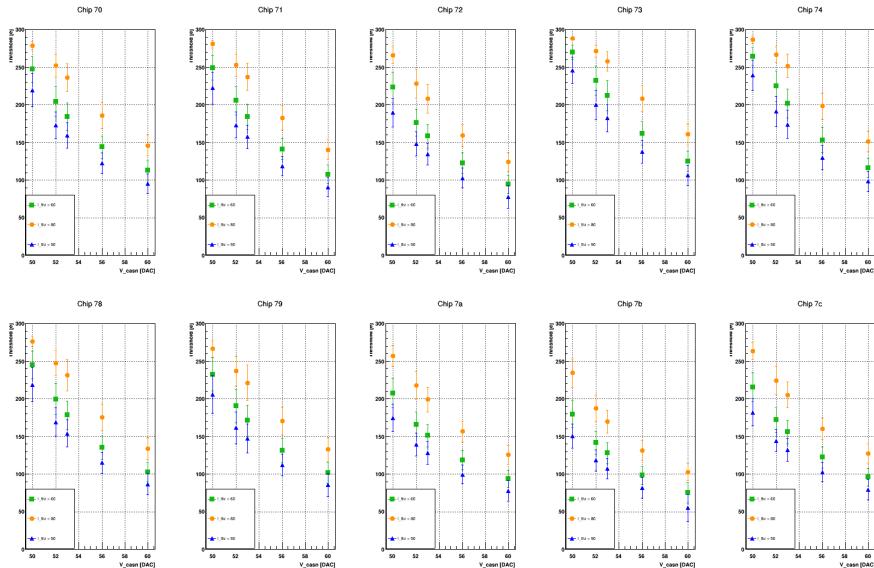


Figure 5.9: Average threshold for different parameter configurations at $V_{bb} = 0V$

The threshold tuning procedure must be carried out for every reverse bias voltage: the satellite power supply can give only $V_{bb} = 0V, -1V, -3V$, values for which the parameters to define the threshold must be found.

This test leads to the definition of the parameters that will be used for the threshold tuning on the tracker once this will be in orbit, they are reported in table 5.2.

V_{bb}	VCLIP	VCASN	VCASN2	ITHR
0V	0	50, 52, 54, 56, 58	VCASN +12	50, 60, 80
-1V	35	76, 78, 80, 82, 84, 86	VCASN +12	50, 60, 80
-3V	60	104, 106, 108, 110, 112	VCASN +12	50, 60, 80

Table 5.2: Parameters values, in DAC units, for the threshold tuning on the final tracker

The threshold tuning was carried out for the HIC 033 at all reverse bias voltages: figure 5.10 reports the obtained curves. For all the reverse bias voltages, the configuration files to have a threshold of 150 equivalent electrons were generated.

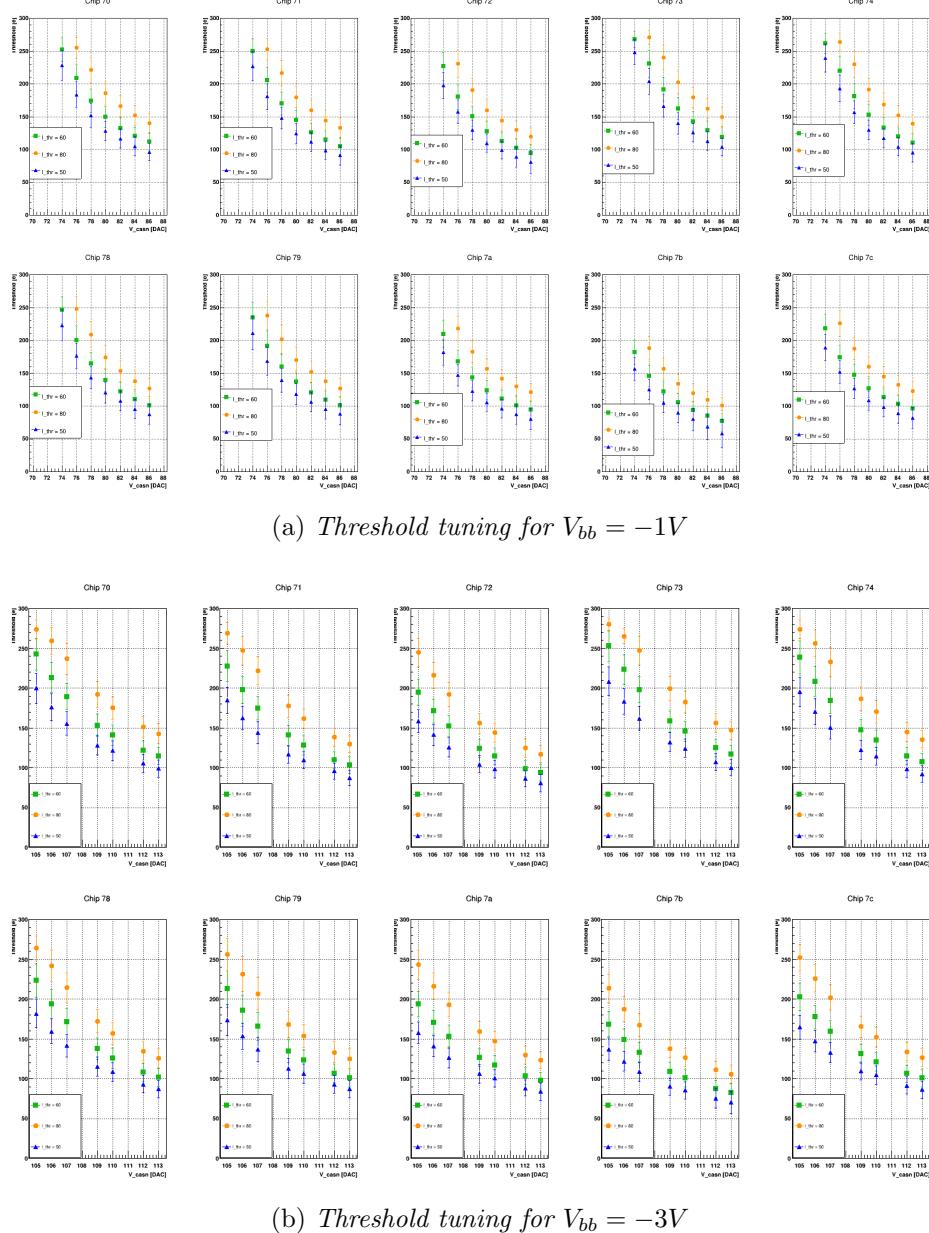


Figure 5.10: Threshold tuning results for HIC 033 when applying a back bias voltage

Chapter 6

Temperature performance dependence studies

As described in 2.1, the performance as a function of temperature is an open point in the HEPD-02 tracker operation. In particular, from figure 2.3, a gradient of $\sim 6^\circ\text{C}$ is expected along each stave, and the collaboration needed to verify if this could induce substantial performance variations.

The Limadou collaboration is interested in the study of the ALPIDE performance at temperatures between 30°C and 40°C . At the same time, the ALPIDE operation at different temperatures was never investigated in detail before. For this reason the range under inquiry was increased to -10°C to 50°C .

Furthermore, the ALICE collaboration is interested in the calibration of the temperature sensor on each ALPIDE chip, between 15°C and 40°C . This target was not easily achievable on their modules, because no temperature reference is present on the ALICE ITS FPC.

Limadou needs a temperature reference, since this is necessary for working in the space environment, where it is mandatory to keep under control the detector operating conditions. As a consequence, six temperature sensors DS18B20U, hereafter called Dallas sensors, were placed on the FPC; they allow a temperature reference in Celsius degree to calibrate the ALPIDE temperature sensor, which was read in ADC units.

6.1 Set-up

The temperature study was performed thanks to the use of a climatic chamber. The setup described in 5.1 was placed near the climatic chamber while the HIC or STAVE under study were placed inside.

The climatic chamber in use does not have a system to control the air humidity and for this reason, a hygrometer was placed inside the chamber. To reach temperatures lower than 20°C , a dry air system was used and can be seen in figure 6.1. The pipe, in figure 6.1, is connected to a compressor plus refrigerator system, and injects air at controlled conditions of temperature and humidity inside the climatic chamber.

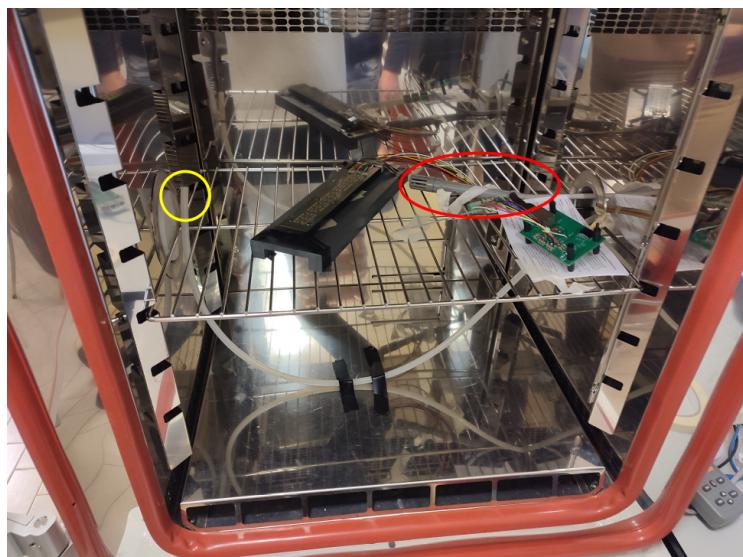


Figure 6.1: Climatic chamber setup: the hygrometer (red circle) and the dry air system (yellow circle) are highlighted

6.2 Dallas Sensors

Six Dallas sensors are placed along the FPC, see figure 6.2, and the sensors readout is made in serial number order. To understand the readout order, a heat gun was used to warm up a sensor and then read all the Dallas: the one that reported the higher temperature corresponded to the heated one.

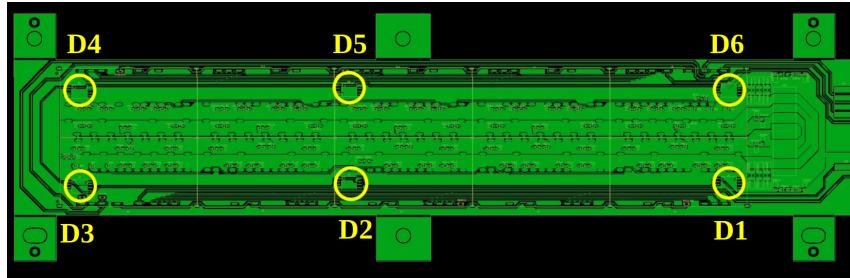


Figure 6.2: Dallas sensor on the FPC with the corresponding position name

The first measurements were aimed at determining if the temperature inside the climatic chamber was uniform, specifically to verify that the chamber temperature sensor reported a value compatible with the one of a thermometer placed near the HIC.

Moreover the temperature measured by the DALLAS was used to determine the relation between the sensor temperature and the climatic chamber temperature both in idle and clock on condition. Furthermore it was also interesting to see whether a difference was seen between Dallas sensor placed over master or slave chips.

The initial ramp was done by taking the climatic chamber from room temperature to 30 °C and measuring the Dallas sensor every 30 s, leaving the HIC without the clock enabled. The same test was repeated with the clock kept on for the whole time.

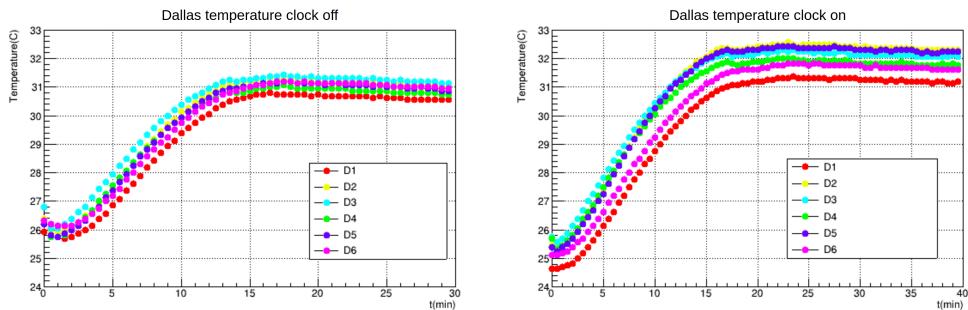


Figure 6.3: Dallas temperature as function of time in a ramp from room temperature to 30 °C: clock off operating condition (on the left) and clock on (on the right)

The results are shown in figure 6.3: no difference is visible between Dallas placed over a master and over a slave chip for clock off but the values become closer (red and magenta dots) for clock on measurements. This is expected since only in clock on mode the master behaviour differs from the slave one. The error on each temperature value corresponds to ~ 0.5 °C. Since the six

temperature measurements are very close, even if not really compatible within errors, the average of all the six Dallas measurements can be used as temperature value for each HIC.

Another observation is that the clock presence causes an increase in the temperature of about $\sim 1.5^{\circ}\text{C}$. The working condition requires the clock enabled, so the subsequent measurements were done all in the clock on condition.

To validate the temperature measurement of the thermometer integrated in the climate chamber, an independent measurement is done using a thermometer placed inside the climatic chamber. All the values are then compared to those measured by the Dallas sensors. The results are shown in figure 6.4 on the left.

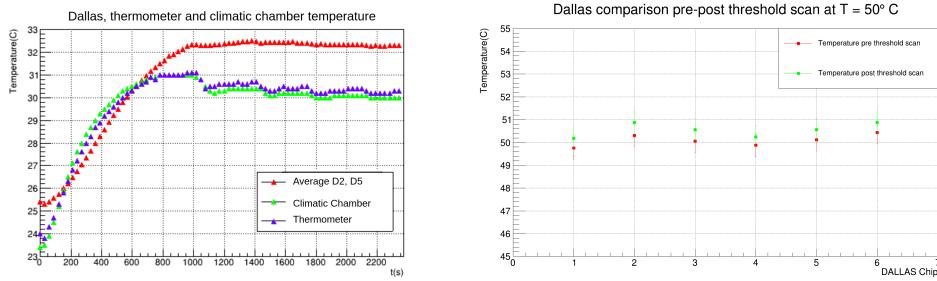


Figure 6.4: On the left: comparison between thermometer, Dallas and climatic chamber temperature values in a ramp from room temperature to 30°C . On the right: comparison between Dallas temperature before and after a threshold scan performed at 50°C .

The temperature measurements made by the thermometer and the climatic chamber sensor are compatible and do not show significant difference, within errors. On the other hand, the Dallas measurements with the clock on condition, shows, at the thermal equilibrium, a difference of about $\sim 2^{\circ}\text{C}$ with respect to the climatic chamber. This difference can be attributed to the fact that the Dallas are placed right above the ALPIDE chips which temperature is higher than the ambient one, even after the thermalization of the climatic chamber.

At the end, before starting the threshold measurements, the chamber was kept at $\sim 50^{\circ}\text{C}$ and a threshold scan was launched measuring the temperature at the beginning and at the end of the test. In figure 6.4, on the right, the results of this measures is reported: a difference of $\sim 0.2^{\circ}\text{C}$ in the temperature values was found, showing that the increase in the temperature due to the operation is not significant, according to the measurement errors of $\sim 0.5^{\circ}\text{C}$. The measure after the threshold scan was hence chosen as reference for the temperature sensor calibration.

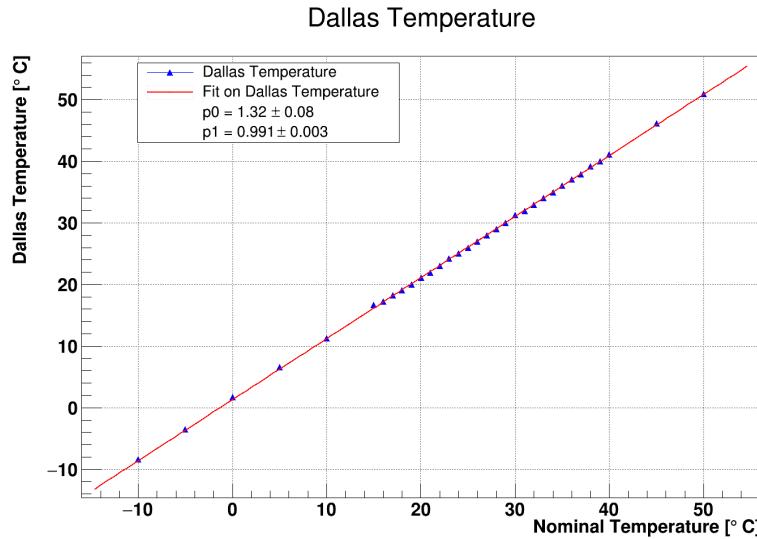


Figure 6.5: Dallas readout temperature value as a function of climatic chamber nominal temperature

The last results for the Dallas temperature measurement is reported in figure 6.5, and shows the temperature acquired between -10°C and 50°C , every 5°C and in the range between 15°C and 40°C every 1°C . The average of the Dallas sensor presents a linear behaviour with respect to temperature, with an angular coefficient of about 0.991 ± 0.003 and an offset of $(1.32 \pm 0.08)^{\circ}\text{C}$, this implies that the HIC works at about 1°C over the nominal temperature.

6.3 Threshold as a function of temperature

The study of the ALPIDE performance as a function of temperature was done by repeating the threshold scan at different temperature values (for a detailed explanation of the threshold scan, see section 5.2). A measure of the temperature using the Dallas sensor and the sensor inside the ALPIDE was done before and after the threshold scan at each temperature.

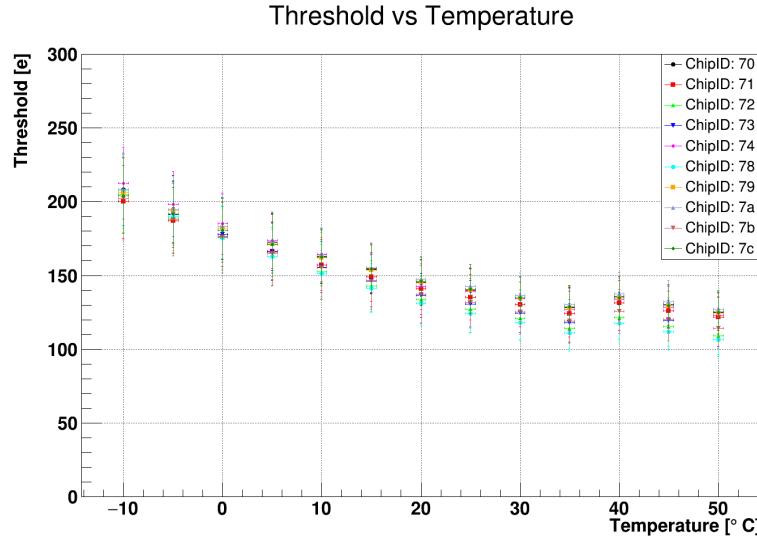


Figure 6.6: Graph of chip threshold as function of temperature for the STAVE 016 (silver chips), after the threshold tuning procedure at $V_{bb} = 0$ V

The temperature study was performed after the threshold tuning procedure that allowed to find the parameters to obtain a threshold of $150e^-$ at room temperature. For each chip, the threshold distribution at a fixed temperature was obtained and by a fit with a Gaussian function, the average threshold of the sensor was calculated. The ten chip thresholds are then plotted as a function of the temperature set on the climatic chamber (see figure 6.6).

The error bars on the threshold values represent the standard deviation of the normal distribution of the threshold of the chip pixels.

At a fixed temperature it is possible to see that the threshold tuning gave the expected result as the ten chips have an average threshold that is compatible within errors. The threshold has a decreasing behavior with respect to temperature until about 30°C , where it stabilizes at $\sim 130e^-$. The threshold remains at every temperature between -10°C and 50°C , below $300e^-$, which is the expected charge release per pixel of a Minimum Ionizing Particle (MIP), granting a good performance of the ALPIDE sensor.

The range investigated has a width of about 60°C and the threshold variation is about $60e^-$: the threshold variation as function of temperature is about $1^\circ/\text{e}^-$, that indicates a weak dependence of the threshold on temperature. Moreover, it allows not to punctually calibrate the threshold along the HEPD-02 tracker because the temperature gradient along the staves is about 6°C and the threshold variation with temperature is lower than the standard deviation of every chip pixel threshold, which is about $20e^-$.

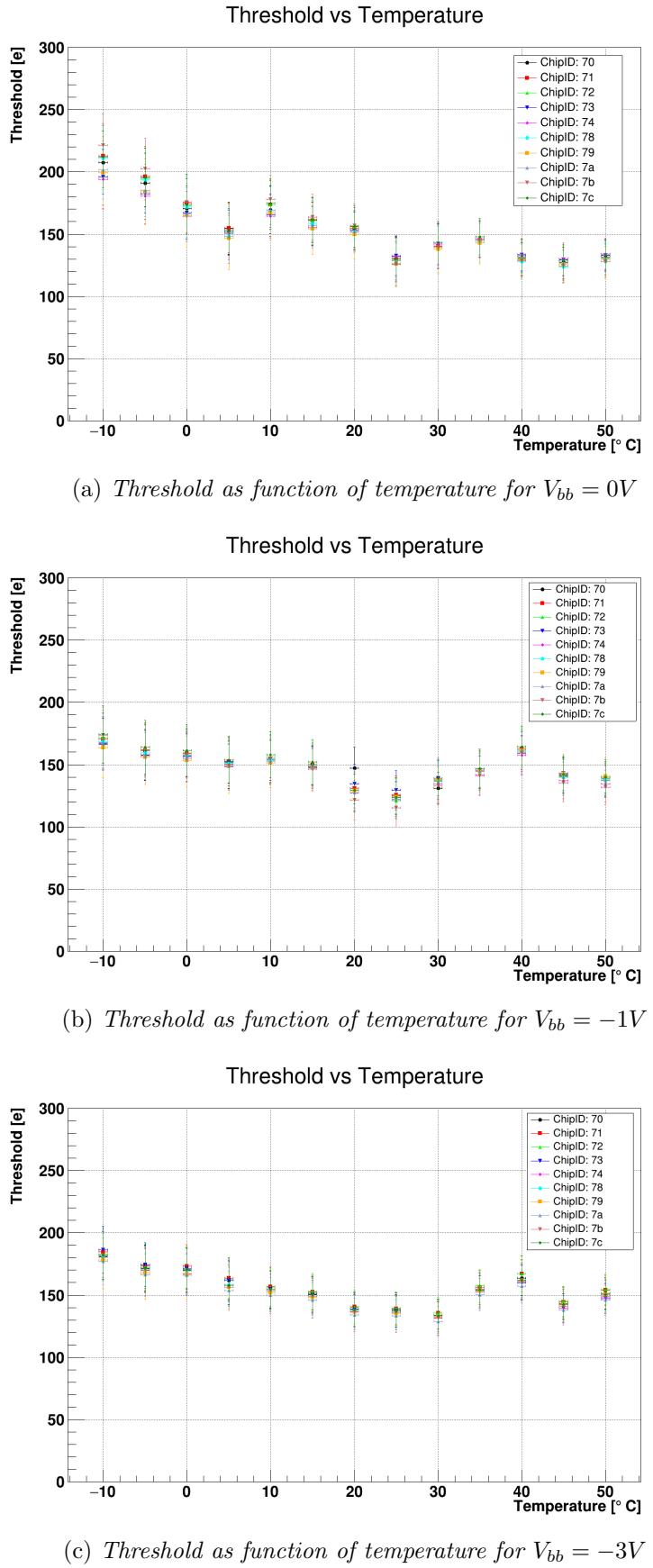


Figure 6.7: Threshold as function of temperature for HIC 033 at different back bias voltages

The graph presented in figure 6.6, is produced using the data acquired on a stave. The same measurements were done on a HIC, see figure 6.7, for which a reverse bias tension was also applicable. When changing reverse bias, the threshold dependence on the temperature is reduced, and the ALPIDE performance becomes even less influenced by the operating temperature.

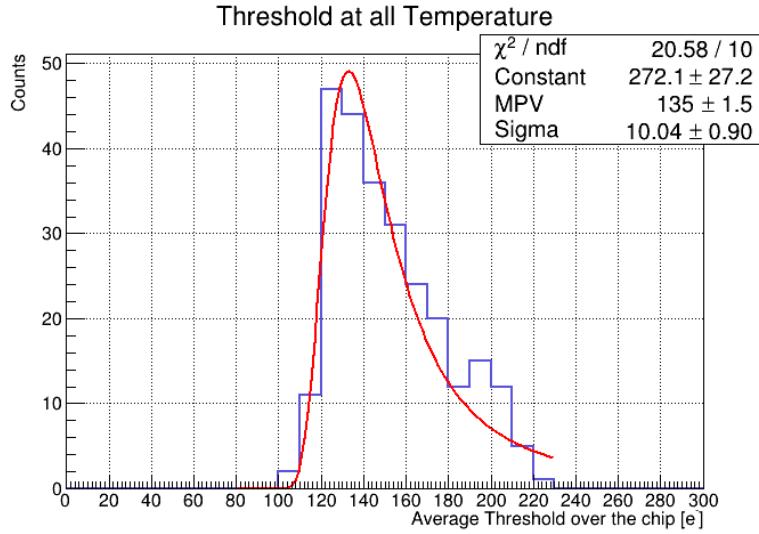


Figure 6.8: Threshold distribution at different temperature condition for ten chip and the threshold tuning for $150e^-$ at room temperature and $V_{bb} = 0V$

The threshold of each chip acquired at $V_{bb} = 0V$, with threshold tuning for $150e^-$ at room temperature, are plotted in figure 6.8: it is possible to see that the distribution is a landau with average value at $(135 \pm 2)e^-$ and root mean square equal to $(10.0 \pm 1)e^-$, which is far less than the threshold distribution sigma, about $20e^-$. It is possible to conclude that a not significant variation in the ALPIDE performance is visible.

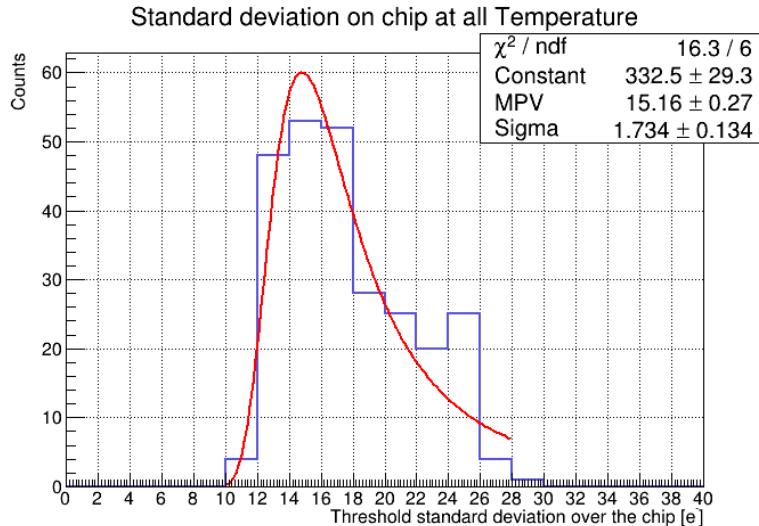


Figure 6.9: Standard deviation distribution at different temperature condition for ten chip and the threshold tuning for $150e^-$ at room temperature and $V_{bb} = 0V$

The same was done for the standard deviation of each chip threshold, leading to the result presented in figure 6.9. The threshold spread is always between $10e^-$ and $30e^-$, with a average of about $15e^-$ that is consistent with the one obtained for a single chip measurement.

The threshold study allowed us to conclude that no different behavior is observed at different temperature and that the ALPIDE performance is not strongly affected by a different temperature condition between -10° and 50°C . In particular no critical behaviour is observed for temperature close to 50°C .

6.4 Noise as a function of temperature

Another interesting study is the behavior of the noise as a function of temperature, see figure 6.10: the noise of each chip is calculated from the noise distribution of all pixel taking the average values. The error is the standard deviation of the noise distribution, which is about $1.5e^-$ for each chip.

The noise has a slow increasing trend as function of temperature, that leads to an increase of about $1e^-$ for the whole range. This is expected since electronic noise strongly depends on sensor temperature.

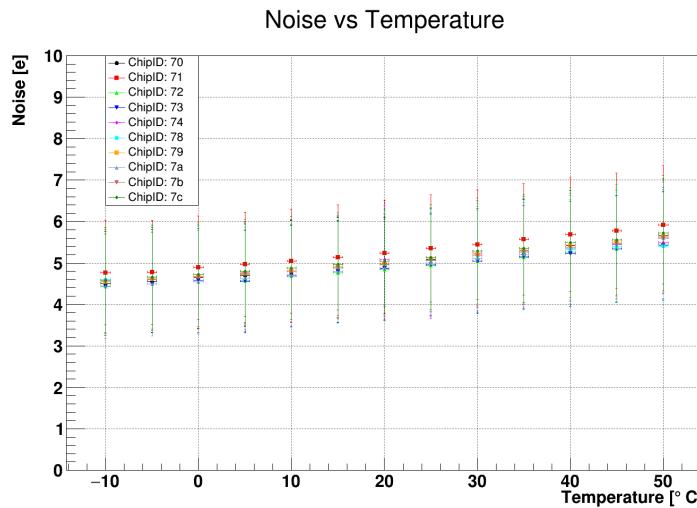


Figure 6.10: Graph of chip noise as function of temperature for the STAVE 016 (silver chip), after the threshold tuning procedure at $V_{bb} = 0 \text{ V}$

The same graph can be obtained for different reverse bias voltages and it is shown in figure 6.11; varying reverse bias, and with the same temperature conditions a diminishing of the noise is expected, because higher values of reverse bias lower the collection time. Another effect to notice, is the fact that the gradient of the noise with respect to temperature is lower when applying a reverse bias voltage.

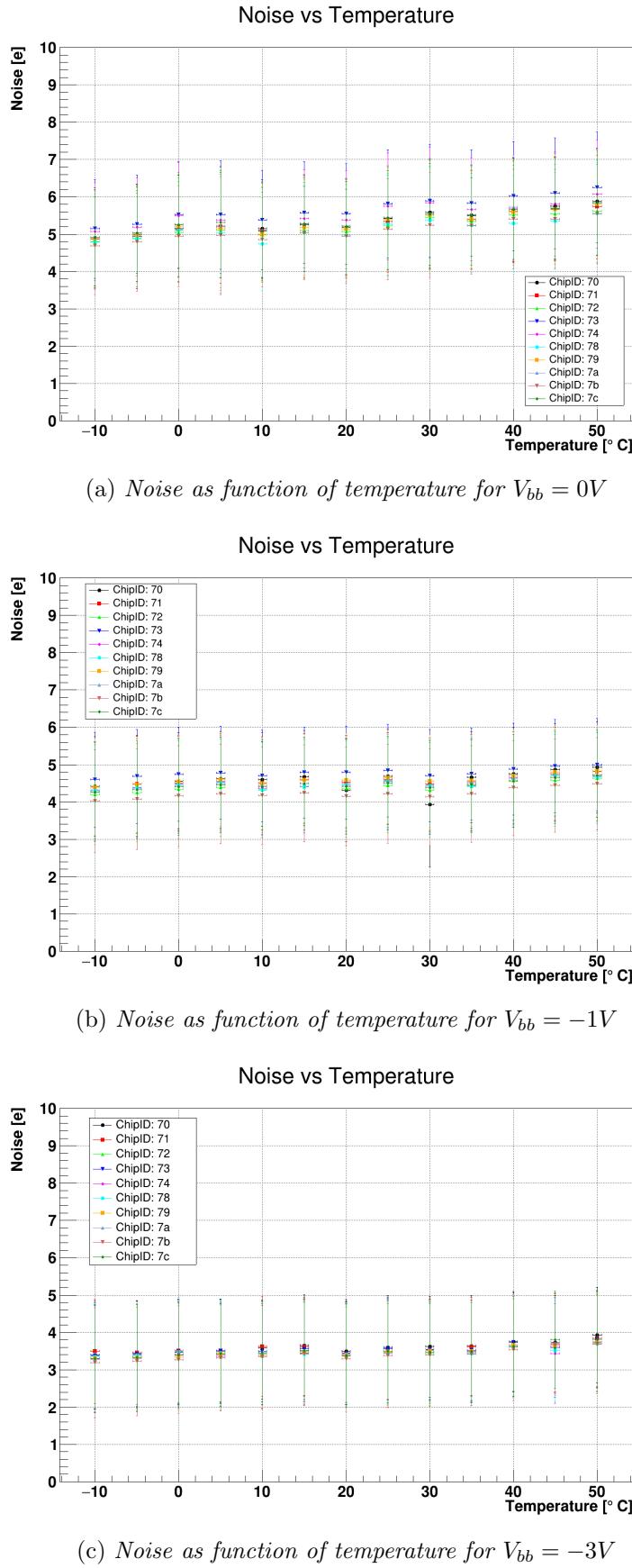


Figure 6.11: Noise as function of temperature for HIC 033 at different back bias voltages

6.5 ALPIDE temperature sensor calibration

The use of the Dallas sensor measurement allows us to complete the calibration of the ALPIDE internal temperature sensor. To achieve a stable calibration we need to take into account the ADC output values dependence on the supply voltage. In figure 6.12, the trend of the ADC readout values are plotted as a function of the power supply voltage, keeping the temperature fixed at 50 °C. A linear dependence between the two quantities can be observed, and this relation can be used to extrapolate a calibration as function of the voltage that powers each ALPIDE sensor.

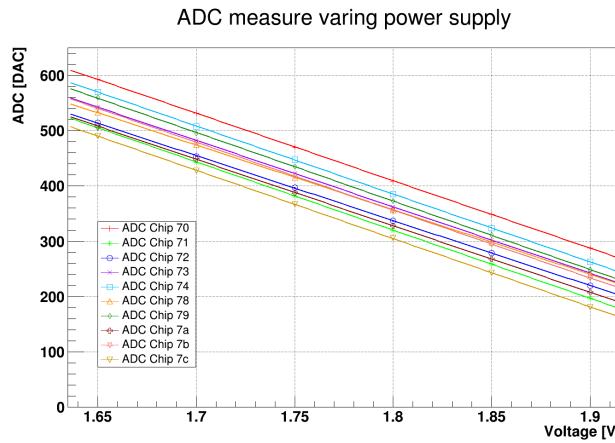


Figure 6.12: Dependence of ADC measured values on the power supply voltage at a temperature of 50 °C

By acquiring Dallas and ADC data at different temperatures, the absolute calibration is possible. In figure 6.13, the ADC trend versus the Dallas readout temperature is shown. It can be observed that the relation between the two quantities is linear, thus allowing an easy calibration of the temperature sensor. It can also be noticed that each ALPIDE has a different calibration curve, this can be due to the implantation process on different regions on the wafer, which can cause a slight difference in the ADC readout values without any effective change of the chip performance.

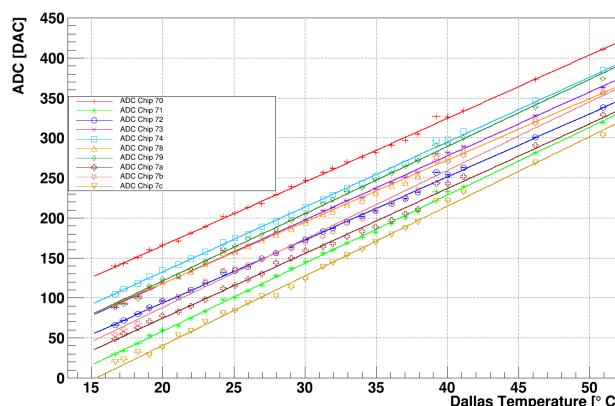


Figure 6.13: ADC temperature calibration as a function of Dallas temperature

Chapter 7

Future Developments of MAPS

The ALICE collaboration is developing a new sensor for the High Luminosity Large Hadron Collider (HL-LHC) project. The long term intent is to achieve the removal of the mechanical support and the ancillary electric flex circuits in the sensitive area to achieve the construction of a tracker where particles cross only the silicon sensor. This will lead to a material budget crossed by particles as low as $0.05\% X_0$.

The removal of all the mechanics from the particle trajectories can be achieved by exploiting the natural flexibility of thin silicon, which can be bent to form cylindrical shaped layers. This implies the production of a very large sensor that must cover at least half tracker length, and the use of very light carbon foam support to hold the layers in place.

To build large area sensors, a process named "stitching" used in commercial CMOS imaging technology is exploited.

Another issue is the production yield: will the performance be uniform on large area sensors? The TowerJazz 65 nm imaging process was chosen. It allows the production of large area stitched sensors with small size of the pixels (down to 10 micrometers) allowing an increase of the spatial resolution.

The many innovations presented by the system require a deep investigation on the best sensor and front-end electronics design.

The ALICE collaboration has just started the characterization phase of sensors prototypes, each one devoted to the optimization of a specific aspect of the final detector.

The test structures are divided in analogue or digital response of the pixels. The ALICE group in Turin is testing the Analogue Pixel Test Structure (APTS) with a front-end electronics devoted to the study of the signal timing response. In particular, the sensor under study has an Operational Amplifier (OA) as last stage of the pixel front-end circuits.

The sensor prototypes were produced on four different wafers that have various dopant density, and on each wafer, various sensor designs with different front end electronics have been implemented.

In this chapter, only the preliminary results concerning the test structure similar to the ALPIDE in terms of design and doping are discussed.

7.1 Set-up

The OA prototype is a matrix of 4×4 pixels each one with a pitch of 10 μm and a sensor thickness of 50 μm , with an epitaxial layer of about 25 μm .

The total size of the sensor is 1.5×1.5 mm. A specific board (carrier board) was designed to hold the chip and allow the connection to the readout and control systems. Another board (Proximity board) was designed to couple the APTS board with the Data Acquisition Board (DAQ) designed originally to test the ALPIDE sensor.

The full test set-up, shown in figure 7.1, is composed of the DAQ board, the proximity board and the carrier board, an oscilloscope Teledyne LeCroy WaveMaster 813Zi-B is used to read the signals and a Rohde & Schwartz HMP4030 power supply is used to power the DAQ board.

The power supply gives 5 V to the DAQ board, and voltage regulators, on the proximity board, are used to distribute the 1.2 V voltage to power up the APTS sensor.

The system is then connected to a computer that is used to control the boards. The test set-up, hardware and software, was developed by the Cagliari ALICE group.

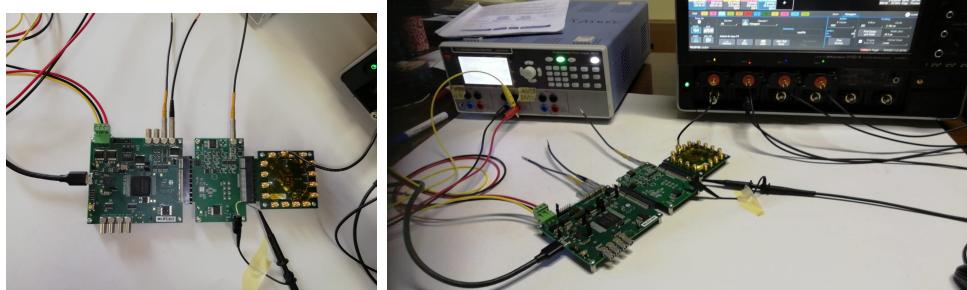


Figure 7.1: On the left: the DAQ, proximity and carrier board used for testing the sensor and on the right the power supply and the oscilloscope used during testing

Each carrier board has an APTS sensor glued on the top, right in the middle of the board. The APTS sensor is glued to the carrier board, and then the sensor pads are wire bonded to the pads on the board, as can be seen in figure 7.2.

The gold square with some holes, on the carrier board, is the heat dissipation system, it was added to avoid reaching too high temperatures on the chip.

The pixels are placed in the center of the chip while the surrounding area is occupied by the power meshes and other structures to read out the signals.

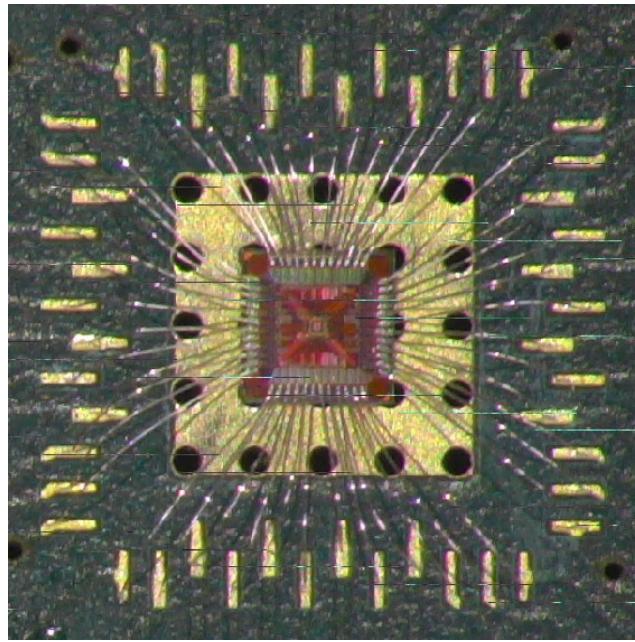


Figure 7.2: APTS sensor glued and bonded to the APTS board

Every pixel is read thanks to an SMA (SubMiniature version A) connector soldered to the carrier board. The SMA coaxial cable allows to acquire high frequency signals avoiding distortions: this, and the high performance of the oscilloscope (13 GHz - 4×40 GS/s) allow us to study the time response of the sensor, that is the main goal for the APTS-OA structures.

7.2 Parameters

The in-pixel front-end electronics has several parameters that determine the proper working condition of the circuit, all of them set by a register on the proximity board. A Digital to Analogue Converter (DAC) is used to transform the set parameter in a tension or a current which is then supplied to the APTS. The typical parameters values are reported in table 7.1.

Parameter	Typical value
IbiasP	80 μ A
IbiasN	-800 μ A
Ireset	1 μ A
Vreset	200 mV
Ibias3	800 μ A
Ibias4	2.5 mA
VcasP	300 mV
VcasN	750 mV

Table 7.1: In-pixel front-end typical parameters used for the APTS characterization

Like for the ALPIDE, it is possible to test the front-end electronics by injecting charge through a capacitor of 242 aF, thus simulating a signal generated by charge collection in the active area. The voltage used to charge the capacitor determine the number of equivalent electrons injected and its value is determined by a parameter called VH.

Moreover it is possible to separately apply a reverse bias voltage both to the sensor substrate (PSUB) and to the transistor p-well (PW).

Furthermore, there are two bits that can determine which pixels receive the VH voltage on the matrix; these two pads are SEL_0 and SEL_1, and they can only assume a binary value.

In figure 7.3, the pads that connect the sensor to the carrier board are shown. Each pad corresponds to a parameter, a voltage or an output signal of the pixels, and by setting the proper voltage or current values for each parameter, the correct configuration of the test structure is obtained.

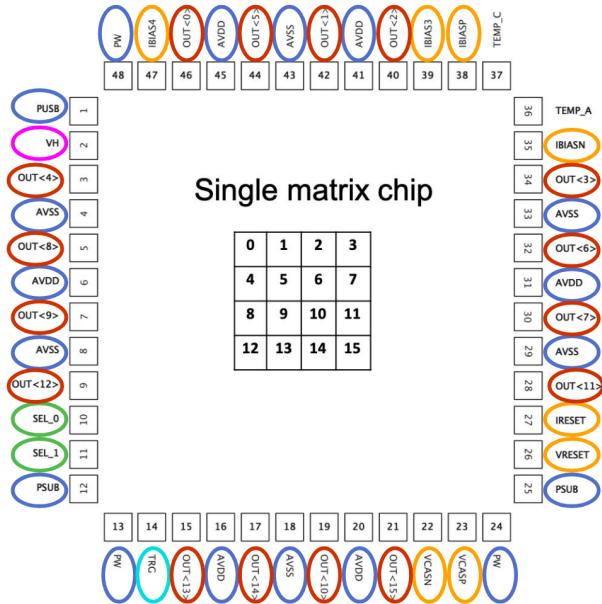


Figure 7.3: Matrix with the pads that are then bonded to the carrier board: the parameters in blue, are the polarising tensions given to the sensor while in red the pads where each pixel signal is collected. In yellow the front-end parameters are highlighted and the VH parameter is the pink one. SEL_0 and SEL_1 are the green one while the trigger coming from the proximity is the cyan one.

7.3 Preliminary results

All the relevant parameters defining a signal were studied:

- the Baseline: voltage level that must be high enough to allow having a positive voltage value even if the signal is negative.
 - the Amplitude: difference between the baseline and the minimum voltage reached by the signal.
 - the Fall time: time difference between the 10% and the 90% of the signal amplitude.
 - the channel to channel Jitter: standard deviation of the time difference, at half height, of the signals obtained by two different pixels.

The Baseline, Amplitude, Fall Time are shown, for a typical signal, in figure 74

In order to minimise the noise contribution, all the measurements are taken as the average value on a distribution of 500 events.

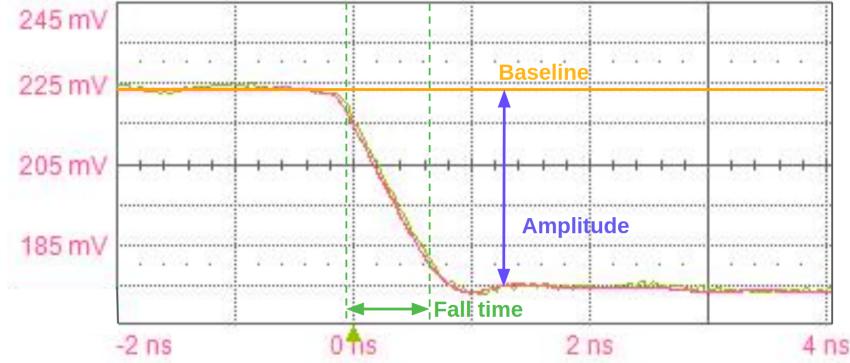


Figure 7.4: Baseline, amplitude and fall time definition on a sample signal

7.3.1 Jitter measurements

The jitter between the pixel signal and the trigger given by the proximity was also studied. The main problem in this measure was that the trigger signal fluctuates a lot, making it impossible to get a clean measurement of the jitter. The jitter between two pixel output signals was also measured, and the results of the jitter as function of the VH voltage value, i.e. various input signal amplitudes, are shown in figure 7.5.

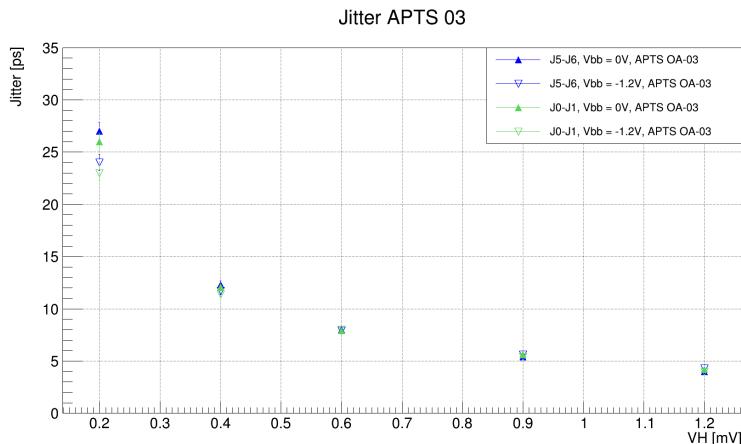


Figure 7.5: Jitter measure between two pixels output signals as function of the VH parameter that is related to the number of injected equivalent electrons

A jitter as low as 5 ps can be obtained with a high VH values. When decreasing the VH parameter, an increase of the jitter measure is seen. This can be due to the fact that the signal has a lot of fluctuation and the lower the number of injected electrons, the more the signal varies and affects the measurement results. We also observed that, as expected, the jitter does not change when applying a reverse bias voltage to the sensor.

7.3.2 Parameter optimization

To optimise the chip configuration, a set of measurements varying each parameter at a time was carried on. At first the Vreset parameter was varied. Vreset fixes the baseline level: in figure 7.6, the trend of amplitude, baseline and fall time as a function of Vreset is plotted.

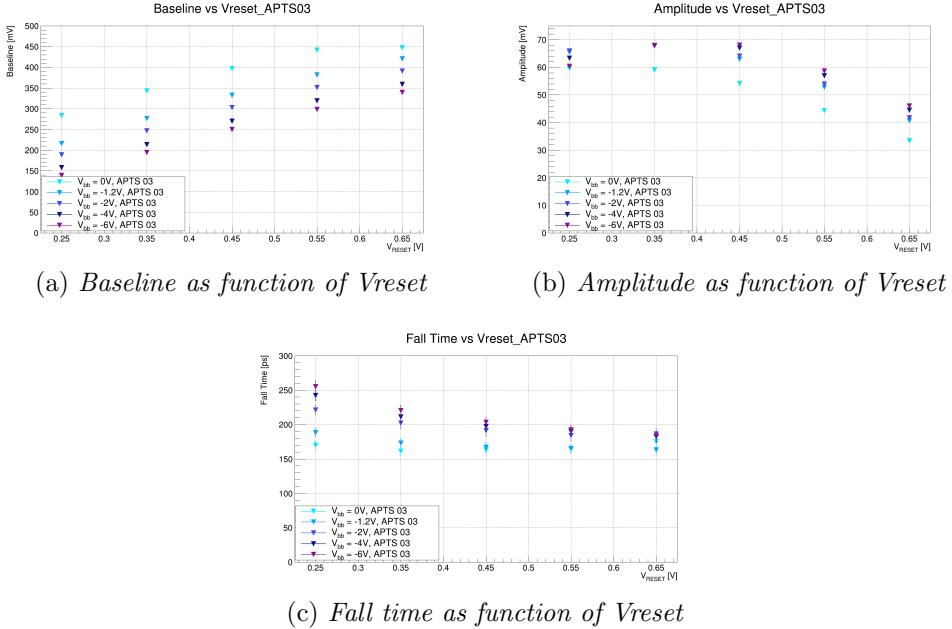


Figure 7.6: Baseline, amplitude and fall time as function of Vreset, on the same graph different back bias voltages are shown.

As shown in figure 7.6, the baseline increases when increasing Vreset but it saturates when a value of ~ 450 mV is reached. When a reverse bias voltage is applied, the baseline decreases; since a high baseline is needed, in order not to have a saturation in the output signal, which is a negative one, the Vreset must be carefully tuned for each reverse bias voltage.

On the other hand, the signal amplitude reaches a maximum and then decreases as function of Vreset. An important thing to notice is that after the maximum, the amplitude trend as function of back bias is inverted: for Vreset lower than 0.3 V the amplitude decreases as function of back bias voltage while when Vreset is greater than 0.3 V, the amplitude increases as function of back bias voltage. However, it is important to have the highest possible signal amplitude, in order to be able to detect also small signals.

The other parameter is the signal fall time: the graph in figure 7.6, shows that when Vreset increases, a decrease of the fall time and a more uniform time response as function of back bias is obtained. Though an increase of Vreset could improve the time response, the main drawback is a worsening of the amplitude response.

The value chosen as a compromise is Vreset = 0.35 V.

Nonetheless, when a high Vreset voltage is set, the circuit performance can be degraded by having one or more transistors too close to the cut off or to the saturation region. For this reason, other two parameters must be carefully tuned: IbiasN and IbiasP.

The first one to be optimized was the IbiasN parameter: figure 7.7 shows the baseline, amplitude and fall time as function of the reverse bias voltage, for different values of the IbiasN parameter. In the graphs, the IbiasP parameter was set to 40 μ A.

The baseline increases when a low value of IbiasN is set: to obtain a baseline

of about 300 mV at back bias voltage equal to 0 V, a IbiasN value of 300 μ A is chosen. This value allows to have an increase of the amplitude when applying a reverse bias voltage and to keep unchanged the time response of the circuit.

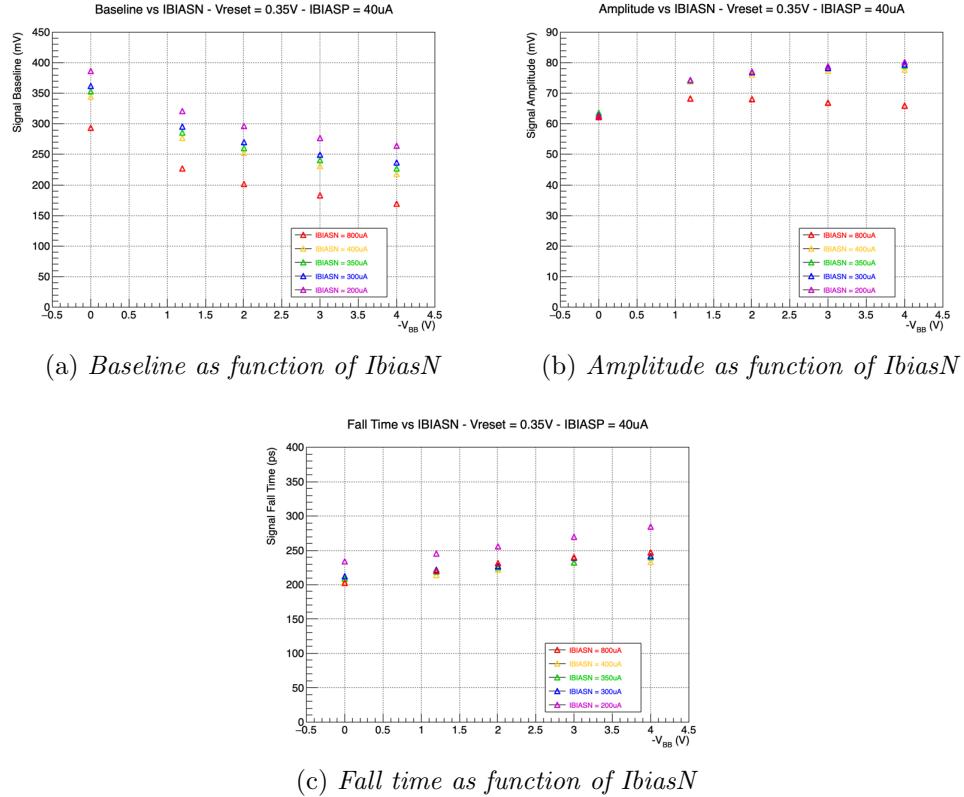


Figure 7.7: Baseline, amplitude and fall time as function of IbiasN keeping $V_{reset} = 0.35$ V and $IbiasP = 40 \mu$ A, on the same graph different back bias voltages are shown.

The other parameter to be optimized is IbiasP: the results are plotted in figure 7.8, as a function of back bias voltage and superimposing different values of IbiasP. The trends of different values for a fixed value of IbiasN equal to 400 μ A are shown.

The baseline decreases when diminishing IbiasP, for this reason it is important not to set a value too low to avoid problems with high signals. However, higher signal amplitudes are possible when decreasing IbiasP, causing on the other hand a slight worsening in the time response. To keep the time response unchanged, but still have a small improvement in the signal amplitude, the proper IbiasP value was chosen equal to 40 μ A.

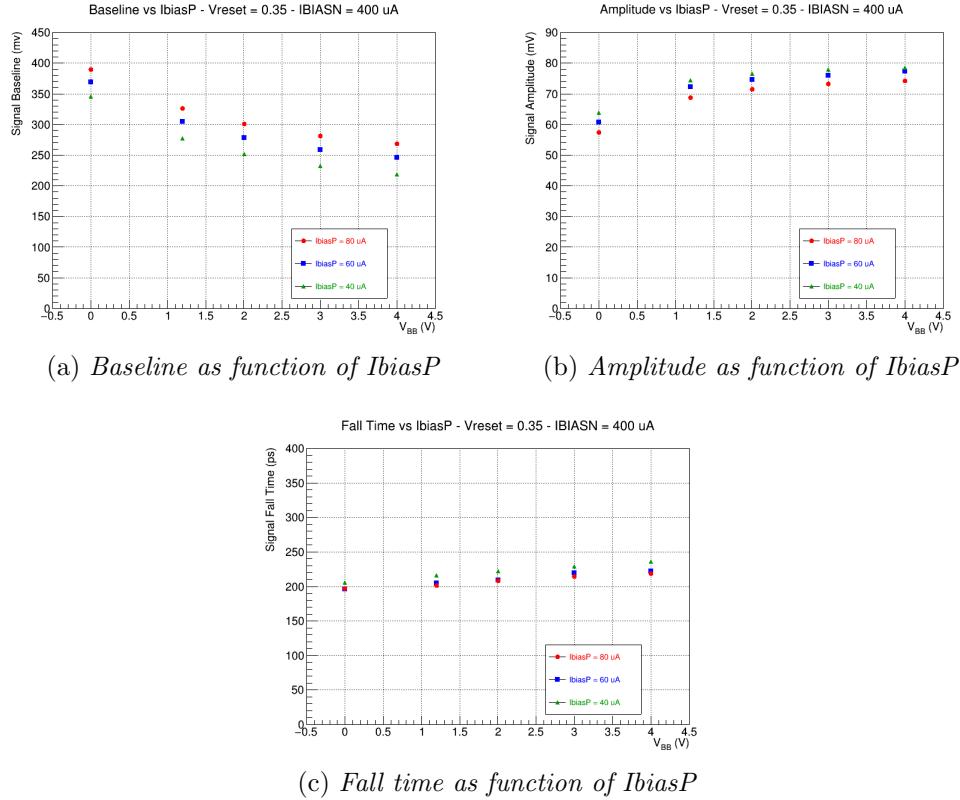


Figure 7.8: Baseline, amplitude and fall time as function of IbiasP keeping Vreset = 0.35 V and IbiasN = 400 μ A, on the same graph different back bias voltages are shown.

In the end, the parameter chosen for the proper working of the circuit are Vreset = 0.35 V, IbiasN = 300 μ A and IbiasP = 40 μ A, also reported in table 7.2.

Parameter	Typical value	Set Value
IbiasP	80 μ A	40 μ A
IbiasN	-800 μ A	300 μ A
Ireset	1 μ A	1 μ A
Vreset	200 mV	350 mV
Ibias3	800 μ A	800 μ A
Ibias4	2.5 mA	2.5 mA
VcasP	300 mV	300 mV
VcasN	750 mV	750 mV

Table 7.2: In-pixel front-end parameters used for the APTS characterization

7.3.3 Reverse bias current

To verify that the chip was correctly working even for higher values of the reverse bias the current as function of the reverse bias voltage applied was measured: a Semiconductor Parameter Analyzer HP 4145B was used; the contribution of the substrate and the pwell currents were measured separately: the results are reported in figure 7.9.

One important observation is that the absolute value of the sum of the currents is always lower than 100 nA, well below the limits. From figure 7.9, it is possible to see that the substrate current is always negative and increases when increasing the reverse bias voltage. On the other hand, the p-well current is positive for $V_{bb} = 0$ V and then decreases until it becomes negative. The total contribution starts at 0 nA for $V_{bb} = 0$ V and then decreases giving a negative current when increasing the reverse bias voltage.

The reason for this behaviour is not understood yet and it is under investigation by the chip designers.

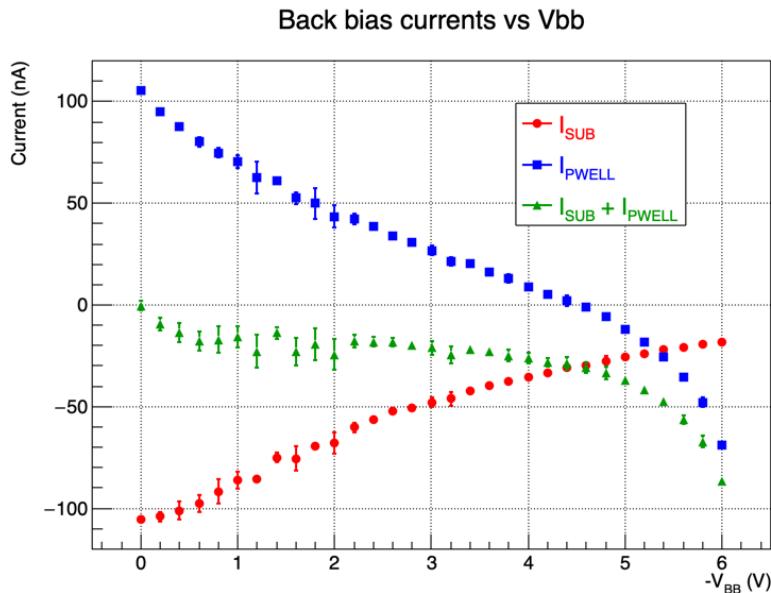


Figure 7.9: Back bias current as function of back bias applied voltage

7.3.4 Future steps of the characterization process

The characterization of different sensor design exploiting X-ray photons from a ^{55}Fe source to generate physical signals is also foreseen. This will allow us to study the cluster size, the fall time and the signal amplitude for the charge collected in the sensor.

Conclusion

In conclusion, this thesis is focused on two main topics: the definition of an assembly and quality assurance procedure for the modules that will constitute the HEPD-02 tracker and on topical study of the ALPIDE performance as a function of temperature.

The first stages for the Qualification Model of the HEPD-02 tracker have been successfully built and the production is currently ongoing to complete the tracker before the end of June 2022, to be ready for the satellite launch in the first half of 2023.

After the assembly of the tracker, the threshold equalization will be carried out using the parameters selected in section 5.3. Several tests, i.e. vibrational and thermal tests, are scheduled to verify the tracker and the whole detector compliance with the requirements of the Chinese Space Agency while beam tests will be performed to study the HEPD-02 response to physical signals.

The ALPIDE temperature performance study was carried out, proving that the sensor behavior is not degraded in the temperature range between -10°C and 50°C . Besides, also the calibration of the ALPIDE in-chip temperature sensor was performed as a function of temperature and power supply giving a linear result in both cases.

Thanks to this study, the ALPIDE has proved once more to be a robust detector that can be operated in very different condition without losing the quality of its performance.

In the meanwhile, research is ongoing to develop a sensor which could exceed the ALPIDE performance granting a higher radiation hardness, an improved spatial resolution and a lower power consumption which is one of the main limits in the use of the ALPIDE in different fields of application. Moreover, the technological improvements could allow the production of detectors with larger area that allow simpler assembly procedures and a substantial reduction of material budget.

List of Figures

1.1	Example of the schematic of a silicon strip detector [2]	12
1.2	On the left: schematic section of a hybrid pixel sensor. On the right: schematic section of a monolithic active pixel detector [13].	14
1.3	Structure of Monolithic Active Pixel Detectors (MAPS), example of the MIMOSA sensor [16]	15
1.4	MAPS depletion region simulation in the case of reverse bias voltage -1 V (on the left) and -6 V (on the right) with a epitaxial layer doping of $1 \times 10^{13}\text{ cm}^{-3}$, and collecting diode dimensions of $3\text{ }\mu\text{m} \times 3\text{ }\mu\text{m}$. The colour code shows the logarithm of the electrical field. [10]	16
1.5	On the left: schematic view of MIMOSA-26 chip [21]. On the right: rolling shutter readout mode [10]	18
1.6	Vertical section of the ALPIDE sensor realized in the 180 nm TowerJazz CMOS imaging process [10].	19
1.7	MIMOSA readout mode [10] (On the left) compared to MIS-TRAL double-row rolling shutter readout [13] (On the right)	20
1.8	ALPIDE readout schematic using the priority encoder mode (on the left) [30]; on the right, microscope view, it is possible to see the collecting diode as octagons inside the green square [32]	21
2.1	Schematic of the HEPD-02 detector. The veto system is not represented in the figure [15]	24
2.2	HEPD-02 tracker structure: master-slave and turrets arrangement are sketched [15]	25
2.3	Thermal dissipation of a single turret during detector operation [15]	26
3.1	Block diagram of the ALPIDE pixel [30].	30
3.2	ALPIDE block diagram [30].	31
3.3	Analogue front-end in-pixel circuitry schematic [30].	32
4.1	HEPD-02 tracker: assembly schematic [37]	34
4.2	CMM reference frame for the ALPIDE alignment	35
4.3	On the left: operator positioning the chip in the correct position. On the right: alignment marker on the ALPIDE back side	36
4.4	FPC kept with the module gripper, covered by the mask and the glue	37
4.5	Tab and wing cut operation	38
4.6	CMM reference frame for the stave assembly	39

4.7	On the left: mask for gluing the ALPIDE on the mechanical support. On the right: glue distribution thanks to a spatula.	40
4.8	Wire soldering on the FPC pads: the stave can now be connected to the final powering and readout system	40
5.1	Set up used for qualification tests: the HIC is powered by a power supply and connected to an FPGA that sends the readout commands from the computer to the device under test (DUT)	42
5.2	Thermal camera photo in the clock on condition	44
5.3	Address of the chips located in their positions along the FPC	44
5.4	Digital scan output for a chip	45
5.5	Map of the ALPIDE with the pixel threshold on the z axis	46
5.6	Map of the ALPIDE with the pixel noise on the z axis	46
5.7	Back bias curve for a HIC, to which back bias is applicable	47
5.8	On the left: threshold cumulative distribution on a chip, on the right: noise cumulative distribution on a chip, both distribution are obtained with $\text{VCASN} = 50$ and $\text{ITHR} = 50$	47
5.9	Average threshold for different parameter configurations at $V_{bb} = 0\text{V}$	48
5.10	Threshold tuning results for HIC 033 when applying a back bias voltage	49
6.1	Climatic chamber setup: the hygrometer (red circle) and the dry air system (yellow circle) are highlighted	52
6.2	Dallas sensor on the FPC with the corresponding position name	53
6.3	Dallas temperature as function of time in a ramp from room temperature to 30°C : clock off operating condition (on the left) and clock on (on the right)	53
6.4	On the left: comparison between thermometer, Dallas and climatic chamber temperature values in a ramp from room temperature to 30°C . On the right: comparison between Dallas temperature before and after a threshold scan performed at 50°C	54
6.5	Dallas readout temperature value as a function of climatic chamber nominal temperature	55
6.6	Graph of chip threshold as function of temperature for the STAVE 016 (silver chips), after the threshold tuning procedure at $V_{bb} = 0\text{V}$	56
6.7	Threshold as function of temperature for HIC 033 at different back bias voltages	57
6.8	Threshold distribution at different temperature condition for ten chip and the threshold tuning for $150e^-$ at room temperature and $V_{bb} = 0\text{V}$	58
6.9	Standard deviation distribution at different temperature condition for ten chip and the threshold tuning for $150e^-$ at room temperature and $V_{bb} = 0\text{V}$	58
6.10	Graph of chip noise as function of temperature for the STAVE 016 (silver chip), after the threshold tuning procedure at $V_{bb} = 0\text{V}$	59
6.11	Noise as function of temperature for HIC 033 at different back bias voltages	60

6.12 Dependence of ADC measured values on the power supply voltage at a temperature of 50 °C	61
6.13 ADC temperature calibration as a function of Dallas temperature	61
7.1 On the left: the DAQ, proximity and carrier board used for testing the sensor and on the right the power supply and the oscilloscope used during testing	65
7.2 APTS sensor glued and bonded to the APTS board	65
7.3 Matrix with the pads that are then bonded to the carrier board: the parameters in blue, are the polarising tensions given to the sensor while in red the pads where each pixel signal is collected. In yellow the front-end parameters are highlighted and the VH parameter is the pink one. SEL_0 and SEL_1 are the green one while the trigger coming from the proximity is the cyan one.	67
7.4 Baseline, amplitude and fall time definition on a sample signal	68
7.5 Jitter measure between two pixels output signals as function of the VH parameter that is related to the number of injected equivalent electrons	68
7.6 Baseline, amplitude and fall time as function of Vreset, on the same graph different back bias voltages are shown.	69
7.7 Baseline, amplitude and fall time as function of IbiasN keeping Vreset = 0.35 V and IbiasP = 40 µA, on the same graph different back bias voltages are shown.	70
7.8 Baseline, amplitude and fall time as function of IbiasP keeping Vreset = 0.35 V and IbiasN = 400 µA, on the same graph different back bias voltages are shown.	71
7.9 Back bias current as function of back bias applied voltage	72

List of Tables

2.1	Comparison between HEPD-01 double sided silicon micro-strip and HEPD-02 MAPS sensor [15, 37]	26
5.1	Currents in idle and clock on for a sample: in the colored cells the reference current value is reported	44
5.2	Parameters values, in DAC units, for the threshold tuning on the final tracker	48
7.1	In-pixel front-end typical parameters used for the APTS char- acterization	66
7.2	In-pixel front-end parameters used for the APTS characterization	71

References

- [1] Colinge, J-P and Colinge, Cynthia A, *Physics of semiconductor devices*, 2005, Springer Science & Business Media.
- [2] Peisert, Anna, *Silicon microstrip detectors*, Instrumentation in High Energy Physics, 1-79, 1992, World Scientific.
- [3] , Bonvicini, V. et al., *The PAMELA experiment in space*, Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment, 461(1-3), 262-268, 2001, Elsevier.
- [4] Zuccon, P. et al., *The AMS silicon tracker: Construction and performance*, Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment, 596(1), 74-78, 2008, Elsevier.
- [5] Ackermann, M. et al., *The Fermi large area telescope on orbit: event classification, instrument response functions, and calibration*, The Astrophysical Journal Supplement Series, 203, 1-4, 2012, IOP Publishing.
- [6] Azzarello, P. et al., *The DAMPE silicon-tungsten tracker*, Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment, 831, 378-384, 2016, Elsevier.
- [7] Rossi, Leonardo and Fischer, Peter and Rohe, Tilman and Wermes, Norbert, *Pixel detectors: From fundamentals to applications*, 2006, Springer Science & Business Media.
- [8] Manzari, V. et al., *The silicon pixel detector (SPD) for the ALICE experiment*, Journal of Physics G: Nuclear and Particle Physics, 30(8), S1091, 2004, IOP Publishing.
- [9] Turchetta, R. et al., *Monolithic active pixel sensors (MAPS) in a VLSI CMOS technology*, Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment, 501(1), 251-259, 2003, Elsevier.
- [10] Abelev, B., et al., *Technical design report for the upgrade of the ALICE inner tracking system*, Journal of Physics G: Nuclear and Particle Physics, 41(8), 087002, 2004, IOP Publishing Ltd.
- [11] Karimäki, V., *The CMS tracker system project: Technical Design Report*, 1997, CMS-TDR-005.

- [12] Aad, G. et al., *ATLAS pixel detector electronics and sensors*, Journal of Instrumentation, 3(07), P07007, 2008, IOP Publishing.
- [13] Hoorne, Jacobus Willem, *Study and development of a novel silicon pixel detector for the upgrade of the ALICE Inner Tracking system*, PhD thesis, 2015, Wien.
- [14] Di Mauro, A. and Alice Collaboration et al., *The new inner tracking system for the ALICE upgrade at the LHC*, Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment, 936, 625-629, 2019, Elsevier.
- [15] Ricci, Ester *The passage from microstrip to pixel silicon detectors for tracking particles in space*, PhD thesis, Trento University, 2020.
- [16] Winter, Marc *Achievements of the first generation of monolithic active pixel sensors for charged particle tracking*, PoS, 264, 2001.
- [17] de Cilladi, Lorenzo *Characterization of Monolithic Pixel Detectors for the ALICE Inner Tracking System*, Master Thesis, Torino University, 2019.
- [18] Fossum, Eric R., *CMOS image sensors: Electronic camera-on-a-chip*, IEEE transactions on electron devices, 44(10), 1689-1698, 1997, IEEE.
- [19] Haas, Daniel, *The EUDET high resolution pixel telescope-towards the final telescope*, 2008 IEEE Nuclear Science Symposium Conference Record, 3292-3297, 2008, IEEE.
- [20] Dorokhov, A. et al., *High resistivity CMOS pixel sensors and their application to the STAR PXL detector*, Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment, 650(1), 174-177, 2011, Elsevier.
- [21] Baudot, J. et al., *First test results of MIMOSA-26, a fast CMOS sensor with integrated zero suppression and digitized output*, 2009 IEEE Nuclear Science Symposium Conference Record (NSS/MIC), 1169-1173, 2009, IEEE.
- [22] Hu-Guo, Ch, et al., *First reticule size MAPS with digital output and integrated zero suppression for the EUDET-JRA1 beam telescope*, Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment, 623(1), 480-482, 2010, Elsevier.
- [23] Greiner, L. et al., *A MAPS based vertex detector for the STAR experiment at RHIC*, Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment, 650(1), 68-72, 2011, Elsevier.
- [24] Contin, G. et al., *The STAR MAPS-based PiXeL detector*, Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment, 907, 60-80, 2018, Elsevier.

- [25] Van Hoorne, J. W. *The upgrade of the ALICE inner tracking system-status of the R&D; on monolithic silicon pixel sensors*, PoS, 125, 2014, SISSA.
- [26] Hillemanns, H. et al., *Radiation hardness and detector performance of new 180nm CMOS MAPS prototype test structures developed for the upgrade of the ALICE Inner Tracking System*, 2013 IEEE Nuclear Science Symposium and Medical Imaging Conference (2013 NSS/MIC), 1-5, 2013.
- [27] Coath, Rebecca et al., *Advanced pixel architectures for scientific image sensors*, Proc. Topical Workshop Electronics for Particle Physics, 57-61, 2009.
- [28] Ravasenga, I., *The upgrade of the Inner Tracking System of the ALICE experiment*, Il nuovo cimento C, 41(1-2), 1-3, 2018, Societá italiana di fisica
- [29] Besson, A. et al., *From vertex detectors to inner trackers with CMOS pixel sensors*, Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment, 845, 33-37, 2017, Elsevier.
- [30] ITS ALICE, *ALPIDE-3 operations manual*, 2016.
- [31] Yang, P. et al., *Low-power priority Address-Encoder and Reset-Decoder data-driven readout for Monolithic Active Pixel Sensors for tracker system*, Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment, 785, 61-69, 2015, Elsevier.
- [32] Šuljić, Miljenko, *Study of Monolithic Active Pixel Sensors for the Upgrade of the ALICE Inner Tracking System*, PhD thesis, University of Trieste, 2017.
- [33] Musa, Luciano *Letter of Intent for an ALICE ITS Upgrade in LS3*, 2019.
- [34] Ambrosi, G., et al., *The HEPD particle detector of the CSES satellite mission for investigating seismo-associated perturbations of the Van Allen belts*, Science China Technological Sciences, 61(5), 643-652, 2018, Springer.
- [35] Picozza, P., et al., *Scientific goals and in-orbit performance of the High-energy Particle Detector on board the CSES*, The Astrophysical Journal Supplement Series, 243(1), 16, 2019, IOP Publishing.
- [36] Scotti, V., et al., *The high energy particle detector onboard CSES-02 satellite*, Proceedings of the 36th International Cosmic Ray Conference (ICRC), Madison, WI, USA, 24, 2019.
- [37] Iuppa, R., et al., *The innovative particle tracker for the HEPD space experiment onboard the CSES-02 satellite*, 37th ICRC Conference, 2021, Proceeding of Science.
- [38] Ricciarini, SB., et al., *Enabling low-power MAPS-based space trackers: a sparsified readout based on smart clock gating for the High Energy Particle Detector HEPD-02*, 37th ICRC Conference, 2021, Proceeding of Science.

Acknowledgements

The present thesis is the last work of a journey started in 2019, when I first enrolled in the master degree in Physics. First of all I'd like to thank all the professors met during these years, who despite the covid pandemic and the difficulties in making online lessons and exams, were always available and passed on the passion for their job. In particular, a heartfelt thanks goes to my supervisor prof.ssa Stefania Beolè, a precious guide during the entire thesis. Her attention, presence and precious advice were the light that guided me in the darkest times of my work.

My sincere thanks also to prof.ssa Elena Botta for her fundamental help during the long laboratory measurements and in the correction of the thesis presentation, your suggestions made me improve a lot.

My gratitude goes also to ing. Silvia Coli and Flori Dumitrache who explained me every step of the tracker assembly doing their jobs with great competence and passion, and who were always available for explanations and support during the work.

I am deeply thankful to Franco Benotto who offered his deep knowledge and his competence from my first day, his presence and the one of Chiara Ferrero, Matilde Dematteis, Andrea Turcato and Umberto Savino made the everyday work a lot easier and enjoyable.

I would like to extend my sincere thanks also to all the other people, professors and technicians with whom I collaborated during the thesis, and who always demonstrated a great competence and passion.

An enormous thanks to Francesco Nozzoli and prof. Roberto Iuppa that guided me in the choice continue my studies in another university, and with whom I worked during the master degree for the publication of the bachelor thesis results.

An heartfelt thanks goes also to my family, who supported me in every step of the way, always believing in me and being there to catch me during my darkest time. In particular to my mother Annachiara, my father Giancarlo, my sisters Matilde and Silvia who are a fundamental part of my life. A thank goes also to my grandparents Marco and Mariella who are always in my heart while I'm away from home and to my aunt Silvana who followed every step of my studies.

My infinite gratitude goes to my friends and roommates Paola, Chiara and Viola that made the past months unforgettable and fill my days with joy and

Acknowledgements

love. We will always remember our adventures with the infamous cockroach, the evening laughter, cooking together, and going to the balloon. I don't know what I would have done if I hadn't met you.

Thanks to my classmate Alessia, who was always there to reassure me during the lessons and exams difficulties, and who was a solid landmark in these two years. Our conversations at the phone and the few times we were able to study together are the things that helped me overcome the two pandemic years while changing the city where I was studying and adapting to the new university.

I would like to particularly thank Matteo Furci, my theoretical physicist friend, with whom I had the privilege to study during the pandemic time. Your help and support mean a lot to me. The time we spent walking, cooking or studying together with Jacopo, Matteo, Luca and Veronica is one of the most precious memories of my bachelor and master degree years.

Thanks to Silvia because since I met her, I am sure to have a fabulous friend by my side, you are one of the most important person in my life. You are the person who made me see the beauty of Torino and make me accept the change in my life. Your enthusiasm and wonder in front of everything that life presents you are for me a life example.

A special thanks to Ester, who is a wonderful friend and who helped me in one of the darkest period in my master degree, supporting me and hosting me in a very difficult moment. You are for me a great inspiration as scientist and as woman.

A unique thanks to Noemi and Ivana, life brought us together and despite the distance, Bologna, Bressanone, Trento and Torino, did not have any chance on our friendship. You are the amazing people that are my companion in this journey and with whom I deal with every obstacles life sends.

Thanks to Giulia, who is my favorite newbie (yes, I know that you are no longer a greenhorn), you are always there to accompany me in my life adventures and you are the one that motivates me to do my best and to reach for harder targets.

My gratitude goes to Viola and Mazzu, who are the best people to go hiking with, we never know what the next mountain will be and what challenges we will meet next.

An enormous thanks also to Eleonora and Marianna for being there for me and for being a great inspiration in my life.

A thanks to "I Regaz di via Sommarive" and to Chiara Vecchi who initiated me to the university life and played a really important role during my first bachelor years.

Finally, I would like to express my gratitude to all the people I met in these years that supported and accompanied me, in the studies and in my life, to all my classmates and to all the people that have been by my side.

Ringraziamenti

Questa tesi è il capitolo finale di un cammino iniziato nel 2019, quando mi sono iscritta al corso di laurea magistrale in fisica. Per prima cosa, voglio ringraziare tutti i professori incontrati in questi anni, che nonostante la pandemia dovuta al covid e le difficoltà nell'organizzare gli esami e le lezioni online sono sempre stati disponibili e sono riusciti a trasmettere la passione per il loro lavoro. In particolare, voglio ringraziare di cuore la mia relatrice, professoressa Stefania Beolè, guida preziosa durante la tesi. La sua attenzione, la sua presenza e i suoi preziosi consigli sono stati la luce che mi ha guidato nei periodi più bui del lavoro.

I miei ringraziamenti più sentiti vanno anche alla professoressa Elena Botta per il suo aiuto fondamentale durante le lunghe misure in laboratorio e per le sue fondamentali correzioni della tesi e della presentazione, che mi hanno fatto migliorare molto.

La mia gratitudine va anche all'ingegnere Silvia Coli e a Flori Dumitache che mi hanno spiegato ogni passaggio dell'assemblaggio del tracciatore svolgendo il loro lavoro con grande competenza e passione e che sono sempre state disponibili per ulteriori spiegazioni e aiuti durante il lavoro.

Sono profondamente riconoscente a Franco Benotto che mi ha offerto la sua profonda conoscenza e competenza dal mio primo giorno la sua presenza e quella di Chiara Ferrero, Matilde Dematteis, Andrea Turcato e Umberto Savino ha reso le giornate di lavoro molto più leggere e piacevoli.

Vorrei estendere i miei più sinceri ringraziamenti a tutte le altre persone, professori e tecnici che hanno collaborato con me durante la tesi e che hanno sempre dimostrato una grande competenza e passione.

Un grande grazie a Francesco Nozzoli e al professor Roberto Iuppa che mi hanno guidato nella scelta di cambiare università e di continuare i miei studi e con cui ho lavorato durante tutta la durata della laurea magistrale per pubblicare i risultati ottenuti durante la laurea triennale.

Un ringraziamento di gran cuore va anche alla mia famiglia che mi ha sostenuto ad ogni passo del cammino, credendo sempre in me e essendo sempre lì a prendermi durante i periodi più bui. In particolare ringrazio mia mamma Annachiara, mio papà Giancarlo, le mie sorelle Matilde e Silvia che svolgono un ruolo fondamentale nella mia vita. Un grande ringraziamento va anche ai miei nonni Marco e Mariella che ricordo sempre quando sono lontana da casa e a mia zia Silvana che ha seguito passo dopo passo i miei studi.

La mia infinita gratitudine va alle mie amiche e coinquiline Paola, Chiara e Viola che hanno reso indimenticabili gli scorsi mesi e riempiono i miei giorni di gioia e amore. Ci ricorderemo sempre le nostre avventure con la blatta infame, le risate serali, cucinare insieme e andare al baloon. Non so come avrei fatto se non vi avessi incontrate.

Grazie alla mia compagna di corso Alessia, che è sempre stata al mio fianco

per rassicurarmi durante le difficoltà degli esami e delle lezioni, e che è stata un solido riferimento in questi due anni. Le nostre conversazioni al telefono e le poche volte che siamo riuscite a studiare insieme sono alcune delle cose che mi hanno permesso di superare questi anni di pandemia mentre cambiavo città dove studiare e mi adattavo alla nuova università.

Vorrei ringraziare particolarmente Matteo, il mio amico fisico teorico, con cui ho avuto il privilegio di studiare durante la pandemia. Il tuo aiuto e il tuo sostegno significano molto per me. Il tempo passato passeggiando, studiando e cucinando insieme a Jacopo, Matteo, Luca e Veronica è uno dei più bei ricordi degli anni del corso di laurea triennale e magistrale.

Grazie a Silvia perché da quando ti ho conosciuta sono certa di avere un'amica fantastica a fianco a me, sei una delle persone più importanti nella mia vita. Tu sei la persona che mi ha fatto vedere la bellezza di Torino e mi ha fatto accettare questo cambiamento nella mia vita. Il tuo entusiasmo e la tua meraviglia di fronte ad ogni cosa che la vita ti presenta sono un esempio per me.

Un ringraziamento speciale va ad Ester, che è un'amica meravigliosa e che mi ha aiutata in uno dei periodi più bui della mia laurea magistrale, sostenendomi e ospitandomi in un momento veramente difficile. Sei per me una fonte di ispirazione sia come scienziata che come donna.

Un grazie va a Noemi e Ivana, la vita ci ha portate insieme e nonostante la distanza, Bologna, Bressanone, Trento e Torino non sono stati ostacoli alla nostra amicizia. Siete le persone straordinarie che sono mie compagne in questo viaggio e con cui affrontare gli ostacoli della vita.

Grazie a Giulia, la mia matricola preferita (sì, lo so che non sei più matricola da un bel pò), sei sempre presente per accompagnarmi nelle avventure della vita e sei quella che mi motiva affinché io faccia del mio meglio e a puntare ad obiettivi sempre più difficili.

La mia gratitudine va a Viola e a Mazzu, che sono le migliori persone con cui andare in montagna, non sappiamo mai quale sarà la prossima montagna e che sfide incontreremo.

Un'enorme grazie ad Eleonora e a Marianna perché ci sono sempre per me e per essere delle grandi fonti di ispirazione nella mia vita.

Un ringraziamento a "I Regaz di via Sommarive" e a Chiara Vecchi che mi hanno iniziato alla vita universitaria e hanno giocato un ruolo importantissimo durante i primi anni del corso di laurea triennale.

In fine, vorrei esprimere la mia gratitudine a tutte le persone che ho incontrato e che mi hanno sostenuta e accompagnata in questi anni negli studi e nella vita, a tutti i compagni di corso e a tutte le persone che sono state al mio fianco.

