# Analog pixel test structures (APTS)

## Overview

- 4*4 pixels with 16 buffered analogue outputs
- Aim to characterize sensor
- DC coupled and AC coupled version, and version with special in-pixel amplifier (IPHC)
- Three sensor versions: standard, modified and modified with gap
- Two versions of output buffer: source follower and opamp, central matrix identical

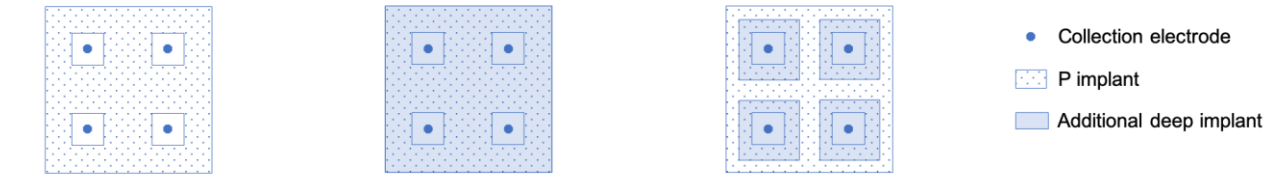
## General Description

APTS features fast analogue readout and includes various sensor flavours, aims at sensor characterization. The APTS family consists of 36 variants of single matrix chips and 2 variants of 4x multiplexed matrix, 44 pixel variants in total. They can be recognized by the on-chip label as follows. A chip list can be found in chip variants section.

**Analog readout structures:**

- F: basic source follower structure offers a robust analog readout, but slower
- A: based on basic source follower structure, an in-pixel amplifier is implemented in the pixel front-end before source follower chain, features higher gain.
- O: high speed OPAMP buffers out frontend output, achieves better timing performance with 50ohm terminating resistance on board. Identical front-end as basic source follower structures.

**Sensor flavors:**

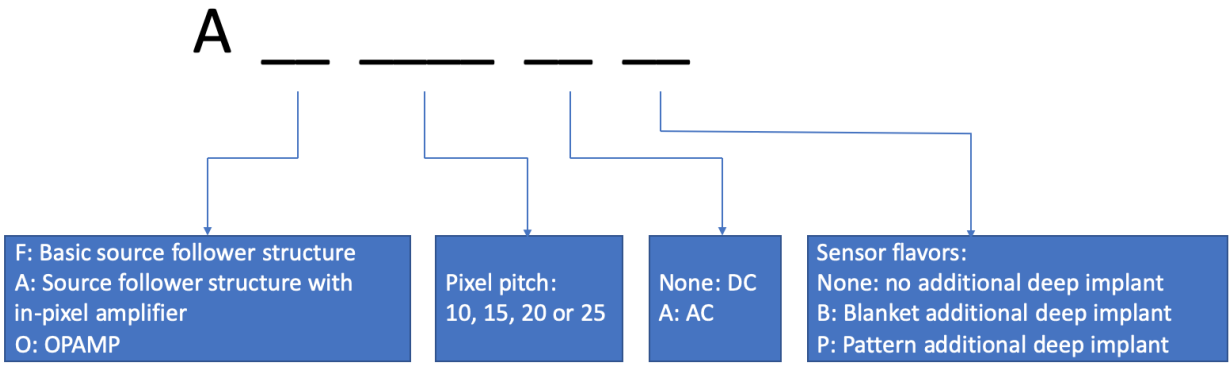



None: standard process

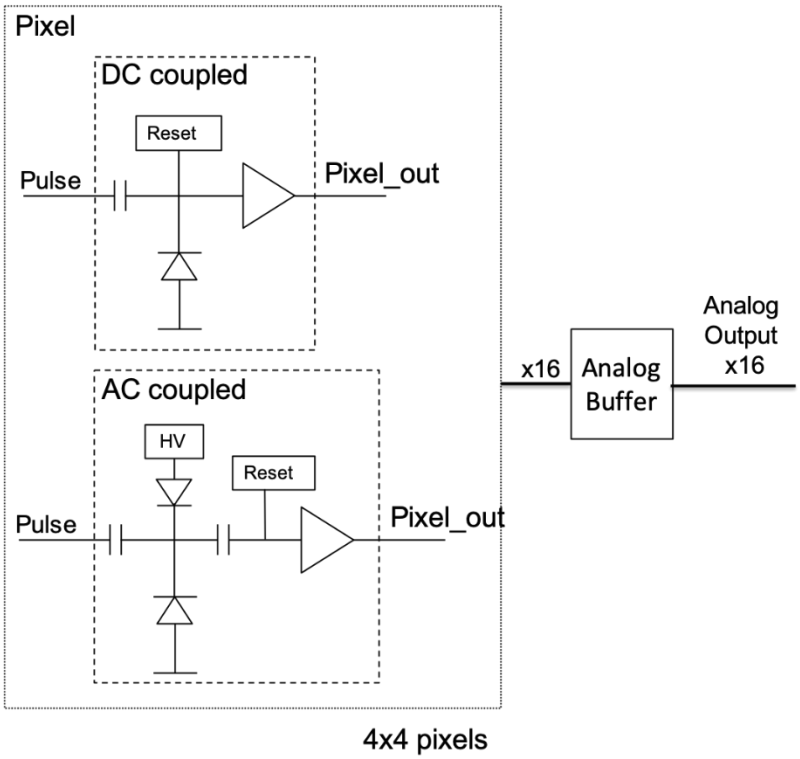
B: modified process with blanket additional deep implant

P: modified process with gap in the additional deep implant

AC coupled version gives the possibility to bias the electrode with higher voltage.



## High level functional block diagram






## Revision History

22/01/2021 V.0.0
25/02/2021 V.1.0 Top-view drawing of sensor is included
03/03/2021 V.1.1 Correct the names of pin 13 and 24 in the table of pads
10/03/2021 V.1.2 Add long-term performance
11/10/2021 V.1.3 Correct the chip labels for AO structures
10/01/2022 V.1.4 Clarify pulsing selection bits SEL_0, SEL_1
25/01/2022 V.1.5 Add schematics under recommended operating conditions

26/04/2022 V.1.6 Remove AF20B in the chip list; Add schematic of in-pixel amplifier

## Document permissions

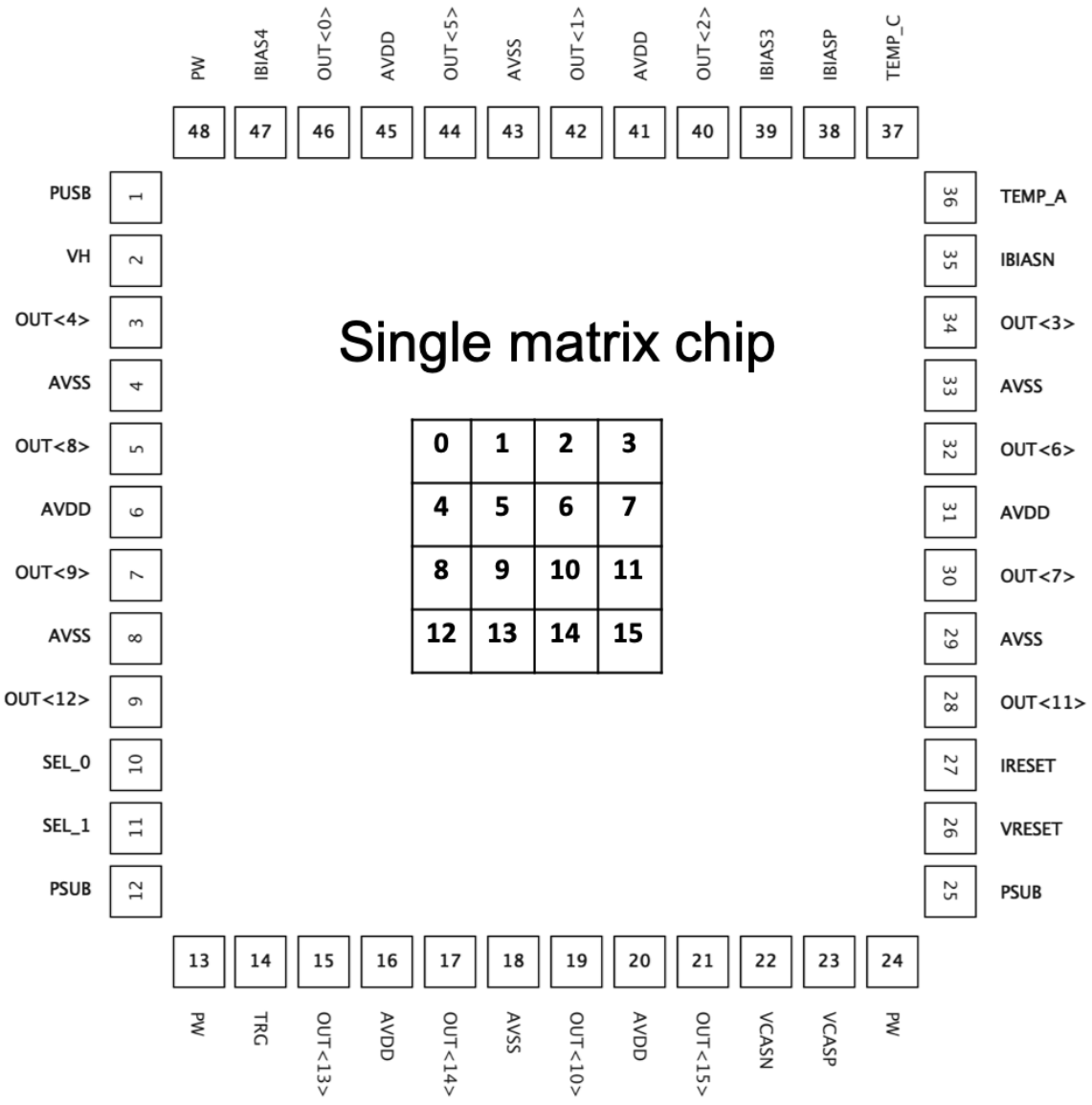
Public

## Chip variants

| Chip label | Pixel pitch (um) | Buffer | AC or DC coupled | Process |
|---|---|---|---|---|
| AF10 | 10 | source follower | DC | standard |
| AF10B | 10 | source follower | DC | modified |
| AF10P | 10 | source follower | DC | modified with gap |
| AF15 | 15 | source follower | DC | standard |
| AF15B | 15 | source follower | DC | modified |
| AF15P | 15 | source follower | DC | modified with gap |
| AF20 | 20 | source follower | DC | standard |
| AF20P | 20 | source follower | DC | modified with gap |
| AF25 | 25 | source follower | DC | standard |
| AF25B | 25 | source follower | DC | modified |
| AF25P | 25 | source follower | DC | modified with gap |
| AA10 | 10 | in-pixel amplifier + source follower | DC | standard |
| AA10B | 10 | in-pixel amplifier + source follower | DC | modified |
| AA10P | 10 | in-pixel amplifier + source follower | DC | modified with gap |
| AA20 | 20 | in-pixel amplifier + source follower | DC | standard |
| AA20B | 20 | in-pixel amplifier + source follower | DC | modified |
| AA20P | 20 | in-pixel amplifier + source follower | DC | modified with gap |
| AF10A | 10 | source follower | AC | standard |
| AF10AB | 10 | source follower | AC | modified |
| AF10AP | 10 | source follower | AC | modified with gap |
| AF20A | 20 | source follower | AC | standard |
| AF20AB | 20 | source follower | AC | modified |
| AF20AP | 20 | source follower | AC | modified with gap |
| AA10A | 10 | in-pixel amplifier + source follower | AC | standard |
| AA10AB | 10 | in-pixel amplifier + source follower | AC | modified |
| AA10AP | 10 | in-pixel amplifier + source follower | AC | modified with gap |
| AA20A | 20 | in-pixel amplifier + source follower | AC | standard |

| | | | | |
|---|---|---|---|---|
| AA20AB | 20 | in-pixel amplifier + source follower | AC | modified |
| AA20AP | 20 | in-pixel amplifier + source follower | AC | modified with gap |
| AO10 | 10 | opamp | DC | standard |
| AO10B | 10 | opamp | DC | modified |
| AO10P | 10 | opamp | DC | modified with gap |
| AO10A | 10 | opamp | AC | standard |
| AO10AB | 10 | opamp | AC | modified |
| AO10AP | 10 | opamp | AC | modified with gap |
| AF10PM | 10 | source follower + multi-plexer | DC | 4 variants modified with gap |
| AF20PM | 20 | source follower +multi-plexer | DC | 4 variants modified with gap |

## Table of pads

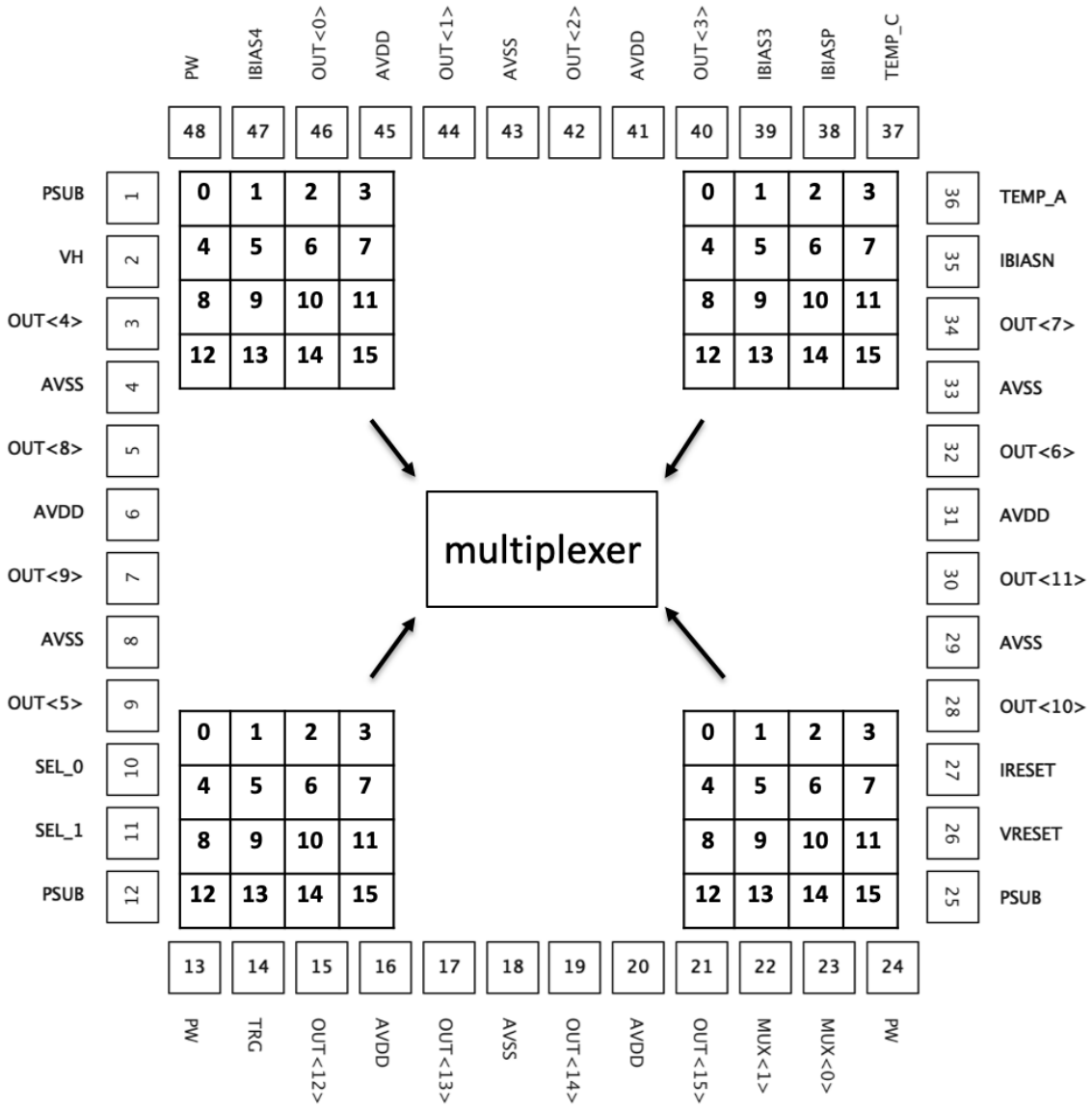



**Single matrix chips:**

| No. | Name | Direction | Description | Type |
|---|---|---|---|---|
| 48 | PW | | Pwell and deep pwell in matrix | Bias |
| 47 | IBIAS4 | | Source follower NMOS current mirror bias<br>or OPAMP PMOS current mirror bias | Bias |
| 46 | OUT<0> | Out | Pixel 0 analog output | Analog output |
| 45 | AVDD | | 1.2V Power | Supply |
| 44 | OUT<5> | Out | Pixel 5 analog output | Analog output |
| 43 | AVSS | | Ground | Supply |
| 42 | OUT<1> | Out | Pixel 1 analog output | Analog output |
| 41 | AVDD | | 1.2V Power | Supply |
| 40 | OUT<2> | Out | Pixel 2 analog output | Analog output |

| | | | | |
|---|---|---|---|---|
| 39 | IBIAS3 | | Source follower PMOS current mirror bias<br>or OPAMP PMOS current mirror bias | Bias |
| 38 | IBIASP | | Source drain follower PMOS current mirror bias | Bias |
| 37 | TEMP_C | | Cathode of temperature diode | Bias |
| 36 | TEMP_A | | Anode of temperature diode | Bias |
| 35 | IBIASN | | Source drain follower NMOS current mirror bias | Bias |
| 34 | OUT<3> | Out | Pixel 3 analog output | Analog output |
| 33 | AVSS | | Ground | Supply |
| 32 | OUT<6> | Out | Pixel 6 analog output | Analog output |
| 31 | AVDD | | 1.2V Power | Supply |
| 30 | OUT<7> | Out | Pixel 7 analog output | Analog output |
| 29 | AVSS | | Ground | Supply |
| 28 | OUT<11> | Out | Pixel 11 analog output | Analog output |
| 27 | IRESET | | Reset current | Bias |
| 26 | VRESET | | Reset voltage | Bias |
| 25 | PSUB | | Psubstrate | Bias |
| 24 | PW | | Pwell and deep pwell in matrix | Bias |
| 23 | VCASP | | OPAMP structure: PMOS voltage bias for OPAMP<br>*No connection for source follower structure | Bias |
| 22 | VCASN | | OPAMP structure: NMOS voltage bias for OPAMP<br>*No connection for source follower structure | Bias |
| 21 | OUT<15> | Out | Pixel selection for pulsing | Analog output |
| 20 | AVDD | | 1.2V Power | Supply |
| 19 | OUT<10> | Out | Pixel 10 analog output | Analog output |
| 18 | AVSS | | Ground | Supply |
| 17 | OUT<14> | Out | Pixel 14 analog output | Analog output |
| 16 | AVDD | | 1.2V Power | Supply |
| 15 | OUT<13> | Out | Pixel 13 analog output | Analog output |
| 14 | TRG | In | Pulsing input | Digital input |
| 13 | PW/HV | | Pwell and deep pwell in matrix<br>*In AC coupled chips, it's high voltage bias on electrode | Bias |
| 12 | PSUB | | Psubstrate | Bias |
| 11 | SEL_1 | In | Pixel selection for pulsing | Digital input |
| 10 | SEL_0 | In | Pixel selection for pulsing | Digital input |
| 9 | OUT<12> | Out | Pixel 12 analog output | Analog output |
| 8 | AVSS | | Ground | Supply |
| 7 | OUT<9> | Out | Pixel 9 analog output | Analog output |
| 6 | AVDD | | 1.2V Power | Supply |
| 5 | OUT<8> | Out | Pixel 8 analog output | Analog output |

| | | | | |
|---|---|---|---|---|
| 4 | AVSS | | Ground | Supply |
| 3 | OUT<4> | Out | Pixel 4 analog output | Analog output |
| 2 | VH | | Voltage bias: amplitude of pulsing signal | Bias |
| 1 | PUSB | | Psubstrate | Bias |




**Multiplexing chip:**

| | | | | |
|---|---|---|---|---|
| 48 | PW | | Pwell and deep pwell in matrix | Bias |
| 47 | IBIAS4 | | Source follower NMOS current mirror bias | Bias |
| 46 | OUT<0> | Out | Pixel 0 analog output | Analog output |
| 45 | AVDD | | 1.2V Power | Supply |
| 44 | OUT<1> | Out | Pixel 1 analog output | Analog output |

| | | | | |
|---|---|---|---|---|
| 43 | AVSS | | Ground | Supply |
| 42 | OUT<2> | Out | Pixel 2 analog output | Analog output |
| 41 | AVDD | | 1.2V Power | Supply |
| 40 | OUT<3> | Out | Pixel 3 analog output | Analog output |
| 39 | IBIAS3 | | Source follower PMOS current mirror bias | Bias |
| 38 | IBIASP | | Source drain follower PMOS current mirror bias | Bias |
| 37 | TEMP_C | | Cathode of temperature diode | Bias |
| 36 | TEMP_A | | Anode of temperature diode | Bias |
| 35 | IBIASN | | Source drain follower NMOS current mirror bias | Bias |
| 34 | OUT<7> | Out | Pixel 7 analog output | Analog output |
| 33 | AVSS | | Ground | Supply |
| 32 | OUT<6> | Out | Pixel 6 analog output | Analog output |
| 31 | AVDD | | 1.2V Power | Supply |
| 30 | OUT<11> | Out | Pixel 11 analog output | Analog output |
| 29 | AVSS | | Ground | Supply |
| 28 | OUT<10> | Out | Pixel 10 analog output | Analog output |
| 27 | IRESET | | Reset current | Bias |
| 26 | VRESET | | Reset voltage | Bias |
| 25 | PSUB | | Psubstrate | Bias |
| 24 | PW | | Pwell and deep pwell in matrix | Bias |
| 23 | MUX<0> | | MUX selection bit | Digital input |
| 22 | MUX<1> | | MUX selection bit | Digital input |
| 21 | OUT<15> | Out | Pixel 15 analog output | Analog output |
| 20 | AVDD | | 1.2V Power | Supply |
| 19 | OUT<14> | Out | Pixel 14 analog output | Analog output |
| 18 | AVSS | | Ground | Supply |
| 17 | OUT<13> | Out | Pixel 13 analog output | Analog output |
| 16 | AVDD | | 1.2V Power | Supply |
| 15 | OUT<12> | Out | Pixel 12 analog output | Analog output |
| 14 | TRG | In | Pulsing input | Digital input |
| 13 | PW | | Pwell and deep pwell in matrix | Bias |
| 12 | PSUB | | Psubstrate | Bias |
| 11 | SEL_1 | In | Pixel selection for pulsing | Digital input |
| 10 | SEL_0 | In | Pixel selection for pulsing | Digital input |
| 9 | OUT<5> | Out | Pixel 5 analog output | Analog output |
| 8 | AVSS | | Ground | Supply |
| 7 | OUT<9> | Out | Pixel 9 analog output | Analog output |
| 6 | AVDD | | 1.2V Power | Supply |
| 5 | OUT<8> | Out | Pixel 8 analog output | Analog output |
| 4 | AVSS | | Ground | Supply |
| 3 | OUT<4> | Out | Pixel 4 analog output | Analog output |
| 2 | VH | | Voltage bias: amplitude of pulsing signal | Bias |
| 1 | PSUB | | Psubstrate | Bias |

Note: pixel number always starts from top left to bottom right in single matrix chips as well as multiplexing chips.

## Absolute Ratings

| Parameter | Rating |
|---|---|
| Analog input voltage | -0.1 to +1.3V |
| Digital input voltage | -0.1 to +1.3V |
| P-well bias voltage | 0 to -6V |
| P-substrate bias voltage* | 0 to -50V |
| High voltage bias for AC coupled chips | 0 to +50V |

*Substrate bias voltage range needs to be tested first.

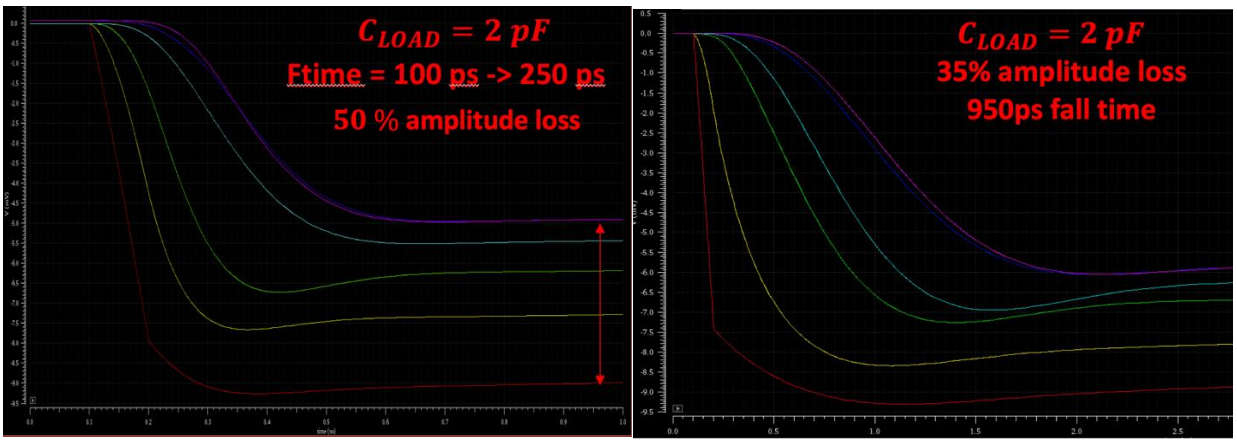
## Recommended Operating Conditions

Applied for all sensor flavours.

| Parameter | | Comments | Min. | Typ. | Max | Unit |
|---|---|---|---|---|---|---|
| Operating temperature | | | -40 | 27 | 85 | °C |
| Power voltage AVDD | | | | 1.2 | | V |
| Front-end bias (same for all chip variants) | IBIASP | ¼ mirror ratio to frontend | | +80 | +100 | uA |
| | IBIASN | ¼ mirror ratio to frontend | | -800 | -1000 | uA |
| | IRESET | $1/10^4$ mirror ratio to frontend | +0.1 | +1 | +1 | uA |
| | VRESET | | +200 | +200 | +400 | mV |
| Source follower bias | IBIAS3 | 1:1 mirror ratio | | +800 | +1000 | uA |
| | IBIAS4 | 1:1 mirror ratio | | -6 | -8 | mA |
| OPAMP bias | IBIAS3 | ¼ mirror ratio | +600 | +800 | +850 | uA |
| | IBIAS4 | 1:1 mirror ratio | +1 | +2.5 | +3 | mA |
| | VCASP | | 200 | 300 | 350 | mV |
| | VCASN | | 700 | 750 | 850 | mV |
| Pulsing bias | VH | | 0 | | +1.2 | V |
| Well bias | PW | Pwell bias voltage | -6 | | 0 | V |
| | PSUB | P-substrate bias voltage | -50 | | 0 | V |
| | HV | For AC coupled chips | 0 | | +50 | V |
| Analog output terminating resistance | | For OPAMP chips | | 50 | | Ω |
| Input signal rise and fall time | | | | | 1 | us |

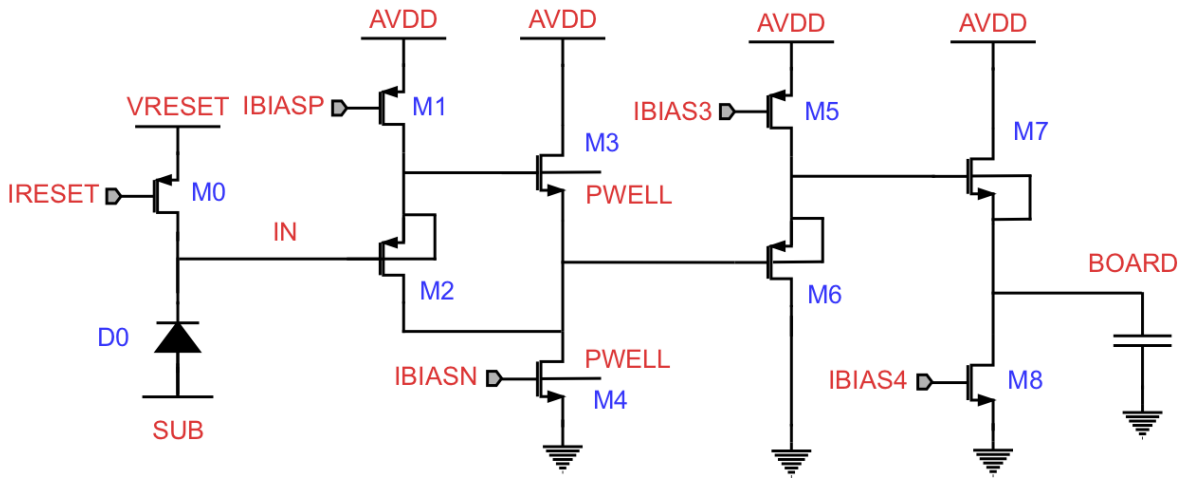
*Assume the positive current direction (+) of current bias is from pin to ground on board

For all the source followers, there is no lower current limit; the lower the current, the slower the source follower. To operate in low power mode, all the currents can be simply scaled by 10x, e.g. IBIASP 8 uA IBIASN -80 uA and so on. The two simulations below show the speed degradation for the two operation modes. Both simulations have been performed with a load capacitance of 2pF; in the high power mode, the output transition time is 250 ps, whilst in the low power case it is around 1 ns.

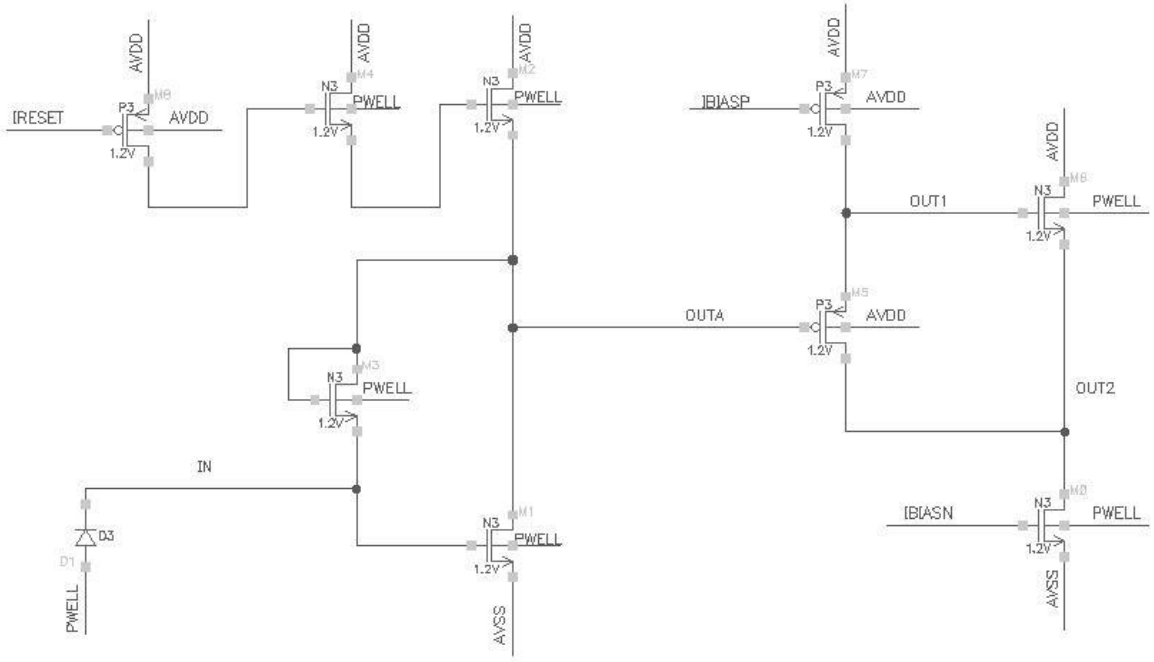



## Schematic

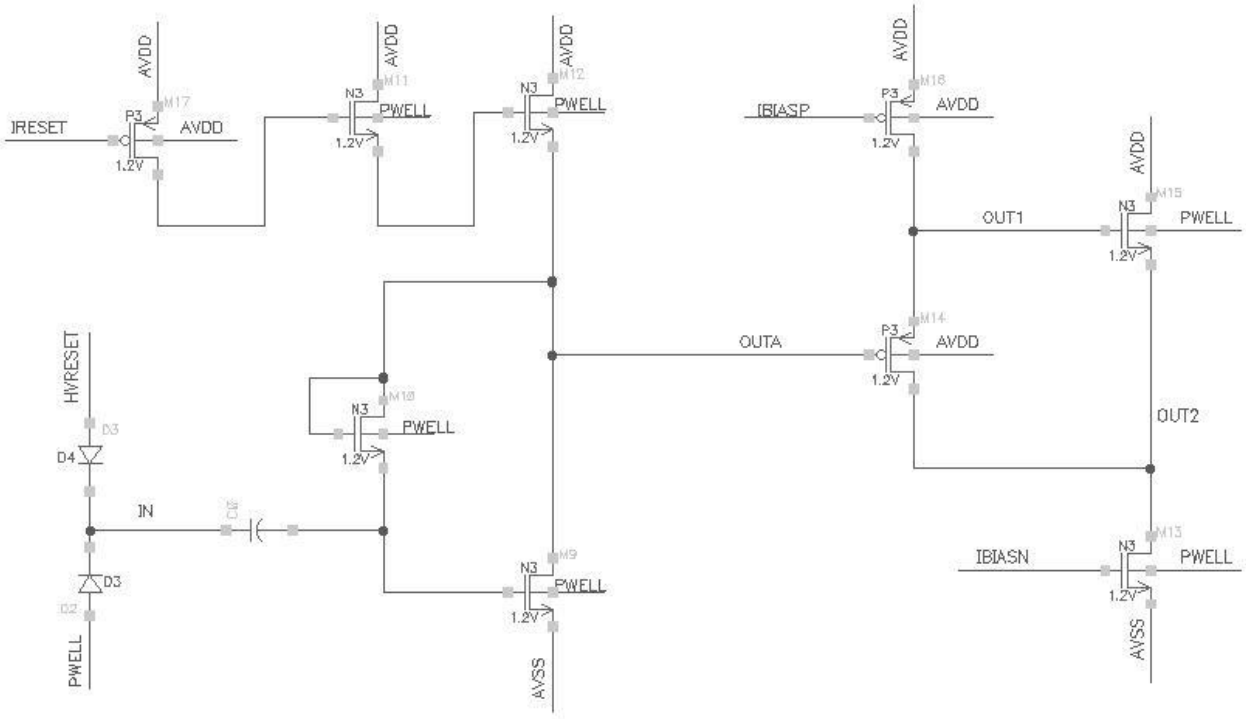
Schematic of APTS source follower version




Schematic of DC coupled in-pixel amplifier

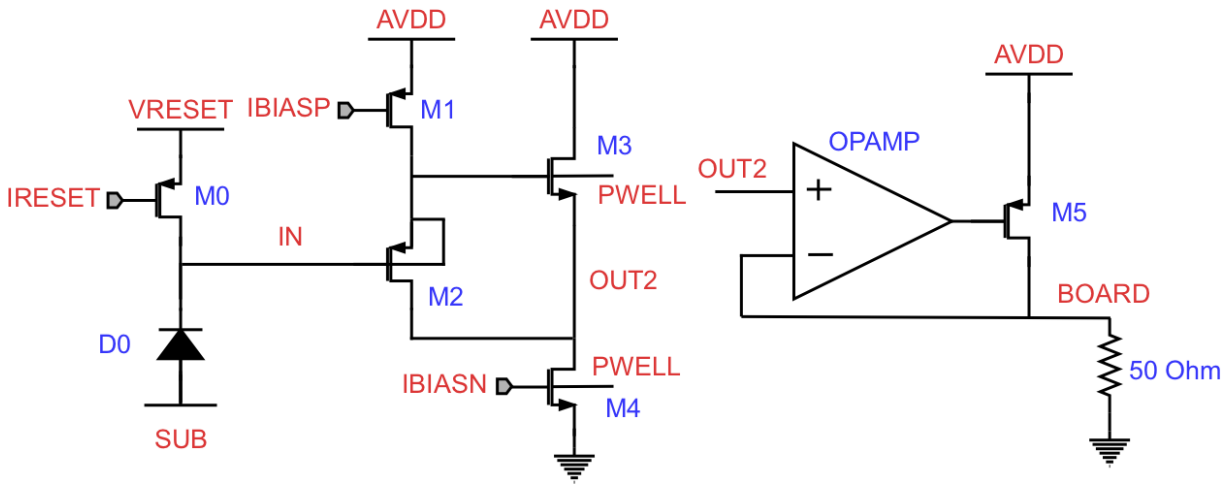


Schematic of AC coupled in-pixel amplifier

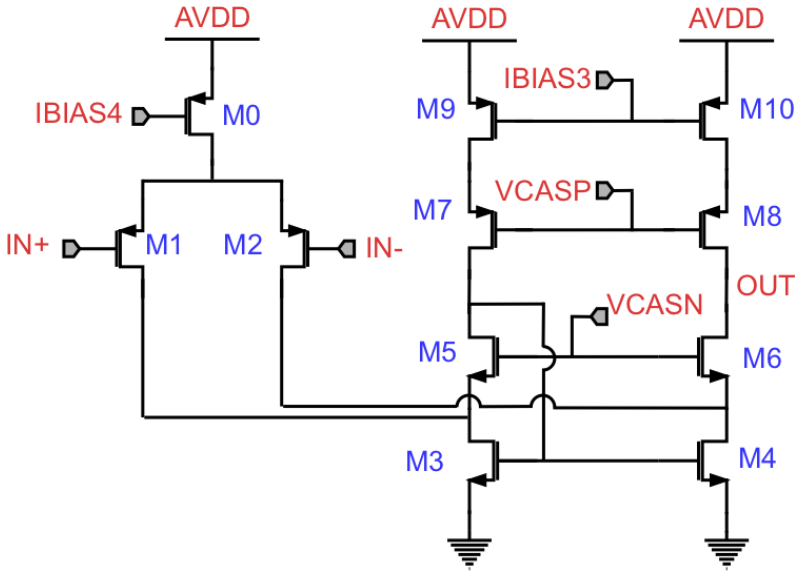



*Note: the output of in-pixel amplifier is followed by the same source follower as APTS source follower version.

Schematic of APTS OPAMP version



Schematic of OPAMP




## Electrical Specifications

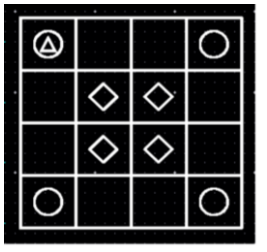
All typical specifications are at TA = 27° C and AVDD = 1.2 V, unless otherwise noted.

| **Parameter** | | **Test conditions/ comments** | **Min.** | **Typ.** | **Max** | **Unit** |
|---|---|---|---|---|---|---|
| Power consumption | SF structures | | | 108 | | mA |
| | OPAMP structures | | | 116.5 | | mA |
| ENC | DC coupled | | | 27 | | e |
| | AC coupled | | | 54 | | e |
| Pulse-IN coupling capacitance | DC coupled | | | 242 | | aF |
| | AC coupled | | | 242 | | aF |
| Collection electrode-input of frontend coupling capacitance in AC chips | | | | 10 | | fF |

## Operating Instructions

### Pulsing selection

To pulse a pixel, first set selection bits (SEL_0, SEL_1), then inject a pulse on TRG (active high)



2 Selection Bits = 4 patterns

- 00 single pixel △
- 01 outer corners ○
- 10 inner corners ◇
- 11 full matrix

| SEL_0 | SEL_1 | Hit Pattern |
|---|---|---|
| 0 | 0 | △ |
| 0 | 1 | ○ |
| 1 | 0 | ◇ |
| 1 | 1 | Full matrix |

Pulsing circuit in pixel:
VH defines the amplitude of pulsing signal
PULSE-IN Coupling = 242 aF

Note: in multiplexing chips, only left bottom matrix has the same single pixel selected as above, which is the first row first column pixel. In other 3 matrixes, the locations of selected pixel are mirrored with respect to center.

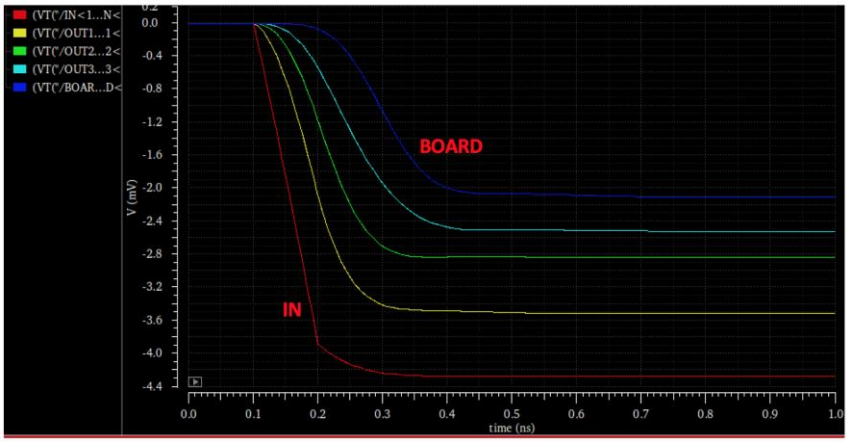
## Matrix selection by MUX:

In multiplexing chips, 2 matrix selection bits (MUX<0> MUX<1>)
00 : (left top) Larger electrode
01 : (right top) Finger shaped pwell enclosure
10 : (left bottom) Identical sensor structure as single matrix chip with pattern NX
11 : (right bottom) Smaller pwell enclosure

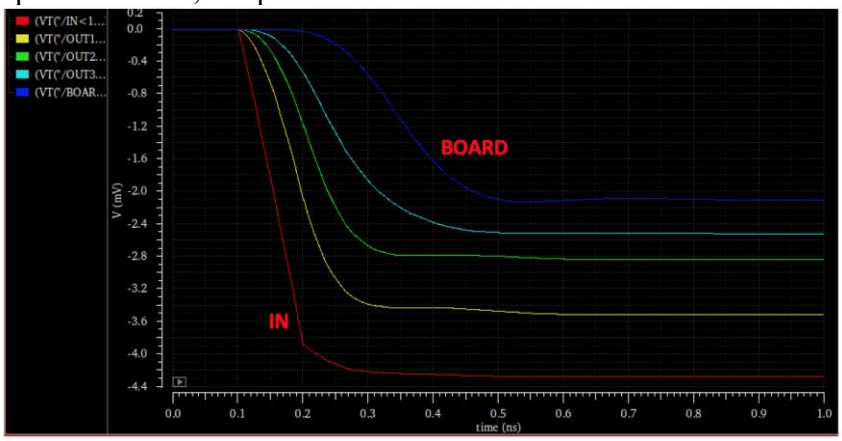
## Typical Performance Characteristics

### Source follower structures:

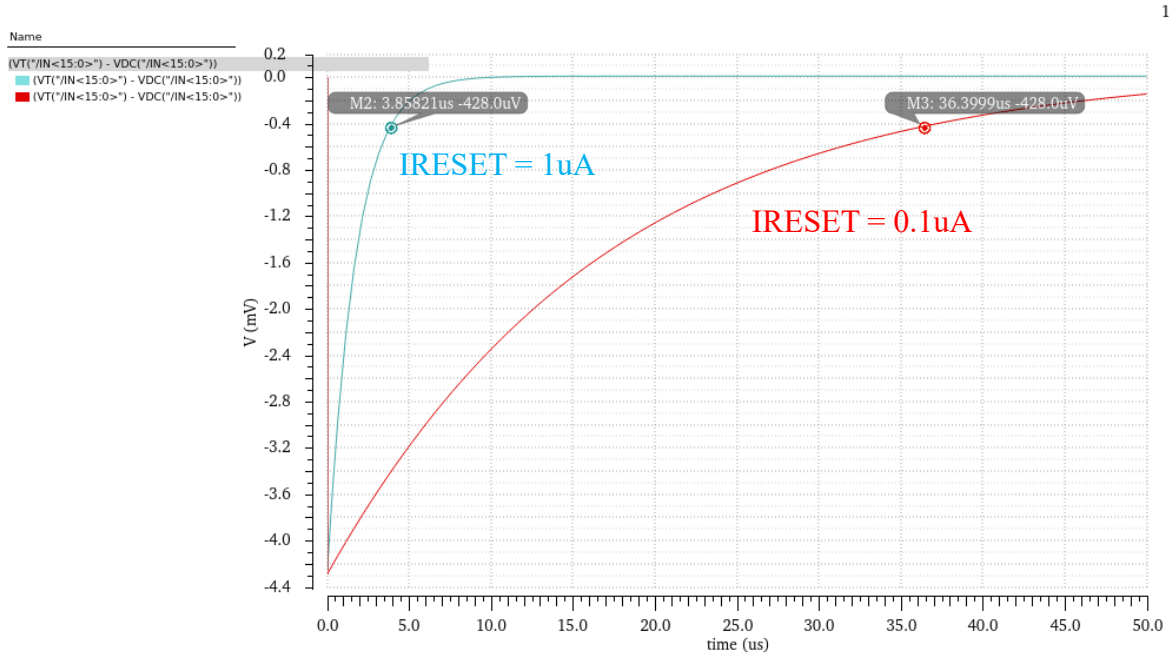
Apply the typical value of biases:
Inject 100e, 1pF board load, ~50% amplitude loss, 140ps of fall time on board.




The fall time degrades quickly with larger capacitance on board.
3pF board load, 200ps of fall time on board




Long-term performance




**In-pixel amplifier**:

The input diode capacitance set to 1fF, PCB capacitance 1pF.

OUT_PIX_AMPL is the output just after in-pixel amplifier, OUT1 and OUT2 after source followers,

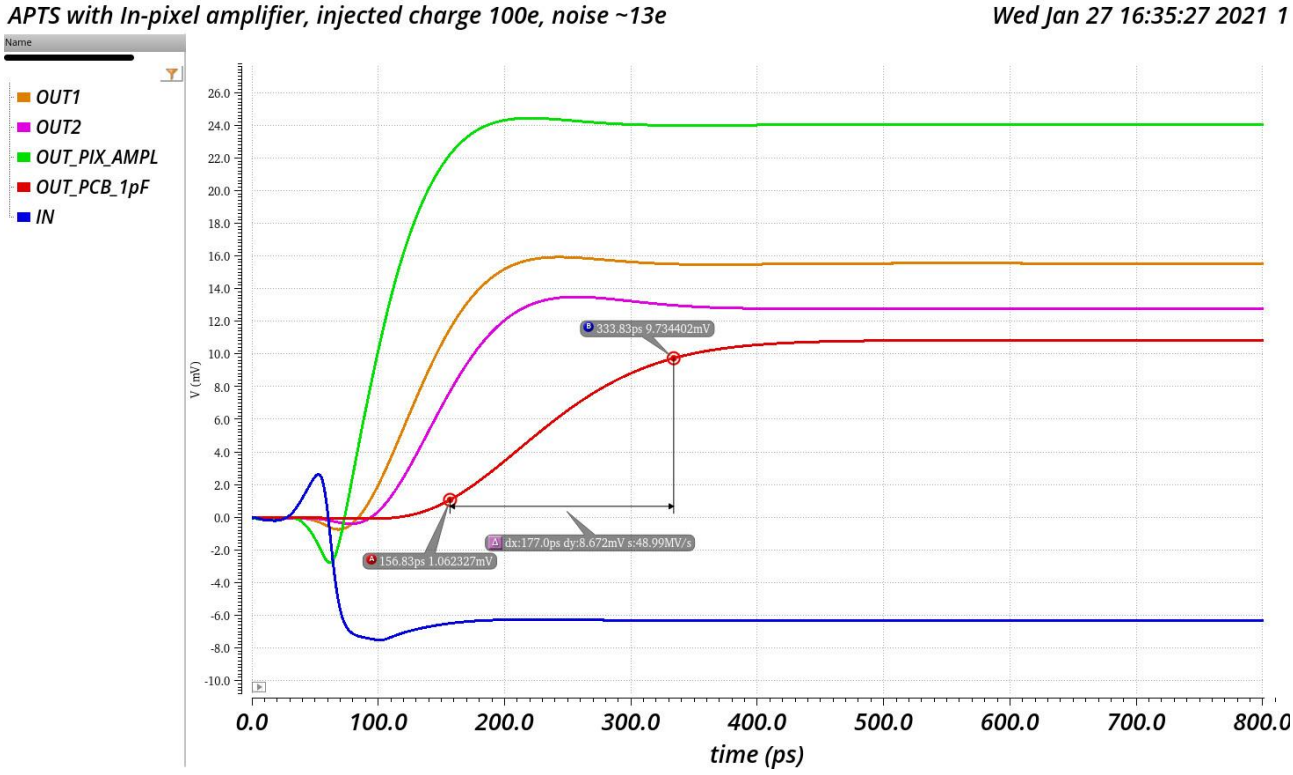
OUT_PCB_1pF - output with PADs and PCB 1pF load.

The injected charge is 100e, ENC is 13e from AC noise simulations.

Each in-pixel amplifier consumes ~15uA. (consumption of source followers are not included, they are same as in SF structures).

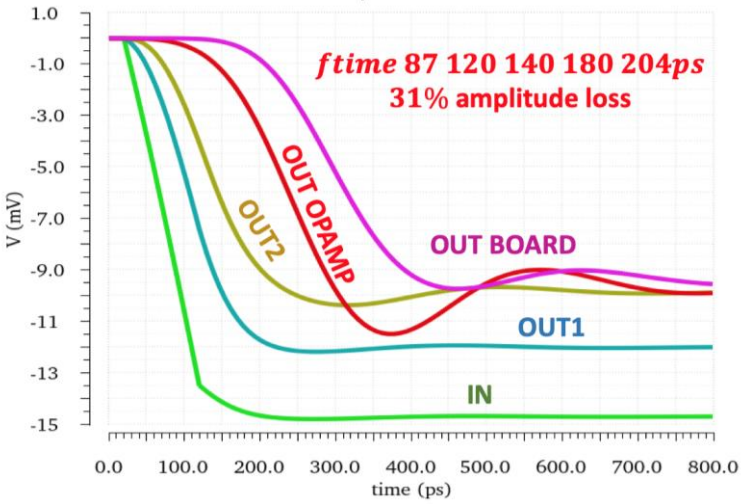
One can see that in-pixel amplifier has gain about ~4, and at the end, conversion factor at PCB is 0.1mV/electron.

Rise time at PCB output <200ps..



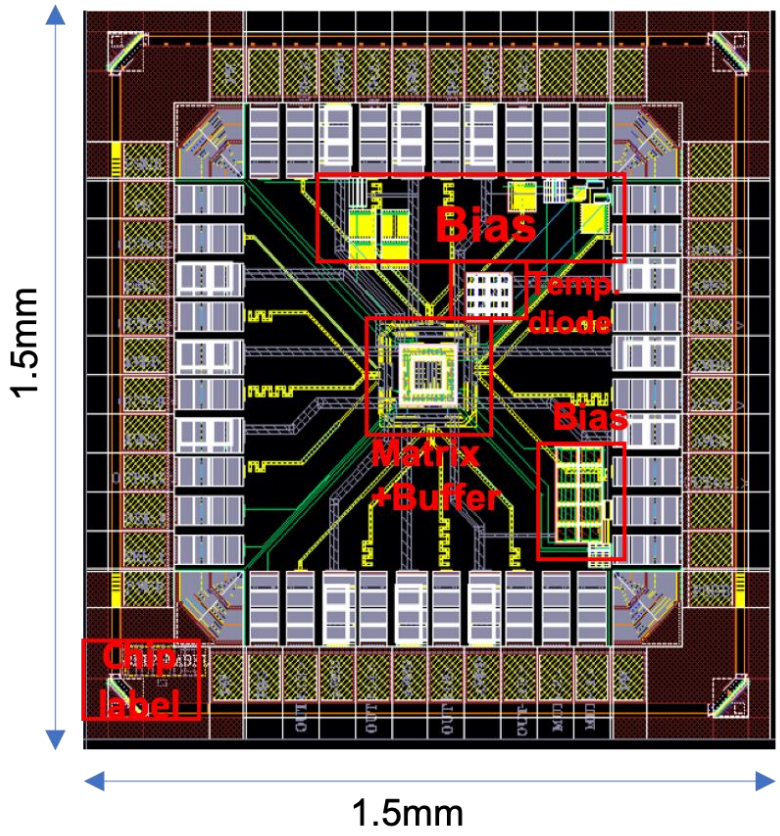
**OPAMP structures:**

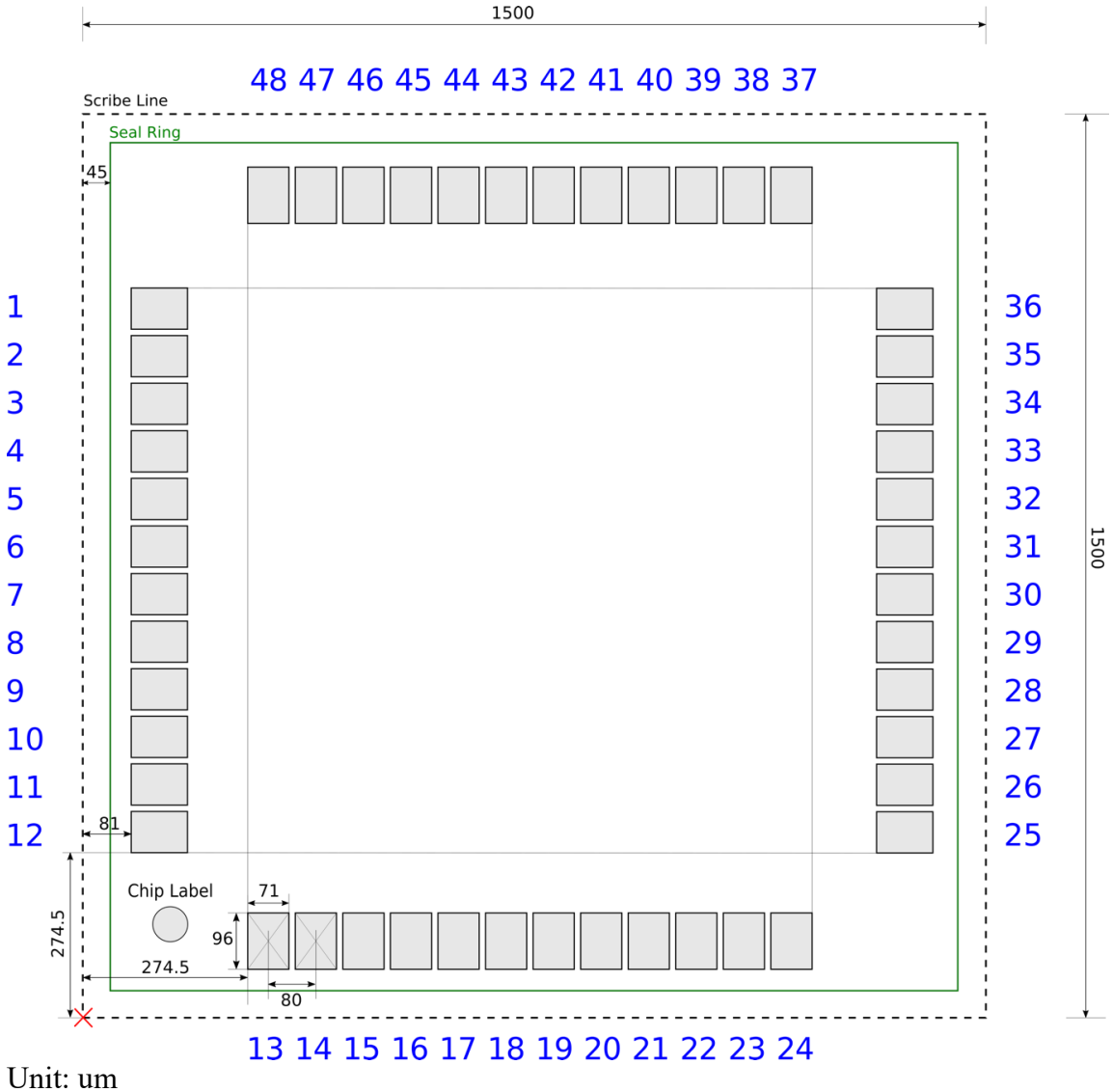
Example waveforms (300e-):




## Mechanical data

Outline / Floorplan / Top Layout Illustration / reference coordinates
Table of pads (name, orientation, centre coordinates of pads)
Geometry and dimensions of pads
Footprint for the layout of PCB carriers (die-on-board bonding)






Unit: um

Pad opening: 96*71

Pad pitch: 80

| Pad # (left) | x (um) | y (um) | Pad # (bottom) | x (um) | y (um) | Pad # (right) | x (um) | y (um) | Pad # (top) | x (um) | y (um) |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | 129 | 1190 | 13 | 310 | 129 | 25 | 1371 | 310 | 37 | 1190 | 1371 |
| 2 | 129 | 1110 | 14 | 390 | 129 | 26 | 1371 | 390 | 38 | 1110 | 1371 |
| 3 | 129 | 1030 | 15 | 470 | 129 | 27 | 1371 | 470 | 39 | 1030 | 1371 |
| 4 | 129 | 950 | 16 | 550 | 129 | 28 | 1371 | 550 | 40 | 950 | 1371 |
| 5 | 129 | 870 | 17 | 630 | 129 | 29 | 1371 | 630 | 41 | 870 | 1371 |
| 6 | 129 | 790 | 18 | 710 | 129 | 30 | 1371 | 710 | 42 | 790 | 1371 |
| 7 | 129 | 710 | 19 | 790 | 129 | 31 | 1371 | 790 | 43 | 710 | 1371 |
| 8 | 129 | 630 | 20 | 870 | 129 | 32 | 1371 | 870 | 44 | 630 | 1371 |
| 9 | 129 | 550 | 21 | 950 | 129 | 33 | 1371 | 950 | 45 | 550 | 1371 |
| 10 | 129 | 470 | 22 | 1030 | 129 | 34 | 1371 | 1030 | 46 | 470 | 1371 |
| 11 | 129 | 390 | 23 | 1110 | 129 | 35 | 1371 | 1110 | 47 | 390 | 1371 |
| 12 | 129 | 310 | 24 | 1190 | 129 | 36 | 1371 | 1190 | 48 | 310 | 1371 |