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Design of an analog monolithic pixel sensor prototype in TPSCo 65 nm CMOS imaging technology

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Abstract: A series of monolithic active pixel sensor prototypes (APTS chips) were manufactured in the TPSCo 65 nm CMOS imaging process in the framework of the CERN-EP R & D on monolithic sensors and the ALICE ITS3 upgrade project. Each APTS chip contains a 4×4 pixel matrix with fast analog outputs buffered to individual pads. To explore the process and sensor characteristics, various pixel pitches (10 µm–25 µm), geometries and reverse biasing schemes

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were included. Prototypes are fully functional with detailed sensor characterization ongoing. The design will be presented with some experimental results also correlating to some transistor measurements.

KEYWORDS: Analogue electronic circuits; Particle tracking detectors (Solid-state detectors); Solid state detectors

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Contents

1 Introduction

Monolithic active pixel sensors (MAPS) receive more and more interest for tracking detectors in high energy physics, and have shown significant progress in recent years. Fabricated in commercial CMOS technologies, normally with some process modifications to improve sensor performance, they offer advantages of detector capacitance, material budget, assembling effort and total cost compared to conventional hybrid structures. Similar to commercial ASICs, the process feature size tends to decrease to improve timing and spatial detection resolution, readout and computing speed and power consumption in high energy physics applications. A series of analog pixel test structures or APTS chips have been fabricated in the TowerJazz Panasonic Semiconductor 65 nm CMOS Image Sensor Process (TPSCo 65 nm ISC) in the framework of the CERN-EP R & D on monolithic sensors (Work package 1.2) to explore this technology as a potential candidate for future high energy physics detectors and related applications, and in particular for the ALICE ITS3 upgrade [1]. As shown in figure 1, each APTS chip measures 1.5 × 1.5 mm^2, and contains a small 4 × 4 pixel matrix with analog outputs directly buffered to output pads for off-chip real-time observation of all pixels in parallel. 34 APTS variants have been submitted, with various combinations of the pixel size, design and process variants, reverse biasing scheme, and peripheral analog output buffer.

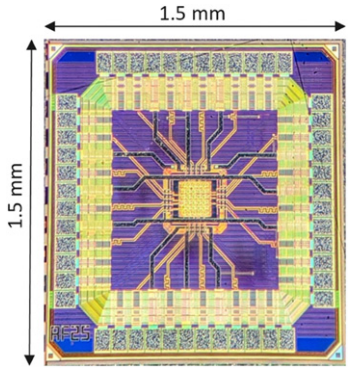

Figure 1. APTS chip with 25 µm pixel pitch.

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2 Sensor variants and analog readout chain

Figure 2 shows the cross-section of a standard pixel variant. Similar to what was implemented in ALPIDE [2] developed for the ALICE ITS2 detector in a 180 nm process, the pixel sensor is made of a small nwell collection electrode and a high-resistivity p-type epitaxial layer grown on p-type substrate. Locating the in-pixel circuitry in a deep pwell allows the usage of full CMOS circuitry for the readout in the pixel matrix without affecting charge collection by additional nwells in the circuitry. However, if the readout circuit occupies a significant fraction of the pixel area, the depletion region will be more or less balloon shaped and not extend over the full pixel width. In the 180 nm process full depletion could be obtained with an additional low dose n-type implant displacing the junction from the nwell collection electrode to deep into the epitaxial layer obtaining a planar junction and depletion over the full pixel width [3]. Introducing a gap in this low dose implant near the pixel border enhanced the lateral electric field pushing the signal charge towards the collection electrode significantly accelerating charge collection especially for hits near the pixel edge [4]. Also here different pixel variants, with similar modifications as in 180 nm, were implemented for pixel pitches of 10 µm, 15 µm, 20 µm and 25 µm in the APTS family. Each chip is equipped with only one pixel variant.

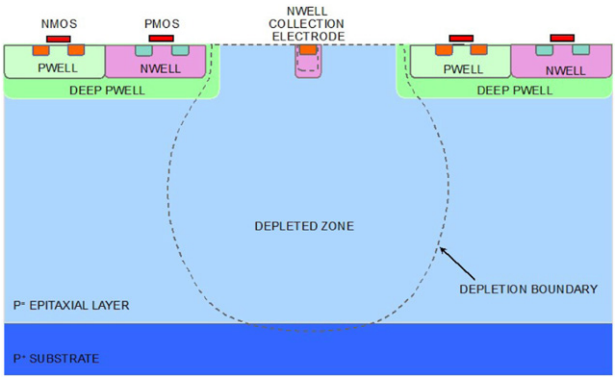

Figure 2. Cross-section of the standard pixel variant.

The pixel matrix is composed of 4 × 4 active pixels surrounded by a ring of dummy pixels, effectively occupying an area corresponding to 6 × 6 pixels. All 16 pixel outputs are read out individually to their dedicated pads. The schematic of the analog readout chain for one pixel is shown in figure 3. Two methods of applying reverse sensor bias have been implemented: applying a positive bias voltage on the nwell collection electrode or a negative bias voltage on the p-type substrate, resulting in slightly different in-pixel circuits. In the first case, the sensing node (the nwell collection electrode) voltage of up to 6 V cannot be withstood by transistors. Therefore, an AC-coupling capacitor is introduced between the sensing node and the gate of the input transistor, while the sensing node is reset via a diode and the substrate is tied to the ground. In the latter case, the sensing node or collection electrode remains directly connected to the gate of the input transistor, DC-coupled. The sensing node is reset by a PMOS transistor, while a negative bias

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voltage is applied to the substrate as well as to the bulk of NMOS transistors in the pixel matrix. The voltage signal amplitude at the sensing node (PIX_IN) is equal to $Q_{\text{in}}/C_{\text{in}}$, where Q_{in} is the collected charge and C_{in} is the total capacitance defined by the sum of the sensor capacitance and the transistor parasitic capacitance. The OUT1 net follows the input voltage signal by the first stage PMOS source follower to some extent, partly compensating the M2 gate-source capacitance. Subsequently, the OUT1 net is buffered off-pixel by an NMOS source follower. The pixel output is fed back to the drain of M2, also partly compensating its gate-drain capacitance. Hence, the charge conversion gain increases as the compensation evolves. In the periphery of the pixel matrix, the pixel analog outputs are buffered to pads by either two stages of source followers or by high speed OPerational AMPlifiers (OPAMP) combined with an output stage capable of driving a 50 Ω load to allow signal termination on board or on the scope and maximize speed capability to characterize charge collection time in the sub-nanosecond range. For the output stage of the OPAMP version, a replica of the common source is used to achieve better stability over a wide range of external capacitive loads as the feedback loop is realized with the internal fixed load.

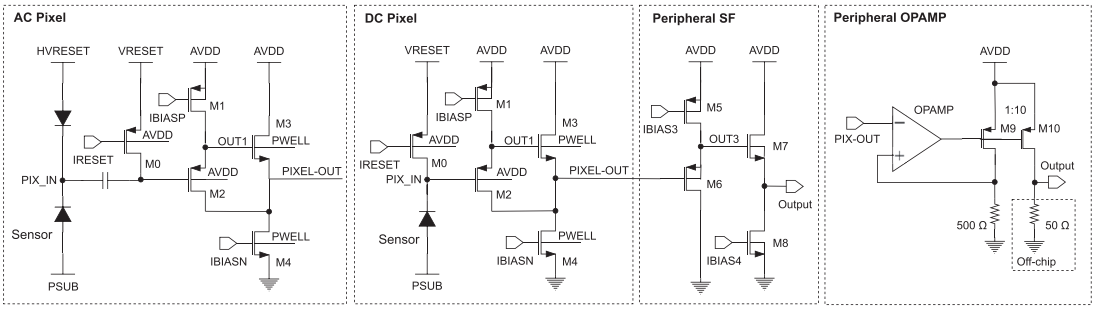

Figure 3. Schematic of the analog readout chain.

Normally one expects the signal amplitude to increase with increasing reverse sensor bias due to the reduction of the sensor capacitance as the depletion increases around the collection electrode. However, initially this was not observed in measurements for the DC coupled version: increasing reverse substrate bias also significantly affects the operating point through the body effect on the transistors, in particular for the input transistor of the NMOS follower within the pixel matrix of which the source cannot be connected to its substrate (M3 in figure 3), in particular for large reverse substrate biases (up to −6 V). As a result, under the standard design settings the gain of the analog readout chain significantly degrades with the increasing reverse substrate bias as the follower outputs approach the ground rail and saturate due to the increasing threshold voltage of M3 caused by the body effect (figure 4). After significant efforts from the ALICE measurement team, optimized operating points were established by reducing the bias current and hence the gate-source voltage of the input transistors in the source followers. As illustrated in figure 4, this significantly enlarged the operating margin and reduced the gain degradation. Further investigation confirmed the body effect was underestimated in the simulations compared to measurements for significant reverse substrate bias outside of the standard supply voltage (<−1.2 V) [5].

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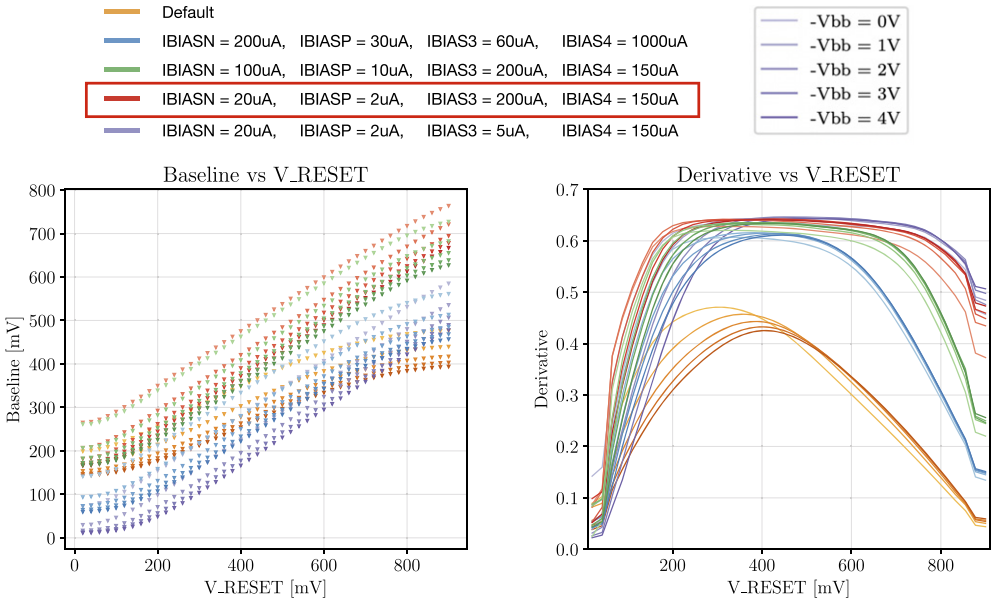

Figure 4. Measured output DC voltage (left) and its derivative (right) versus VRESET for different biasing settings. The chosen parameters for an optimized operating point are marked in the red box.

3 Sensor characterization using ^{55}Fe source

An ^{55}Fe source is used as the radioactive source for the measurement in the laboratory. It produces two X-rays with energies of 5.9 keV (K_α) and 6.5 keV (K_β), known to release on average 1640 and 1800 electron/hole pairs in silicon, respectively. Figure 5 compares the ^{55}Fe seed pixel spectrum for different pixel variants. It clearly demonstrates that different pixel variants have significantly different charge collection properties, and that the APTS chips, here in the source follower variant, are capable of putting this into evidence. A significantly larger fraction of signals within the peak indicates that most of the charge is collected in a single pixel with less charge sharing. For such variant, figure 6 compares the spectrum for varying reverse substrate bias. The amplitude increases with increasing reverse bias, as expected, illustrating the reduction of the sensor capacitance as the depletion around the collection electrode progresses. The sensor capacitance (including the circuit input capacitance) becomes comparable for all pixel variants (~2 fF) for a bias around −5 V and the signal amplitude saturates afterwards, as at that point the depletion reaches the higher doping levels within the nwell collection electrode. This is observed for all pixel pitches. Figure 7 compares the time response of the seed signal versus its amplitude for two different pixel variants, a standard version on the left, and another version strongly accelerating the charge collection on the right. Here APTS OPAMP chips were used, and they can sufficiently resolve the sub-nanosecond transition time of the pixel output to put the difference into evidence.

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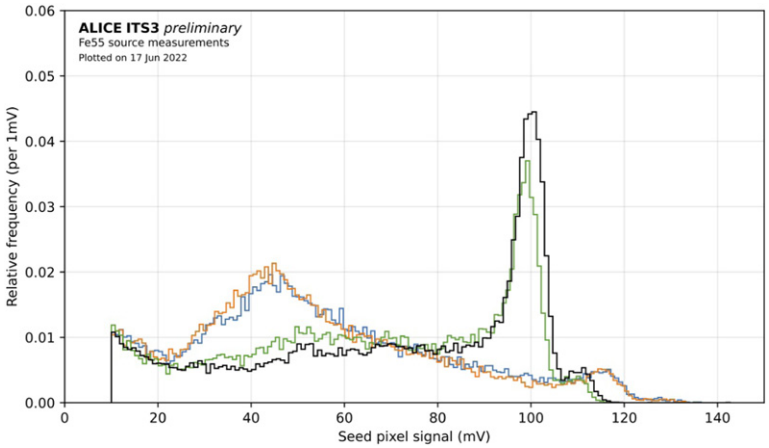

Figure 5. ^{55}Fe seed pixel spectra comparison for different pixel variants measured at $V_{\text{sub}} = V_{\text{pwell}} = -2.4\,\text{V}$. For two of the four pixel variants (green and black) additional measures were taken to accelerate the charge to the collection electrode.

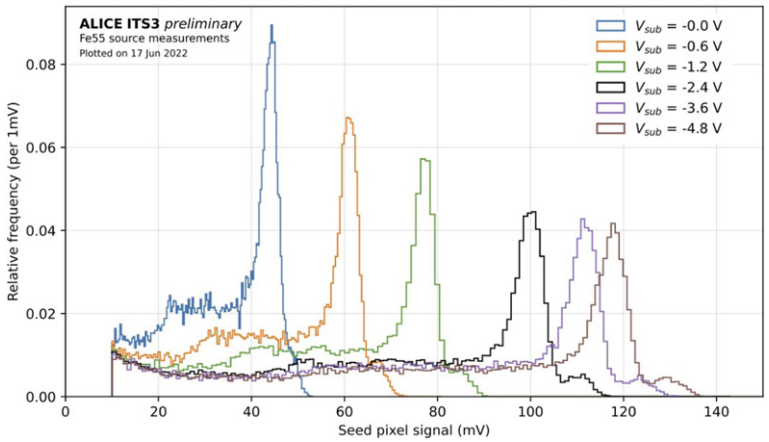

Figure 6. ^{55}Fe seed pixel spectra comparison for varying reverse bias voltage.

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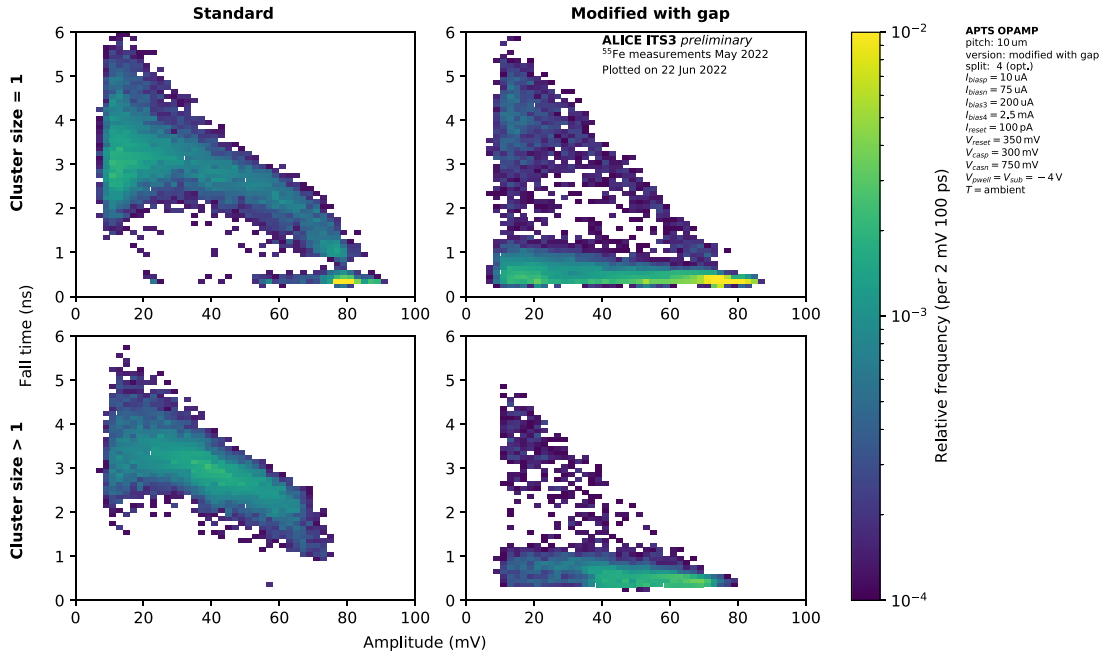

Figure 7. Time response of seed signal versus its amplitude for different pixel variants, one without (left) and one with (right) extra measures to accelerate the charge collection.

4 Summary

The APTS family contains various pixel flavors and fast analog readout, designed to characterize and optimize the charge collection performance. The presented results show that the APTS chips are fully functional and allow an in-depth study of the charge collection properties for different pixel variants. The pixel modifications significantly accelerate the charge collection and concentrate it on a single pixel as expected from simulations. The effects of reverse bias on sensor and readout circuits are also analysed in correlation with individual transistor measurements. Detailed measurements are still ongoing in the laboratory and in test beams also including irradiated sensors to complete the characterization and to validate the TPSCo 65 nm CMOS imaging technology for future high energy physics experiments.

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