UNIVERSITÀ DEGLI STUDI
DI TRENTO

Assignment Optimal Control Problem

Advanced optimiza

Jacopo Antonini, Giorgio Checola

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Department of Industrial Engineering

Università degli studi di Trento

Abstract

The metal-oxide semiconductor or MOS is a type of transistor which consists of a doped silicon substrate, two heavily doped regions called drain and source, an oxide layer deposited on top and between drain and source. In figure 1 is shown the layout of the structure.

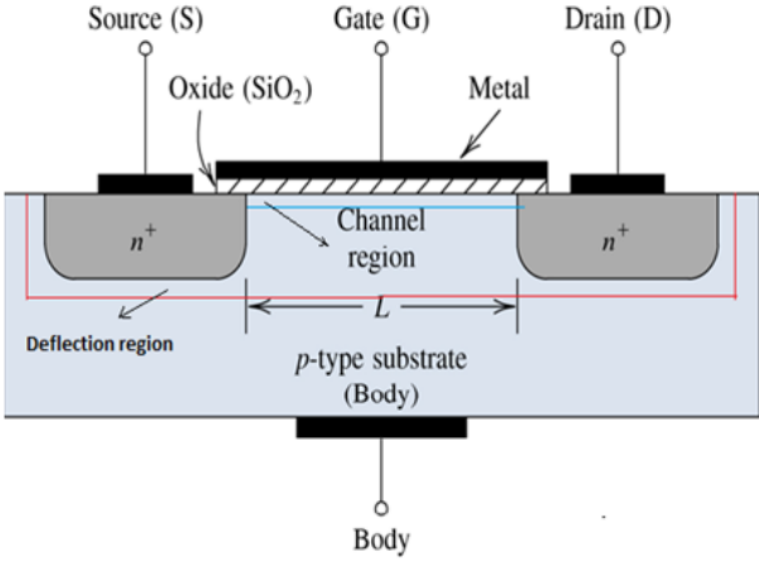


Figure 1: Basic structure of a MOSFET device.

1. asas

1 Introduction

This project is done starting by the structure shown in figure 2. The substrate is obtained by an epitaxial layer on top of a silicon bulk. The drain and the source are obtained doping two regions of the substrate with a n^+ Gaussian profile with junction depth x_j. All the geometrical parameters are listed in the Table 1.

Table 1: Geometrical Parameters

Parameter	$[\mu m]$	Parameter	$[\mu m]$
W_{DEV}	4	t_{EPI}	3
t_{SUB}	1	L	3
L_{DIMP}	0.5	L_{SIMP}	0.5
L_D	0.3	L_S	0.3
t_{ox}	$30 \cdot 10^{-3}$	-	-

2 Structure

The structure obtained is shown in figure 3, in which we can see that there is a constant profile in the epitaxial region and in the remaining substrate, with concentration $10^{16} \frac{at.B}{cm^3}$ and $10^{19} \frac{at.B}{cm^3}$ respectively.

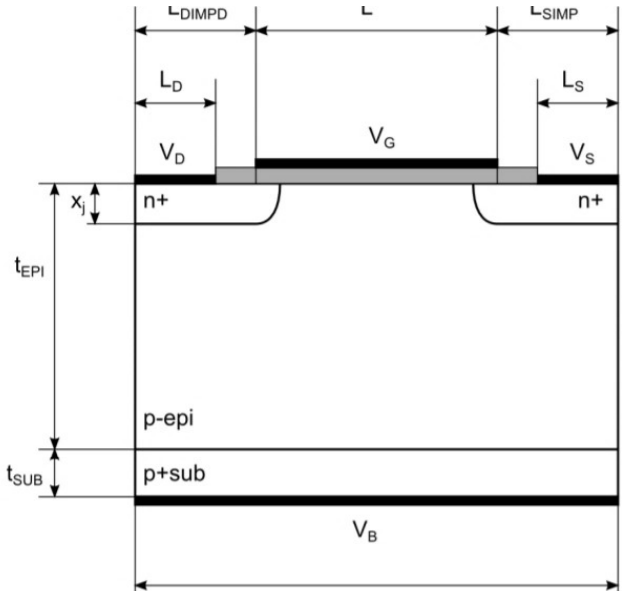


Figure 2: Structure of the NPN MOSFET used for simulation.

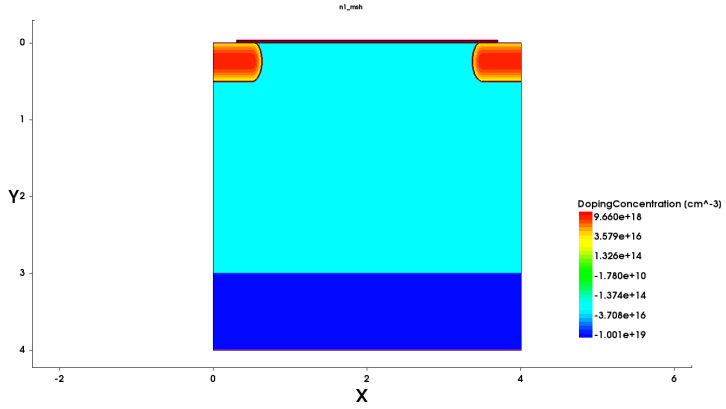


Figure 3: Doping profile of the MOSFET device.

It can also be noticed that the doping profile in the source and drain regions is Gaussian. The specification of the problem imposed the junction depth x_j to be $0.5\mu m$, the characteristic length L_c to be $0.1\mu m$ and the peak donor concentration C_p is $10^{19}\frac{at.P}{cm^3}$. The location of the peak concentration in the profile is not specified, and if we assume it to be at the surface of the device the two situations shown in figure 4a and 4b arise. So clearly the position of the maximum should be elsewhere and the mathematical expression becomes:

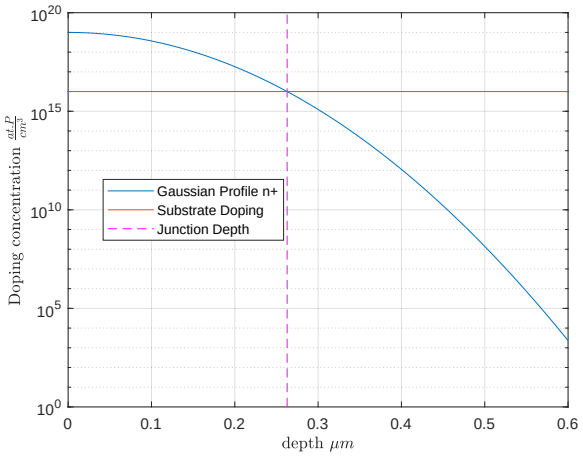
$$C(x) = C_p \cdot e^{-(\frac{x-x_p}{L_c})^2},$$

where $x_p = 0.24\mu m$. The final Gaussian profile is shown in figure 5. The mesh used for the simulation is represented in figure 6 and a detail about a critical region in figure 7.

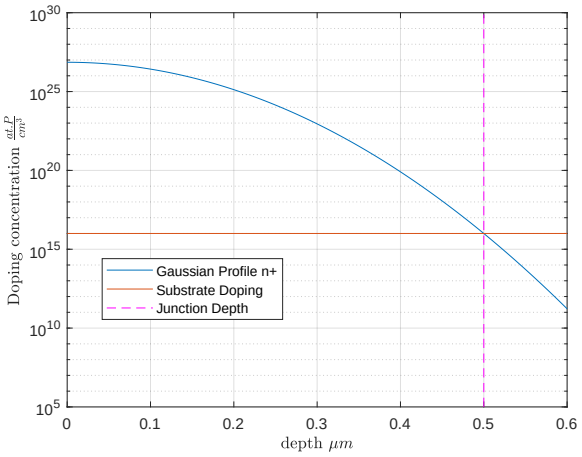
3 Simulations

3.1 Equilibrium

The first simulation done, whose result is in figure 8, is about the equilibrium state, where in 8a the electrostatic potential is shown and in figure 8b the total current due to the normal movement of the



(a) Doping profile if peak is imposed.



(b) Doping profile if junction depth is imposed.

Figure 4: Gaussian profile with peak on the surface.

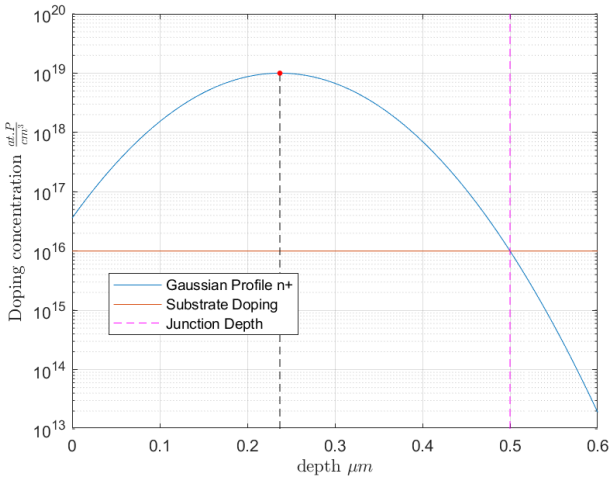


Figure 5: Final Gaussian profile

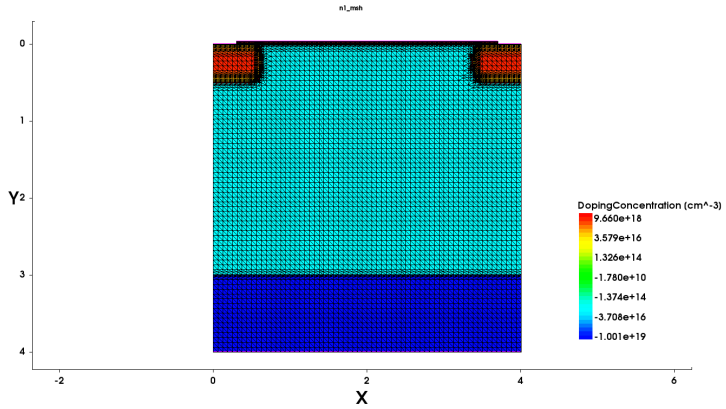


Figure 6: Mesh

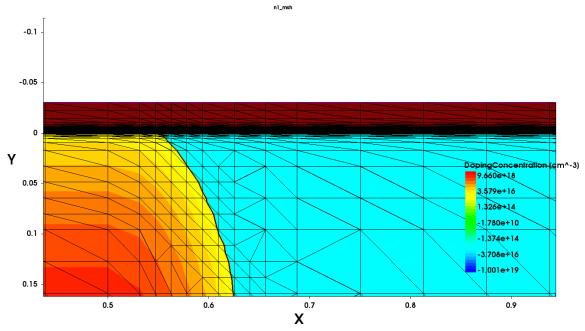
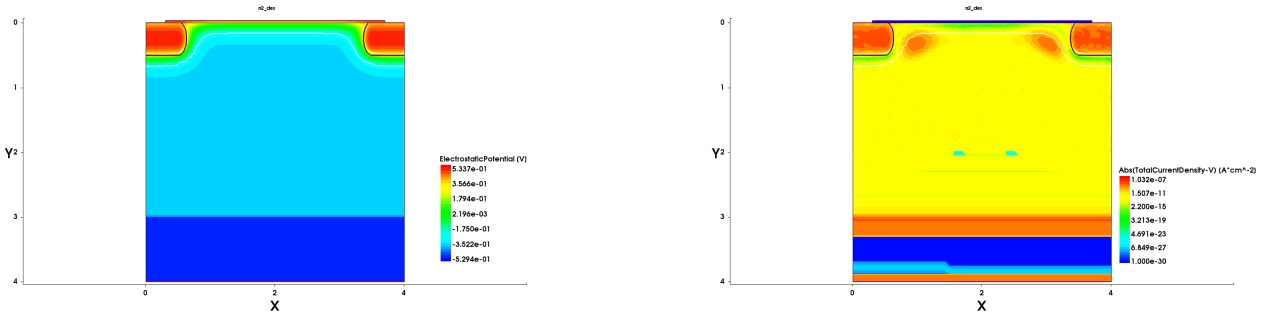


Figure 7: Detail of the mesh



(a) Electrostatic potential.

(b) Absolute current density.

Figure 8: Simulation at equilibrium condition.

charge carriers. They are calculated imposing all the electrodes to 0V.

3.2 Transfer Characteristic

The second simulation consists in finding the transfer characteristic, which is the relation that express the dependency of the drain current I_D with respect to the gate and threshold voltages. The formula is the following:

$$I_D = \frac{K_n}{2}(V_{GS} - V_{TH})^2. \tag{1}$$

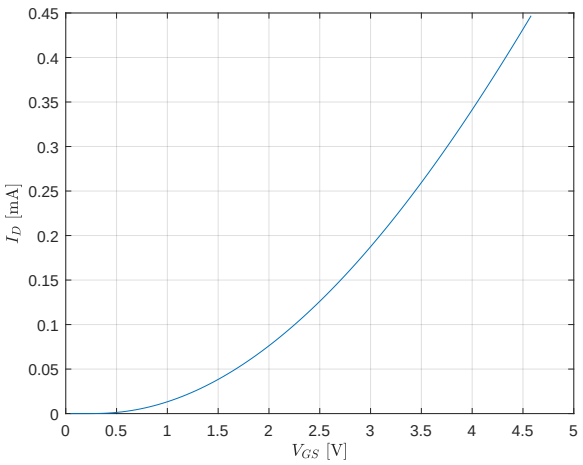
This relation holds when the MOSFET is in saturation, namely when $V_{DS} \geq V_{GS} - V_{TH}$. The simulation has been done by sweeping the gate voltage from 0 to a 5V because, since the bias imposed by the problem is $V_{DS} = 5V$ and the analytical calculation give $V_{TH} \approx 0.4V$, going further with the V_{GS} value could make the MOSFET be in the quasi-linear region where the output characteristic is

$$I_D = K_n \left[(V_{GS} - V_{TH})\, V_{DS} - \frac{{V_{DS}}^2}{2} \right]. \tag{2}$$

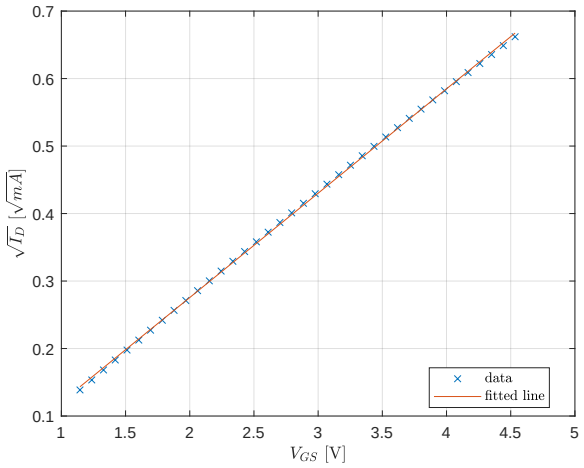
Also this formula could be used to identify K_n and V_{TH} since we know the value of V_{DS}, but finding a single function that describe these two behaviours (quasi-linear and saturated) can be too difficult. Anyway, the identification is done by linear interpolation of the square of the transfer characteristic:

$$\sqrt{I_D} = \sqrt{\frac{K_n}{2}}(V_{GS} - V_{TH}). \tag{3}$$

Figure 9 and table 2 show the processing done and the results obtained.



(a) Simulated transfer characteristic.



(b) Square root of drain current.

Figure 9: Identification of Threshold and Current Gain.

Table 2: Results of the identification

Parameter	Value	Measure Unit
V_{TH}	0.22	V
β	$4.78 \cdot 10^{-2}$	$\frac{mA}{V^2}$

3.3 Small Signal Output Resistance

In order to know the small signal output resistance, the first simulation to do is a sweep from 0V to 5V of the V_{DS}, biased at $V_{GS} = 2, 3, 4V$. A small signal is an AC voltage that is overlapped to a DC one whose amplitude is quite higher than the other one. In the case of the drain-source voltage it can be called $v_{DS} = V_{DS} + v_{ds}$. The result, at a certain gate voltage, will be $i_D = I_D + i_d$, so a small AC current plus a DC bias. This kind of result is due to the superposition effect, that holds for linear devices. A MOSFET transistor is not a linear device with respect to v_{DS}, especially in the quasi-linear region, expressed by equation 2, where the dependency is quadratic. But if the channel modulation effect is considered, the equation 1 of saturation condition becomes:

$$i_D = \frac{K_n}{2}(v_{GS} - V_{TH})^2(1 + \lambda v_{DS}), \tag{4}$$

that is linear in v_{DS}. Since i_D is a function of v_{DS} it can be expressed as $i_D(V_{DS} + v_{ds}) = I_D + i_d$ and can be seen as a Taylor expansion of the first order:

$$f(x) = f(X + \Delta x) = f(X) + \frac{df(x)}{dx}\Big|_{x=X} \Delta x. \tag{5}$$

Using this reasoning we can understand that $i_d = \frac{di_D}{dv_{DS}}\Big|_{v_{DS}=V_{DS}} v_{ds} = \frac{1}{R_{ss}} v_{ds}$, so the small signal output resistance is just the inverse of the slope of the I-V curve evaluated at V_{DS}. Since $V_{TH} > 0$, the saturation condition for $V_{DS} = 4$ is valid for each of the V_{GS} that we are going to use. Figure 10 shows the results of the simulation and table 3 reports the small signal output resistances for the three values of V_{GS}.

3.4 Gate Capacitance

The metal-oxide structure of the gate region works exactly like a capacitor, because is like two conductive plates and a dielectric material in between. Since the area is much larger than the thickness

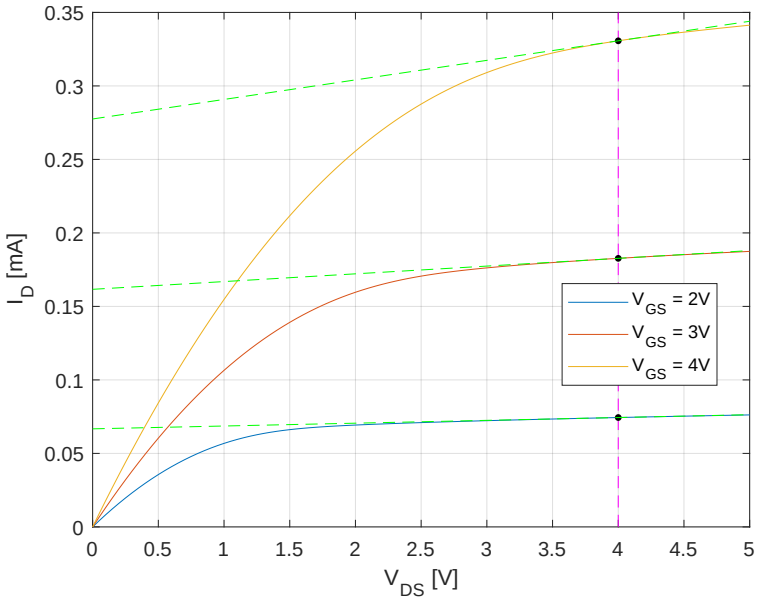


Figure 10: Output characteristic

Table 3: Small signal output resistances

Gate Bias	$[V]$	Resistance	$[k\Omega]$
V_{GS2}	2	R_{ss2}	520
V_{GS3}	3	R_{ss3}	190
V_{GS4}	4	R_{ss4}	75

of the oxide, the general formula for the capacitance holds:

$$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}}. \tag{6}$$

In addition to this behaviour, the is another capacitor cascaded to the previous one, whose dielectric material is the silicon itself and the plates are represented by the charges of the space-charge-region. Actually they are not real conductive plate, but since there are two opposite charge distributions around a dielectric material, a capacitive behaviour is observed. Therefore, the thickness of the silicon dielectric is represented by the space-charge-region width. This quantity is not fixed, like the oxide thickness as a technological parameter, but depends on the gate voltage, increasing from zero to a maximum as the gate bias reaches the threshold voltage.

$$w[\Psi_s(V_{GS})] = \sqrt{\frac{2\epsilon_s}{qN_A}(\Psi_s(V_{GS}))}. \tag{7}$$

The maximum space-charge-region is reached when $V_{GS} = V_{TH} \Rightarrow \Psi_s = 2\varphi_F$ and is equal to:

$$w_m = \sqrt{\frac{2\epsilon_s}{qN_A}(2\varphi_F)}. \tag{8}$$

So, given that the relation for planar capacitors holds:

$$C_{si} = \frac{\epsilon_s}{w[\Psi_s(V_{GS})]} = \frac{\epsilon_s}{\sqrt{\frac{2\epsilon_s}{qN_A}(\Psi_s(V_{GS}))}} \quad for \quad V_{GS} < V_{TH} \tag{9}$$

and the minimum value is:

$$C_{min} = \frac{\epsilon_s}{w_m} = \frac{\epsilon_s}{\sqrt{\frac{2\epsilon_s}{qN_A}(2\varphi_F)}} \quad for \quad V_{GS} \geq V_{TH}. \tag{10}$$

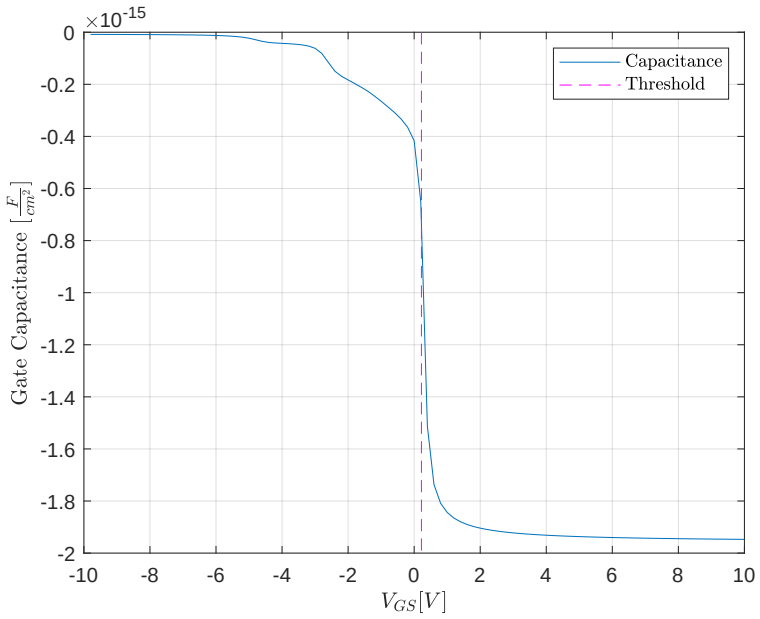


Figure 11: Gate capacitance as a function of V_{GS}

The overall value of the capacitance is obtained by calculating the series of the two capacitors:

$$C_{tot} = \frac{C_{ox} \cdot C_{si}}{C_{ox} + C_{si}}. \tag{11}$$

The simulated result of capacitance as a function of the gate voltage is shown in figure 11.

4 Threshold Adjustment

An operation that can be done on a MOSFET transistor to adjust the value of the threshold voltage is an ion implantation. Equations from 12 to 15, quantify how much the threshold can be shifted related to the charge density deposited by the ion implantation process. Φ_{ms} is the metal-semiconductor workfunction difference, Q_{eq} is the equivalent charge density of the oxide due to ionic contamination.

$$V_{TH-IDEAL} = \frac{\sqrt{2\epsilon_s q N_A (2\varphi_F)}}{\epsilon_{ox}/t_{ox}} + 2\varphi_F \tag{12}$$

$$V_{FB} = \Phi_{ms} - \frac{Q_{eq}}{C_{ox}} - \frac{\pm Q_{ii}}{C_{ox}} \tag{13}$$

$$V_{TH} = V_{TH-IDEAL} + V_{FB} \tag{14}$$

$$\Delta V_{TH} = \pm \frac{Q_{ii}}{C_{ox}} \tag{15}$$

In order to design a process to achieve the threshold adjustment, the concentration of atoms is needed rather than the charge concentration. Equation 17 represents the doping profile, where r_p is obtained by solving iteratively the non-linear equation 18. x_j and C_j are the wanted junction depth and the dopants concentration at that position, respectively.

$$N_{ii} = \frac{Q_{ii}}{q} \tag{16}$$

$$C(x) = \frac{N_{ii}}{\sqrt{\pi}\left(\sqrt{2}\Delta r_p\right)} e^{-\left(\frac{x}{\sqrt{2}\Delta r_p}\right)^2} \tag{17}$$

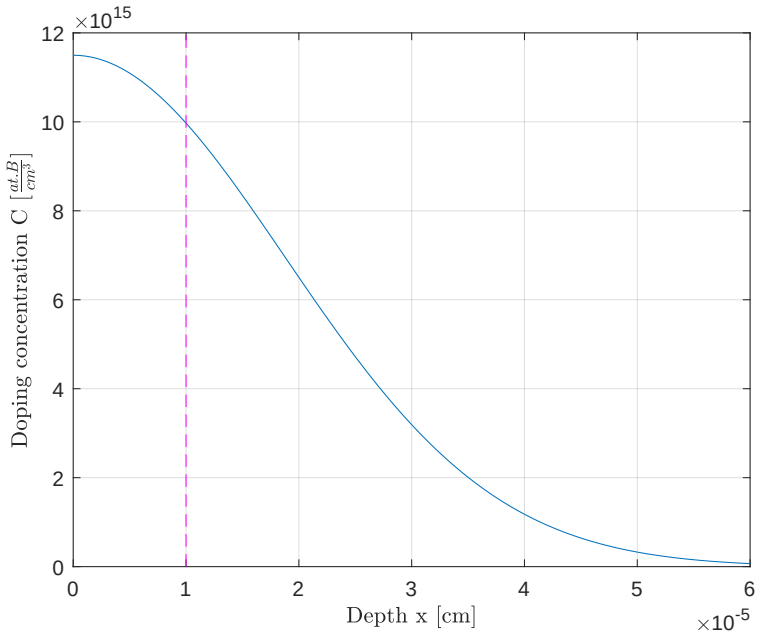


Figure 12: Doping concentration for threshold adjustment

Table 4: Threshold adjustment, first attempt.

Parameter	Value	Measure Unit
C_{ox}	113	$\frac{nF}{cm^2}$
ΔV_{TH}	0.78	V
N_{ii}	$5.4 \cdot 10^{11}$	$\frac{at.B}{cm^2}$
Δr_p	0.18	μm
C_p	$1.15 \cdot 10^{16}$	μm
C_j	10^{16}	$\frac{at.B}{cm^3}$
x_j	0.1	μm

$$\Delta r_p = \frac{N_{ii}}{\sqrt{\pi}\left(\sqrt{2}C_j\right)} e^{-\left(\frac{x_j}{\sqrt{2}\Delta r_p}\right)^2} \tag{18}$$

Table 4 lists the analytical results for the concentration profile. Unfortunately, the threshold obtained with the same identification process is equal to $V_{TH} = 0.4V$. To know why the threshold has not increased as much as expected, the integral of the doping concentration, in figure 12, is performed and is equal to $S_{ii} = 2.69 \cdot 10^{11} \frac{at.B}{cm^2}$. Actually, this value is just half of the surface concentration demanded, but the increase of the threshold is so low that it couldn't be the only reason. Probably, another possible explanation is that the acceptor distribution is too deep in the substrate, showing a total surface concentration which is correct, but that can't be exploited in the channel region. So now, the objective is to find a combination of junction depth and peak concentration in order to increase the integral value (now from 0 to 0.1 μm, instead of 0 to 1 μm). With a try and error approach a good increase of threshold is obtained with the parameters listed in table 5 and represented in figure 13.

4.1 Equilibrium

The previous simulations are done again, starting by the equilibrium condition one. In figure 14 the results are presented, where the left part of the section is about the previous simulation and the right side is about the new one. Since these results are symmetric with respect to the midline, there is no loss of information due to the overlapping. In figure 14a it can be seen that the depletion region in

Table 5: Final threshold adjustment parameters.

Parameter	Value	Measure Unit
N_{ii}	$5 \cdot 5.4 \cdot 10^{11}$	$\frac{at.B}{cm^2}$
Δr_p	0.23	μm
C_p	$5.005 \cdot 10^{16}$	$\frac{at.B}{cm^3}$
C_j	10^{16}	$\frac{at.B}{cm^3}$
x_j	0.42	μm
$\int_0^{0.1} C(x)dx$	$4.86 \cdot 10^{11}$	$\frac{at.B}{cm^3}$
V_{TH}	1.03	V

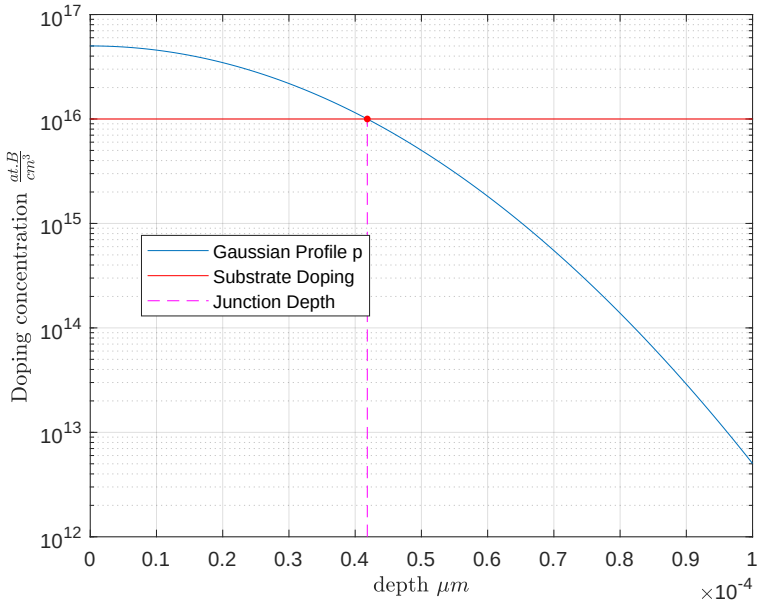
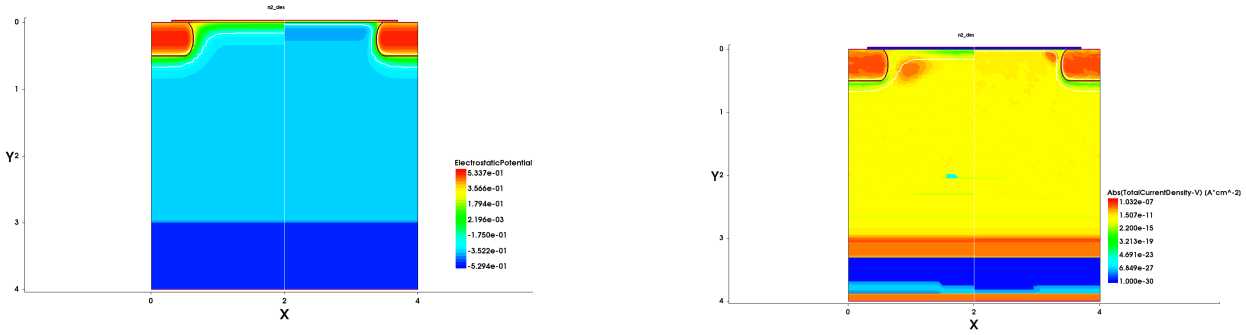


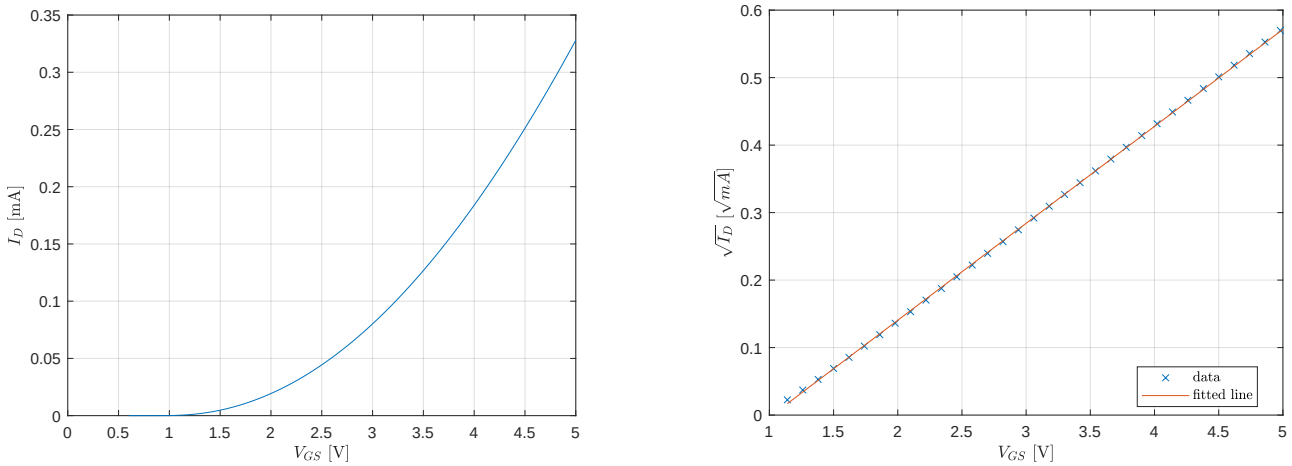
Figure 13: Final doping concentration for threshold adjustment



(a) Electrostatic Potential.

(b) Current density.

Figure 14: Simulation at equilibrium condition before and after threshold adjustment.



(a) Simulated transfer characteristic.

(b) Square root of drain current.

Figure 15: Identification of Threshold and Current Gain.

quite narrower, increasing the expected gate capacitance. In figure 14b there is no significant change of behaviour in the substrate but in the corner of the space charge region. The orange region has more or less the same total current density, but it is more concentrated due to due different shape of the corner.

4.2 Transfer Characteristic

The simulations about the transfer characteristic gives a parabola-shaped signal as expected (figure 15a), and the identification procedure gives the values collected in table 6

Table 6: Results of the identification

Parameter	Value	Measure Unit
V_{TH}	1.03	V
β	$4.13 \cdot 10^{-2}$	$\frac{mA}{V^2}$

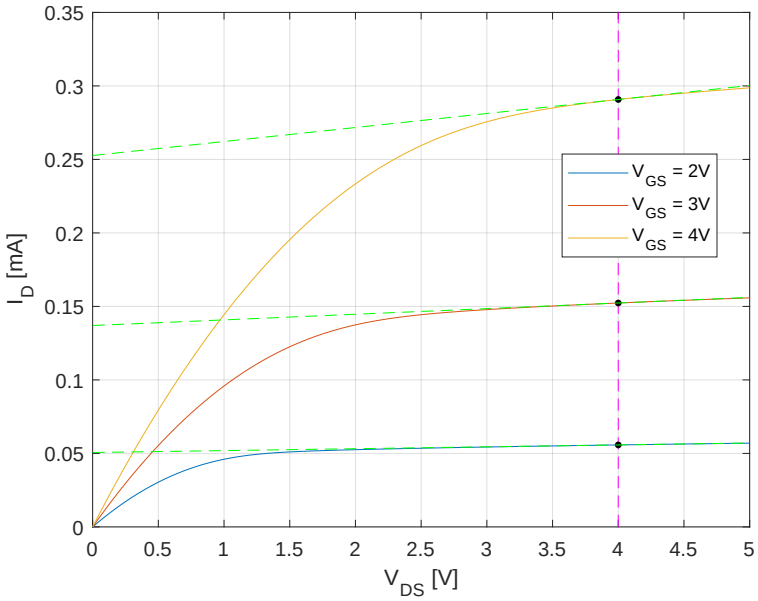


Figure 16: Output characteristic after threshold adjustment

Table 7: Small signal output resistances after threshold adjustment

Gate Bias	$[V]$	Resistance	$[k\Omega]$
V_{GS2}	2	R_{ss2}	777
V_{GS3}	3	R_{ss3}	261
V_{GS4}	4	R_{ss4}	105

4.3 Small signal output resistance

At a first glance to the output characteristic, simulated and presented in figure 16, it can be seen that the slope of the tangent lines is generally lower than before. This behaviour results in a higher value of the small signal resistances, listed in table 7. This experiment confirms that the threshold value significantly affects the channel modulation length λ.

4.4 Gate capacitance

As expected by the space charge width reduction, the overall gate capacitance increased. The only parts that remain unchanged despite the threshold adjustment are the minimum and maximum values. The maximum is equal to C_{ox} because in both cases the oxide geometry and properties is same same. The minimum depends on C_{min} (equation 10), which is constant as long as V_{GS} is higher than the threshold.

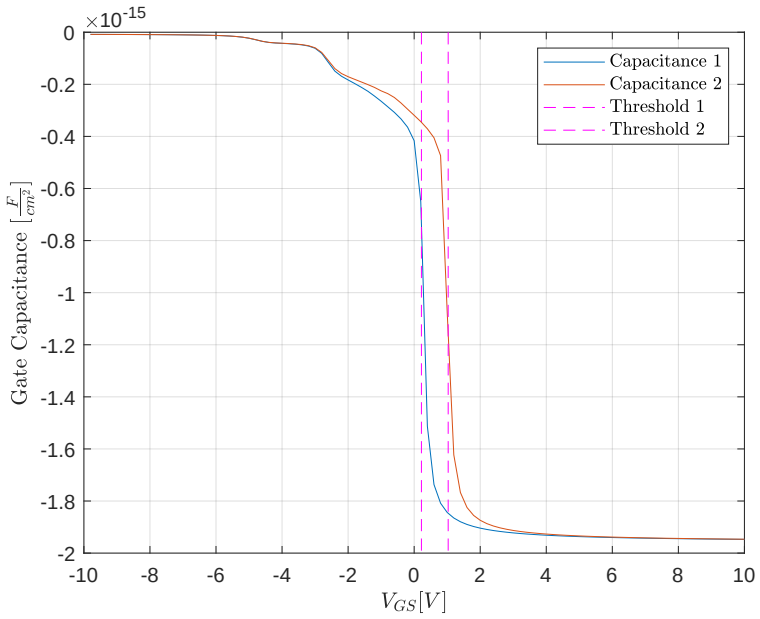


Figure 17: Gate capacitance before and after threshold adjustment.

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