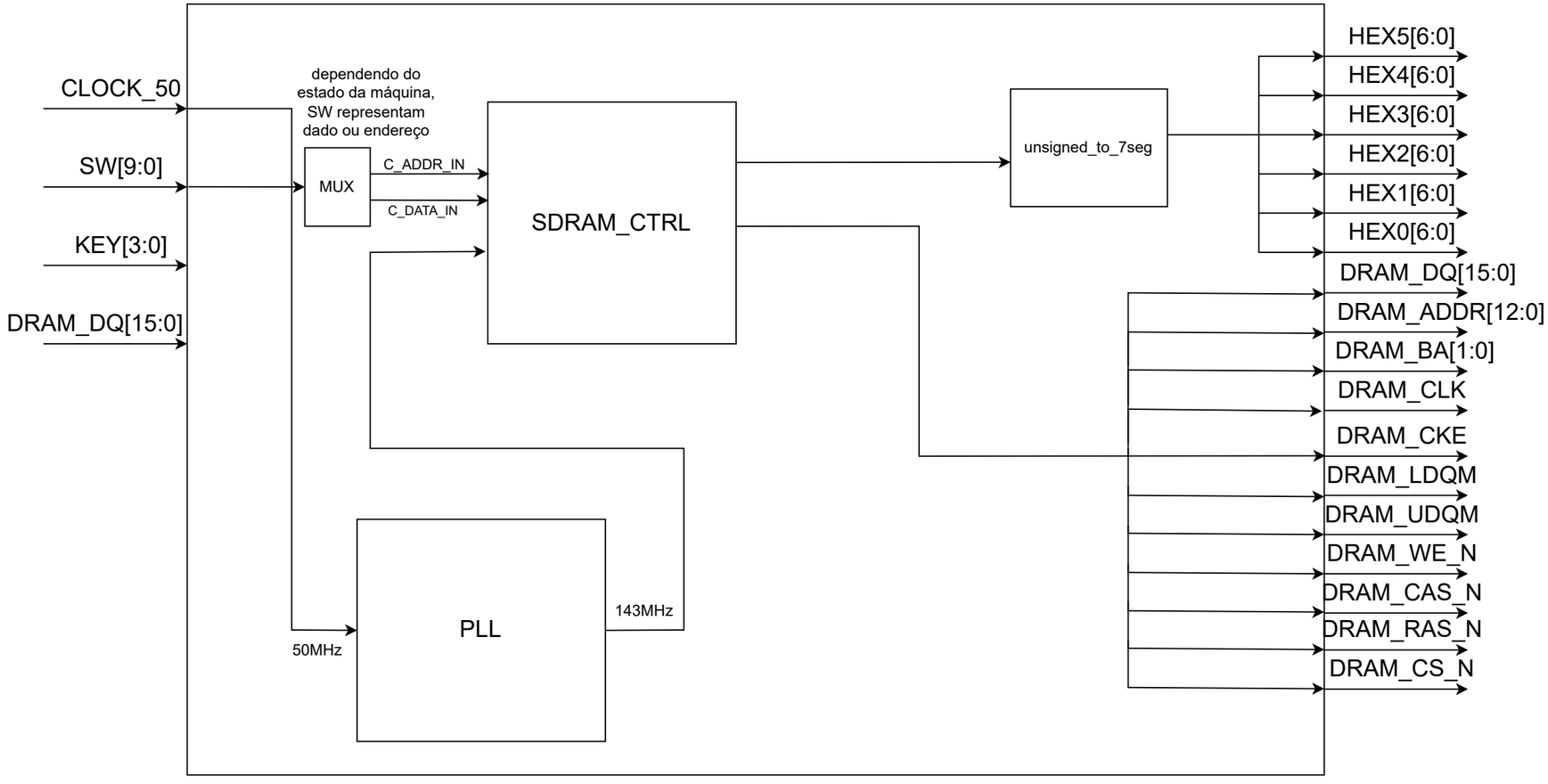
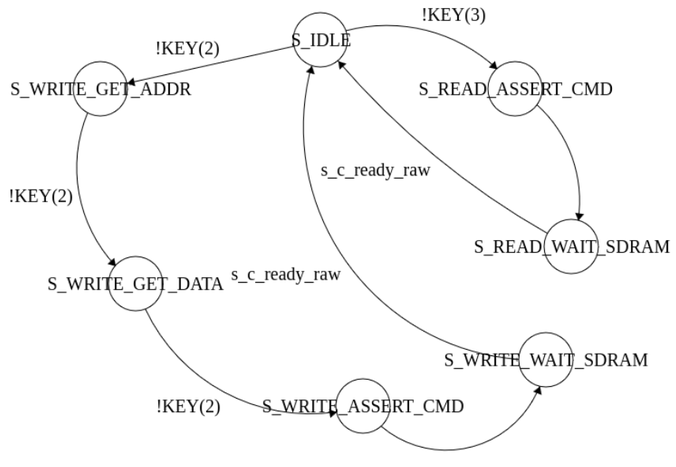
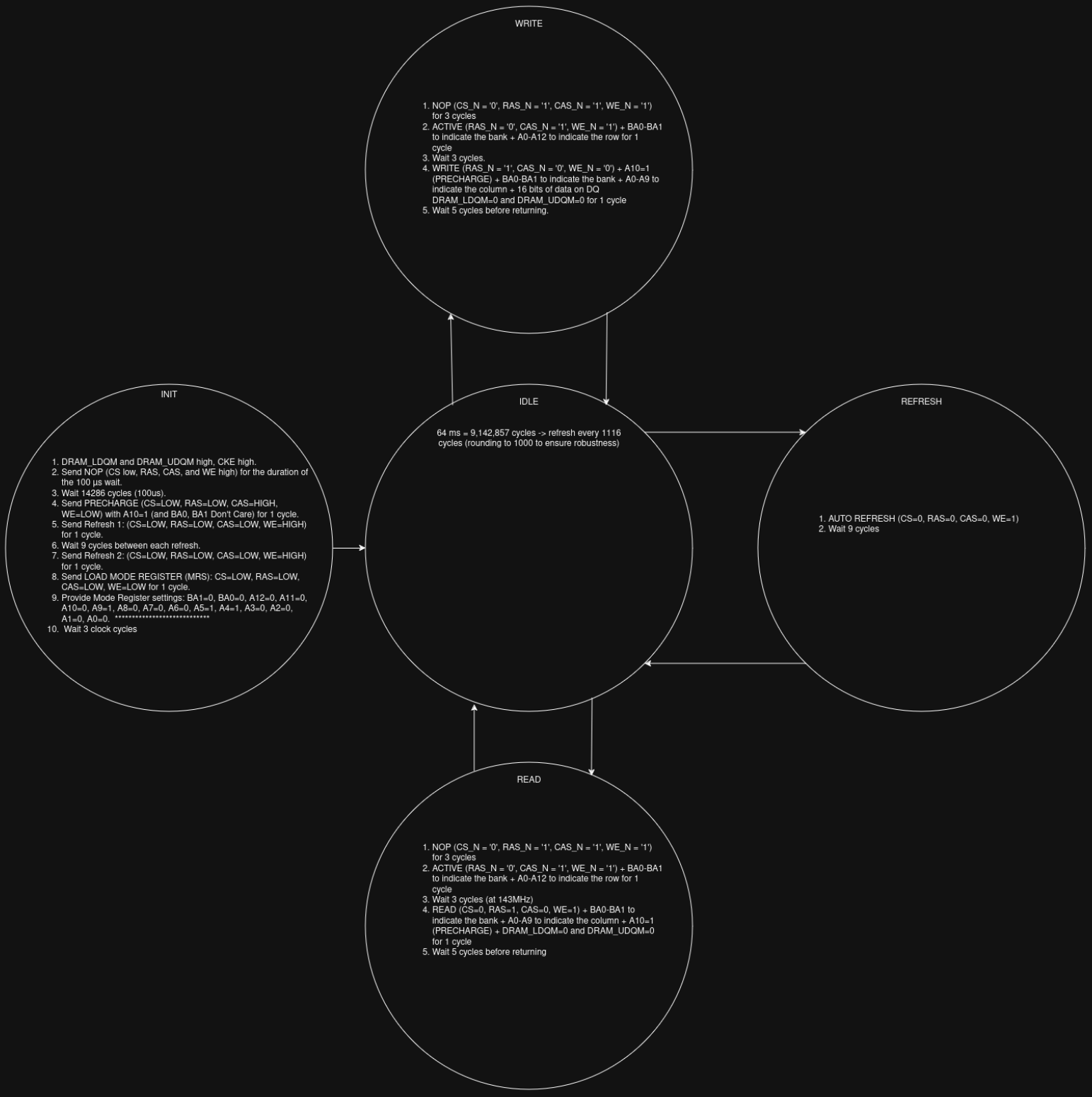
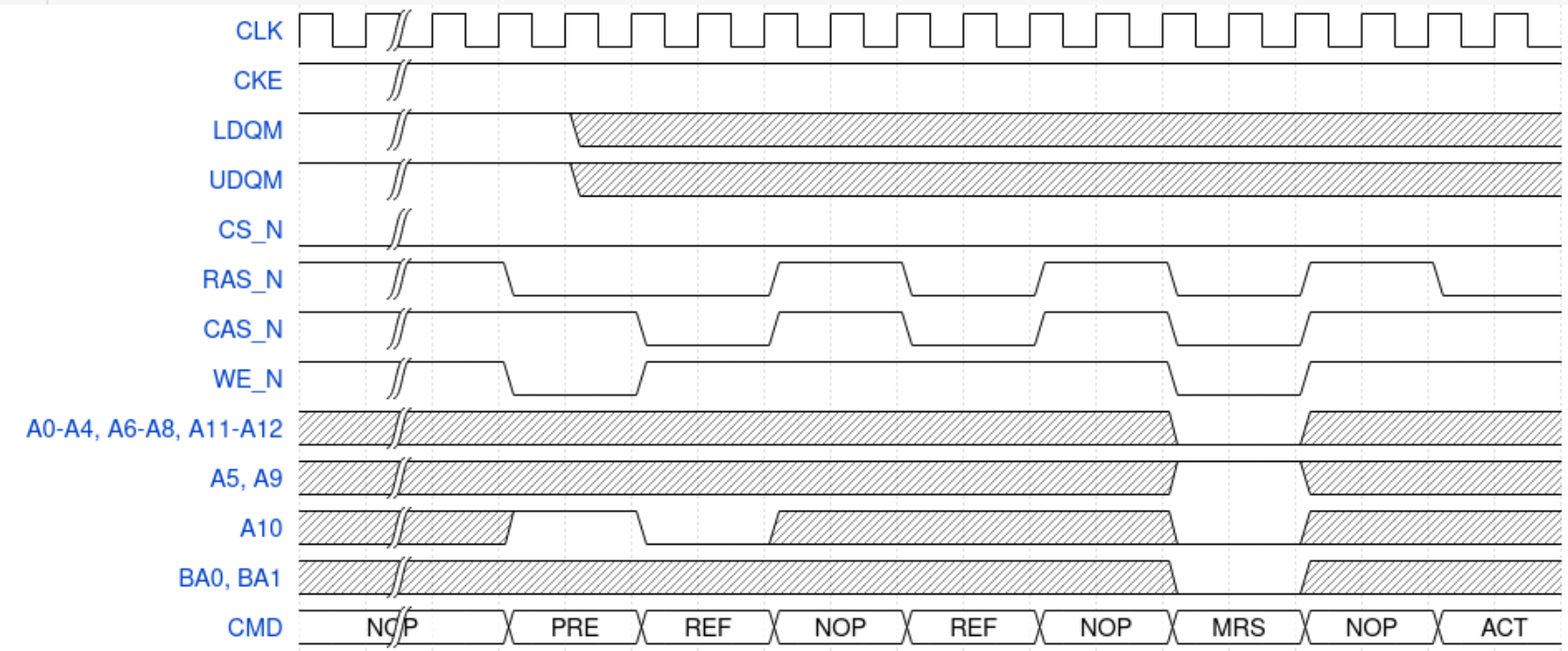

CLOCK_50
SW[9:0]
KEY[3:0]
DRAM_DQ[15:0]
dependendo do estado da máquina, SW representam dado ou endereço
MUX
C_ADDR_IN
C_DATA_IN
SDRAM_CTRL
unsigned_to_7seg
HEX5[6:0]
HEX4[6:0]
HEX3[6:0]
HEX2[6:0]
HEX1[6:0]
HEX0[6:0]
DRAM_DQ[15:0]
DRAM_ADDR[12:0]
DRAM_BA[1:0]
DRAM_CLK
DRAM_CKE
DRAM_LDQM
DRAM_UDQM
DRAM_WE_N
DRAM_CAS_N
DRAM_RAS_N
DRAM_CS_N
PLL
50MHz
143MHz


S_IDLE
!KEY(3)
!KEY(2)
S_WRITE_GET_ADDR
S_READ_ASSERT_CMD
s_c_ready_raw
!KEY(2)
S_READ_WAIT_SDRAM
S_WRITE_GET_DATA
s_c_ready_raw
S_WRITE_WAIT_SDRAM
!KEY(2)
S_WRITE_ASSERT_CMD


WRITE
1. NOP (CS_N = '0', RAS_N = '1', CAS_N = '1', WE_N = '1') for 3 cycles
2. ACTIVE (RAS_N = '0', CAS_N = '1', WE_N = '1') + BA0-BA1 to indicate the bank + A0-A12 to indicate the row for 1 cycle
3. Wait 3 cycles.
4. WRITE (RAS_N = '1', CAS_N = '0', WE_N = '0') + A10=1 (PRECHARGE) + BA0-BA1 to indicate the bank + A0-A9 to indicate the column + 16 bits of data on DQ DRAM_LDQM=0 and DRAM_UDQM=0 for 1 cycle
5. Wait 5 cycles before returning.
INIT
1. DRAM_LDQM and DRAM_UDQM high, CKE high.
2. Send NOP (CS low, RAS, CAS, and WE high) for the duration of the 100 µs wait.
3. Wait 14286 cycles (100us).
4. Send PRECHARGE (CS=LOW, RAS=LOW, CAS=HIGH, WE=LOW) with A10=1 (and BA0, BA1 Don't Care) for 1 cycle.
5. Send Refresh 1: (CS=LOW, RAS=LOW, CAS=LOW, WE=HIGH) for 1 cycle.
6. Wait 9 cycles between each refresh.
7. Send Refresh 2: (CS=LOW, RAS=LOW, CAS=LOW, WE=HIGH) for 1 cycle.
8. Send LOAD MODE REGISTER (MRS): CS=LOW, RAS=LOW, CAS=LOW, WE=LOW for 1 cycle.
9. Provide Mode Register settings: BA1=0, BA0=0, A12=0, A11=0, A10=0, A9=1, A8=0, A7=0, A6=0, A5=1, A4=1, A3=0, A2=0, A1=0, A0=0. **********
10. Wait 3 clock cycles
IDLE
64 ms = 9,142,857 cycles -> refresh every 1116 cycles (rounding to 1000 to ensure robustness)
REFRESH
1. AUTO REFRESH (CS=0, RAS=0, CAS=0, WE=1)
2. Wait 9 cycles
READ
1. NOP (CS_N = '0', RAS_N = '1', CAS_N = '1', WE_N = '1') for 3 cycles
2. ACTIVE (RAS_N = '0', CAS_N = '1', WE_N = '1') + BA0-BA1 to indicate the bank + A0-A12 to indicate the row for 1 cycle
3. Wait 3 cycles (at 143MHz)
4. READ (CS=0, RAS=1, CAS=0, WE=1) + BA0-BA1 to indicate the bank + A0-A9 to indicate the column + A10=1 (PRECHARGE) + DRAM_LDQM=0 and DRAM_UDQM=0 for 1 cycle
5. Wait 5 cycles before returning

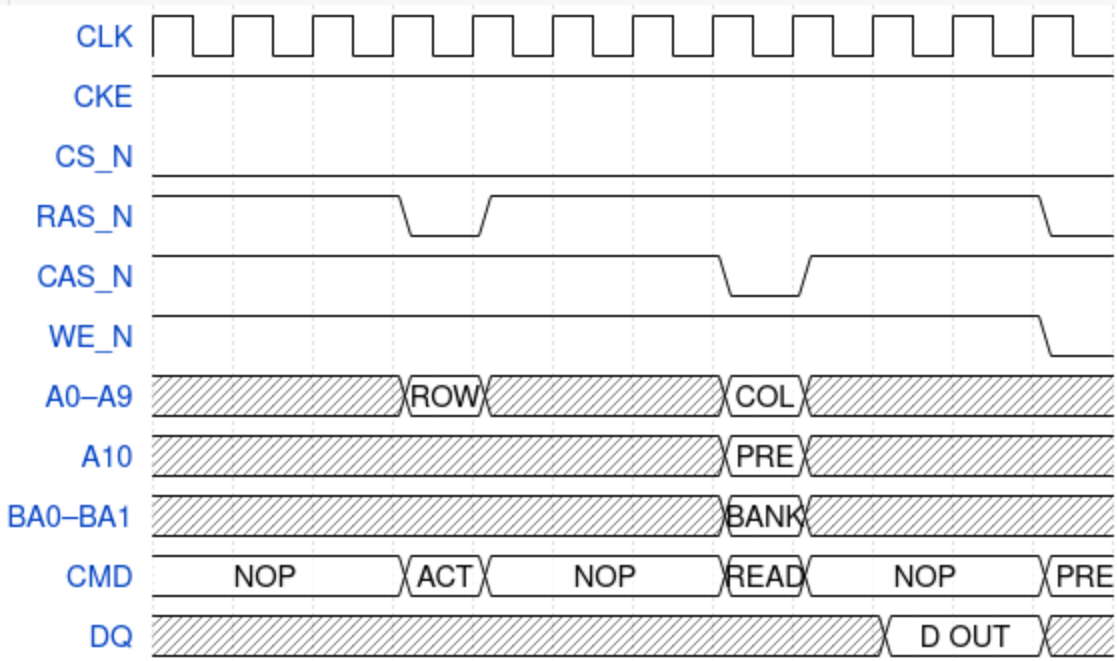
```
{ signal: [
    { name: "CLK",                    wave: "p|..............." },
    { name: "CKE",                    wave: "1|..............." },
    { name: "LDQM",                   wave: "1|..xxxxxxxxxxxxxx" },
    { name: "UDQM",                   wave: "1|..xxxxxxxxxxxxxx" },
    { name: "CS_N",                   wave: "0|..............." },
    { name: "RAS_N",                  wave: "1|.0...1.0.1.0.1.0." },
    { name: "CAS_N",                  wave: "1|...0.1.0.1.0.1..." },
    { name: "WE_N",                   wave: "1|.0.1.......0.1..." },
    { name: "A0-A4, A6-A8, A11-A12",  wave: "x|..........0.x..." },
    { name: "A5, A9",                 wave: "x|..........1.x..." },
    { name: "A10",                    wave: "x|.1.0.x.....0.x..." },
    { name: "BA0, BA1",               wave: "x|..........0.x..." },
    { name: "CMD",                    wave: "=|.=.=.=.=.=.=.=.=.",
      data: [ "NOP", "PRE", "REF", "NOP", "REF", "NOP", "MRS", "NOP", "ACT"]
    }
]}
```

INIT



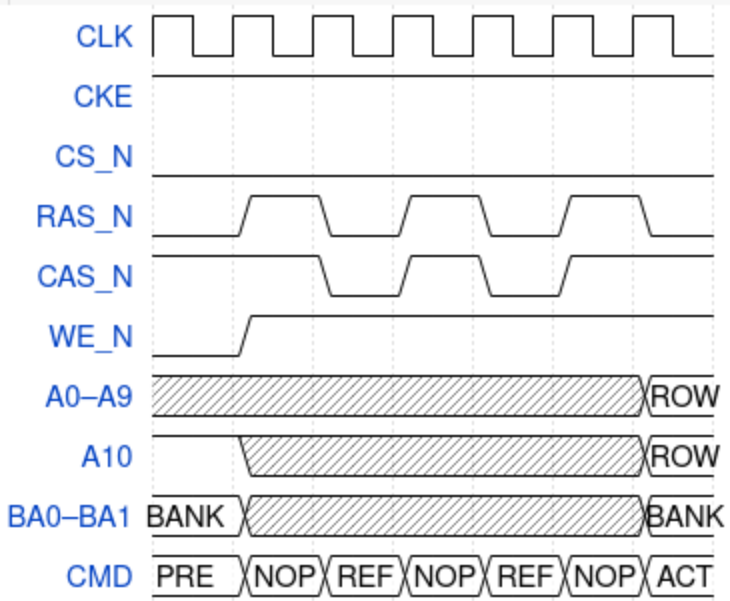
READ

```
{ signal: [
  { name: "CLK",     wave: "p.........." },
  { name: "CKE",     wave: "1.........." },
  { name: "CS_N",    wave: "0.........." },
  { name: "RAS_N",   wave: "1..01......0" },
  { name: "CAS_N",   wave: "1......01..." },
  { name: "WE_N",    wave: "1.........0" },
  { name: "A0-A9",   wave: "xxx=xxx=xxxx", data: ["ROW", "COL"] },
  { name: "A10",     wave: "xxxxxxx=xxxx", data: ["PRE"] },
  { name: "BA0-BA1",wave: "xxxxxxx=xxxx", data: ["BANK"] },
  { name: "CMD",     wave: "=..==..==..=", data: ["NOP", "ACT", "NOP", "READ","NOP","PRE"]},
  { name: "DQ",      wave: "x........=.x", data: ["D OUT"]}
]}
```



REFRESH

```
{ signal: [
  { name: "CLK",     wave: "p......" },
  { name: "CKE",     wave: "1......" },
  { name: "CS_N",    wave: "0......" },
  { name: "RAS_N",   wave: "0101010" },
  { name: "CAS_N",   wave: "1.0101." },
  { name: "WE_N",    wave: "01....." },
  { name: "A0-A9",   wave: "xxxxxx=", data: ["ROW"] },
  { name: "A10",     wave: "1xxxxx=", data: ["ROW"] },
  { name: "BA0-BA1",wave: "=xxxxx=", data: ["BANK", "BANK"] },
  { name: "CMD",     wave: "=======", data: ["PRE", "NOP", "REF", "NOP","REF","NOP", "ACT"]}
]}
```



WRITE

```
{ signal: [
  { name: "CLK",     wave: "p.........." },
  { name: "CKE",     wave: "1.........." },
  { name: "CS_N",    wave: "0.........." },
  { name: "RAS_N",   wave: "1..01......0" },
  { name: "CAS_N",   wave: "1......01..." },
  { name: "WE_N",    wave: "1......01..0" },
  { name: "A0-A9",   wave: "xxx=xxx=xxxx", data: ["ROW", "COL"] },
  { name: "A10",     wave: "xxxxxxx=xxxx", data: ["PRE"] },
  { name: "BA0-BA1",wave: "xxxxxxx=xxxx", data: ["BANK"] },
  { name: "CMD",     wave: "=..==..==..=", data: ["NOP", "ACT", "NOP", "WRITE","NOP","PRE"]},
  { name: "DQ",      wave: "x......=x...", data: ["D IN"]}
]}
```