Fabrication of Patterned Gate Devices for High-Resolution Scanning Tunneling Microscopy

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Abstract

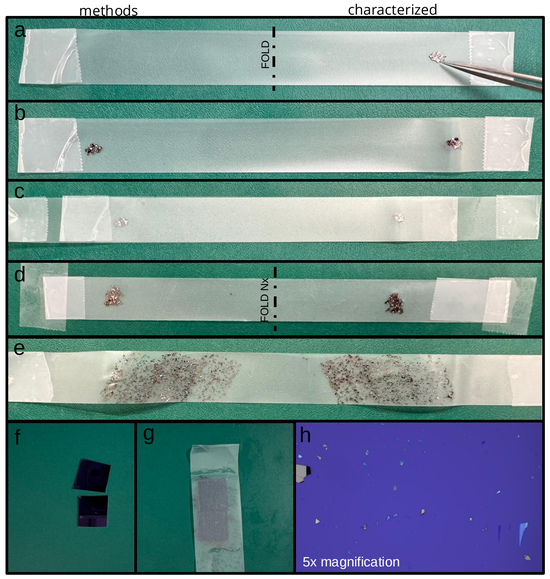
High-Resolution Scanning Tunneling Microscopy is used to image novel quantum states in the spectra of strongly-correlated materials. Here the design and fabrication of a micro-scale device engineered to allow the imaging of strongly-correlated states in monolayer graphene (MLG) is presented. The device is designed as a layered hetero-structure comparable to a traditional layered transistor; the hetero-structure is composed of graphite gates, insulating hexagonal BN layers and an active layer of MLG. In particular, the central graphite gate is etched using the Electrode Free Local Anodic Oxidation (EFLAO) method in the AFM; this etched 'patterned gate' serves to control the local potential felt by the carriers in the active MLG layer. The patterned gate (PG) used in the presented device is designed with nanopores with diameters on the order of ~100nm. When a strong out-of-plane magnetic field is applied, the charge carriers in the MLG layer are forced into Landau levels and are thus strongly-correlated; the PG is then used to trap quasiparticles. Finally, the STM is used to image novel quantum states such as those exhibiting the Fractional Quantum Hall Effect (FQHE).

Mechanical Exfoliation

- Flakes are prepared using Mechanical Exfoliation method.
- Pure samples of material are placed on 'scotch tape', folded and refolded repeatedly to cleave the materials to the desired thickness.

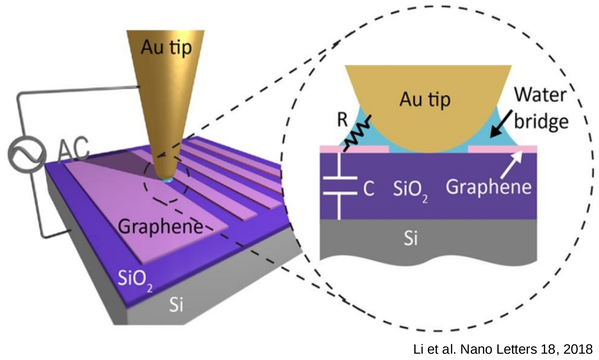
Pros:
- Easy/Cheap
- Cleaner results than other methods

Cons:
- Difficult to control
- Flakes must be manually characterized



a-b) Creation of the 'mother' tape.
c) Creation of a 'daughter' tape.
d-e) Folding a daughter tape repeatedly leaves a field of very thin cleaved graphite on the tape.
f-g) Prepared Si/SiO_2 chips covered with daughter tapes.
h) Resulting graphite flakes of various sizes along with glue residue on Si/SiO_2 chips seen at 5x magnification.

Patterned Gate Fabrication



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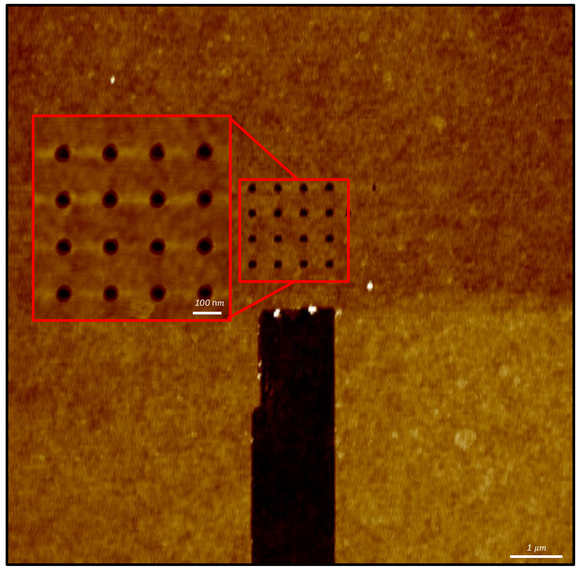
- High-frequency AC is applied through a DI water bridge from a conducting AFM tip (Cathode) to a SiO_2/Si chip (Anode).
- The flake of material between the Anode and Cathode is etched away in the path required for the device design.

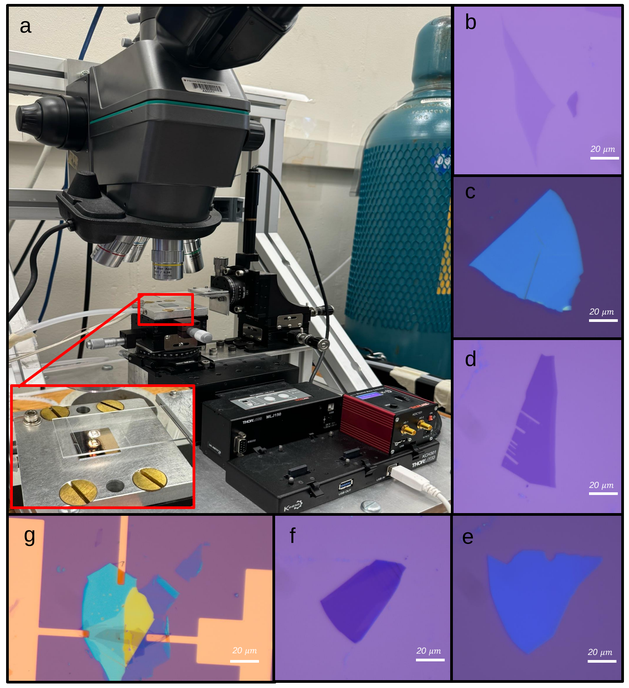
Etching Tuning Knobs:
- Applied AC frequency
- Applied tip voltage
- Size of water bridge (RH%)
- Thickness of SiO_2 layer
- Thickness of flake to be etched



- Wide channels etched into flake allow for STM tip navigation towards nanopore array
- Variable pore profile is a result of nearing the limit of accuracy with etching path
- Debris from etching is a large source of disorder, along with tape residue from mechanical exfoliation

Device Assembly

- Individual flakes are picked up using a sticky PVA polymer 'handle' on a glass slide, controlled by a motorized transfer stage.
- The pickup of each flake is meticulously controlled w.r.t temperature and timing. This reduces the chance of destroying the flake.
- Pickup order: 1- MLG, 2- Thick hBN, 3-PG, 4-Thin hBN, 5-BG
- Once picked up, the stack is placed on a pre-patterned gold chip. The resulting stack is covered in glue and debris and must be washed before measurements can be taken.



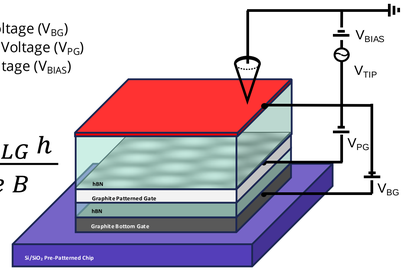
a) The transfer stage, loaded with the pickup handle and a target flake on a Si/SiO_2 chip. The inset shows a closeup view of the handle and chip on the stage. a-g) show 50x optical microscope images of:
b) Monolayer Graphene
c) Thin hexagonal Boron Nitride
d) Pattern Gate (PG) graphite, etched by EFLAO process
e) Thick hexagonal Boron Nitride
f) Bottom Gate (BG) graphite.
g) Device – contact on of the Au pre-patterned Si/SiO_2 chip.

- After successful placement onto the pre-patterned chip, the device is washed and mounted into the sample holder.
- The sample holder is then installed into the STM and prepared for imaging.
- Control voltages are supplied to the relevant device layers through the pre-patterned chip.

Measurement Setup

- Bottom Gate Voltage (V_{BG})
- Patterned Gate Voltage (V_{PG})
- STM tip Bias Voltage (V_{BIAS})

$$\nu = \frac{n_{MLG}\, h}{e\, B}$$



- High-Resolution STM measurements are performed on the sample under UHV conditions.
- Temperature is kept low at 1.4 K.
- Magnetic fields of up to 6 T are applied in the z-direction to force carriers in the active layer into **Landau Levels (LL)**

High-Resolution Tunneling Microscopy:

- Landau Level Spectroscopy: V_{BG} (drives active layer carrier density) is held fixed while V_{PG} (drives active layer carrier energy) and V_{BIAS} (between tip and sample) are swept and dI/dV is measured.
- dI/dV is proportional to the Local Density of States (LDOS). Calculation of ν (filling factor) necessary to determine presence of Fractional or Integer Quantum Hall states etc.

- Evolution of Localized States: Additional spectra of trapped/localized states taken by measuring Bias Voltage w.r.t position and the resulting dI/dV.
  - Spectra taken at sequential BG voltages shows evolution of the trapped state(s).

- Constant Current Topography: Tunneling current between the STM tip and the sample surface is held constant while the STM tip feedback loop varies z-offset distance. This distance is mapped in the scan area to get a topographical map.

Outlook

- The subject of this poster, device VF-24, will be installed in the STM once the current measurement cycle is completed.
- The nanopore arrays will be measured in the hopes that a quasiparticle state trapped in the array will exhibit novel physics. Ideally, a fractional charge quasiparticle state will be trapped.