# FEATURES

* Ultra Low Quiescent Power Dual output 8 phase (8+0/7+1/ 6+2) PWM Controller
* VR12 Rev 1.7, VR12.5 Rev 1.5, IMVP8 Rev 1.2, AMD

SVI2, and Memory VR modes

* Switching frequency from 194KHz to 2MHz per phase in 56 steps
* IR Efficiency Shaping Features including Dynamic Phase Control and Automatic Power State Switching
* Programmable 1-phase or 2-phase operation for Light Loads and Active Diode Emulation for very Light Loads
* IR Adaptive Transient Algorithm (ATA) on both loops minimizes output bulk capacitors and system cost
* Auto-Phase Detection with PID Coefficient auto- scaling
* Fault Protection: OVP, UVP, OCP, OTP, CAT\_FLT
* I2C/SMBus/PMBus system interface for reporting of Temperature, Voltage, Current & Power telemetry for both loops
* Multiple Time Programming (MTP) with integrated charge pump for easy non-volatile programming
* Compatible with 3.3V tri-state drivers

 +3.3V supply voltage; -40oC to 85oC ambient operation; -40oC to 125oC junction

* Pb-Free, RoHS, 7x7mm 56-pin, 0.4mm pitch QFN

# APPLICATIONS

* VR12, VR12.5 and IMVP8 (overclocking only), AMD SVI2 based systems
* Servers and High End Desktop CPU VRs
* High Performance Graphics Processors, Memory VR

# DESCRIPTION

The IR35201 is a dual-loop digital multi-phase buck controller designed for CPU voltage regulation, and is fully compliant with Intel®, VR12 Rev 1.7, VR12.5 Rev 1.5, IMVP8**2** Rev 1.2, and

AMD SVI2 REV 1.06 specifications.

The IR35201 includes IR’s Efficiency Shaping Technology to deliver exceptional efficiency at minimum cost across the entire load range. IR’s Dynamic Phase Control adds/drops phases based upon load current. The IR35201 can be configured to enter 1 or 2-phase PS1 operation and active diode emulation mode automatically or by command.

IR’s unique Adaptive Transient Algorithm (ATA), based on proprietary non-linear digital PWM algorithms, minimizes output bulk capacitors.

IR35201 has 127 possible address values for both the PMBus and I2C bus interfaces. The device configuration can be easily defined using the IR PowIRCenter GUI, and is stored in the on-chip Non-Volatile Memory (NVM). This reduces external components and minimizes the package size.

The IR35201 provides extensive OVP, UVP, OCP, OTP & CAT\_FLT fault protection, and includes thermistor based temperature sensing or per phase temperature reporting when using the IR powIRstage. The controller is designed to work with either Rdson current sense PowIRstages or with DCR current sense.

The IR35201 also includes numerous VR design simplifying and differentiating features, like register diagnostics, which enable fast time-to-market.

# ORDERING INFORMATION

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Base Part Number** | **Package Type** | **Standard Pack** | | **Orderable Part Number** |
| Form | Quantity |
| [IR35201](http://www.irf.com/) | 56-pin, QFN 7 mm x 7 mm | Tape and Reel | 3000 | IR35201MxxyyTRP1 |
| [IR35201](http://www.irf.com/) | 56-pin, QFN 7 mm x 7 mm | Tape and Reel | 3000 | IR35201MTRPBF |
| [IR35201](http://www.irf.com/) | 56-pin, QFN 7 mm x 7 mm | Tray | 4900 | IR35201MTYPBF |

**Notes:**

* 1. Customer Specific Configuration File, where xx = Customer ID and yy = Configuration File (Codes assigned by IR Marketing).
  2. IR35201 is not intended for application where ultra low power PS4 shutdown functionality is required.

[www.irf.com](http://www.irf.com/) | © 2016 International Rectifier February 8, 2015 | V1.6

**1**

# ORDERING INFORMATION



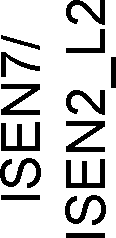
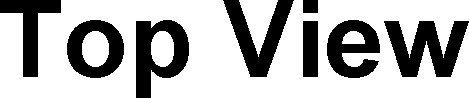
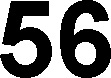
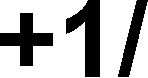
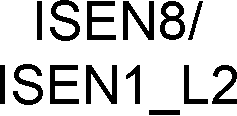
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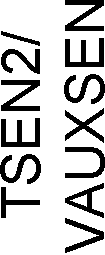


**P/PBF** – Lead Free

**TR** – Tape & Reel / **TY** - Tray

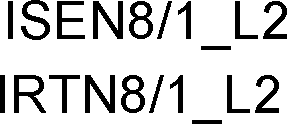
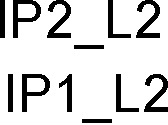
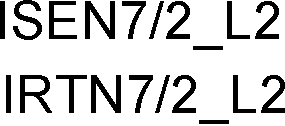
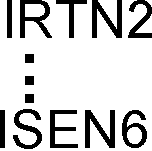
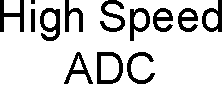
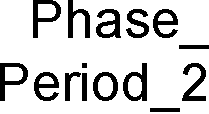
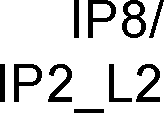
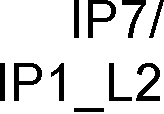
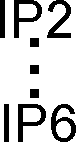
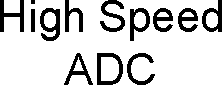
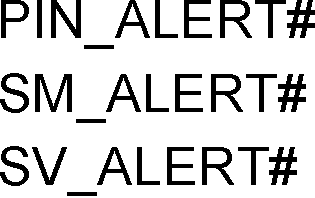
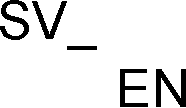
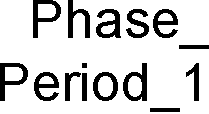
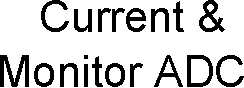
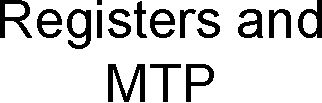
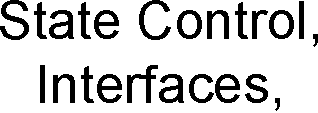
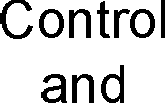
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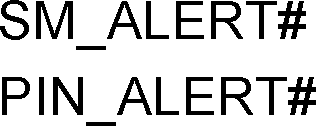
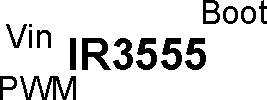
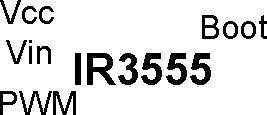
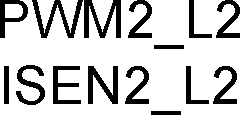
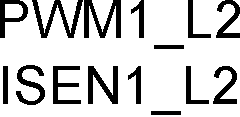
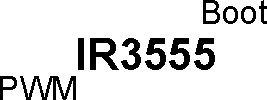
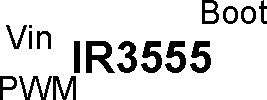
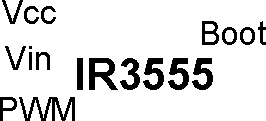
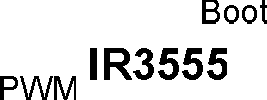
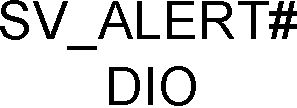
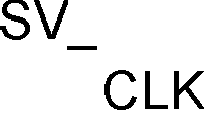
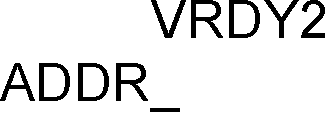
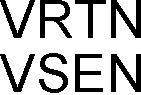
**Figure 1: IR35201 Pin Diagram**

# FUNCTIONAL BLOCK DIAGRAM



**Figure 2: IR35201 Block Diagram**

# TYPICAL APPLICATION DIAGRAM



**V**

**V**

**V V**

**V**

**V**



**Figure 3: VR using IR35201 Controller and IR3555 PowIR Stage in 6+2 Configuration**

# PIN DESCRIPTIONS

|  |  |  |  |
| --- | --- | --- | --- |
| PIN# | PIN NAME | TYPE | PIN DESCRIPTION |
| 1 | ISEN6 | A [I] | **Phase 6 Current Sense Input.** Phase 6 sensed current input (+).Short to GND if not used. |
| 2 | RCSP | A [O] | **Resistor Current Sense Positive.** This pin is connected to an external network to set the load line slope, bandwidth and temperature compensation for Loop 1. |
| 3 | RCSM | A [O] | **Resistor Current Sense Minus.** This pin is connected to an external network to set the load line slope, bandwidth and temperature compensation for Loop 1. |
| 4 | VRDY2 | D [O] | **Voltage Regulator Ready Output (Loop #2).** Open-drain output that asserts high when the VR has completed soft-start to Loop #2 boot voltage. Pull-up to an external voltage through a resistor. |
| 5 | VSEN | A [I] | **Voltage Sense Input.** This pin is connected directly to the VR output voltage of Loop #1 at the load and should be routed differentially with VRTN. |
| 6 | VRTN | A [I] | **Voltage Sense Return Input.** This pin is connected directly to Loop#1 ground at the load and should be routed differentially with VSEN. |
| 7 | NC |  | **Do Not Connect** |
| 8 | I\_IN | A [I] | **I in.** Input current signal that ranges from 0 to 1.25Vdc indicating a maximum input current of  62.5 Amps. |
| 9 | TSEN1 | A [I] | **Temperature Sense Input Loop 1.** An NTC network or the temperature reporting output from an IR PowIRstage can be connected to this pin to measure temperature for VRHOT and OTP shutdown. When connected to the IR PowIRstage’s temperature output; the scaled input voltage to the controller needs to be at a gain of 4.88mV per degC and an offset of 0.365 Vdc so the controller can correctly report temperature. Typically a 10kohm and 6.49kohm resistive divider is used to accomplish the scaling between the power stage and the controller. |
| 10 | CFILT | A [O] | **1.8V Decoupling.** A 1F capacitor on this pin provides decoupling for the internal 1.8V supply. |
| 11 | VRDY1 | D [O] | **Voltage Regulator Ready Output (Loop #1).** Open-drain output that asserts high when the VR has completed soft-start to Loop #1 boot voltage. Pull-up to an external voltage through a resistor. |
| 12 | EN\_L2 PWROK CAT\_FLT | D[I]  D[I]  D[O] | **Enable Input for Loop #2.** This pin may be configured as an Enable input for loop #2. |
| **Power OK Input (AMD).** An input that when low indicates to return to the Boot voltage and when high indicates to use the SVI bus**.** |
| **Catastrophic Fault Output Pin.** This pin may be used as a Catastrophic Fault CMOS Output Pin that is driven to VCC under output OVP, NVM CRC errors or a TSEN fault input. |
| 13 | NC |  | **Do Not Connect** |
| 14 | VINSEN | A [I] | **Voltage Sense Input.** This is used to detect and measure a valid input supply voltage (typically 4.5V-13.2V) to the VR. |
| 15 | NC |  | **Do Not Connect** |
| 16 | SV\_ADDR VDDIO | A[I]  A[P] | **Serial VID Address.** If present, a resistor to ground sets the offset to the SVID address set in NVM. If not, the value stored in NVM is used. Requires a 0.01µF to ground for noise filtering. |
| **VDDIO Input (AMD).** This pin provides the voltage to which the SVT line and the SVD Acknowledge are driven high. |
| 17 | SV\_ALERT# SVT | D [O] | **Serial VID ALERT# (INTEL).** SVID ALERT# is pulled low by the controller to alert the CPU of new IMVP8/VR12/VR12.5 Status. Pull-up to an external voltage through a resistor. |
| **SVI Telemetry Output (AMD).** Telemetry and VOTF information output by the IR35201 |
| 18 | SV\_CLK | D [I] | **Serial VID Clock Input.** Clock input driven by the CPU Master. |
| 19 | SV\_DIO | D [B] | **Serial VID Data I/O.** Is a bi-directional serial line over which the CPU Master issues commands to slave/s and receives data back. |
| 20 | VRHOT\_ICRIT# | D [O] | **VRHOT\_ICRIT# Output.** Active low alert pin that can be programmed to assert if temperature or average load current exceeds user-definable thresholds. Pull-up to an external voltage through a resistor. |

|  |  |  |  |
| --- | --- | --- | --- |
| PIN# | PIN NAME | TYPE | PIN DESCRIPTION |
| 21 | EN | D [I] | **VR Enable Input.** ENABLE is used to power-on the regulator, provided Vin and Vcc are present. ENABLE is not pulled up in the controller. The polarity of the chip enable function is bit-settable to either an active high or an active low configuration. When the controller is disabled, the controller de-asserts VR READY and shuts down the regulator. ENABLE pin cannot be left  floating. ENABLE pin must be pulled high or low. |
| 22 | ADDR\_PROT | D [B]/ | **Bus Address & I2C Bus Protection.** A resistor to ground on this pin sets the offset to the NVM value of the I2C address if configured to do so. Subsequently, this pin becomes a logic input to enable or disable communication on the I2C bus when protection is enabled. Requires a 0.01µF to ground for noise filtering. |
| 23 | SM\_ALERT# | D [O] | **SMBus/PMBus Alert Line.** Active low alert pin to indicate that the regulator status has changed. Requires a pull-up. Ground if not used. |
| 24 | SM\_DIO | D [B] | **Serial Data Line I/O.** I2C/SMBus/PMBus bi-directional serial data line. Ground if not used. |
| 25 | SM\_CLK | D [I] | **Serial Clock Line Input.** I2C/SMBus/PMBus clock input. The interface is rated to 1 MHz. Ground if not used. |
| 26 | PIN\_ALERT# | D [O] | **PIN\_ALERT# Output.** Active low alert pin that can be programmed to assert if the input power exceeds user-defined threshold. Pull-up to an external voltage through a resistor. |
| 27 | TSEN2  /VAUXSEN | A [O]  A [I] | **Temperature Sense Input Loop #2.** An NTC network or the temperature reporting output from an IR PowIRstage can be connected to this pin to measure temperature for VRHOT. Float if not used. |
| **Auxiliary Voltage Sense Input.** Monitors an additional power supply to ensure that both the IR35201 Vcc and other voltages (such as VCC to the driver) are operational. Float if not used. |
| 28 - 33 | PWM1 – PWM6 | A [O] | **Phase 1-6 Pulse Width Modulation Outputs.** PWM signal pin which is connected to the input of an external MOSFET gate driver. The power-up state is high-impedance until ENABLE goes active. Float if not used. |
| 34 | PWM7/ PWM2\_L2 | A [O] | **Phase 7 Pulse Width Modulation Outputs.** PWM signal pin which is connected to the input of an external MOSFET gate driver. The power-up state is high-impedance until ENABLE goes active. Float if not used. |
| **Loop 2 Phase 2 Pulse Width Modulation Outputs.** PWM signal pin which is connected to the input of an external MOSFET gate driver. The power-up state is high-impedance until ENABLE goes active. |
| 35 | PWM8/ PWM1\_L2 | A [O] | **Phase 8 Pulse Width Modulation Outputs.** PWM signal pin which is connected to the input of an external MOSFET gate driver. The power-up state is high-impedance until ENABLE goes active. Float if not used. |
| **Loop 2 Phase 1 Pulse Width Modulation Outputs.** PWM signal pin which is connected to the input of an external MOSFET gate driver. The power-up state is high-impedance until ENABLE goes active. |
| 36 | VRTN\_L2 | A [I] | **Voltage Sense Return Input Loop#2.** This pin is connected directly to Loop 2 ground at the load and should be routed differentially with VSEN\_L2. Short to GND if not used |
| 37 | VSEN\_L2 | A [I] | **Voltage Sense Input Loop#2.** This pin is connected directly to the VR output voltage of Loop 2 at the load and should be routed differentially with VRTN\_L2. Short to GND if not used |
| 38 | VCC | A [P] | **Input Supply Voltage.** 3.3V supply to power the device. |
| 39 | RCSM\_L2 | A [I] | **Resistor Current Sense Minus Loop#2.** This pin is connected to an external network to set the load line slope, bandwidth and temperature compensation for Loop 2. Connect to RCSP\_L2 with 10K resistor if not used |
| 40 | RCSP\_L2 | A [I] | **Resistor Current Sense Positive Loop#2.** This pin is connected to an external network to set the load line slope, bandwidth and temperature compensation for Loop 2. |
| 41 | NC |  | **Do Not Connect** |
| 42 | ISEN 1\_L2/  ISEN8 | A [I] | **Loop 2 Phase 1 Current Sense Input.** Loop 2 Phase 1 sensed current input (+).Short to GND if not used. |
| **Phase 8 Current Sense Input.** Phase 8 sensed current input (+).Short to GND if not used. |
| 43 | IRTN 1\_L2/ IRTN8 | A [I] | **Loop 2 Phase 1 Current Sense Return Input.** Loop 2 Phase 1 sensed current input return (-).Short to GND if not used. |
| **Phase 8 Current Sense Return Input.** Phase 8 sensed current input return (-).Short to GND if not used. |

|  |  |  |  |
| --- | --- | --- | --- |
| PIN# | PIN NAME | TYPE | PIN DESCRIPTION |
| 44 | ISEN 2\_L2/  ISEN7 | A [I] | **Loop 2 Phase 2 Current Sense Input.** Loop 2 Phase 2 sensed current input (+).Short to GND if not used. |
| **Phase 7 Current Sense Input.** Phase 7 sensed current input (+).Short to GND if not used. |
| 45 | IRTN 2\_L2/ IRTN7 | A [I] | **Loop 2 Phase 2 Current Sense Return Input.** Loop 2 Phase 2 sensed current input return (-).Short to GND if not used. |
| **Phase 7 Current Sense Return Input.** Phase 7 sensed current input return (-).Short to GND if not used. |
| 46 | ISEN 5 | A [I] | **Phase 5 Current Sense Input.** Phase 5 sensed current input (+).Short to GND if not used. |
| 47 | IRTN 5 | A [I] | **Phase 5 Current Sense Return Input.** Phase 5 sensed current input return (-). Short to GND if not used.. |
| 48 | ISEN 4 | A [I] | **Phase 4 Current Sense Input.** Phase 4 sensed current input (+).Short to GND if not used.. |
| 49 | IRTN 4 | A [I] | **Phase 4 Current Sense Return Input.** Phase 4 sensed current input return (-).Short to GND if not used. |
| 50 | ISEN 3 | A [I] | **Phase 3 Current Sense Input.** Phase 3 sensed current input (+).Short to GND if not used. |
| 51 | IRTN 3 | A [I] | **Phase 3 Current Sense Return Input.** Phase 3 sensed current input return (-).Short to GND if not used.. |
| 52 | ISEN 2 | A [I] | **Phase 2 Current Sense Input.** Phase 2 sensed current input (+).Short to GND if not used. |
| 53 | IRTN 2 | A [I] | **Phase 2 Current Sense Return Input.** Phase 2 sensed current input return (-).Short to GND if not used. |
| 54 | ISEN 1 | A [I] | **Phase 1 Current Sense Input.** Phase 1 sensed current input (+).Short to GND if not used. |
| 55 | IRTN 1 | A [I] | **Phase 1 Current Sense Return Input.** Phase 1 sensed current input return (-).Short to GND if not used. |
| 56 | IRTN6 | A [I] | **Phase 6 Current Sense Return Input.** Phase 6 sensed current input return (-).Short to GND if not used.. |
| 57 (PAD) | GND |  | **Ground.** Ground reference for the IC. The large metal pad on the bottom must be connected to Ground. |

**Note 1:** A - Analog; D – Digital; [I] – Input; [O] – Output; [B] – Bi-directional; [P] - Power

# ABSOLUTE MAXIMUM RATINGS

|  |  |
| --- | --- |
| Supply Voltage (VCC) | GND-0.3V to 4.0V |
| RCSPx, RCSMx | 0 to 2.2V |
| VSEN, VRTN, ISENx, IRTNx | GND-0.2V to VCC + 0.3V |
| CFILT, VINSEN, I\_IN | GND-0.2V to 2.2V |
| TSENx | GND-0.3V to VCC |
| SV\_CLK, SV\_DIO, SV\_ALERT#, SV\_ADDR | GND-0.3V to VCC |
| VRDYx, ENx, ADDR\_PROT, VRHOT\_ICRIT#, PIN\_ALERT# | GND-0.3V to VCC |
| PWMx, | GND-0.3V to 4.1V |
| SM\_DIO, SM\_CLK, SM\_ALERT# | GND-0.3V to 5.5V |
| **ESD Rating** | |
| Human Body Model | 2000V |
| Machine Model | 200V |
| Charge Device Model | 1000V |
| **Thermal Information** |  |
| Thermal Resistance (θJA & θJC)1 | 29°C/W & 3°C/W |
| Maximum Operating Junction Temperature | -40°C to +125°C |
| Maximum Storage Temperature Range | -65°C to +150°C |
| Maximum Lead Temperature (Soldering 10s) | 300°C |

**Note:** 1. θJA is measured with the component mounted on a high effective thermal conductivity test board in free air.

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications are not implied.

# ELECTRICAL SPECIFICATIONS

##### RECOMMENDED OPERATING CONDITIONS FOR RELIABLE OPERATION WITH MARGIN

|  |  |
| --- | --- |
| Recommended Operating Ambient Temperature Range | -40°C to 85°C |
| Supply Voltage Range | +2.90V to +3.63V |

The electrical characteristics table lists the spread of values guaranteed within the recommended operating conditions. Typical values represent the median values, which are related to 25°C.

##### ELECTRICAL CHARACTERISTICS

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **PARAMETER** | **SYMBOL** | **CONDITIONS** | **MIN** | **TYP** | **MAX** | **UNIT** |
| **Supply** | **VCC/GND** |  | | | | |
| Supply Voltage | Vcc |  | 2.90 | 3.3 | 3.63 | V |
| Supply Current | Ivcc | No PWM switching | - | 48 | - | mA |
| 3.3V UVLO Turn-on Threshold |  |  | - | 2.80 | 2.90 | V |
| 3.3V UVLO Turn-off Threshold |  |  | 2.60 | 2.70 | - | V |
| **Input Voltage (4.5V-13.2V) Sense Input** | **VINSEN** |  | | | | |
| Input Impedance |  |  | 1 | - | - | MΩ |
| Input Range | V12 | With 14:1 divider | 0 | 0.857 | 1.1 | V |
| UVLO Turn-on Programmable Range**1** |  | With 14:1 divider | - | 4.5 –13.2 | - | V |
| UVLO Turn-off Programmable Range**1** |  | With 14:1 divider | - | 4.5 –13.2 | - | V |
| OVP Threshold (if enabled) **1** |  |  | 14.3 | 14.6 | 14.9 | V |
| **AUX Voltage Sense Input** | **VAUXSEN** |  | | | | |
| Input Impedance1 |  |  | - | 1 | - | MΩ |
| UVLO Turn-on Threshold**1** |  | VAUXSEN\_on | 0.642 | 0.664 | 0.686 | mV |
| UVLO Turn-off Threshold**1** |  | VAUXSEN\_off | 0.564 | 0.586 | 0.608 | mV |
| **Reference Voltage and DAC** | | | | | | |
| VBoot Voltage Range |  | Intel®, VR12.5,VR12and IMVP8 mode, and AMD SVI2 | Meets spec | | | V |
| System Accuracy (0 to 85°C ambient) |  | VID = 2.005–3.04V | -1.1 | - | 1.1 | %VID |
| VID = 1.0V–2.0V | -0.5 | - | 0.5 | %VID |
| VID = 0.8 – 0.995V | -5 | - | 5 | mV |
| VID = 0.25 –0.795V | -8 | - | 8 | mV |
| System Accuracy  (-40°C to 125°C junction) |  | VID = 2.005–3.04V | -1.65 | - | 1.65 | %VID |
| VID = 1.0V–2.0V | -0.75 | - | 0.75 | %VID |
| VID = 0.8 – 0.995V | -7.5 | - | 7.5 | mV |
| VID = 0.25 –0.795V | -12 | - | 12 | mV |
| **Oscillator & PWM Generator** | | | | | | |
| Internal Oscillator1 |  |  | - | 96 | - | MHz |
| Frequency Accuracy |  | 0°C to 85°C | -2.5 | - | 2.5 | % |
| Frequency Accuracy |  | -40°C to 125°C | -5 |  | +5 | % |
| PWM Frequency Range1 |  |  | 194 | - | 2000 | kHz |

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **PARAMETER** | **SYMBOL** | **CONDITIONS MIN** | | **TYP** | **MAX** | **UNIT** |
| PWM Resolution1 |  |  | - | 163 | - | ps |
| **NTC Temperature Sense** | **TSEN\_NTC** |  | | | | |
| Output Current |  | For TSEN = 0 to 1.2V | 96 | 100 | 104 | µA |
| Accuracy1 |  | at 100°C (ideal NTC) | 96 | - | 104 | °C |
| **Tout Temperature Sense** | **TSEN\_IR3555** |  | | | | |
| Input Voltage |  | For TSEN = 0 to 1.2V | - | 4.88 | - | mV/°C |
| Offset Voltage |  |  | - | 0.365 | - | Vdc |
| Fault Threshold |  |  | 1.45 |  |  | Vdc |
| Divider Ratio to interface IR3555 to IR35201 |  |  | - | 1:1.64 | - |  |
| **Digital Inputs – Low Vth Type 1** | **EN(\_L2) (Intel), VRHOT\_ICRIT# (during PoR),** | | | | | |
| Input High Voltage |  |  | 0.7 | **-** | **-** | V |
| Input Low Voltage |  |  | - | - | 0.35 | V |
| Input Leakage Current |  | Vpad = 0 to 2V | - | **-** | ±5 | µA |
| **Digital Inputs – Low Vth Type 2** | **SV\_CLK, SV\_DIO** |  | | | | |
| Input High Voltage |  |  | 0.65 | **-** | **-** | V |
| Input Low Voltage |  |  | - | - | 0.45 | V |
| Hysteresis |  |  | - | 95 | - | mV |
| Input Leakage Current |  | Vpad = 0 to 2V | - | **-** | ±1 | µA |
| **Digital Inputs – LVTTL** | **SM\_DIO, SM\_CLK, EN(\_L2), ADDR\_PROT** | | | | | |
| Input High Voltage |  |  | 2.1 | **-** | **-** | V |
| Input Low Voltage |  |  | - | - | 0.8 | V |
| Input Leakage |  | Vpad = 0 to 3.6V | - | - | ±1 | µA |
| **Remote Voltage Sense Inputs** | **VSENx, VRTNx** |  | | | | |
| VSEN Input Current |  | VCPU = 0.5V to 3.04V | - | -25 to  +100 | - | µA |
| VRTN Input Current |  |  | - | -50 | - | µA |
| Differential Input Voltage Range1 |  | VRTN = ±100mV | - | 0 to 3.04 | - | V |
| VRTN Input CM Voltage1 |  |  | - | -100 to  100 | - | mV |
| **Remote Current Sense Inputs** | **ISENx/IRTNx** |  | | | | |
| Voltage Range1 |  |  | - | -0.1 to  VCC - 0.65 | - | V |
| **Input Current Sense Input** | **I\_IN** |  |  |  |  |  |
| Voltage Range |  |  | - | 0 to 1.25 | - | V |
| **Analog Address/Level Inputs** | **ADDR\_PROT,SV\_ADDR,** | | | | | |
| Output Current1 |  | Vpad = 0 to 1.2V | 96 | 100 | 104 | µA |
| **CMOS Outputs ― 3.3V** | **CAT\_FLT** | | | | | |
| Output High Voltage |  | loh = -20mA | VCC – 0.4 | - | - | V |
| Output Low Voltage |  | lol = 20mA | - | - | 0.4 | V |
| **Open-Drain Outputs – 4mA Drive** | **VRDY, SM\_DIO, SM\_ALERT#** | | | | | |
| Output Low Voltage |  | 4mA | - | - | 0.3 | V |

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **PARAMETER** | **SYMBOL** | | **CONDITIONS MIN** | | | **TYP** | **MAX** | **UNIT** |
| Output Leakage |  | | Vpad = 0 to 3.6V | - | | - | ±5 | µA |
|  | | | | | | | | |
| **Open-Drain Outputs – 20mA Drive** | | **VR\_HOT\_ICRIT#, SV\_DIO, SV\_ALERT#, PIN\_ALERT#** | | | | | | |
| Output Low Voltage1 | |  | I = 20mA | - | | - | 0.26 | V |
| On Resistance1 | |  | I = 20mA | 7 | | 9 | 13 | Ω |
| Tri-State Leakage | | Ileak | Vpad = 0 to 3.6V | - | | - | ±5 | µA |
| **PWM I/O** | | **PWMx** |  | | | | | |
| Output Low Voltage (Tri-state mode) | |  | I = -4mA | - | | - | 0.4 | V |
| Output High Voltage (Tri-State mode) | |  | I =+4mA | 2.9 | | - | - | V |
| Tri-State Leakage | |  | loop\_x\_pwm\_en\_ats = 0, Vpad = 0 to Vcc | - | | - | ±1 | µA |
| **PWM Auto-Detect Inputs (when 3.3V Vcc is applied) – if enabled** | | | | | | | | |
| Input Voltage High | |  |  | | 0.7 | - | - | V |
| Input Voltage Low | |  |  | | - | - | 0.35 | V |
| **AMD SVI2 Bus** | | | | | | | | |
| Tperiod (SVC Period)1 | | SVC |  | | 47.6 |  | 10,000 | nSec |
| SVI2 SVC Frequency1 | | SVC |  | | 0.1 | 20.0 | 21.0 | MHz |
| **I2C/PMBus & Reporting** | | | | | | | | |
| Bus Speed1 | |  | Normal | | - | 100 | - | kHz |
| Fast | | - | 400 | - | kHz |
| Maximum | | - | 1000 | - | kHz |
| Iout , Vout , Iin, Vin, Pin and Temperature Filter Rate1 | |  | Selectable  (Selected Frequency applies to all parameters) | | - | 0.69, 1.39,  2.78, 5.55,  11.1, 22.2,  44.6, 89.5 | - | Hz |
| Iout Update Rate1 | |  |  | | - | 250 | - | kHz |
| Vout Update Rate1 | |  |  | | - | 35.7 | - | kHz |
| Vin & Temperature Update Rate1 | |  |  | | - | 35.7 | - | kHz |
| Vin Range Reporting1 | |  | With 14:1 divider | | - | 0 to 13.2 | - | V |
| Vin Accuracy Reporting | |  | With 1% resistors | | -2 | - | +2 | % |
| Vin Resolution Reporting -PMBUS1 | |  |  | | - | 31.25 | - | mV |
| Vin Resolution Reporting –I2C1 | |  |  | | - | 125 | - | mV |
| Vout Range Reporting1 | |  |  | | - | - | 4 | V |
| Vout Accuracy Reporting1 | |  | No load-line | |  | ±0.5 |  | % |
| Vout Resolution Reporting-PMBUS1 | |  | Vout < 2V | | - | 1.95 | - | mV |
| Vout Resolution Reporting-I2C1 | |  | Vout < 4V | | - | 15.6 | - | mV |
| Iout Per Phase Range Reporting**1** | |  |  | | 0 | - | 62 | A |
| Iout Accuracy Reporting1 | |  | Maximum load, all phase active (based on DCR, NTC and # active phases) | | - | ±2 | - | % |
| Loop1 Iout Resolution Reporting-PMBUS 1 | |  | \*0.5A if >255.75A | | - | 0.25\* | - | A |
| Loop2 Iout Resolution Reporting-PMBUS 1 | |  |  | | - | 0.25 | - | A |
| Loop1 Iout Resolution Reporting-I2C 1 | |  |  | | - | 1 | - | A |
| Loop2 Iout Resolution Reporting-I2C 1 | |  |  | | - | 0.5 | - | A |
| Loop1 Iin Resolution Reporting-PMBUS 1 | |  |  | | - | 31.25 | - | mA |

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **PARAMETER SYMBOL** | | **CONDITIONS MIN** | | **TYP** | **MAX** | **UNIT** |
| Loop2 Iin Resolution Reporting-PMBUS 1 |  |  | - | 31.25 | - | mA |
| Loop1 Iin Resolution Reporting-I2C1 |  |  | - | 0.125 | - | A |
| Loop2 Iin Resolution Reporting-I2C1 |  |  | - | 0.0625 | - | A |
| P\_in Resolution Reporting-PMBUS1 |  |  | - | 0.5 | - | W |
| P\_out Resolution Reporting-PMBUS1 |  |  | - | 0.5 | - | W |
| Temperature Range Reporting1 |  | IR3555 mode | 0 | - | 158 | °C |
| Temperature Accuracy Reporting1 |  | IR3555 mode | 3.5 | - | 3.5 | % |
| Temperature Range Reporting**1** |  |  | 0 | - | 134 | °C |
| Temperature Accuracy Reporting1 |  | At 100°C, with ideal NTC | -4 | - | 4 | % |
| Temperature Resolution Reporting1 |  |  | - | 1 | - | °C |
| **Fault Protection** | | | | | | |
| OVP Threshold During Start-up (until output reaches 1V) |  | Selectable | - | 1.2, 1.275,  1.35, 2.5 | - | V |
| OVP Operating Threshold**1** (programmable) |  | Relative to VID | - | 50 to 400 | - | mV |
| OVP Filter Delay**1** |  |  | - | 160 | - | ns |
| Output UVP Threshold**1** (programmable) |  | Relative to VID | - | 50 to 400 | - | mV |
| Fast OCP Range (per phase)1 |  |  | - | 0 to 62 | - | A |
| Fast OCP Filter Bandwidth**1** |  |  | - | 60 | - | kHz |
| Slow OCP Filter Bandwidth**1** |  | Selectable | - | 0.69, 1.39,  2.78, 5.55,  11.1, 22.2,  44.6, 89.5 | - | Hz |
| OCP System Accuracy**1** |  | System excluding DCR/sense resistor | - | ±2 | - | % |
| PIN\_ALERT# Bandwidth |  |  |  | 2000 |  | Hz |
| VR\_HOT Range**1** |  |  | - | 64 to 127 | - | °C |
| OTP Range1, 2 |  | OTP Range (added to VR\_HOT level) | - | 0 to 31 | - | °C |
| **Dynamic Phase Control** | | | | | | |
| Current Filter Bandwidth**1** |  | For Phase drop | - | 4 | - | kHz |
| **Timing Information** | | | | | | |
| Automatic Configuration from MTP**1** | t3-t2 | 3.3V ready to end of configuration | - | 0.4 |  | ms |
| Automatic Trim Time**1** | t4-t3 |  | - | 2 |  | ms |
| EN Delay (to ramp start) **1** |  |  | - | 3 | - | µs |
| VID Delay (to ramp start) **1** |  | Loop bandwidth dependent | - | 5 | - | µs |
| VRDY Delay**1** |  | After reaching Boot voltage | - | 20 | - | µs |

**Notes:**

1 Guaranteed by design.

2 OTP max setting with NTC TEMP SENSE is 134°C.

**8+0/7+1/6+2 Dual Output Digital Multi-Phase Controller**

# GENERAL DESCRIPTION



**IR35201**

The IR35201 is a flexible, dual-loop, digital multiphase PWM buck controller optimized to convert a 12V input supply to the core voltage required by Intel high performance microprocessors and DDR memory. It is easily configurable for 1 to 8 phases of operation on Loop #1 and 0 to 2 phase operation on Loop #2.

However, at a single time, a total of only 8 phases can be in operation.

The unique partitioning of analog and digital circuits within the IR35201 provides the user with easy configuration capability while maintaining the required accuracy and performance. Access to on-chip Multiple Time Programming memory (MTP) to store the IR35201 configuration parameters enables power supply designers to optimize their designs without changing external components.

### OPERATING MODES

The IR35201 can be used for Intel® VR12, VR12.5, IMVP8 designs, AMD SVI2, and DDR Memory designs without significant changes to the external components (Bill of Materials). The required mode is selected in MTP and the pin-out, VID table and relevant functions are automatically configured. This greatly reduces time-to-market and eliminates the need to manage and inventory different PWM controllers.

### DIGITAL CONTROLLER & PWM

A linear Proportional-Integral-Derivative (PID) digital controller provides the loop compensation for system regulation. The digitized error voltage from

the high-speed voltage error ADC is processed by the digital compensator. The digital PWM generator uses the outputs of the PID and the phase current balance control signals to determine the pulse width for

each phase on each loop. The PWM generator has enough resolution to ensure that there are no limit cycles. The compensator coefficients are user configurable to enable optimized system response. The compensation algorithm uses a PID with two additional programmable poles. This provides the digital equivalent of a Type III analog compensator.

### ADAPTIVE TRANSIENT ALGORITHM (ATA)

Dynamic load step-up and load step-down transients require fast system response to maintain the output voltage within specification limits. This is achieved by a unique adaptive non-linear digital transient control loop based on a proprietary algorithm.

### MULTIPLE TIME PROGRAMMING MEMORY

The multiple time programming memory (MTP) stores the device configuration. At power-up, MTP contents are transferred to operating registers for access during device operation. MTP allows customization during both design and high-volume manufacturing. MTP integrity is verified by Cyclic Redundancy Code (CRC) checking on each power up. The controller will not start up in the event of a CRC error.

The IR35201 offers up to 6 writes to configure basic device parameters such as frequency, fault operation characteristics, and boot voltage. This represents a significant size and component saving compared to traditional analog methods. The following pseudo- code illustrates how to write the MTP:

*# write data*

*Set MTP Command Register = WRITE, Line Pointer = An unused line*

*Poll MTP Command Register until Operation = IDLE.*

*# verify data was written correctly*

*Issue a READ Command; then poll OTP Operation Register till Operation = IDLE*

*Verify that the Read Succeeded*

### INTERNAL OSCILLATOR

The IR35201 has a single 96MHz internal oscillator that generates all the internal system clock frequencies required for proper device function. The oscillator frequency is factory trimmed for precision, and has extremely low jitter ([Figure 4](#_bookmark0)) even in light- load mode ([Figure 5](#_bookmark1)). A single internal oscillator is used to set the switching frequency on each loop independently.

#### 8+0/7+1/6+2 Dual Output Digital Multi-Phase Controller



**Vdd**

**IR35201**



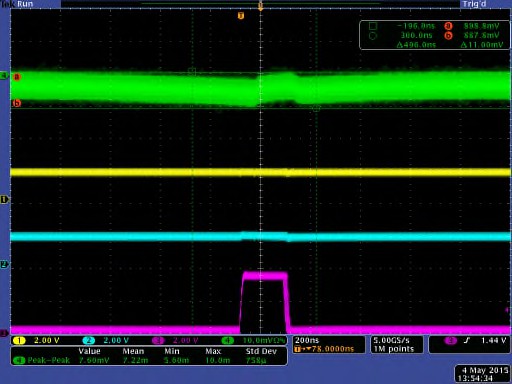
**VCORE**

**PWM3**

**PWM2**

**PWM1**

**Figure 4: Persistence plot of a 3Φ, 50A system**



**VCORE**

**PWM1**

**Figure 5: Persistence plot in 1Φ, 10A**

### HIGH-PRECISION VOLTAGE REFERENCE

The internal high-precision voltage reference supplies the required reference voltages to the VID DACs, ADCs and other analog circuits. This factory trimmed reference is guaranteed over temperature and manufacturing variations.

### VOLTAGE SENSE

An error voltage is generated from the difference between the target voltage, defined by the VID and load line (if implemented), and the differential, remotely sensed, output voltage. For each loop, the error voltage is digitized by a high-speed, high- precision ADC. An anti-alias filter provides the necessary high frequency noise rejection.

The gain and offset of the voltage sense circuitry for each loop is factory trimmed to deliver the required accuracy.

### CURRENT SENSE

Lossless inductor DCR or precision resistor current sensing is used to accurately measure individual phase currents. Using a simple off-chip thermistor, resistor and capacitor network for each loop, a thermally compensated load line is generated to meet the given power system requirement. A filtered voltage, which is a function of the total load current and the target load line resistance, is summed into each voltage sense path to accomplish the Active Voltage Positioning (AVP) function.

The IR35201 can also be used with Rdson current sensing PowIRstages. This algorithm helps reduce component by eliminating the need for the R-C sense components. Also, the thermistor used for thermal compensation would no longer be required, as this function is inherently designed into the Rdson sensing PowIRstages. The R-C network across the pins would still be required.

### VID DECODER

The VID decoder receives a VID code from the CPU that is converted to an internal code representing the VID voltage. This block also outputs the signal for VR disable if a VID shutdown code has been received.

The 8 bit VID code supports Intel® VR12 & VR12.5 modes and VID settings are selectable as either 5mV/code or 10mV/code on each loop independently. When AMD SVI2 mode is choosen, both loops will be set to 6.25mV/code

### MOSFET DRIVER, POWER STAGE AND DRMOS COMPATIBILITY

The PWM output signals of the IR35201 are designed for compatibility with industry standard +3.3V Tri-State MOSFET drivers

### I2C & PMBUS INTERFACE

An I2C or PMBus interface is used to communicate with the IR35201. This two-wire serial interface consists of clock and data signals, and operates as fast as 1MHz. The bus provides read and write access to the internal registers for configuration, and for monitoring of operating parameters. The bus is also used to program on-chip non-volatile memory (MTP) to store operating parameters.

To ensure operation with multiple devices on the bus, an exclusive address for the IR35201 is programmed

into MTP. The IR35201, additionally, supports pin- programming of the address.

To protect customer configuration and information, the I2C interface can be configured for either limited access with a 16-bit software password, or completely locked. Limited access includes both write and read protection options. In addition, there is a telemetry- only mode which only allows reads from the telemetry registers.

The IR35201 provides a hardware pin security option to provide extra protection. The protect pin is shared with the ADDR pin and is automatically engaged once the address is read. The pin must be driven high to disable protection. The pin can be enabled or disabled by a configuration setting in MTP.

The IR35201 supports the Packet Error Checking (PEC) protocol and a number of PMBus commands to monitor voltages and currents. For more information, refer to the PMBus Command Codes in [Table](#_bookmark59) 56.

##### IR POWIRCENTER GUI

The IR PowIRCenter GUI provides the designer with a comprehensive design environment that includes interactive tools to calculate VR efficiency and DC error budget, design the thermal compensation and feedback loop networks, and produce calculated Bode plots and output impedance plots. The PowIRCenter GUI environment is a key utility for design optimization, debug, and validation of designs that saves the designer significant time, allowing faster time-to-market (TTM).

The PowIRCenter GUI allows real-time design optimization and monitoring of key parameters such as output current and power, input current and power, efficiency, phase currents, temperature, and faults.

The IR PowIRCenter GUI also allows access to the system configuration settings for switching frequency, MOSFET driver compatibility, soft start rate, VID table, PSI, loop compensation, transient control system parameters, input under-voltage, output over-voltage, output under-voltage, output over-current and over- temperature.

##### PROGRAMMING

Once a design is complete, the PowIRcenter produces a complete configuration file.

The configuration file can be re-coded into an I2C/PMBus master (e.g. a Test System) and loaded into the IR35201 using the bus protocols described on page 48.

##### REAL-TIME MONITORING

The IR35201 can be accessed through the use of PMBus Command codes (described in [Table](#_bookmark59) 56), to read the real time status of the VR system including input voltage, output voltage, input and output current, input and output power, efficiency, and temperature.

# THEORY OF OPERATION



##### OPERATING MODE

The IR35201 changes its functionality based on the user-selected operating mode, allowing one device to be used for multiple applications without significant BoM changes. This greatly reduces the user’s design cycles and Time-to-Market (TTM).

The functionality for each operating mode is completely configurable by simple selections in MTP. The mode configuration is shown in [Table 1](#_bookmark2).

**Table 1: Mode Selection**

|  |  |
| --- | --- |
| **Mode** | **Description** |
| **VR12** | Intel® VR12 (Selected via MTP). |
| **VR12.5** | Intel® VR12.5 (Selected via MTP). |
| **IMVP8** | Intel® IMVP8 (Selected via MTP). |
| **SVI2** | AMD SVI2 (Selected via MTP). |
| **MPoL** | Memory Mode, with Loop 2 output voltage = ½ Loop 1 output voltage. |

##### DEVICE POWER-ON AND INITIALIZATION

The IR35201 is powered from a 3.3V DC supply. [Figure 6](#_bookmark3) shows the timing diagram during device initialization. An internal LDO generates a 1.8V rail to power the control logic within the device. During initial startup, the 1.8V rail follows the rising 3.3V supply voltage, proportional to an internal resistor tree. The internal oscillator becomes active at *t1* as the 1.8V rail is ramping up. Until soft-start begins, the IR35201 PWM outputs are disabled in a high impedance state to ensure that the system comes up in a known state.

The controller comes out of power-on reset (POR) at *t2* when the 3.3V supply is high enough for the internal bias control to generate 1.8V. The contents of the MTP are transferred to the registers by time *t3* and the automatic trim routines are complete by time *t4*. At this time, if enabled in MTP and when the VINSEN voltage is valid, the controller will detect the populated phases by sensing the voltage on the PWM pins. If the voltage is less than the Auto Phase Detect threshold (unused PWMs are grounded), the controller assumes the phase is unpopulated. The register settings and number of phases define the controller performance specific to the VR configuration, including trim settings, soft start ramp rate and boot voltage.

**Figure 6: Controller Startup and Initialization**

Once the registers are loaded from MTP, the designer can use I2C to re-configure the registers to suit the specific VR design requirements if desired.

##### TEST MODE

Having the ADDR\_PROT pin high as the IC goes through 3.3V POR engages a special test mode in which the I2C address changes to 0Ah. This allows individual in-circuit programming of the controller. This is specifically useful in multi-controller systems that use a single I2C bus. *Note that MTP will not load to the working registers until the ADDR\_PROT pin goes low.*

##### SUPPLY VOLTAGE

The controller is powered by the 3.3V supply rail. Once initialization of the device is complete, steady and stable supply voltage rails and a VR Enable signal (EN) are required to change the controller into an active state. The Enable signal is used to enable the PWM signals and begin the soft start sequence after the 3.3V and VIN supply rails are determined to be within the defined operating bands. The polarity of the chip enable function is bit-settable to either an active high or an active low configuration. When the controller is disabled by deactivating the Enable signal, it de-asserts VR READY and shuts down the regulator.

The recommended decoupling for the 3.3V is shown in [Figure 7](#_bookmark4). The Vcc pin should have a 0.1µF and 1µF X5R-type ceramic capacitors placed as close as possible to the package.



###### Figure 7: Vcc 3.3V decoupling

The CFILT pin must have a 1µF, X5R type decoupling capacitor connected close to the package as shown in [Figure 8](#_bookmark5).





###### Figure 8: CFILT decoupling

The IR35201 is designed to accommodate a wide variety of input power supplies and applications and offers programmability of the VINSEN turn-on/off voltages,

###### Table 2: VINSEN Turn-on/off Voltage Range

|  |  |
| --- | --- |
| **Threshold** | **Range** |
| Turn-on | 4.5V to 13.1875V in 1/16V steps1 |
| Turn-off | 4.5V to 13.1875V in 1/16V steps1 |

**1** *Must not be programmed below 4.5V*

The supply voltage on the VINSEN pin is compared against a programmable threshold. Once the rising VINSEN voltage crosses the turn-on threshold and EN is asserted, all PWM outputs become active. The VINSEN supply voltage is valid until it declines below its programmed turn-off level.

A 14:1 attenuation network is connected to the VINSEN pin as shown in Figure 9. Recommended values for a 12V system are RVIN\_1 = 13kΩ and RVIN\_2

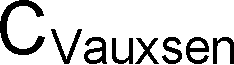
= 1kΩ, with a 1% tolerance or better. CVINSEN is required to have a minimum 1nF for noise suppression, with a maximum value of 10nF.

###### Figure 9: VINSEN resistor divider network



If enabled, VAUXSEN can be used to sense an auxiliary voltage like a 5V driver VCC, for

example. The on and off thresholds are adjusted by selecting the correct divider network, R1 and R2.



###### Figure 10: VAUXSEN resistor divider network

VAUX on and off thresholds are defined as: VAUX\_on = VAUXSEN\_on\*(1+R1/R2)

VAUX\_off = VAUXSEN\_off\*(1+R1/R2)

With R2 set to 1KΩ, [Table 3](#_bookmark6) shows the on and off

thresholds for various values of R1.

###### Table 3: VAUXSEN Turn-on/off Voltages

|  |  |  |
| --- | --- | --- |
| **R1** | **VAUX\_on** | **VAUX\_off** |
| KΩ | Volt | Volt |
| 5.77 | 4.50 | 3.97 |
| 8.78 | 6.50 | 5.74 |
| 11.80 | 8.50 | 7.50 |
| 14.81 | 10.50 | 9.27 |

Telemetry for VAUX is provided with 8 bit read only register, vaux\_supply. VAUX\_reported can be calculated with the following formula:

VAUX\_reported = vaux\_supply(dec)\*4.883E- 3\*(1+R1/R2)

##### POWER-ON SEQUENCING

The VR power-on sequence is initiated when all of the following conditions are satisfied:

* IR35201 Vcc (+3.3V rail) > VCC UVLO
* Input Voltage (VINSEN rail) > Vin UVLO
* Aux Voltage (VAUXSEN rail) > VAUXSEN UVLO

(if configured)ENABLE is HIGH

* VR has no Over-current, Over-voltage, Over- temperature or Under-voltage faults
* MTP transfer to configuration registers occurred without parity error

Once the above conditions are cleared, start-up behavior is controlled by the operating mode.



VCORE

VRRDY

ENABLE

**Figure 11: Enable-based Startup**

##### POWER-OFF SEQUENCING

When +12Vdc goes below controller turn-off threshold, the controller tristates all PWM’s. When enable goes low the controller ramps down Vout on both loops as shown in Figure12.



VCORE

VRRDY

ENABLE

**Figure 12: Enable-based Shutdown**

##### INTEL MODE

When the power-on sequence is initiated, and with VBOOT set to > 0V, the output voltage will ramp to its configured boot voltage and assert VRDY. The slew rate to VBOOT is programmed per [Table 2](#_bookmark28)1.

If Vboot = 0V, the VR will stay at 0V and will not soft- start until the CPU issues a VID command to the loop. In VR 13 mode, as soon as the IC is ready for SVID communication, VR\_READY will be asserted with Vboot = 0V.

###### Intel Boot Voltage

The IR35201 Vboot voltage is fully programmable in MTP to the range specified in the Intel VID tables. [Table](#_bookmark11) 14 and [Table](#_bookmark12) 15 show the Intel VID tables for for 5mV and 10mV VID steps respectively.

###### Table 8: Vboot Range

|  |  |
| --- | --- |
| **Loop** | **Boot Voltage** |
| Loop 1 | Per Intel VR12 and VR12.5 VID table |
| Loop 2 | Per Intel VR12 and VR12.5 VID table |

**Intel SVID Interface**

The IR35201 implements a fully compliant Intel® VR12 & VR12.5 Serial VID (SVID) interface. This is a three- wire interface between an Intel® VR12 ,VR12.5 & IMVP8 compliant processor and a VR that consists of clock, data and alert# signals.

The IR35201 architecture is based upon a digital core and hence lends itself very well to digital communications. As such, the IR35201 implements all the required SVID registers and commands. The IR35201 also implements many of the optional commands and registers with very few exceptions.

The Intel CPU is able to detect and recognize the extra functionality that the IR35201 provides and thus gives the Intel® VR 13/12/12.5/IMVP8 CPU unparalleled ability to monitor and optimize its power.

The SVID address of the IR35201 defaults to 0. This address may be re-programmed in MTP. An address lock function prevents accidental overwrites of the address.

The pseudo-code below illustrates the MTP address programming:

*# unlock the address register to write, then lock Set Address\_lock\_bit=0*

*Write new SVID address Set Address\_lock\_bit=1*

###### Intel VID Offset

The output voltage can be offset instead of setting a manual VID value, according to Table 9. This is especially useful for memory applications where voltages higher than the standard VID table may be required.

**Table 9: VID Offset**

|  |  |  |  |
| --- | --- | --- | --- |
| **Parameter** | **Memory** | **Range** | **Step Size** |
| Output Voltage | R/W | -128 to  +127 | 1 VID code |

*Maximum allowed voltage is 3.04V (VR12.5)*

Note that the Vmax register must be set appropriately to allow the required output voltage offset.

###### Intel Reporting Offsets

In addition to the mandatory features of the SVID bus, the IR35201 provides optional volatile SVID registers which allow the user to offset the reporting on the SVID interface as detailed in Table 10.

**Table 10: SVID Offset Registers**

|  |  |  |  |
| --- | --- | --- | --- |
| **Parameter** | **Memory** | **Range** | **Step size** |
| Output Current | NVM | -4A to +3.75A | 0.25A |
| Temperature | R/W | -32°C to +31°C | 1°C |

###### All Call SUPPORT

All Call for each loop of IR35201 can be configured in following ways:

* 0E and 0F.
* 0E only.
* 0F only.
* No All Call

IR35201 can be configured to be used as VR for CPU which is All Call 0F or Memory which is All Call 0E.

###### VR12.5 Operation

VR12.5 mode is selectable via MTP bit. The boot voltage in VR12.5 is also selectable and can be taken from the boot registers.

###### IMVP8 Operation

IMVP8 mode is selectable via MTP bit. The boot voltage in IMVP8 mode is configured in the boot register in 5mV steps compatible to VR12 mode VID table i.e. Table 14 or in 10mV steps compatible to VR12.5 mode VID table i.e. Table 15. In IMVP8 mode, bit 3 of SVID register “Status 1” (10h) is defined as “VID DAC high”. This bit when set is an indicator to the CPU that the VR VID DAC is greater than 30mV above a new VID recently set by an SetVID command.

In IMVP8 mode, IR35201 does support PS4 command, however, it does not shut down the circuitry to reduce quiescent power consumption to

<1mW. Thus, IR35201 is meant to be operated in IMVP8 mode for overclocking applications only where it is not expected for VR to shut down its circuitry to reduce quiescent power consumption.

###### Loop Start-Up Sequence and Delay

IR35201 can be configured to enable both loops in one of the following possible sequences:

* Both loops start together.
* Loop 2 follows Loop 1.
* Loop1 follows Loop 2.

If IR35201 is configured such that one loop follows the other, the delay between the two loops can be adjusted for following pre-defined intervals:

* 0 mS, 0.25 mS, 0.5 mS, 1 mS, 2.5 mS, 5 mS,

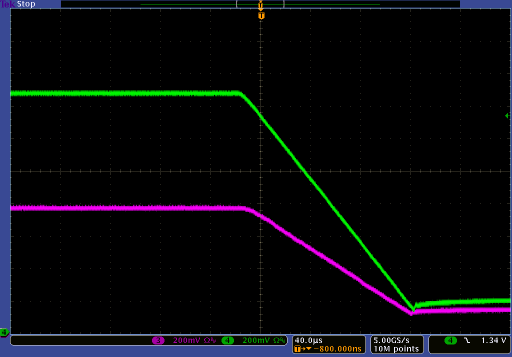
10 mS.

###### Memory (MPoL) Mode

In MPoL mode the IR35201 configures Loop 2 VID to 50% of Loop 1. Communication with and control of the IR35201 may occur either through the SVID interface when an Intel SVID Master is present, or alternatively through the I2C/SMBus/PMBus interface for non-Intel applications.

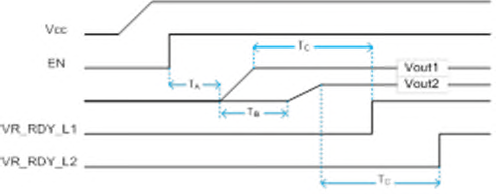
The IR35201 follows startup and timing requirements as shown in [Figure 13](#_bookmark7). When the power-on sequence is initiated, and with VBOOT set to > 0V, both rails will ramp to their configured voltages and assert VR\_READY\_L1 and VR\_READY\_L2. The slew rates for both loops are set independently per [Table 2](#_bookmark28)1. If tracking is required during the slew, then care must be

taken to ensure that the Loop 2 slew rate is set to ½ of the Loop 1 slew rate. Typical MPoL start-up and shut- down waveforms are shown in [Figure 14](#_bookmark8) and [Figure](#_bookmark9) [15.](#_bookmark9)



Vout 1

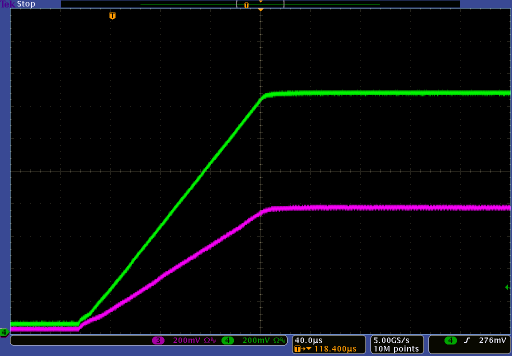
Vout 2



**Figure 13: MPoL Startup**

**Table 12: MPoL Start-up Timing**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Time** | **Description** | **Min** | **Typ** | **Max** |
| **TA** | VR\_EN to Loop 1 start |  | 3µs |  |
| **TB** | Loop 2 delay |  | [Table](#_bookmark10) |  |
| **TC** | Voltage ramp complete to VR\_RDY\_L1/L2 |  |  | 1µs |



Vout 1

Vout 2

**Figure 14: MPoL Tracking Startup**

**Figure 15: MPoL Tracking Shutdown**

In MPoL mode, Loop 2 start-up can be delayed relative to Loop 1 according to 2.

**Table 13: MPoL Loop 2 Start-up Delay**

**Loop 2 Delay**

0 – 678.3usec in 2.66usec Steps

**Table 14: Intel VR12 VID Table – 5mV VID Step**

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **VID**  **(Hex)** | **Voltage (V)** | **VID**  **(Hex)** | **Voltage (V)** | **VID**  **(Hex)** | **Voltage (V)** | **VID**  **(Hex)** | **Voltage (V)** | **VID**  **(Hex)** | **Voltage (V)** |
| FF | 1.52 | DA | 1.335 | B5 | 1.15 | 90 | 0.965 | 6B | 0.78 |
| FE | 1.515 | D9 | 1.33 | B4 | 1.145 | 8F | 0.96 | 6A | 0.775 |
| FD | 1.51 | D8 | 1.325 | B3 | 1.14 | 8E | 0.955 | 69 | 0.77 |
| FC | 1.505 | D7 | 1.32 | B2 | 1.135 | 8D | 0.95 | 68 | 0.765 |
| FB | 1.5 | D6 | 1.315 | B1 | 1.13 | 8C | 0.945 | 67 | 0.76 |
| FA | 1.495 | D5 | 1.31 | B0 | 1.125 | 8B | 0.94 | 66 | 0.755 |
| F9 | 1.49 | D4 | 1.305 | AF | 1.12 | 8A | 0.935 | 65 | 0.75 |
| F8 | 1.485 | D3 | 1.3 | AE | 1.115 | 89 | 0.93 | 64 | 0.745 |
| F7 | 1.48 | D2 | 1.295 | AD | 1.11 | 88 | 0.925 | 63 | 0.74 |
| F6 | 1.475 | D1 | 1.29 | AC | 1.105 | 87 | 0.92 | 62 | 0.735 |
| F5 | 1.47 | D0 | 1.285 | AB | 1.1 | 86 | 0.915 | 61 | 0.73 |
| F4 | 1.465 | CF | 1.28 | AA | 1.095 | 85 | 0.91 | 60 | 0.725 |
| F3 | 1.46 | CE | 1.275 | A9 | 1.09 | 84 | 0.905 | 5F | 0.72 |
| F2 | 1.455 | CD | 1.27 | A8 | 1.085 | 83 | 0.9 | 5E | 0.715 |
| F1 | 1.45 | CC | 1.265 | A7 | 1.08 | 82 | 0.895 | 5D | 0.71 |
| F0 | 1.445 | CB | 1.26 | A6 | 1.075 | 81 | 0.89 | 5C | 0.705 |
| EF | 1.44 | CA | 1.255 | A5 | 1.07 | 80 | 0.885 | 5B | 0.7 |
| EE | 1.435 | C9 | 1.25 | A4 | 1.065 | 7F | 0.88 | 5A | 0.695 |
| ED | 1.43 | C8 | 1.245 | A3 | 1.06 | 7E | 0.875 | 59 | 0.69 |
| EC | 1.425 | C7 | 1.24 | A2 | 1.055 | 7D | 0.87 | 58 | 0.685 |
| EB | 1.42 | C6 | 1.235 | A1 | 1.05 | 7C | 0.865 | 57 | 0.68 |
| EA | 1.415 | C5 | 1.23 | A0 | 1.045 | 7B | 0.86 | 56 | 0.675 |
| E9 | 1.41 | C4 | 1.225 | 9F | 1.04 | 7A | 0.855 | 55 | 0.67 |
| E8 | 1.405 | C3 | 1.22 | 9E | 1.035 | 79 | 0.85 | 54 | 0.665 |
| E7 | 1.4 | C2 | 1.215 | 9D | 1.03 | 78 | 0.845 | 53 | 0.66 |
| E6 | 1.395 | C1 | 1.21 | 9C | 1.025 | 77 | 0.84 | 52 | 0.655 |
| E5 | 1.39 | C0 | 1.205 | 9B | 1.02 | 76 | 0.835 | 51 | 0.65 |
| E4 | 1.385 | BF | 1.2 | 9A | 1.015 | 75 | 0.83 | 50 | 0.645 |
| E3 | 1.38 | BE | 1.195 | 99 | 1.01 | 74 | 0.825 | 4F | 0.64 |
| E2 | 1.375 | BD | 1.19 | 98 | 1.005 | 73 | 0.82 | 4E | 0.635 |
| E1 | 1.37 | BC | 1.185 | 97 | 1 | 72 | 0.815 | 4D | 0.63 |
| E0 | 1.365 | BB | 1.18 | 96 | 0.995 | 71 | 0.81 | 4C | 0.625 |
| DF | 1.36 | BA | 1.175 | 95 | 0.99 | 70 | 0.805 | 4B | 0.62 |
| DE | 1.355 | B9 | 1.17 | 94 | 0.985 | 6F | 0.8 | 4A | 0.615 |
| DD | 1.35 | B8 | 1.165 | 93 | 0.98 | 6E | 0.795 | 49 | 0.61 |
| DC | 1.345 | B7 | 1.16 | 92 | 0.975 | 6D | 0.79 | 48 | 0.605 |
| DB | 1.34 | B6 | 1.155 | 91 | 0.97 | 6C | 0.785 | 47 | 0.6 |

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **VID**  **(Hex)** | **Voltage (V)** | **VID**  **(Hex)** | **Voltage (V)** | **VID**  **(Hex)** | **Voltage (V)** | **VID**  **(Hex)** | **Voltage (V)** | **VID**  **(Hex)** | **Voltage (V)** |
| 46 | 0.595 | 37 | 0.52 | 28 | 0.445 | 19 | 0.37 | 0A | 0.295 |
| 45 | 0.59 | 36 | 0.515 | 27 | 0.44 | 18 | 0.365 | 09 | 0.29 |
| 44 | 0.585 | 35 | 0.51 | 26 | 0.435 | 17 | 0.36 | 08 | 0.285 |
| 43 | 0.58 | 34 | 0.505 | 25 | 0.43 | 16 | 0.355 | 07 | 0.28 |
| 42 | 0.575 | 33 | 0.5 | 24 | 0.425 | 15 | 0.35 | 06 | 0.275 |
| 41 | 0.57 | 32 | 0.495 | 23 | 0.42 | 14 | 0.345 | 05 | 0.27 |
| 40 | 0.565 | 31 | 0.49 | 22 | 0.415 | 13 | 0.34 | 04 | 0.265 |
| 3F | 0.56 | 30 | 0.485 | 21 | 0.41 | 12 | 0.335 | 03 | 0.26 |
| 3E | 0.555 | 2F | 0.48 | 20 | 0.405 | 11 | 0.33 | 02 | 0.255 |
| 3D | 0.55 | 2E | 0.475 | 1F | 0.4 | 10 | 0.325 | 01 | 0.25 |
| 3C | 0.545 | 2D | 0.47 | 1E | 0.395 | 0F | 0.32 | 00 | 0 |
| 3B | 0.54 | 2C | 0.465 | 1D | 0.39 | 0E | 0.315 |  |  |
| 3A | 0.535 | 2B | 0.46 | 1C | 0.385 | 0D | 0.31 |  |  |
| 39 | 0.53 | 2A | 0.455 | 1B | 0.38 | 0C | 0.305 |  |  |
| 38 | 0.525 | 29 | 0.45 | 1A | 0.375 | 0B | 0.3 |  |  |

**Table 15: Intel VR12.5 VID Table – 10mV VID Step**

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| VID (HEX) | Voltage (V) | VID (HEX) | Voltage (V) | VID (HEX) | Voltage (V) | VID (HEX) | Voltage (V) | VID (HEX) | Voltage (V) |
| FF | 3.04 | E1 | 2.74 | C3 | 2.44 | A5 | 2.14 | 87 | 1.84 |
| FE | 3.03 | E0 | 2.73 | C2 | 2.43 | A4 | 2.13 | 86 | 1.83 |
| FD | 3.02 | DF | 2.72 | C1 | 2.42 | A3 | 2.12 | 85 | 1.82 |
| FC | 3.01 | DE | 2.71 | C0 | 2.41 | A2 | 2.11 | 84 | 1.81 |
| FB | 3.00 | DD | 2.70 | BF | 2.40 | A1 | 2.10 | 83 | 1.80 |
| FA | 2.99 | DC | 2.69 | BE | 2.39 | A0 | 2.09 | 82 | 1.79 |
| F9 | 2.98 | DB | 2.68 | BD | 2.38 | 9F | 2.08 | 81 | 1.78 |
| F8 | 2.97 | DA | 2.67 | BC | 2.37 | 9E | 2.07 | 80 | 1.77 |
| F7 | 2.96 | D9 | 2.66 | BB | 2.36 | 9D | 2.06 | 7F | 1.76 |
| F6 | 2.95 | D8 | 2.65 | BA | 2.35 | 9C | 2.05 | 7E | 1.75 |
| F5 | 2.94 | D7 | 2.64 | B9 | 2.34 | 9B | 2.04 | 7D | 1.74 |
| F4 | 2.93 | D6 | 2.63 | B8 | 2.33 | 9A | 2.03 | 7C | 1.73 |
| F3 | 2.92 | D5 | 2.62 | B7 | 2.32 | 99 | 2.02 | 7B | 1.72 |
| F2 | 2.91 | D4 | 2.61 | B6 | 2.31 | 98 | 2.01 | 7A | 1.71 |
| F1 | 2.90 | D3 | 2.60 | B5 | 2.30 | 97 | 2.00 | 79 | 1.70 |
| F0 | 2.89 | D2 | 2.59 | B4 | 2.29 | 96 | 1.99 | 78 | 1.69 |
| EF | 2.88 | D1 | 2.58 | B3 | 2.28 | 95 | 1.98 | 77 | 1.68 |
| EE | 2.87 | D0 | 2.57 | B2 | 2.27 | 94 | 1.97 | 76 | 1.67 |
| ED | 2.86 | CF | 2.56 | B1 | 2.26 | 93 | 1.96 | 75 | 1.66 |
| EC | 2.85 | CE | 2.55 | B0 | 2.25 | 92 | 1.95 | 74 | 1.65 |
| EB | 2.84 | CD | 2.54 | AF | 2.24 | 91 | 1.94 | 73 | 1.64 |
| EA | 2.83 | CC | 2.53 | AE | 2.23 | 90 | 1.93 | 72 | 1.63 |
| E9 | 2.82 | CB | 2.52 | AD | 2.22 | 8F | 1.92 | 71 | 1.62 |
| E8 | 2.81 | CA | 2.51 | AC | 2.21 | 8E | 1.91 | 70 | 1.61 |
| E7 | 2.80 | C9 | 2.50 | AB | 2.20 | 8D | 1.90 | 6F | 1.60 |
| E6 | 2.79 | C8 | 2.49 | AA | 2.19 | 8C | 1.89 | 6E | 1.59 |
| E5 | 2.78 | C7 | 2.48 | A9 | 2.18 | 8B | 1.88 | 6D | 1.58 |
| E4 | 2.77 | C6 | 2.47 | A8 | 2.17 | 8A | 1.87 | 6C | 1.57 |
| E3 | 2.76 | C5 | 2.46 | A7 | 2.16 | 89 | 1.86 | 6B | 1.56 |
| E2 | 2.75 | C4 | 2.45 | A6 | 2.15 | 88 | 1.85 | 6A | 1.55 |

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| VID (HEX) | Voltage (V) | VID (HEX) | Voltage (V) | VID (HEX) | Voltage (V) | VID (HEX) | Voltage (V) | VID (HEX) | Voltage (V) |
| 69 | 1.54 | 53 | 1.32 | 3D | 1.10 | 27 | 0.88 | 11 | 0.66 |
| 68 | 1.53 | 52 | 1.31 | 3C | 1.09 | 26 | 0.87 | 10 | 0.65 |
| 67 | 1.52 | 51 | 1.30 | 3B | 1.08 | 25 | 0.86 | F | 0.64 |
| 66 | 1.51 | 50 | 1.29 | 3A | 1.07 | 24 | 0.85 | E | 0.63 |
| 65 | 1.50 | 4F | 1.28 | 39 | 1.06 | 23 | 0.84 | D | 0.62 |
| 64 | 1.49 | 4E | 1.27 | 38 | 1.05 | 22 | 0.83 | C | 0.61 |
| 63 | 1.48 | 4D | 1.26 | 37 | 1.04 | 21 | 0.82 | B | 0.60 |
| 62 | 1.47 | 4C | 1.25 | 36 | 1.03 | 20 | 0.81 | A | 0.59 |
| 61 | 1.46 | 4B | 1.24 | 35 | 1.02 | 1F | 0.80 | 9 | 0.58 |
| 60 | 1.45 | 4A | 1.23 | 34 | 1.01 | 1E | 0.79 | 8 | 0.57 |
| 5F | 1.44 | 49 | 1.22 | 33 | 1.00 | 1D | 0.78 | 7 | 0.56 |
| 5E | 1.43 | 48 | 1.21 | 32 | 0.99 | 1C | 0.77 | 6 | 0.55 |
| 5D | 1.42 | 47 | 1.20 | 31 | 0.98 | 1B | 0.76 | 5 | 0.54 |
| 5C | 1.41 | 46 | 1.19 | 30 | 0.97 | 1A | 0.75 | 4 | 0.53 |
| 5B | 1.40 | 45 | 1.18 | 2F | 0.96 | 19 | 0.74 | 3 | 0.52 |
| 5A | 1.39 | 44 | 1.17 | 2E | 0.95 | 18 | 0.73 | 2 | 0.51 |
| 59 | 1.38 | 43 | 1.16 | 2D | 0.94 | 17 | 0.72 | 1 | 0.50 |
| 58 | 1.37 | 42 | 1.15 | 2C | 0.93 | 16 | 0.71 | 0 | 0.00 |
| 57 | 1.36 | 41 | 1.14 | 2B | 0.92 | 15 | 0.70 |  |  |
| 56 | 1.35 | 40 | 1.13 | 2A | 0.91 | 14 | 0.69 |  |  |
| 55 | 1.34 | 3F | 1.12 | 29 | 0.90 | 13 | 0.68 |  |  |
| 54 | 1.33 | 3E | 1.11 | 28 | 0.89 | 12 | 0.67 |  |  |

##### PHASING

The number of phases enabled on each loop of the IR35201 is shown in Table 16. The phase of the PWM outputs is automatically adjusted to optimize phase interleaving for minimum output ripple. Phase interleaving results in a ripple frequency that is the product of the switching frequency and the number of phases. A high ripple frequency results in reduced ripple voltage, thereby minimizing the output filter capacitance requirements, resulting in significant total BOM cost reduction.

**Table 16: Loop Configuration**

|  |  |  |
| --- | --- | --- |
| Configuration | Loop 1 | Loop 2 |
| **8+0** | 8-phases | - |
| **7+0** | 7-phases | - |
| **6+0** | 6-phases | - |
| **5+0** | 5-phases | - |
| **4+0** | 4-phases | - |
| **3+0** | 3-phases | - |
| **2+0** | 2-phases | - |
| **1+0** | 1-phase | - |
| **7+1** | 7-phases | 1-phase |
| **6+1** | 6-phases | 1-phase |
| **5+1** | 5-phases | 1-phase |
| **4+1** | 4-phases | 1-phase |
| **3+1** | 3-phases | 1-phase |
| **2+1** | 2-phases | 1-phase |
| **1+1** | 1-phase | 1-phase |
| **6+2** | 6-phases | 2-phase |
| **5+2** | 5-phases | 2-phase |
| **4+2** | 4-phases | 2-phase |
| **3+2** | 3-phases | 2-phase |
| **2+2** | 2-phases | 2-phase |
| **1+2** | 1-phase | 2-phase |

##### UNUSED PHASES

Phases are disabled based upon the configuration shown in Table 16. Disabled PWM outputs should be left floating unless the auto-populate phase detection feature is used. Unused phases should be disconnected in reverse order to ensure a correct phase relationship. E.g. a 4+0 configuration must

have PWMs on phases 3 and 4 disconnected in order to operate in 2+0 mode. If phases 1 or 2 were disconnected instead, the remaining phases would not have a symmetrical relationship, leading to unreliable performance. If the auto-populate phase detection feature is used, unused PWM outputs should be grounded so that their voltage is below the threshold (phase is disabled). IR35201 automatically adjusts

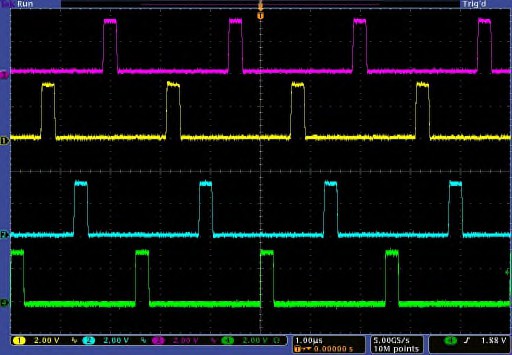
the phase configuration to operate with the populated phases (up to the configuration allowed by the settings in Table 16).

In addition, the IR35201 detects the number of populated phases at start-up by comparing the voltage on the PWM pin against the phase detection threshold. In order for populated phases to be detected, the MOSFET drivers need to be powered up before the VCC, +12Vin and Vaux to the IR35201 exceeds its POR threshold.

Typical PWM pulse phase relationships are shown in Table 17 and [Figure 16](#_bookmark13).

**Table 17: Phase Relationship**

|  |  |
| --- | --- |
| **Phases** | **Phasing** |
| 1 | - |
| 2 | 180º |
| 3 | 120º |
| 4 | 90º |
| 5 | 72º |
| 6 | 60º |
| 7 | 51.42º |
| 8 | 45º |

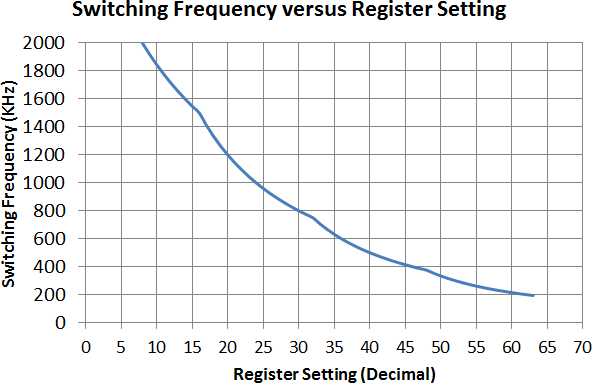
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**Figure 16: 4-phase PWM interleaved operation**

##### SWITCHING FREQUENCY

The phase switching frequency (Fsw) of the IR35201 is set by a user configurable register. The switching frequency can be set indepently on each loop. The switching frequency variation with register setting has been plotted in [Figure 17](#_bookmark14).

The IR35201 oscillator is factory trimmed to guarantee high accuracy and very low jitter compared to analog controllers.



**Figure 17: Switching Frequency Variation with Register Setting**

##### MOSFET DRIVER AND POWERSTAGE SELECTION

The PWM signals from the active phases of the IR35201 are designed to operate with industry standard tri-state type drivers or PowIRstage devices. The logic operation for these types of tri-state drivers is depicted in [Figure 18](#_bookmark15).

When in tri-state, the IR35201 floats the outputs so that the voltage level is determined by an external voltage divider which is typically inside the MOSFET driver. Sometimes external resistors are added to improve the speed of the PWM signal going into tri- state.

Note that the PWM outputs are tri-stated whenever the controller is disabled (EN = low), the shut-down ramp has completed or before the soft-start ramp is initiated.

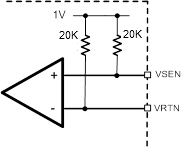


**Figure 18: 3.3V Tri-state Driver Logic Levels**

##### OUTPUT VOLTAGE DIFFERENTIAL SENSING

The IR35201 VSEN and VRTN pins for each loop are connected to the load sense pins of the output voltage to provide true differential remote voltage sensing with high common-mode rejection. Each loop has a high bandwidth error amplifier that generates the error voltage between this remote sense voltage and the target voltage. The error voltage is digitized by a fast, high-precision ADC.

[As shown in Figure 19, the Vsen and Vrtn inputs have](#_bookmark16) a 20kΩ pull-up to an internal 1V rail. This causes some current flow in the Vsen and Vrtn lines. To minimize the offset created by this current flow, the external series impedance on these lines needs to be kept to a minimum.



**Figure 19: Output Voltage sensing impedance**

##### INPUT CURRENT SENSING

The IR35201 provides input current sensing to measure the power drawn by the load from the source. A precision current sense resistor is connected in series with the input path as shown in Figure 21. The voltage across the current sense resistor is differentially amplified by a current sense amplifier and fed to I\_IN pin of IR35201. An internal ADC converts the sensed voltage into its digital equivalent. The I\_IN pin input voltage range is 0 to 1.25Vdc.

𝐼\_𝐼𝑁(𝑉) = 𝐼𝑖𝑛 ∗ 𝑅𝑆𝐸𝑁𝑆𝐸 ∗ 𝐶𝑆𝐴𝐺𝐴𝐼𝑁

The IR35201 offers four full-scale ranges for input current.

1. 0 – 62.5A.
2. 0 – 31.25A.
3. 0 – 15.625A.
4. 0 – 7.8125A.



**Figure 20 Input Current Sensing**

##### PIN\_ALERT

The IR35201 has a PIN\_ALERT# pin to alert the system when the input power has exceeded a preset threshold. The pin is an open drain output that is high until the input power threshold is exceeded at which point it pulls low. The output stays low until the input power drops below 90% of the Pin\_Alert

threshold. The PIN\_ALERT# pin will de-assert

current is also summed with the VID DAC output to implement the AVP function.

The recommended value for Csen is 220nF, with an NPO type dielectric. To prevent undershooting of the output voltage during load transients, the Rsen resistor can be calculated by:

*R*  1.05 \* *L* \_ *out*

100mS after the input power drops below 90% of the PIN\_ALERT threshold. In an Intel system the Pin\_alert pin is pulled up with a 4.99kohm resistor to

*sen*

*Csen*

 *DCR*

3.3 Vdc. The PIN is filtered by a 2KHz BW filter. The PIN\_ALERT# pin assertion will be belayed by up to 300uS.

##### OUTPUT CURRENT SENSING

The IR35201 provides per-phase output current sensing to support accurate Adaptive Voltage Positioning (AVP), current balancing, and over-current protection. The differential current sense scheme supports both lossless inductor DCR and RDS (ON) (or per-phase series precision resistor) current sensing techniques.

For DCR sensing, a suitable resistor-capacitor network of Rsen and Csen is connected across the inductor in each phase as shown in [Figure 21](#_bookmark17) below. The time constant of this RC network is set to equal the inductor time constant (L/DCR) such that the voltage across the capacitor Csen is equal to the voltage across the inductor DCR.





**Figure 21: DCR Current Sensing**

A current proportional to the inductor current in each phase is generated and used for per-phase current balancing. The individual phase current signals are summed to arrive at the total current.

The phase currents and total current are quantized by the monitoring ADC and used to implement the current monitoring and OCP features. The total

**Note: Use thick film resistor (0603) for Rsen.**

**VCC\_Core**



12V

**V cc**

**BOOT**

**V in**

PWM

**P WM**

I  Iphase

L\_out

+

ISEN

R1 IR3555

10K

**IO UT**

**S witch**

-

2.49K

IRTN R2

**REF IN**

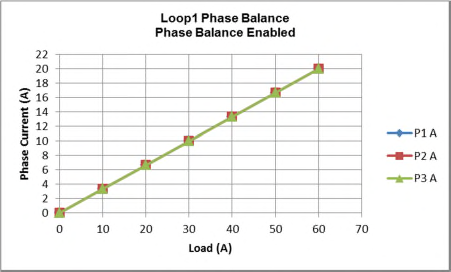
**Figure 22 RDS (ON) Current Sense**

Additionally, the current sense inputs to the IR35201 can also be directly fed the current information from a PowIRstage having RDS (ON) sensing capability, thereby eliminating the need for the R-C sense components, RSEN and CSEN as shown in [Figure 22](#_bookmark18). The IR3555 has an IOUT gain of 5mV/A. A divider of 5:1 should be used to match the ISENSE amp input dynamic range. The recommended values are 10K and 2.49K. The REFIN pin is offset above 0V by connecting it to the 1.8V CFILT pin.

##### CURRENT BALANCING & OFFSET

The IR35201 provides accurate digital phase current balancing in any phase configuration. Current balancing equalizes the current across all the phases. This improves efficiency, prevents hotspots and reduces the possibility of inductor saturation.

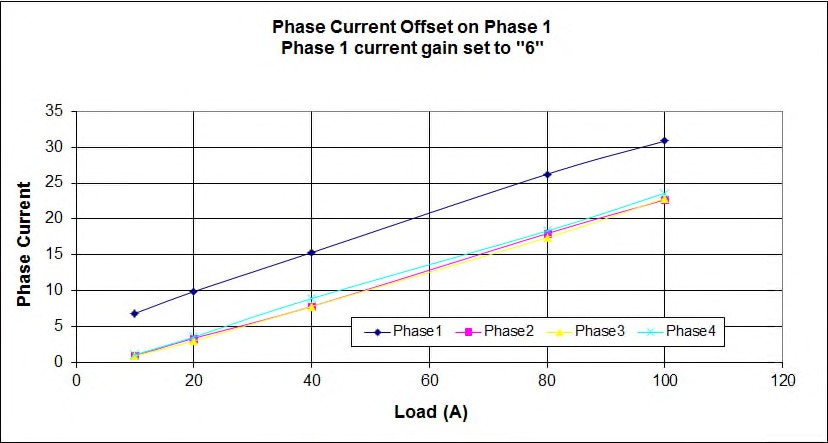
The sensed currents for each phase are converted to a voltage and are multiplexed into the monitoring ADC. The digitized currents are low-pass filtered and passed through a proprietary current balance algorithm to enable the equalization of the phase currents as shown in [Figure 23](#_bookmark19).



**Figure 23: Typical Phase Current Balance (3-phases enabled)**

The proprietary high-speed active phase current balance operates during load transients to eliminate current imbalance that can result from a load current oscillating near the switching frequency. The order in which the phases output PWM pulses is decided based on an adaptive High Speed Phase Balance (HSPB) to ensure that the phases remain balanced during high frequency load transients. Once the VR returns to steady-state operation, the phases return to the normal phase firing order.

In addition, the IR35201 allows the user to offset phase currents to optimize the thermal solution. [Figure 24](#_bookmark20) shows Phase 1 current gain offset to a value of 6. This scales the current in phase 1 to have approximately 30% more current than the other phases.



**Figure 24: Phase 1 Current Offset**

##### CURRENT CALIBRATION

For optimizing the current measurement accuracy of a design, the IR35201 contains a register in MTP, which can store a user-programmed per phase Current Offset, to zero out the no-load current reading. Refer to

[Table 43 for output current calibration registers.](#_bookmark48)

##### LOAD LINE

The IR35201 enables the implementation of an accurate, temperature compensated load line.

The nominal load line is set by an external resistor RCS, as shown in [Figure 25](#_bookmark21). This load line value also needs to be stored in MTP. The stored values for load line, scaling and gain provide the scaling factors required for digital computation of the total current, in order to determine the true current, OCP threshold, and output voltage telemetry registers.

For each loop, the sensed current from all the active phases is summed and applied differentially to a resistor network across the RSCP and RCSM pins as shown in [Figure 25](#_bookmark21). This generates a precise proportional voltage, which is summed with the sensed output voltage and VID DAC reference to form the error voltage.

IR35201 supports two types of current sense techniques.

1. DCR Current Sense.
2. RDS (ON) Current Sense.

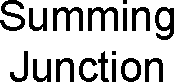
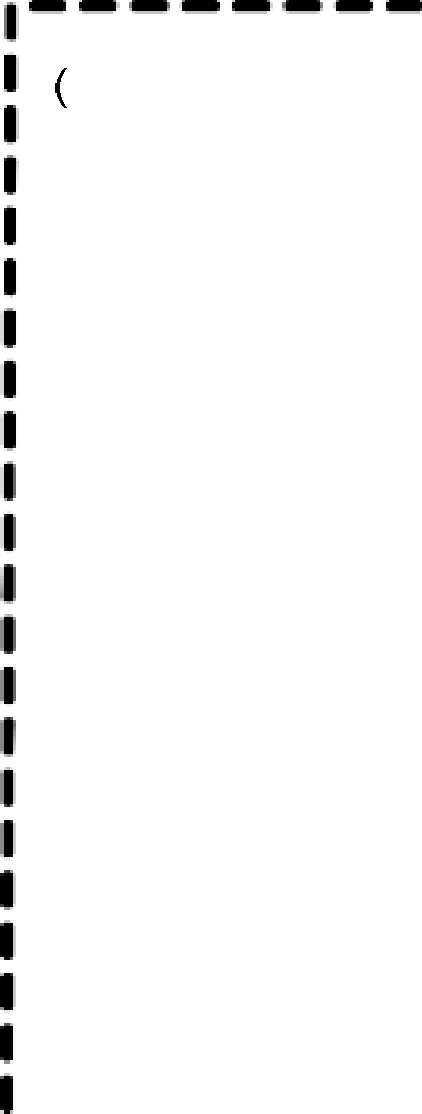
###### DCR Current Sense

DCR current sense technique measures the voltage drop across DCR of the inductor as shown in [Figure](#_bookmark17)

[21. DCR of the inductor has a positive temperature](#_bookmark17) coefficient of resistance. Hence, to compensate for increase in DCR with respect to temperature and thermistor RTh having negative temperature coefficient of resistance is also part of the network. For proper load line temperature compensation, the thermistor is placed near the phase one inductor to accurately sense the inductor temperature.

|  |  |
| --- | --- |
| **Murata** | NCP18XH103F03RB |
| **Panasonic** | ERTJ1VG103FA |
| **TDK** | NTCG163JF103F |

1. Calculate RCS using the following equation:





*RCS* 

1

## 1  1

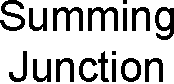
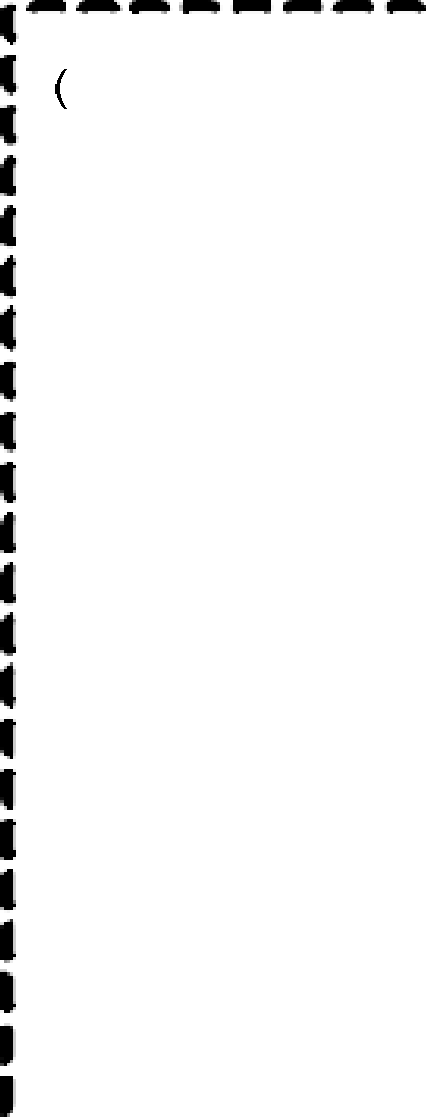
*RCS effective*  2  *Rseries RTh*

**Figure 25: Load Line & Thermal Compensation for DCR Sense**

Rseries is selected to achieve minimum load line error over temperature. The IR PowIRCenter GUI provides a graphical tool that allows the user to easily calculate the resistor values for minimum error.

The capacitor CCS is defined by the following equation:

*CCS*



 2  *π*  *R*  *f*

*CSeffective AVP*

1





where fAVP is the user selectable current sense AVP bandwidth. The recommended bandwidth is typically in the range of 200kHz to 300kHz.

**Figure 26 Load Line for RDS (ON) Current Sense**

The resistor RCS is calculated using the following procedure:

1. Calculate the RCSeffective or the total effective parallel resistance across the RSCP and RCSM pins as defined by:

*R*

###### RDS (ON) Current Sense

IR35201 reads the current value from individual power stages as shown in [Figure 22](#_bookmark18). The power stage measures the output current by sensing the voltage drop across lower side MOSFET. The current sensed by the power stage is thermally compensated hence there is no need of an external thermistor for temperature compensation. Thus, RDS (ON) current sense reduces the component count required for loadline measurement as shown in [Figure 26](#_bookmark22).

*RCS effective*

 8  *R* \_ *ISEN*   *LL*

*DCR*

The resistor Rcs for R

DS ON

current sense is calculated

where RLL is the desired load line, DCR is DC resistance of the phase inductor, and R\_ISEN is the internal series resistor = 1000.

1. Select a suitable NTC thermistor, Rth. This is typically selected to have the lowest thermal coefficient and tightest tolerance in a standard available package. A typical NTC used in these applications is a 10kΩ, 1% tolerance device. Recommended thermistors are shown in Table 18.

by using the following procedure.

𝑅𝑐𝑠 = 8 ∗ 𝑅𝐼𝑆𝐸𝑁 ∗ 𝑅𝐿𝐿/(𝐼𝑅𝐷𝑆0𝑁 𝑆𝑐𝑎𝑙𝑒 ∗ 𝐷𝑖𝑣𝑖𝑑𝑒𝑟 𝑅𝑎𝑡𝑖o)

Where IRDS ON Scale = current scale of Power Stage in V/A

Divider Ratio = 𝑅2 [.Refer to Figure 22](#_bookmark18)

𝑅1+𝑅2

The capacitor CCS is defined by the following equation:

**TABLE 18: 10K 1% NTC THERMISTORS**

*CCS*

 1

2  *π*  *RCS*

 *f AVP*

where fAVP is the user selectable current sense AVP bandwidth. The recommended bandwidth is typically in the range of 200kHz to 300kHz.

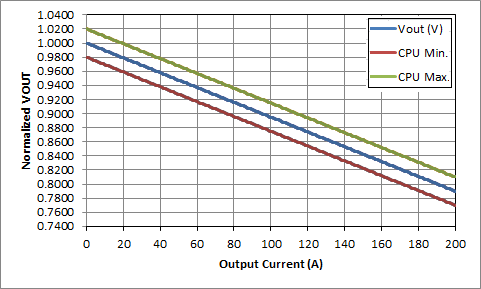
###### Setting a 0mΩ Load Line

The load line is turned off by setting the Loadline Enable bit low. This is a separate bit from the load line settings for each loop.

Even though the load line is disabled digitally, the load-line resistors and scaling registers should be set such that the load line is at least 3 times the value of low ohmic DCR inductors (<0.5mΩ) or equal to the DCR value for high ohmic inductors (>0.5mΩ). For example, if the inductor(s) DCR is 0.3mΩ, a nominal

0.9 mΩ load line should be set. For accurate current measurement and OCP threshold with the load line disabled, the output current gain and scaling registers must be set to the same value as the load line set with the external resistor network. With load line disabled, the thermistor and Ccs capacitor must still be installed to insure accuracy of the current measurement.

[Figure 27 shows a typical 1.05mΩ load line](#_bookmark23) measurement with minimum and maximum error ranges. The controller accuracy lies well within common processor requirements.



**Figure 27: Load Line Measurements**

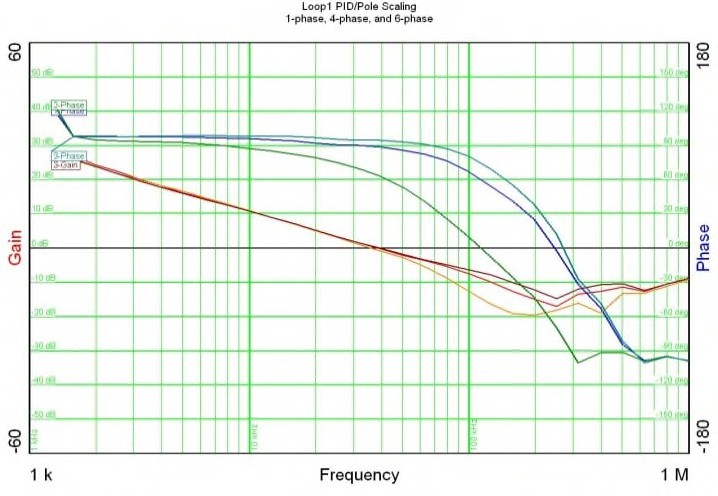
The load line range for IR35201 is shown in Table 19.

**Table 19: Load Line Settings**

The IR35201 uses a digital feedback loop to minimize the requirement for output decoupling, and to maintain a tightly regulated output voltage. The error between the target and the output voltage is digitized and passed through a low pass filter. This filtered signal is then passed through an initial single-pole filter stage, followed by the PID (Proportional Integral Derivative) compensator, and an additional single-pole filter stage. The loop compensation parameters Kp (proportional coefficient), Ki (integral coefficient), and Kd (derivative coefficient), as well as the low-pass filter pole locations are user-configurable to optimize the VR design for the chosen external components.

The adaptive PID control used in IR35201 intelligently scales the coefficients and the low-pass filters in real- time, to maintain optimum stability, as phases are added and dropped dynamically in the application.

This auto-scaling feature significantly reduces design time by virtue of having to design the PID coefficients design only for one loop combination. ([Figure 28](#_bookmark24)).



**Figure 28: Stability with Phase Add/Drop**

Each of the proportional, integral and derivative terms is a 6-bit value stored in MTP that is decoded by the IC’s digital core. This allows the designer to set the converter bandwidth and phase margin to the desired values.

The compensator transfer function is defined as:

   

(*Kp*  *Ki*  *Kd*  *s*) 

|  |  |  |
| --- | --- | --- |
|  | **Loop #1** | **Loop #2** |
| **Minimum** | 0.0 mΩ | 0.0 mΩ |
| **Maximum** | 6.375 mΩ | 12.75 mΩ |
| **Resolution** | 0.025 mΩ | 0.050 mΩ |

## 1   1 

*s* 1

 



 

1 *s*

*ωp* 



2 





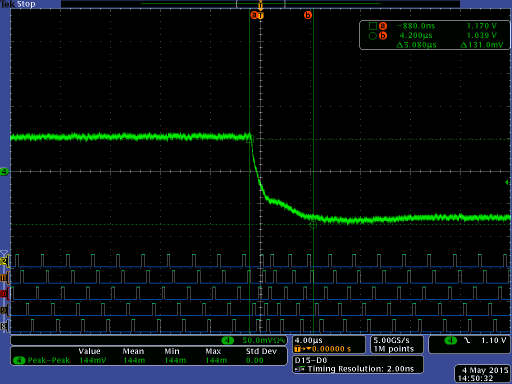
*s*

*ωp*1

##### DIGITAL FEEDBACK LOOP & PWM

where ωp1 and ωp2 are the two configurable poles, typically positioned to filter noise, and to roll off the high-frequency gain that the Kd term creates.

The outputs of the compensator and the phase current balance block are fed into a digital PWM pulse generator to generate the PWM pulses for the active phases. The digital PWM generator has a native time resolution of 1.3ns which is combined with digital dithering to provide an effective PWM resolution of 163ps. This ensures that there is no limit cycling when operating at the highest switching frequency.

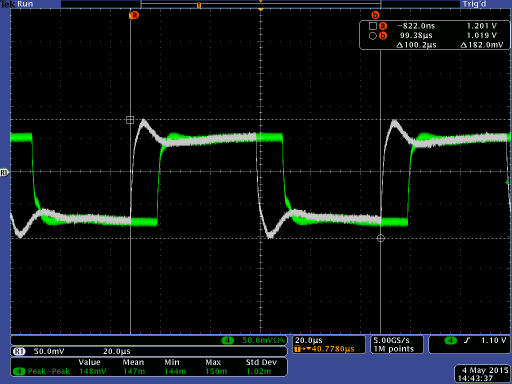


VCORE

##### ADAPTIVE TRANSIENT ALGORITHM (ATA)

The IR35201 Adaptive Transient Algorithm (ATA) is a high speed non-linear control technique that allows compliance with CPU voltage transient load regulation requirements, with minimum output bulk capacitance for reduced system cost.

A high-speed digitizer measures both the magnitude and slope of the error signal to predict the load current transient. This prediction is used to control the pulse widths and the phase relationships of the PWM pulses. The ATA bypasses the PID control momentarily during load transients to achieve very wideband closed loop control and smoothly transitions back to PID control during steady state load conditions. [Figure 29](#_bookmark25) illustrates the transient performance improvement provided by the ATA showing the clear reduction in undershoot and overshoot. [Figure 30](#_bookmark26) is a zoomed-in scope capture of a load step, illustrating the fast reaction time of the ATA, and how the algorithm changes the pulse phase relationships. IR35201 provides the option to enable or disable this feature, using a digitally programmable bit.



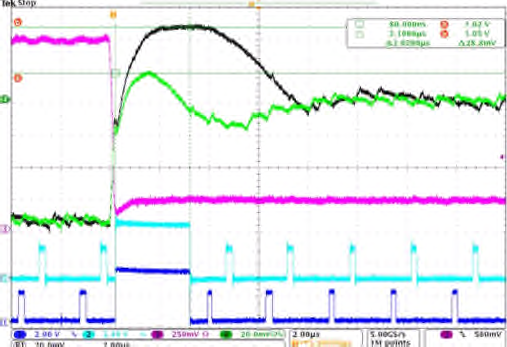
ATA Enabled

ATA Disabled

**Figure 29: ATA Enable/Disable Comparison**

**Figure 30: ATA feature – zoomed-in**

In addition, during a load transient overshoot, the ATA may also be programmed to turn off the low-side MOSFETS instead of leaving them on. This forces the load current to flow through the larger FET body diode, and helps to reduce the overshoot created during a load release, as showing in [Figure 31](#_bookmark27) below.



io e Em ation: Disabled Enabled

**Figure 31: Diode Emulation during a load release**

##### HIGH-SPEED PHASE BALANCE

The IR35201 provides phase balance during high frequency load oscillations. The balance is provided through phase skipping. Whenever a set error voltage threshold and load oscillation frequency threshold are exceeded for a particular phase, that phase is skipped, resulting in a lowering of current in the skipped phase and a corresponding increase in current in the other phases. Both these thresholds, listed in Table 20, are user programmable, to provide flexibility in high-speed phase balance for a wide variety of systems. In addition, the IR35201 allows the user to disable HSPB by resetting a bit in MTP.

**Table 20: High-speed thresholds**

|  |  |
| --- | --- |
| **Register** | **Function** |
| **Hspb\_enable** | Dedicated bit to enable/disable HSPB. Resetting this bit will result in the HSPB function not being activated, regardless of the error voltage or load oscillation frequency settings. |
| **Hspb\_hth** | Error Voltage threshold.  Activates HSPB when the threshold is exceeded.  **0mV – 60mV, 4mV resolution** |
| **Hspb\_fth** | Load Oscillation Frequency Threshold.  Activates HSPB when the load oscillation frequency is above threshold.  **0kHz – 703.5kHz, 46.9kHz resolution.** |

##### DYNAMIC VID SLEW RATE

The IR35201 provides the VR designer 16 fast slew rates each of which can be further configured to 4 different slow slew rates by selecting a slew rate setting as shown . *These slew rates can be further reduced ½, 1/4, 1/8, and 1/16*

##### DYNAMIC VID COMPENSATION

The IR35201 can compensate for the error produced by the current feedback in a system with AVP (Active Voltage Positioning) when the output voltage is ramping to a higher voltage. An output capacitance term and an AVP bandwidth term are provided in the MTP registers to help model the effects of variation in output voltage during a voltage ramp, due to the inrush current seen by the output bulk capacitors.

Once properly modeled, the output voltage will follow the DAC more closely during a positive dynamic VID, and provide better dynamic VID alert timing, as required by Intel® processors. [Figure 32](#_bookmark29) shows the effects that Dynamic VID Compensation has on the output voltage and the alert timing.

**Table 21: Slew Rates**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **mV/ µs** | **Fast Rate** | **x 1/2 Factor** | **x 1/4 Factor** | **x 1/8 Factor** | **x 1/16 Factor** |
| 10 | 5.0 | 2.50 | 1.25 | 0.0625 |
| 15 | 7.5 | 3.75 | 1.875 | 0.94 |
| 20 | 10 | 5.00 | 2.50 | 1.25 |
| 25 | 12.5 | 6.25 | 3.125 | 1.56 |
| 30 | 15 | 7.5 | 3.75 | 1.88 |
| 35 | 17.5 | 8.75 | 4.375 | 2.19 |
| 40 | 20 | 10 | 5.0 | 2.5 |
| 45 | 22.5 | 11.25 | 5.625 | 2.81 |
| 50 | 25 | 12.5 | 6.25 | 3.125 |
| 55 | 27.5 | 13.75 | 6.875 | 3.4375 |
| 60 | 30 | 15 | 7.5 | 3.75 |
| 65 | 32.5 | 16.25 | 8.125 | 4.0625 |
| 70 | 35 | 17.5 | 8.75 | 4.375 |
| 80 | 40 | 20 | 10 | 5 |
| 85 | 42.5 | 21.25 | 10.625 | 5.3125 |
| 95 | 47.5 | 23.75 | 11.875 | 5.9375 |

**Note:** The maximum DVID rate is limited by the inductor current available to charge the output capacitors. High DVID rates may not be possible if the output capacitor and inductor combination does not allow the output voltage to change at the selected rate.

**Figure 32: Dynamic VID Compensation**



DVID COMP ON; 3000uF

DVID COMP OFF

##### EFFICIENCY SHAPING

In addition to CPU-specified Power States, the IR35201 features Efficiency Shaping Technology that enables VR designers to cost-effectively maximize system efficiency. Efficiency Shaping Technology consists of Dynamic Phase Control to achieve the best VR efficiency at a given cost point.

##### POWER-SAVING STATES

The IR35201 uses Power States to set the power- savings mode. These are summarized in Table 22.

**Table 22: Power States**

**Power State**

**Mode**

**Recommended Current**

|  |  |  |
| --- | --- | --- |
| **Exit** | SVID Clock Toggle.  b) In Multi Mode – Any SetVID Command |  |

The Power States may be commanded through I2C/PMBus, the SVID interface, or the IR35201 can autonomously step through the Power States based upon the regulator conditions as summarized in [Table](#_bookmark30)

|  |  |  |
| --- | --- | --- |
| **PS0** | Full Power | Maximum |
| **PS1** | Light Load 1-2Φ | <20A |
| **PS2** | 1Φ Active Discontinuous  (Diode Emulation) | <5A |
| **PS3** | 1Φ Passive Discontinuous  (Diode Emulation) | <1A |
| **PS4** | Output Voltage DVID or Decay Down to zero depending upon configuration in “ps4\_dvid\_or\_decay” registor. PWM signals of all phases are tristated. | Near OFF |

23. PS4 can only be commanded with an SVID command

##### IVID REGISTER

IVID efficiency registers are new additions to the family of SVID registers of the IMVP8 specification. When sent an SVID command associated with IVID registers, IR35201 acknowledges the command and stores the received information into the IVID registers. However, IR35201 does not use the information received in IVID registers for any purpose. Instead, it uses the user set-up phase shed function to optimize the VR’s efficiency across the entire operating current range.

###### Table 23: Power State Entry/Exit

|  |  |  |
| --- | --- | --- |
|  | **Command Mode** | **Auto Mode** |
| **PS1**  **Entry** | 1. Command | n/a if Phase Shed enabled |
| **PS1**  **Exit** | 1. Command to PS0 2. DVID to PS0 3. Current limit to PS0 | n/a if Phase Shed enabled |
| **PS2**  **Entry** | 1. Command | Current level in 1Φ |
| **PS2**  **Exit** | 1. Command to PS1/0 2. DVID to PS0 3. Current limit to PS0 | Fsw > Fsw\_desired to PS0, DVID to PS0,  Current limit to PS0 |
| **PS3**  **Entry** | 1. Command | Current level in 1Φ |
| **PS3**  **Exit** | 1. Command to PS2/1/0 2. DVID to PS0 3. Current limit to PS0 | Fsw > Fsw\_desired to PS0, DVID to PS0,  Current limit to PS0 |
| **PS4**  **Entry** | 1. Command | n/a |
| **PS4** | 1. In Single Mode- Any | n/a |

.

##### DYNAMIC PHASE CONTROL (DPC) IN PS0

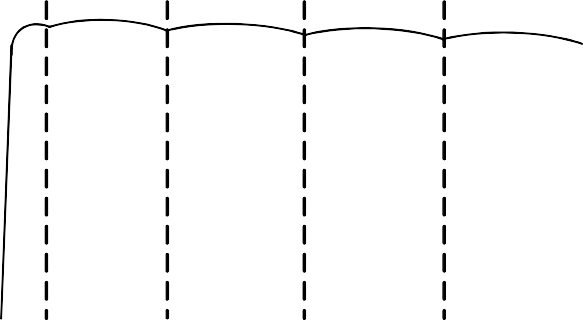
IR35201 optionally supports the ability to autonomously adjust the number of phases with load current, thus optimizing efficiency over a wide range of loads.

The output current level at which a phase is added can be programmed individually for each phase for optimum results (Table 24).

**Table 24: DPC Thresholds**

|  |  |
| --- | --- |
| **Register (2A steps)** | **Function** |
| **Phase1\_thresh** | 2Φ when I > Phase1\_thresh |
| **Phase2\_delta** | 3Φ when I > Phase1\_thresh +  Phase2\_delta |
| **Phase3\_delta** | 4Φ when I > Phase1\_thresh +  Phase2\_delta+Phase3\_delta |
| **Phase4\_delta** | 5Φ when I > Phase1\_thresh + Phase2\_delta+Phase3\_delta+ Phase4\_delta |
| **Phase5\_delta** | 6Φ when I > Phase1\_thresh + Phase2\_delta+Phase3\_delta+ Phase4\_delta+Phase5\_delta |
| **Phase6\_delta** | 7Φ and 8Φ when I > Phase1\_thresh + Phase2\_delta + Phase3\_delta + Phase4\_delta + Phase5\_delta + Phase6\_delta |

[As shown in Figure 33 (loop one, 8-phase example](#_bookmark31) shown), the designer can configure the VR to dynamically add or shed phases as the load current varies. Both control loops of the IR35201 have the DPC feature.



Programmable Threshold for Auto DCM

Per-phase Programmable Threshold for Auto Phase Shed

1Ø

2Ø

3Ø

8Ø

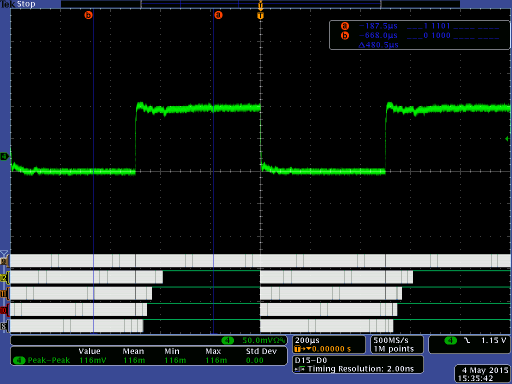
Load Current

Efficiency

DCM

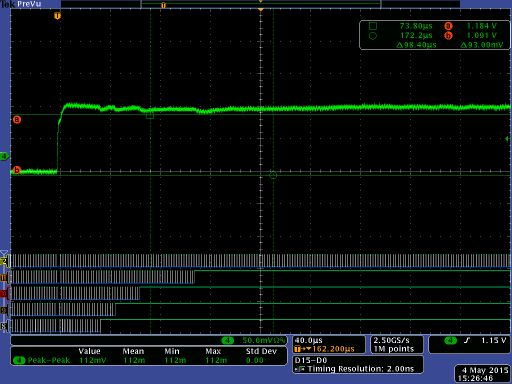
**Figure 33: Dynamic Phase Control Regions**

The IR35201 Dynamic Phase Control reduces the number of phases ([Figure 34](#_bookmark32)) based upon monitoring both the filtered total current and the error voltage over the DPC filter window. Monitoring the error voltage insures that the VR does not drop phases during large load oscillations.



**VCORE**

**Figure 34: Phase Shed 5Φ****1Φ**



**VCORE**

**PWM1**

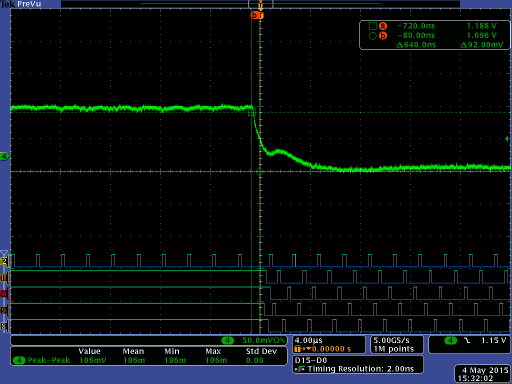
**PWM2**

**PWM3**

**PWM4**

**PWM5**

During a large load step, and based on the error voltage, the controller instantly goes to the maximum programmed number of phases. It remains at this level for a period equivalent to the DPC filter delay, after which phases get dropped depending on the load current. The Dynamic Phase Control (DPC) algorithm is designed to meet customer specifications even if the VR experiences a large load transient when operating with a lower number of phases. The ATA circuitry ensures that the idle phases are activated with optimum timing during a load step as shown in [Figure 35](#_bookmark33) and [Figure 36](#_bookmark34) below.



**VCORE**

**PWM1**

**PWM2**

**PWM3**

**PWM4**

**PWM5**

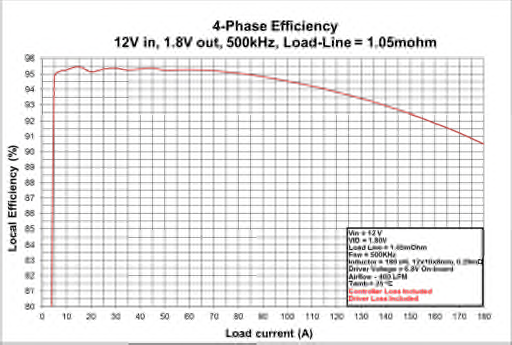
**Figure 35: Phase Add 1Φ****5Φ**

**Figure 36: Zoomed-out view of Phase Shed/Add**

Current limit and current balancing circuits remain active during ATA events to prevent inductor saturation and maintain even distribution of current across the active phases.

The add/drop points for each phase can be set in 2A increments from 0 to 62A per phase, with a fixed 4A hysteresis. This results in a uniform per-phase current density as the load increases or decreases.

Having DPC enabled optimizes the number of phases used in real time, Resulting in significant light and medium-load efficiency improvements, as shown in [Figure 37](#_bookmark35).



**Figure 37: Light Load Efficiency Improvement with DPC**

##### VARIABLE FREQUENCY WITH LOAD ON LOOP1

In addition, the controller can be made to operate at a high frequency when only a few phases are running, and lower the frequency as more phases are added. This skew feature is based on monitoring the per- phase current. The different skews of the switching frequency available are:

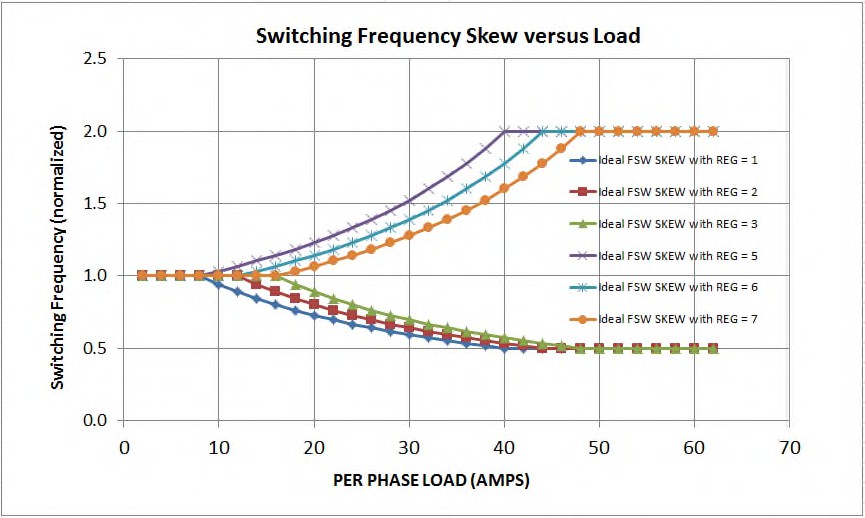
**Table 25: Switching Period Skew Factor Options**

|  |  |
| --- | --- |
| **de\_pw** | Sets the duration of the ON time pulse in 40ns steps during diode emulation. |
| **off\_time\_adj** | Reduces the calculated low-side FET ON time during diode emulation in 60ns  steps. Useful for compensating for DrMOS or other drivers’ tri-state delay for better zero-crossing prediction. |

|  |  |
| --- | --- |
| **Switching Period Skew Range** | **Per-Phase Starting Current (A)** |
| Fsw to 2 x Fsw | **8** |
| Fsw to 2 x Fsw | **12** |
| Fsw to 2 x Fsw | **16** |
| Fsw to 0.5 x Fsw | **8** |
| Fsw to 0.5 x Fsw | **12** |
| Fsw to 0.5 x Fsw | **16** |

Note: Per Phase Current is limited to 62A in normal mode, 124A in doubler mode.

Using the above feature, the switching frequency can be skewed based on the different register settings and per-phase currents – the switching frequency skew factor versus per-phase currents have been plotted in [Figure 38](#_bookmark36) below for 3 of the register settings for reference.



**Figure 38: Normalized Switching Frequency**

##### DISCONTINUOUS MODE OPERATION - PS2, PS3

Under very light loads, the VR efficiency is dominated by MOSFET switching losses. In PS2 mode, the IR35201 operates as a constant on-time controller where the user sets the desired peak-to-peak ripple by programming an error threshold and an on-time duration (Table 26). PS3 operation is identical to PS2, with the additional ability to disable the internal current sense amplifiers within the controller for further reduction in power consumption.

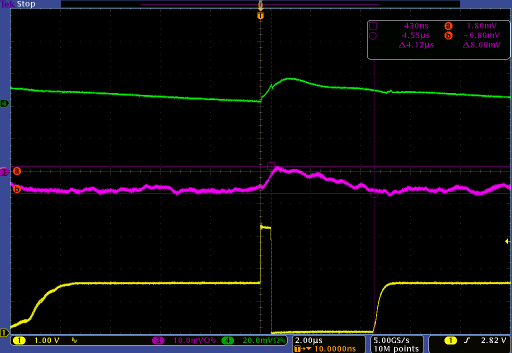
**Table 26: PS2/PS3 Mode Constant On-time Control**

|  |  |
| --- | --- |
| **MTP Register** | **Function** |
| **ni\_thresh** | Sets the current level below which PS2/PS3 is entered. |
| **de\_thresh** | Sets the error threshold to start a pulse during diode emulation, in 3mV resolution. |

In PS2 mode (Active Diode Emulation Mode), the internal circuitry estimates when the inductor current declines to zero on a cycle-by-cycle basis, and shuts off the low-side MOSFET at an appropriate time in each cycle ([Figure 39](#_bookmark37)). This effectively lowers the switching frequency, resulting in lowered switching losses and improved efficiency.

Industry standard tri-state drivers typically have delays when entering tri-state, typically 150ns to 300ns, which allows negative current to build up, causing switch node ringing and reducing efficiency.

The off\_time\_adj variable allows for compensation of the tri-state delay by reducing the low-side FET on- time by an equivalent amount.



VOUT

Zero-crossing prediction at the correct time

IΦ1

Programmed on-time

Calculated low-side FET on-time

PWM(Φ1)

**Figure 39: PS2 Active Diode Emulation Mode**

##### PS4 MODE

The IR35201 controller supports the PS4 command but does not reduce controller power consumption .

When a valid PS4 command is received by the controller, the IR35201 does the following:

* Acknowledge the command.
* Output voltage is DVID or Decay down to 0 Vdc depending upon the configuration in “ps4\_dvid\_or\_decay” register.
* PWM signals of all phases are tristated.

The controller does not shutdown the circuitry for lowest power consumption.

PS4 wake up can be set to wake on any SVID clock or alternatively on any SVID Set\_VID or SetPS0/1/2/3 command.

##### PS4 REGISTER SUPPORT

IR35201 controller supports SVID register “PS4 Exit Latency” (2B). This register holds the encoded value for PS4 exit latency calculated as

𝑥

𝐿𝑎𝑡𝑒𝑘𝑐𝑦 (𝜇𝑆) =  ∗ 2𝑦

16

Where x =bits[3:0], y = bits[7:4]

##### FAULTS & PROTECTION

The comprehensive fault coverage of the IR35201 protects the VR against a variety of fault conditions. Faults can be configured and monitored through the IR PowIRCenter GUI. There are two types of fault monitoring registers. In addition to real-time fault registers, there are “sticky” fault registers that can only be cleared with an I2C command or 3.3V power cycle. These will indicate if any fault has occurred since the last power cycle, even if the fault has cleared itself and the VR has resumed normal operation.Table 27 lists the available faults.

**Table 27: Sticky & Non-Sticky Faults**

|  |  |
| --- | --- |
| **Register Type** | **Faults** |
| Sticky | OTP, OCP, OVP, UVP, VIN UVLO, 3.3V UVLO,  phase-fault, slow-OCP |
| Non-Sticky |

###### Output Over-voltage Protection (OVP)

If the output voltage exceeds a user-programmable threshold (Table 32) above the VID set-point, the IR35201 detects an output over-voltage fault and latches ON the low-side MOSFETS to limit the output voltage rise.

**Table 28: OVP Action**

|  |
| --- |
| **OVP Action** |
| Low-side MOSFET latched on |
| Low-side MOSFET on until Output<0.248V |

Per Table 28 above, the low-side MOSFETs may be configured to either latch ON indefinitely ([Figure 40](#_bookmark38)) or stay ON until the output voltage falls below the release threshold ([Figure 41](#_bookmark39)), in case of an over-

voltage condition. This release mode reduces the undershoot of the output voltage during recovery from an OVP condition. If the output voltage rises above the OVP threshold during recovery, the low side MOSFET’s will again be turned on until Vout drops below the release threshold level. *Note that OVP is disabled during a DVID-down event to prevent false triggering.*

During soft-start, OVP is triggered at a user-selectable level from one of the thresholds listed in Table 29 below.

**Table 29: OVP Thresholds During Start-up**

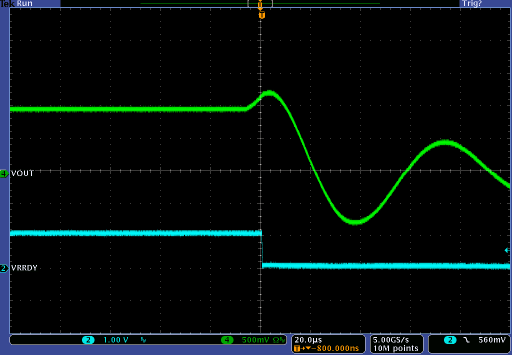
|  |  |
| --- | --- |
| **Value** | **Threshold** |
| 0 | 2.5V |
| 1 | 1.2V |
| 2 | 1.275V |
| 3 | 1.35V |

The IR35201 also provides the option to allow OVP to remain active when the device is disabled, in order to prevent system leakage from causing over-voltage on the output (Table 30).

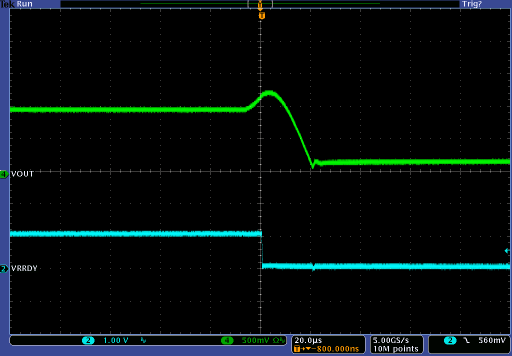
*Note: OVP functionality is only available when both the controller and drivers or power stages have Vcc power.*

**Table 30: OVP Options**

|  |  |
| --- | --- |
| **OVP\_when-disabled setting** | **When active** |
| On | IC disabled & IC enabled |
| Off | IC enabled |

****

**Figure 40: OVP - MOSFET latched on**



**Figure 41: OVP - MOSFET released when output<0.3V**

###### Output Under-voltage Protection (UVP)

The IR35201 detects an output under-voltage condition if the sensed voltage at the CPU is below the user-programmable UVP threshold ([Table 3](#_bookmark40)2) or a fixed 248mV (if the ADC detection is used instead of the comparator), as shown inTable 31.

**Table 31: UVP Threshold Options**

Use the ADC

Use the common comparator

The user also has the option to choose if the threshold needs to factor in the load line or not. Upon detecting an output under-voltage condition, the IR35201 responds in the same manner as the OCP, according to the setting selected inTable 33.

**TABLE 32: OVP & UVP THRESHOLDS**

|  |  |
| --- | --- |
| **Value** | **Threshold** |
| 0 | 50mV |
| 1 | 100mV |
| 2 | 150mV |
| 3 | 200mV |
| 4 | 250mV |
| 5 | 300mV |
| 6 | 350mV |
| 7 | 400mV |

###### Over-current Protection (OCP)

The IR35201 provides a programmable output over- current protection threshold of up to 62A per phase. This would translate to an overall maximum system OCP threshold of 62A times the number of phases.

The controller action during an OCP event can be configured as shown in TABLE 33. *Note that the OCP protection is disabled during start up and during VID transitions. Also, the threshold scales by a factor of 2x in the doubler mode and 4x in the quad mode.*

**Table 33: OCP & UVP Mode Selection**

|  |
| --- |
| **OCP/UVP Behavior Mode** |
| Per phase OCP Threshold (0 to 62A) |
| Shutdown immediately (cycle power or enable to restart) |
| Hiccup 2X before Shutdown |
| Hiccup indefinitely |

###### Slow Current Limit

In addition to the (fast) OCP, a Slow Current Limit can be programmed to monitor and protect against the thermal effects of the average current over time. This allows the system designer to operate close to the TDP level of the system. The slow current limit bandwidth is set by the telemetry bandwidth to one of the following options:

**Table 34: Telemetry Bandwidth Setting Options**

|  |  |
| --- | --- |
| **Value** | **Bandwidth (Hz)** |
| 0 | 0.69 |
| 1 | 1.39 |
| 2 | 2.78 |
| 3 | 5.55 |
| 4 | 11.1 |
| 5 | 22.2 |
| 6 | 44.6 |
| 7 | 89.5 |

When the slow OCP threshold is exceeded, the VR will shut down based upon the OCP mode programmed in the MTP.

*Note that the slow OCP protection is disabled during start up and during VID transitions.*

###### VR\_HOT and Over Temperature Protection (OTP)

The IR35201 provides a temperature measurement capability at the TSEN pin that is used for over temperature protection, VR\_HOT flag and temperature monitoring. The temperature is measured with either an NTC network or by monitoring IR PowIRstage temperature reporting outputs. Sense devices need to be placed close to the thermal hot spot for optimal performance. The thresholds are

programmable in 1°C increments within the range shown in Table 35. If the measured temperature exceeds the OTP threshold, the IR35201 will latch off the VR, requiring a system power recycle or an ENABLE recycle to resume operation.

**TABLE 35: VR\_HOT & OTP**

|  |
| --- |
| **Function** |
| VR\_HOT threshold (64°C to 127°C) |
| OTP threshold (VR\_HOT + 0°C to 32°C) max 135°C MAX 158C with IR3555 temp sense |

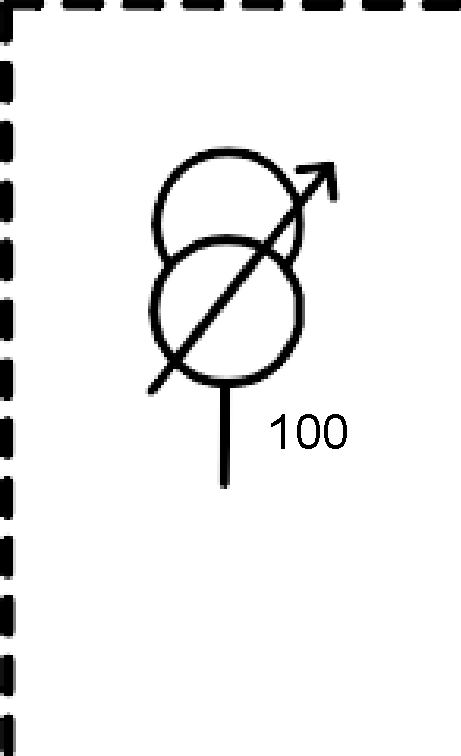
###### NTC Temperature Sense

The IR35201 includes a pre-programmed look-up table that is optimized for the recommended NTC options shown in Table 36. The NTC network is connected to the TSEN pin as shown in [Figure 42](#_bookmark41).

A 0.01µF capacitor is recommended for filtering when used with the NTC sense network.

**Table 36: NTC Temperature Sense Range**

|  |  |  |
| --- | --- | --- |
| **NTC** | **Value** | **Rparallel** |
| Murata NCP15WB473F03RC or Panasonic ERT-J0EP473J | 47KΩ | 13KΩ |



**Figure 42: Temperature Sense NTC Network**

###### IR Power Stage Temperature Sense

The controller is designed to interface to the IR3555 power stage to receive temperature and fault information from the IR3555 power stage. The power stage temperature output is scaled to 8mV/C and a 1:1.64 divider is required to scale this down to the

4.88mV/C gain of the controller input as shown in [Figure 43](#_bookmark42). Fault communication from the IR3555 is a

3.3Vdc high. The 3.3Vdc high from the power stage indicates either 1) a power stage phase fault, 2) an over temperature, 3) a persistent overcurrent or 4) an

over voltage condition. The controller will shut down and assert the CAT\_FLT pin (high) upon receiving the power stage fault.

To controller



TSEN

6.49KOhm

TOUT

From IR3555 100pF 10KOhm

**Figure 43: Temperature Sense IR Power Stage Network**

###### VR\_HOT\_ICRIT Pin Functionality Options

The functionality of the VR\_HOT\_ICRIT pin can be set to assert when levels of Temp\_max, Icc\_max, and/or OCP levels are exceeded. [Table](#_bookmark43) 37 shows the multiple configurations of the VR\_HOT\_ICRIT pin.

**Table 37: Vr\_Hot\_Icrit Pin Options**

|  |
| --- |
| Temp\_max Only |
| Temp\_max or Icc\_max |
| Temp\_max or OCP |
| Icc\_max Only |

###### Icritical Flag

The IR35201 VR\_HOT\_ICRIT pin can optionally be programmed to assert when a user programmable output current level is exceeded. The assertion is not a fault, and the VR continues to regulate. I\_CRITICAL monitors a long term averaged output current, which is a useful indicator of average operating current and thermal condition. The user can select between the I\_CRITICAL filters bandwidths shown in [Table](#_bookmark44) 38.

**Table 38: I\_critical Over-Current Options**

|  |  |
| --- | --- |
| **Value** | **Bandwidth (Hz)** |
| 0 | 0.69 |
| 1 | 1.39 |
| 2 | 2.78 |
| 3 | 5.55 |
| 4 | 11.1 |
| 5 | 22.2 |
| 6 | 44.6 |
| 7 | 89.5 |

I\_CRITICAL has a 5% hysteresis level and the VR\_HOT\_ICRIT pin will de-assert when the average output current level drops below 95% of the programmed current level threshold.

###### Input Over-voltage Protection

The IR35201 offers protection against input supply over- voltage. When enabled (Table 39), the VINSEN pin is compared to a fixed threshold of 14.5V with a 14:1 divider, and shuts down the IC if the threshold is exceeded.

**Table 39: Input Over-voltage Options**

enabled

disabled

###### Phase Faults

The IR35201 can detect and declare a phase fault when the current in one or more phases is too high or too low. It detects the fault when the duty cycle of a particular phase is 5% higher or lower than the average duty cycle of all the phases. This feature helps detect severe imbalances in the phase currents, an unpowered or damaged MOSFET driver, or a phase that is disconnected from Vin. The phase fault feature can be enabled or disabled through an MTP bit. When a phase fault occurs, the controller shuts down the loop where the fault occurred, and sets register bits to display which phase had the fault and whether it faulted high or low.

The phase fault registers are cleared via a register bit and the VR will restart once ENABLE or Vcc is cycled.

**Table 40: Phase Current Fault Registers**

|  |  |
| --- | --- |
| **Register** | **Function** |
| **pi\_fault\_en** | Enables phase current fault shutdown. |
| **clear\_phase\_faults** | Clears all phase faults for each loop. |
| **pi\_fault** | Indicates which phase has a phase current fault. 0 – phase1, 1 – phase2, 2 – phase3, 3 – phase4…7-phase 8 |
| **max\_cond** | Indicates one or more phase currents are too high. |
| **min\_cond** | Indicates one or more phase currents are too low. |

### I2C/PMBUS COMMUNICATION

The IR35201 simultaneously supports I2C and PMBus through the use of exclusive addressing. This means that a motherboard PMBus master may communicate with as many as 127 IR35201-based VRs. Optionally, a resistor offset can be enabled as shown in [Table 41](#_bookmark45)

(note that a 0.01µF capacitor is required across the resistor per [Figure 44)](#_bookmark47), with the offsets shown in [Table 42.](#_bookmark46)

As an example, setting a base 7-bit I2C address of 28h with a resistor offset of +15 sets the 7-bit I2C address to 37h. Similarly setting a base 7-bit PMBus address of 40h with a resistor offset of +15 sets the 7-bit PMBus address to 4Fh.

The IR35201 can also set the I2C address indepen- dently from the PMBus address. By using a 7-bit address the user can configure the device to any one of 127 different I2C addresses.

Once the address of the IR35201 is set, it is locked to protect it from being overridden.

For default programmed devices, the I2C/PMBus address can be temporarily forced to address 0Ah for I2C and 0Dh for PMBus by setting EN=VR\_HOT=low*.*

**TABLE 41: I2C OFFSET OPTIONS**

|  |  |
| --- | --- |
| **Enable\_I2C Addr\_Offset MTP bit** | **I2C Address Offset** |
| 0 | disabled |
| 1 | enabled |

**Table 42: ADDR Resistor Offset**

|  |  |
| --- | --- |
| **ADDR Resistor** | **I2C Address Offset** |
| 0.845kΩ | +0 |
| 1.30kΩ | +1 |
| 1.78kΩ | +2 |
| 2.32kΩ | +3 |
| 2.87kΩ | +4 |
| 3.48kΩ | +5 |
| 4.12kΩ | +6 |
| 4.75kΩ | +7 |
| 5.49kΩ | +8 |
| 6.19kΩ | +9 |
| 6.98kΩ | +10 |
| 7.87kΩ | +11 |
| 8.87kΩ | +12 |
| 10.00kΩ | +13 |
| 11.00kΩ | +14 |
| 12.10kΩ | +15 |

*Note: Extends the range of PMBus addresses.*



**Figure 44: ADDR pin components**

20%

15%

10%

Iout Error

CPU spec with 7% inductors

5%

0%

0 10 20 30 40 50 60 70 80 90 100

-5%

-10%

-15%

-20%

**E-Load (A)**

Error

### REAL-TIME I2C MONITORING FUNCTIONS

IR35201 provides real-time accurate measurement of input voltage, input current, output voltage, output current and temperature over the I2C interface.

Output voltage is calculated based upon the VID setting and load line, and the result is reported through the I2C.

###### Accuracy Optimization Registers

The IR35201 provides excellent factory-trimmed chip accuracy. In addition, the designer has calibration capability that can be used to optimize reporting accuracy for a given design, with minimum component changes. Once a design is optimized, the IR35201 provides excellent repeatability from board to board.

The IR35201 also provides capability for individual board calibration and programming in production for best accuracy.

[Table 43 shows the MTP registers used to fine tune](#_bookmark48) the accuracy of the reported measurements. [Figure](#_bookmark49) [45 to](#_bookmark49) [F](#_bookmark50)[igure 47 show the typical accuracy of the](#_bookmark49) output current, input voltage and output voltage measurements using the IR35201.

**Table 43: Accuracy Optimization Registers**

|  |  |
| --- | --- |
| **NVM Register** | **Function** |
| **IIN Fixed Offset** | Offsets the input current in 1/32A steps. |
| **IIN Per Phase Offset** | Offsets the input current dependent upon the number of active phases in 1/128A steps e.g. the drive current for the MOSFET’s. This current increases every time a new phase is added. |
| **IOUT Current Offset** | Offsets the output current from  -2A to +1.875A per phase in 0.125A steps |
| **Vout Offset** | Offsets the output voltage +40mV to -35mV in 5mV steps (Intel® VR12 mode), or +80mV to  -70mV in 10mV steps (Intel® VR12.5 mode). |
| **Temperature Offset** | Offsets the temperature +31°C to -32°C in 1°C steps to compensate for offset between the hottest component and the NTC sensing location. |
| **Duty Cycle Adjust** | Adjusts the input current calculation to compensate for a non-ideal driver. |

**Figure 45: I2C IOUT Error using 10% DCR Inductors**

**Figure 46: I2C Input Voltage Measurements**

12.3

**1.0%**

12.2

**0.5%**

12.1

12

**0.0%**

11.9

Vin (DMM) Vin (I2C)

Vin error (2nd axis)

**-0.5%**

11.8

11.7

**-1.0%**

0

20

40

60

80

100

**E-Load (A)**

1.050

**1.00%**

1.025 **0.75%**

1.000 **0.50%**

0.975 **0.25%**

0.950 **0.00%**

0.925 **-0.25%**

0.900 **-0.50%**

0.875 **-0.75%**

0.850 **-1.00%**

0 20 40 60 80 100

**E-Load (A)**

**Vin (V)**

Vout (V)

**Error**

**Error**

Vout (DMM) Vout (I2C)

Vout error (2nd axis)

**Figure 47: I2C Output Voltage Measurements**

**I2C SECURITY**

The IR35201 provides robust and flexible security options to meet a wide variety of customer applications. A combination of hardware pin and software passwords prevent accidental overwrites, discourages hackers, and secures custom configurations and operating data. The Read and Write Security can be in set in MTP ([Table](#_bookmark51) 44 and [Table](#_bookmark52) 45) with the protection methods shown in [Table](#_bookmark53) 46.

**Table 44: Read Security**

|  |
| --- |
| No Protection |
| Configuration Registers Only |
| Protect All Registers But Telemetry |
| Protect All |

**Table 45: Write Security**

|  |
| --- |
| No Protection |
| Configuration Registers Only |
| Protect All |

**Table 46: Read or Write Unlock Options**

|  |
| --- |
| Password Only |
| Pin Only |
| Pin & Password |
| Lock Forever |

###### Password Protection

The system designer can set any 16-bit password (other than 00h). This password is stored in MTP. To unlock, a user must write the correct password into the “Password Try” register, which is a volatile read/write register. After four incorrect tries, the IC will lock up to prevent unauthorized access.

**T**

|  |  |  |  |
| --- | --- | --- | --- |
| **Pointer Value** | **Reading** | **Signal bandwidth** | **Resolution of reading value** |
| 0 | loop\_1\_current\_min | 62 KHz/ 3.93  KHz (based on minmax  \_output\_i\_bw) | 2A |
| 1 | loop\_1\_current\_max |
| 2 | loop\_2\_current\_min | 0.5A |
| 3 | loop\_2\_current\_max |
| 4 | loop\_1\_input  \_current\_min | 102Hz | 0.125A |
| 5 | loop\_1\_input  \_current\_max |
| 6 | loop\_2\_input  \_current\_min | 0.0625A |
| 7 | loop\_2\_input  \_current\_max |
| 8 | loop\_1\_output\_ voltage\_min | Telemetry\_bw | 0.0625V |
| 9 | loop\_1\_output\_ voltage\_max |
| 10 | loop\_2\_output\_ voltage\_min |
| 11 | loop\_2\_output\_ voltage\_max |
| 12 | input\_voltage\_min | 760Hz | 0.125V |
| 13 | input\_voltage\_max |
| 14 | temp1\_min | Telemetry\_bw | 1 C |
| 15 | temp1\_max | 1 C |
| 16 | temp2\_min | Telemetry\_bw | 1 C |
| 17 | temp2\_max | 1 C |

**Min/Max Registers**

Min/Max registers for IOUT, IIN, VOUT, VIN, and TEMPERATURE are available. The data is read by setting a pointer and reading the value from a register that contains the minimum and maximum data. These registers store high and low values from startup or the last read, whichever was the latest to occur. The registers are automatically cleared when the data is read back from the controller

The minmax\_sel[4:0] register is the pointer used to select the appropriate signal and the minmax\_val[7:0] register will show the min or max value of what has been selected. The list of available min/max values, bandwidth, and resolutions are shown in [Table](#_bookmark54) 50.

**TABLE 50: MIN/MAX REGISTER SETTINGS**

**able 47: Password Registers**

|  |  |  |
| --- | --- | --- |
| **Register** | **Length** | **Location** |
| Password | 16 bit (2 bytes) | MTP |
| Try | 16 bit (2 bytes) | R/W |

The following pseudo-code illustrates how to change a password:

*# first unlock the IC*

*Write old password high Byte to R/W high Byte Try register Write old password low Byte to R/W low Byte Try register*

*# now write new password into MTP*

*Write new password high Byte to high Byte Password register*

*# password has changed! Must unlock to change the low byte Write new password high Byte to R/W high Byte Try register Write new password low Byte to low Byte Password register*

*# password change complete, status is locked*

*# Need to write new low byte to Try register to unlock*

###### Pin Protection

The ADDR/PROTECT pin is a dual function pin.

When the IC is enabled, the resistor value is latched and stored for use in the I2C address offset function.

Thereafter, the pin acts entirely as a PROTECT pin. If enabled, the PROTECT pin must be driven high to unlock and low to lock. If the resistor address offset

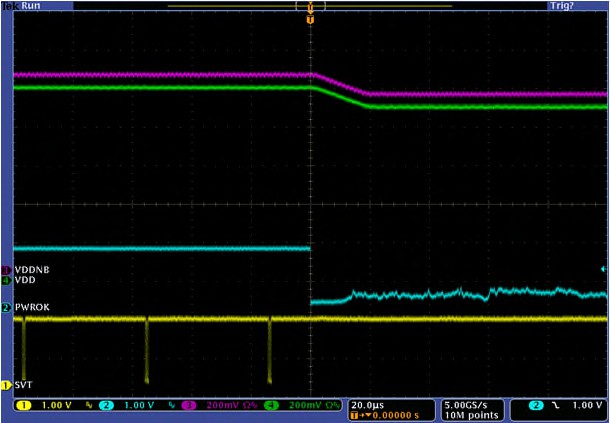
function is being used, care must be taken to allow the IC to read the resistor value before driving the pin high or low to set the security state. Failure to follow this precaution may result in an erroneous address offset value being latched in. The user should at least wait until the completion of the auto-trim time t4 in [Figure](#_bookmark3) 6.

### AMD SVI2 MODE

When the power-on sequence is initiated, both rails will ramp to the configured Vboot voltage and assert the PWRGD on each loop. The soft-start occurs at the

½ or ¼ multiplier slew rate as selected in [Table](#_bookmark55) 51.

**Table 51: Slew Rates**



**PWROK**

|  |  |  |  |
| --- | --- | --- | --- |
| **mV/µs** | **FAST rate** | **½ Multiplier** | **¼ Multiplier** |
| 10 | 5.0 | 2.50 |
| 15 | 7.5 | 3.75 |
| 20 | 10 | 5.00 |
| 25 | 12.5 | 6.25 |

The boot voltage is decoded from the SVC and SVD levels when the EN pin is asserted high as shown in Table 52. This value is latched and will be re-used in the event of a soft reset (de-assertion and re-assertion of PwrOK).

###### Note: VCC and VDDIO must be stable for a minimum 5ms before the IC is enabled to ensure that the Boot voltage is decoded from the SVC, SVD pins correctly.

**TABLE 52: AMD SVI BOOT TABLE**

|  |  |  |
| --- | --- | --- |
| **Boot Voltage** | **SVC** | **SVD** |
| 1.1V | 0 | 0 |
| 1.0V | 0 | 1 |
| 0.9V | 1 | 0 |
| 0.8V | 1 | 1 |

Alternatively, the AMD Boot voltage can be set by an MTP register instead of decoding the SVC, SVD pins as shown in Table 53. Boot values are shown in Table 54.

**Table 53: AMD Boot Options**

|  |  |
| --- | --- |
| **MTP Boot Register** | **Boot Location** |
| Bit[7] = low | Decode from SVC, SVD pins per Table 52 |
| Bit[7] = high | Use MTP boot register bits [6:0] |

###### PWROK De-assertion

The IR35201 responds to SVI commands on the SVI bus interface when PWROK is high. In the event that PWROK is de-asserted the controller resets the SVI state machine, drives the SVT pin high and returns to the Boot voltage, initial load line slope and offset.

**Figure 49: PWROK De-assertion**

###### SVI2 Interface

The IR35201 implements a fully compliant AMD SVI2 Serial VID interface (SVI). SVI2 is a three-wire interface between a SVI2 compliant processor and a VR. It consists of clock, data, and telemetry/alert signals. The processor will send a data packet with the clock (SVC) and data (SVD) lines. This packet has SVI commands to change VID, go to a low power state, enable and configure telemetry, change load line slope and change VID offset. The VR, when configured to do so, will send telemetry to the processor. The telemetry data consists of voltage only, or voltage and current of each output rail (VDD, VDDNB). The telemetry line (SVT) is also used as an alert signal (VOTF complete) to alert the processor when a positive going VID change in complete, or an offset or load line scale change has occurred.

###### VID Change

The IR35201 accepts an 8-bit VID within the SVD packet and will change the output voltage at the FAST rate specified in [Table](#_bookmark55) 51 of one or both of the loops based on the VID in [Table 54](#_bookmark56). This is a VID-on-the-fly- request (VOTF Request).

**TABLE 54: SVI2 VID TABLE**

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **VID**  **(Hex)** | **Voltage (V)** | **VID**  **(Hex)** | **Voltage (V)** | **VID**  **(Hex)** | **Voltage (V)** | **VID**  **(Hex)** | **Voltage (V)** | **VID**  **(Hex)** | **Voltage (V)** |
| 0 | 1.55000 | 32 | 1.23750 | 64 | 0.92500 | 96 | 0.61250 | C8 | 0.30000 |
| 1 | 1.54375 | 33 | 1.23125 | 65 | 0.91875 | 97 | 0.60625 | C9 | 0.29375 |
| 2 | 1.53750 | 34 | 1.22500 | 66 | 0.91250 | 98 | 0.60000 | CA | 0.28750 |
| 3 | 1.53125 | 35 | 1.21875 | 67 | 0.90625 | 99 | 0.59375 | CB | 0.28125 |
| 4 | 1.52500 | 36 | 1.21250 | 68 | 0.90000 | 9A | 0.58750 | CC | 0.27500 |
| 5 | 1.51875 | 37 | 1.20625 | 69 | 0.89375 | 9B | 0.58125 | CD | 0.26875 |
| 6 | 1.51250 | 38 | 1.20000 | 6A | 0.88750 | 9C | 0.57500 | CE | 0.26250 |
| 7 | 1.50625 | 39 | 1.19375 | 6B | 0.88125 | 9D | 0.56875 | CF | 0.25625 |
| 8 | 1.50000 | 3A | 1.18750 | 6C | 0.87500 | 9E | 0.56250 | D0 | 0.25000 |
| 9 | 1.49375 | 3B | 1.18125 | 6D | 0.86875 | 9F | 0.55625 | D1 | 0.24375 |
| A | 1.48750 | 3C | 1.17500 | 6E | 0.86250 | A0 | 0.55000 | D2 | 0.23750 |
| B | 1.48125 | 3D | 1.16875 | 6F | 0.85625 | A1 | 0.54375 | D3 | 0.23125 |
| C | 1.47500 | 3E | 1.16250 | 70 | 0.85000 | A2 | 0.53750 | D4 | 0.22500 |
| D | 1.46875 | 3F | 1.15625 | 71 | 0.84375 | A3 | 0.53125 | D5 | 0.21875 |
| E | 1.46250 | 40 | 1.15000 | 72 | 0.83750 | A4 | 0.52500 | D6 | 0.21250 |
| F | 1.45625 | 41 | 1.14375 | 73 | 0.83125 | A5 | 0.51875 | D7 | 0.20625 |
| 10 | 1.45000 | 42 | 1.13750 | 74 | 0.82500 | A6 | 0.51250 | D8 | 0.20000 |
| 11 | 1.44375 | 43 | 1.13125 | 75 | 0.81875 | A7 | 0.50625 | D9 | 0.19375 |
| 12 | 1.43750 | 44 | 1.12500 | 76 | 0.81250 | A8 | 0.50000 | DA | 0.18750 |
| 13 | 1.43125 | 45 | 1.11875 | 77 | 0.80625 | A9 | 0.49375 | DB | 0.18125 |
| 14 | 1.42500 | 46 | 1.11250 | 78 | 0.80000 | AA | 0.48750 | DC | 0.17500 |
| 15 | 1.41875 | 47 | 1.10625 | 79 | 0.79375 | AB | 0.48125 | DD | 0.16875 |
| 16 | 1.41250 | 48 | 1.10000 | 7A | 0.78750 | AC | 0.47500 | DE | 0.16250 |
| 17 | 1.40625 | 49 | 1.09375 | 7B | 0.78125 | AD | 0.46875 | DF | 0.15625 |
| 18 | 1.40000 | 4A | 1.08750 | 7C | 0.77500 | AE | 0.46250 | E0 | 0.15000 |
| 19 | 1.39375 | 4B | 1.08125 | 7D | 0.76875 | AF | 0.45625 | E1 | 0.14375 |
| 1A | 1.38750 | 4C | 1.07500 | 7E | 0.76250 | B0 | 0.45000 | E2 | 0.13750 |
| 1B | 1.38125 | 4D | 1.06875 | 7F | 0.75625 | B1 | 0.44375 | E3 | 0.13125 |
| 1C | 1.37500 | 4E | 1.06250 | 80 | 0.75000 | B2 | 0.43750 | E4 | 0.12500 |
| 1D | 1.36875 | 4F | 1.05625 | 81 | 0.74375 | B3 | 0.43125 | E5 | 0.11875 |
| 1E | 1.36250 | 50 | 1.05000 | 82 | 0.73750 | B4 | 0.42500 | E6 | 0.11250 |
| 1F | 1.35625 | 51 | 1.04375 | 83 | 0.73125 | B5 | 0.41875 | E7 | 0.10625 |
| 20 | 1.35000 | 52 | 1.03750 | 84 | 0.72500 | B6 | 0.41250 | E8 | 0.10000 |
| 21 | 1.34375 | 53 | 1.03125 | 85 | 0.71875 | B7 | 0.40625 | E9 | 0.09375 |
| 22 | 1.33750 | 54 | 1.02500 | 86 | 0.71250 | B8 | 0.40000 | EA | 0.08750 |
| 23 | 1.33125 | 55 | 1.01875 | 87 | 0.70625 | B9 | 0.39375 | EB | 0.08125 |
| 24 | 1.32500 | 56 | 1.01250 | 88 | 0.70000 | BA | 0.38750 | EC | 0.07500 |
| 25 | 1.31875 | 57 | 1.00625 | 89 | 0.69375 | BB | 0.38125 | ED | 0.06875 |

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **VID**  **(Hex)** | **Voltage (V)** | **VID**  **(Hex)** | **Voltage (V)** | **VID**  **(Hex)** | **Voltage (V)** | **VID**  **(Hex)** | **Voltage (V)** | **VID**  **(Hex)** | **Voltage (V)** |
| 26 | 1.31250 | 58 | 1.00000 | 8A | 0.68750 | BC | 0.37500 | EE | 0.06250 |
| 27 | 1.30625 | 59 | 0.99375 | 8B | 0.68125 | BD | 0.36875 | EF | 0.05625 |
| 28 | 1.30000 | 5A | 0.98750 | 8C | 0.67500 | BE | 0.36250 | F0 | 0.05000 |
| 29 | 1.29375 | 5B | 0.98125 | 8D | 0.66875 | BF | 0.35625 | F1 | 0.04375 |
| 2A | 1.28750 | 5C | 0.97500 | 8E | 0.66250 | C0 | 0.35000 | F2 | 0.03750 |
| 2B | 1.28125 | 5D | 0.96875 | 8F | 0.65625 | C1 | 0.34375 | F3 | 0.03125 |
| 2C | 1.27500 | 5E | 0.96250 | 90 | 0.65000 | C2 | 0.33750 | F4 | 0.02500 |
| 2D | 1.26875 | 5F | 0.95625 | 91 | 0.64375 | C3 | 0.33125 | F5 | 0.01875 |
| 2E | 1.26250 | 60 | 0.95000 | 92 | 0.63750 | C4 | 0.32500 | F6 | 0.01250 |
| 2F | 1.25625 | 61 | 0.94375 | 93 | 0.63125 | C5 | 0.31875 | F7 | 0.00625 |
| 30 | 1.25000 | 62 | 0.93750 | 94 | 0.62500 | C6 | 0.31250 | F6-FF | OFF |
| 31 | 1.24375 | 63 | 0.93125 | 95 | 0.61875 | C7 | 0.30625 |  |  |

###### PSI[x]\_L and TFN

PSI0\_L is Power State Indicator Level 0. When this bit is asserted the IR35201 will drop to 1 phase depending on configuration. This will only occur if the output current is low enough (typically <20A) to enter PSI0, else the VR will remain in full phase operation.

PSI1\_L is Power State Indicator Level 1. When this bit is asserted along with the PSI0\_L bit, the IR35201 will enter diode emulation mode. This will only occur if the output current is low enough (typically <5A) to enter PSI1, else the VR will enter PSI0\_L mode of operation.

TFN is an active high signal that allows the processor to control the telemetry functionality of the VR. If TFN=1, then the VR telemetry will be configured per [Table](#_bookmark57) 55.

**Table 55: TFN Truth Table**

|  |  |
| --- | --- |
| **VDD, VDDNB Domain Selector bit** | **Meaning** |
| 0, 0 | Telemetry is in voltage only mode. |
| 0, 1 | Telemetry is in voltage & current mode. |
| 1, 0 | Telemetry is disabled. |
| 1, 1 | Reserved. |

###### SVT Telemetry

The IR35201 has the ability to sample and report voltage and current for the VDD and VDDNB domains. The IR35201 reports this telemetry serially over the SVT wire which is clocked by the processor driven SVC. If in voltage-only telemetry mode then the sampled voltage for VDD and VDDNB are sent together in every SVT telemetry packet at a rate of 20kHz. If in voltage and current mode then the sampled voltage and current for VDD is sent out in one SVT telemetry packet followed by the sampled voltage and current for VDDNB in the next SVT telemetry packet at a rate of 40kHz. The voltage and current are moving averages based on the filters and update rates specified in the Electrical Specification Table. The voltage is reported as a function of the Set VID minus Iout times the Load Line Resistance. The current is reported as a percentage of the Icc\_max register, where a value of FFh represents 100% and 00h represents 0% of the Icc\_max setting. Resolution of the current reporting is 0.39% (1/256).

###### Load Line Slope Trim

The IR35201 has the ability for the processor to change the load line slope of each loop independently through the SVI2 bus while ENABLE and PWROK are asserted via the serial VID interface. The slope change applies to initial load line slope as set by the external RCSP/RCSM resistor network. The load line slope can be disabled or adjusted by -40%, -20%, 0%,

+20%, +40%, +60%, or +80%.

###### Offset Trim

The IR35201 has the ability for the processor to change the offset of each loop independently while ENABLE and PWROK are asserted via the serial VID interface. The offset can be left unchanged, disabled, or changed +25mV or -25mV.

###### Ispike/Dual OCP Support

The IR35201 has two current limit thresholds. One threshold is for short duration current spikes (Fast OCP). When this threshold, typically a percentage above the peak processor current, is exceeded, the VR quickly shuts down. The other threshold, typically a percentage above the thermal design current (TDC), is heavily filtered (Slow OCP) and shuts down the VR when the average current exceeds it. To meet AMD specifications, exceeding both thresholds will assert the OCP\_L (VR\_HOT) pin and delay the over-current shut down by 10usec for FAST threshold and 20usec for the SLOW threshold, typically. Figure 50 and Figure 51 show the delay action of the OCP shutdown with the OCP\_L (VR\_HOT) and PWRGD pins.



**Over-current detected**

**Vdd**

**Idd**

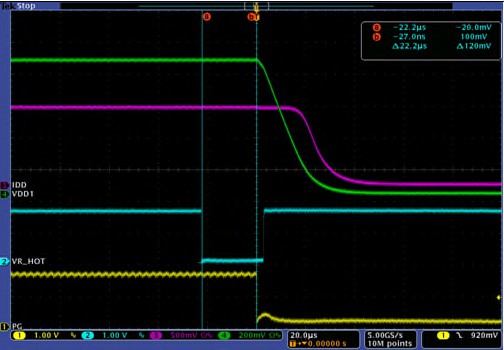
**OCP Delay (fast)**

**OCP\_L**

**PG**

**VR shuts down**

**Figure 50: OCP\_L (VR\_HOT) assertion with OCP\_spike (Fast) threshold. OCP delay action (11usec)**



**Over-current detected**

**Vdd**

**Idd**

**OCP Delay (slow)**

**OCP\_L**

**PG**

**VR shuts down**

**Figure 51: OCP\_L (VR\_HOT) assertion with OCP\_TDC (Slow) threshold. OCP delay action (22usec)**

###### Thermal Based Protection

The IR35201 can also assert the PROC\_HOT\_L (VR\_HOT) pin when the temperature of the VR exceeds a configurable temp\_max threshold (typically 100⁰ C). If the temperature continues to rise and exceeds a second configurable threshold (OTP\_thresh) then the VR will shut down and latch off. The VR can only be restarted if ENABLE or VCC is cycled.

###### AMD SVI Address Programming

By default, loop 1 is addressed as the VDD rail and loop 2 is addressed as the VDDNB rail which is sufficient for most applications. The IR35201 however, can also be configured with a single bit change to swap this addressing scheme so that loop 1 can be addressed as the VDDNB rail and loop 2 can be addressed as the VDD rail. This is for application where the VDDNB requires more than two phases and VDD only requires two.

# I2C PROTOCOLS

All registers may be accessed using either I2C or PMBus protocols. I2C allows the use of a simple format whereas PMBus provides error checking capability. [Figure](#_bookmark58) 52 shows the I2C format employed by the IR35201.





|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  |  |  |  |  |  |  |  |  |



|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
|  |  |  |  |  |  |  |

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
|  |  |  |  |  |  |  |

******Figure 52: I2C Format**



### PMBUS PROTOCOLS

To access IR’s configuration and monitoring registers, 4 different protocols are required:

* the PMBus Send Byte protocol with/without PEC (for CLEAR\_FAULTS only)
* the PMBus Read/Write Byte/Word protocol with/without PEC (for status and monitoring)
* the PMBus Block Read and Block Write protocols with Byte Count = 1 and Byte Count = 2
* the PMBus Block Read Process call (for accessing Configuration Registers)

An explanation of which command codes and protocols are required to access them is given in [Table](#_bookmark59) 6. In addition, the IR35201 supports:

* Alert Response Address (ARA)
* Bus timeout (30ms)
* Group Command for writing to many VRs within one command

**LEGEND:**

****



|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  |  |  |  |  |  |  |  |  |

**Figure 53: PMBus Send Byte**



|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  |  |  |  |  |  |  |  |  |  |  |

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
|  |  |  |  |  |  |  |  |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  |  |  |  |  |

**Figure 54: PMBus Write Byte/Word**



|  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  |  |  |  |  |  |  |  |  |  |  |  |

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  |  |  |  |  |  |  |  |  |

**Figure 55: PMBus Read Byte/Word**



****

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  |  |  |  |  |  |  |  |  |  |

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
|  |  |  |  |  |  |  |

**Figure 56: PMBus Block Read with Byte Count=1**



|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  |  |  |  |  |  |  |  |  |  |

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  |  |  |  |  |  |  |  |  |

**Figure 57: PMBus Block Read with Byte Count=2**

|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  |  |  |  |  |  |  |  |  |  |  |  |  |

**Figure 58: PMBus Block Write with Byte Count=1**

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

**Figure 59: PMBus Block Write with Byte Count=2**

|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  |  |  |  |  |  |  |  |  |  |  |  |  |

**Figure 60: MFR\_WRITE\_REG**

S

PMBus Address

W

Command D0h

Register Address

**...**

Sr

PMBus Address

R

A

A\*

N P

**Figure 61: MFR\_READ\_REG**

...

PEC\*

Address+1 Data Byte

A Data Byte

A

A

A

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| S | PMBus  Address | W | A | Command | A | 1 | A | Command | A |

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Sr | PMBus  Address | R | A | 1 | A | Data Byte | A\* | PEC\* | N | P |

**Figure 62: Block Read Process Call**



|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
|  |  |  |  |  |  |  |  |

|  |  |  |  |
| --- | --- | --- | --- |
|  |  |  |  |

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
|  |  |  |  |  |  |  |  |

|  |  |  |  |
| --- | --- | --- | --- |
|  |  |  |  |

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
|  |  |  |  |  |  |  |  |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  |  |  |  |  |

**Figure 63: Group Command**



**Table 56: PMBus Commands**

|  |  |  |  |
| --- | --- | --- | --- |
| **COMMAND** | **PMBUS PROTOCOL** | **COMMAND CODE** | **DESCRIPTION** |
| OPERATION | Read/Write Byte | 01h | Enables or disables the output and controls margining. Ignores OVP on Margin High, UVP on Margin Low. |
| ON\_OFF\_CONFIG | Read/Write Byte | 02h | Configures the combination of CONTROL pin and OPERATION command needed to turn the unit on and off. |
| CLEAR FAULTS | Send Byte | 03h | Clear contents of Fault registers |
| WRITE\_PROTECT | Read/Write Byte | 10h | Provides protection from accidental changes |
| RESTORE\_DEFAULT\_ALL | Send Byte | 12h | Reloads the OTP |
| CAPABILITY | Read Byte | 19h | Returns 1010xxxx to indicate Packet Error Checking is supported and Maximum bus speed is 400kHz |
| SMBALERT\_MASK | Block Write/ Block Read Process Call | 1Bh | Set to prevent warning or fault conditions from asserting the SMBALERT# signal. Write command code for STATUS register to be masked in the low byte, the bit to be masked in the High byte. |
| VOUT\_MODE | Read/Write Byte | 20h | Sets the format for VOUT related commands. Linear mode, -8 and -9 exponents supported. |
| VOUT\_COMMAND | Read/Write Word | 21h | Sets the voltage to which the device should set the output. Format according to VOUT\_MODE. |
| VOUT\_TRIM | Read/Write Word | 22h | Applies a fixed offset to the output voltage command value. Format according to VOUT\_MODE. |
| VOUT\_MAX | Read/Write Word | 24h | Sets an upper limit on the output voltage the unit can command. Format according to VOUT\_MODE. |
| VOUT\_MARGIN\_HIGH | Read/Write Word | 25h | Sets the margin high voltage when commanded by OPERATION. Must be in format determined by VOUT\_MODE. |
| VOUT\_MARGIN\_LOW | Read/Write Word | 26h | Sets the margin low voltage when commanded by OPERATION. Must be in format determined by VOUT\_MODE. |
| VOUT\_TRANSITION\_RATE | Read/Write Word | 27h | Sets the rate at which the output changes voltage due to VOUT\_COMMAND or OPERATION commands.  mV/s; exp = [0.-1,-2,-3,-4] |
| VOUT\_DROOP | Read/Write Word | 28h | Sets the rate at which the output voltage decreases or increases with increasing or decreasing output current for use with Adaptive Voltage Positioning. |
| VOUT\_SCALE\_LOOP | Read/Write Word | 29h | Sets the gain of the output voltage sensing circuitry to take |

|  |  |  |  |
| --- | --- | --- | --- |
| **COMMAND** | **PMBUS PROTOCOL** | **COMMAND CODE** | **DESCRIPTION** |
|  |  |  | into account an external resistor divider.  Fixed to E8 08h |
| FREQUENCY\_SWITCH | Read/Write Word | 33h | Sets the switching frequency in KHz per table found in user note UN00044. Exp = 0, 1 |
| VIN\_ON | Read/Write Word | 35h | Sets the value of the input voltage at which the unit should begin power conversion. Exp = -1. |
| VIN\_OFF | Read/Write Word | 36h | Sets the value of the input voltage that the unit, once operation has started, should stop power conversion. Exp = -1. |
| IOUT\_CAL\_OFFSET | Read/Write Word | 39h | Used to null out any offsets in the output current sensing circuitry. Exp = -2. |
| VOUT\_OV\_FAULT\_LIMIT | Read Only | 40h | Returns the value of the output voltage, measured at the sense or output pins, that causes an output overvoltage fault. |
| VOUT\_OV\_FAULT\_RESPONSE | Read/Write Byte | 41h | Instructs the device on what action to take in response to an output overvoltage fault. Only shutdown and ignore are supported. |
| VOUT\_OV\_WARN\_LIMIT | Read/Write Word | 42h | Sets the value of the output voltage, measured at the sense or output pins, that causes an output overvoltage warning. Format as determined by VOUT\_MODE. |
| VOUT\_UV\_WARN\_LIMIT | Read/Write Word | 43h | Sets the value of the output voltage, measured at the  sense or output pins, that causes an output voltage low warning. Format as determined by VOUT\_MODE. |
| VOUT\_UV\_FAULT\_LIMIT | Read Only | 44h | Returns the value of the output voltage, measured at the  sense or output pins, that causes an output undervoltage fault. |
| VOUT\_UV\_FAULT\_RESPONSE | Read/Write Byte | 45h | Instructs the device on what action to  take in response to an output undervoltage fault. Only shutdown and ignore are supported. |
| IOUT\_OC\_FAULT\_LIMIT | Read/Write Word | 46h | Sets the value of the output current, in amperes, that causes the overcurrent detector to indicate an overcurrent fault condition. Set by writing this command in Linear format with a -1 exponent. |
| IOUT\_OC\_FAULT\_RESPONSE | Read/Write Byte | 47h | Instructs the device on what action to take in response to an output overcurrent fault.  Only C0h (shutdown immediately), F8h (hiccup forever), and D8 (hiccup 3 times) are supported. |
| IOUT\_OC\_WARN\_LIMIT | Read/Write Word | 4Ah | Sets the value of the output current that causes an output overcurrent warning. Set by writing this command in Linear format with a -1 exponent. |
| OT\_FAULT\_LIMIT | Read/Write Word | 4Fh | Sets the temperature, in degrees Celsius, of the unit at which it should indicate an overtemperature fault.  Exp = 0. |
| OT\_FAULT\_RESPONSE | Read/Write Byte | 50h | Instructs the device on what action to take in response to an overtemperature fault. Only shutdown and ignore are supported. |
| OT\_WARN\_LIMIT | Read/Write Word | 51h | Sets the temperature, in degrees Celsius, of the unit at which it should indicate an Overtemperature Warning alarm. Exp = 0. |
| VIN\_OV\_FAULT\_LIMIT | Read/Write Word | 55h | Sets the value of the input voltage that causes an input overvoltage fault. Exp = -4. |

|  |  |  |  |
| --- | --- | --- | --- |
| **COMMAND** | **PMBUS PROTOCOL** | **COMMAND CODE** | **DESCRIPTION** |
| VIN\_OV\_FAULT\_RESPONSE | Read/Write Byte | 56h | Instructs the device on what action to take in response to an input overvoltage fault. Only shutdown and ignore are  supported. |
| VIN\_UV\_WARN\_LIMIT | Read/Write Word | 58h | Sets the value of the input voltage that causes an input voltage low warning. Exp = -4. |
| IIN\_OC\_WARN\_LIMIT | Read/Write Word | 5Dh | Sets the value of the input current, in amperes,  that causes a warning that the input current is high. Exp = -1. |
| POWER\_GOOD\_ON | Read/Write Word | 5Eh | Sets the output voltage at which an optional  POWER\_GOOD signal should be asserted. Format according to VOUT\_MODE. |
| POWER\_GOOD\_OFF | Read/Write Word | 5Fh | Sets the output voltage at which an optional  POWER\_GOOD signal should be negated. Format according to VOUT\_MODE. |
| TON\_DELAY | Read/Write Word | 60h | Sets the time, in milliseconds, from when a start condition is received (as programmed by the ON\_OFF\_CONFIG command) until the output voltage starts to rise. Exp = 0. |
| TON\_RISE | Read/Write Word | 61h | Sets the time, in milliseconds, from when the output starts to rise until the voltage has entered the regulation band.  Exp = 0. |
| TON\_MAX\_FAULT\_LIMIT | Read/Write Word | 62h | Sets an upper limit, in milliseconds, on how  long the unit can attempt to power up the output without reaching the output undervoltage fault limit. Exp = 0. |
| TON\_MAX\_FAULT\_RESPONSE | Read/Write Byte | 63h | Instructs the device on what action to take in response to a TON\_MAX fault. Only shutdown and ignore are supported. |
| TOFF\_DELAY | Read/Write Word | 64h | Sets the time, in milliseconds, from when a stop condition is received (as programmed by the ON\_OFF\_CONFIG command) until the unit stops transferring energy to the output. Exp = 0. |
| TOFF\_FALL | Read/Write Word | 65h | Sets the time, in milliseconds, from the end of the turn-off delay time until the voltage is commanded to zero. Exp = 0. |
| STATUS\_BYTE | Read/Write Byte | 78h | Returns 1 byte where the bit meanings are: Bit <7> Reserved  Bit <6> Output off (due to fault or enable) Bit <5> Output over-voltage fault  Bit <4> Output over-current fault Bit <3> Input Under-voltage fault Bit <2> Temperature fault  Bit <1> Communication/Memory/Logic fault  Bit <0>: Reserved |
| STATUS\_WORD | Read/Write Word | 79h | Returns 2 bytes where the Low byte is the same as the STATUS\_BYTE data. The High byte has bit meanings are:  Bit <7> Output high or low fault Bit <6> Output over-current fault Bit <5> Input under-voltage fault Bit <4> MFR\_SPECIFIC  Bit <3> POWER\_GOOD#  Bit <2:0> Reserved |
| STATUS\_VOUT | Read/Write Byte | 7Ah | Bit <7> Output Overvoltage Fault  Bit <6> Output Overvoltage Warning Bit <5> Output Undervoltage Warning |

|  |  |  |  |
| --- | --- | --- | --- |
| **COMMAND** | **PMBUS PROTOCOL** | **COMMAND CODE** | **DESCRIPTION** |
|  |  |  | Bit <4> Output Undervoltage Fault Bit <3> VOUT\_MAX Warning  Bit <2> TON\_MAX\_FAULT  Bit <1> Reserved  Bit <0> Reserved |
| STATUS\_IOUT | Read/Write Byte | 7Bh | Bit <7> Output Overcurrent Fault Bit <6> Reserved  Bit <5> Output Overcurrent Warning Bit <4> Reserved  Bit <3> Current Share Fault  Bit <2:0> Reserved |
| STATUS\_INPUT | Read/Write Byte | 7Ch | Bit <7> Input Overvoltage Fault Bit <6> Reserved  Bit <5> Input Undervoltage Warning Bit <4> Input Undervoltage Fault  Bit <3> Unit Off For Insufficient Input Voltage Bit <2> Reserved  Bit <1> Input Overcurrent Warning  Bit <0> Reserved |
| STATUS\_TEMPERATURE | Read/Write Byte | 7Dh | Bit <7> Over Temperature Fault  Bit <6> Over Temperature Warning Bit <5:0> Reserved |
| STATUS\_CML | Read/Write Byte | 7Eh | Returns 1 byte where the bit meanings are: Bit <7> Invalid or unsupported command Bit <6> Invalid or unsupported data  Bit <5> PEC fault Bit <4:2> Reserved  Bit <1> Other communication fault not listed here  Bit <0> Reserved |
| STATUS\_MFR\_SPECIFIC | Read/Write Byte | 80h | Returns 1 byte where the bit meanings are: Bit <7:4> Reserved  Bit <3> Loss of SYNC Bit <2> Driver Fault  Bit <1> Unpopulated Phase  Bit <0> External Overtemperature Fault |
| READ\_VIN | Read Word | 88h | Returns the input voltage in Volts |
| READ\_IIN | Read Word | 89h | Returns the input current in Amperes |
| READ\_VOUT | Read Word | 8Bh | Returns the output voltage in the format set by VOUT\_MODE |
| READ\_IOUT | Read Word | 8Ch | Returns the output current in Amperes |
| READ\_TEMPERATURE\_1 | Read Word | 8Dh | Returns the addressed loop NTC temperature in degrees Celsius |
| READ\_TEMPERATURE\_2 | Read Word | 8Eh | Returns the other loop NTC temperature in degrees Celsius |
| READ\_DUTY\_CYCLE | Read Word | 94h | Returns the duty cycle of the PMBus device’s main power converter in percent. |
| READ\_POUT | Read Word | 96h | Returns the output power in Watts |
| READ\_PIN | Read Word | 97h | Returns the input power in Watts |
| PMBUS\_REVISION | Read Byte | 98h | Reports PMBus Part I rev 1.1 & PMBUs Part II rev 1.2(draft) |
| MFR\_ID | Block Read/Write | 99h | The MFR\_ID is set to IR (ASCII 52 49) unless programmed |

|  |  |  |  |
| --- | --- | --- | --- |
| **COMMAND** | **PMBUS PROTOCOL** | **COMMAND CODE** | **DESCRIPTION** |
|  | Byte count = 2 |  | different in the USER registers of the controller. |
| MFR\_MODEL | Block Read, byte count = 1 | 9Ah | The MFR\_Model is the same as the device ID if the USER register for Manufacturer model is 00. Otherwise MFR\_Model command returns the value in the USER register for MFR\_Model. |
| MFR\_REVISION | Block Read, byte count = 2 | 9Bh | The MFR\_Revision is the same as the device revision if the USER register for Manufacturer revision is 00. Otherwise MFR\_Revision command returns the value in the USER register for MFR\_Revison. |
| MFR\_DATE | Block Read/Write Byte count = 2 | 9Dh | The MFR\_DATE command returns the value in the USER register called MFR\_DATE |
| IC\_DEVICE\_ID | Block Read | ADh | Returns a 1 byte code with the following values: 4D = IR35201 |
| IC\_DEVICE\_REV | Block Read | AEh | The IC revision that is stored inside the IC |
| MFR\_READ\_REG | Custom MFR protocol | D0h | Read I2C registers |
| MFR\_WRITE\_REG | Write Word | D1h | Write to I2C registers, High Byte is reg, low byte is data |

### 11-BIT LINEAR DATA FORMAT

Monitored parameters use the Linear Data Format ([Figure](#_bookmark60) 64) encoding into 1 Word (2 bytes), where:

*Value* *Y* 2*N*

Note: N and Y are “signed” values.

**Databyte High Databyte Low**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| 7 | 6 | 5 | 4 | 3 |

|  |  |  |
| --- | --- | --- |
| 2 | 1 | 0 |

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

**N Y**

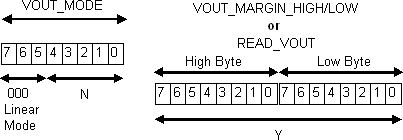
**Figure 64: 11-bit Linear Data Format**

### 16-BIT LINEAR DATA FORMAT

This format is only used for VOUT related commands (READ\_VOUT, VOUT\_MARGIN\_HIGH, VOUT\_MARGIN\_LOW, VOUT\_COMMAND):

*Value* *Y* 2*N*

Note: N is a “signed” value. If VOUT is set to linear format (by VOUT\_MODE), then N is set by the VOUT\_MODE command and only Y is returned in the data-field as a 16-bit unsigned number.



**Figure 65: 16-bit Linear Data Format**

**SVID REGISTERS**

A list of all the SVID registers is given in [Table](#_bookmark61) 57. SVID registers supported by IR35201 in VR12.5 and IMVP8 mode conform to VR12.5 and IMVP8 specifications respectively.

**Table 57: SVID Registers**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Register Address** | **Register Name** | **Access** | **VR12.5 Mode** | **IMVP8 Mode** |
| 00 | Vendor ID | RO | Supported | Supported |
| 01 | Product ID | RO | Supported | Supported |
| 02 | Product Revision | RO | Supported | Supported |
| 03 | Product Date Code | - | Not Supported | Not Supported |
| 04 | Lot Code | - | Not Supported | Not Supported |
| 05 | Protocol ID | RO | Supported | Supported |
| 06 | Capability | RO | Supported | Supported |
| 07 | Vendor-Timeout | RW | Supported | Supported |
| 08 | Vendor Use | RO | Supported | Supported |
| 09 | Vendor Use | - | Not Supported | Not Supported |
| 0A | Vendor Use | - | Not Supported | Not Supported |
| 0B | Vendor Use | - | Not Supported | Not Supported |
| 0C | Vendor Use | - | Not Supported | Not Supported |
| 0D | Vendor Use | RO | Supported, For Factor Use Only | Supported, For Factor Use Only |
| 0E | Vendor Use | RW | Supported, For Factor Use Only | Supported, For Factor Use Only |
| 0F | Vendor Use | RW | Supported, For Factor Use Only | Supported, For Factor Use Only |
| 10 | Status\_1 | RO | Supported | Supported |
| 11 | Status\_2 | RO | Supported | Supported |
| 12 | Temperature Zone | RO | Supported | Supported |
| 13 | Reserved | - | Not Supported | Not Supported |
| 14 | Reserved | - | Not Supported | Not Supported |
| 15 | Output Current | RO | Supported | Supported |
| 16 | Output Voltage | RO | Supported | Supported |
| 17 | VR Temperature | RO | Supported | Supported |
| 18 | Output Power | RO | Supported | Supported |
| 19 | Input Current | RO | Supported | Supported |
| 1A | Input Voltage | RO | Supported | Supported |
| 1B | Input Power | RO | Supported | Supported |
| 1C | Status 2 Last Read | RO | Supported | Supported |
| 1D | Future Command | - | Not Supported | Not Supported |
| 1E | Future Command | - | Not Supported | Not Supported |
| 1F | Future Command | - | Not Supported | Not Supported |
| 20 | Future Command | - | Not Supported | Not Supported |
| 21 | ICC Max | RO | Supported | Supported |
| 22 | Temp Max | RO | Supported | Supported |
| 23 | DC\_LL | RO | Supported | Supported |
| 24 | SR\_Fast | RO | Supported | Supported |
| 25 | SR\_Slow | RO | Supported | Supported |
| 26 | Vboot | RO | Supported | Supported |
| 27 | VR Tolerance | - | Not Supported | Not Supported |
| 28 | Current-Offset | RO | Supported | Supported |
| 29 | Temperature Offset | RO | Supported | Supported |
| 2A | Slow Slew Rate Select | RO | Not Supported | Supported |
| 2B | PS4 Exit Latency | RO | Not Supported | Supported |
| 2C | PS3 Exit Latency | RO | Not Supported | Supported |
| 2D | Enable to Ready | RO | Not Supported | Supported |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Register Address** | **Register Name** | **Access** | **VR12.5 Mode** | **IMVP8 Mode** |
| 2E | Pin Max | RO | Not Supported | Supported |
| 2F | Pin Alert Threshold | RW | Not Supported | Supported |
| 30 | VOUT Max | RW | Supported | Supported |
| 31 | VID Setting | RW | Supported | Supported |
| 32 | Pwr State | RW | Supported | Supported |
| 33 | Offset | RW | Supported | Supported |
| 34 | Multi VR Config | RW | Supported | Supported |
| 35 | Set RegADR | RW | Supported | Supported |
| 36 | Future Command | - | Not Supported | Not Supported |
| 37 | Future Command | - | Not Supported | Not Supported |
| 38 | Future Command | - | Not Supported | Not Supported |
| 39 | Future Command | - | Not Supported | Not Supported |
| 3A | Work Point 0 | RW | Not Supported | Not Supported |
| 3B | Work Point 1 | RW | Not Supported | Not Supported |
| 3C | Work Point 2 | RW | Not Supported | Not Supported |
| 3D | Work Point 3 | RW | Not Supported | Not Supported |
| 3E | Work Point 4 | RW | Not Supported | Not Supported |
| 3F | Work Point 5 | - | Not Supported | Not Supported |
| 40 | Work Point 6 | - | Not Supported | Not Supported |
| 41 | Work Point 7 | - | Not Supported | Not Supported |
| 42 | IVID1-VID | RW | Not Supported | Supported |
| 43 | IVID1-I | RW | Not Supported | Supported |
| 44 | IVID2-VID | RW | Not Supported | Supported |
| 45 | IVID2-I | RW | Not Supported | Supported |
| 46 | IVID3-VID | RW | Not Supported | Supported |
| 47 | IVID3-I | RW | Not Supported | Supported |

# MARKING INFORMATION

**PIN 1**



**35201**

**AYWWX XXXXX**

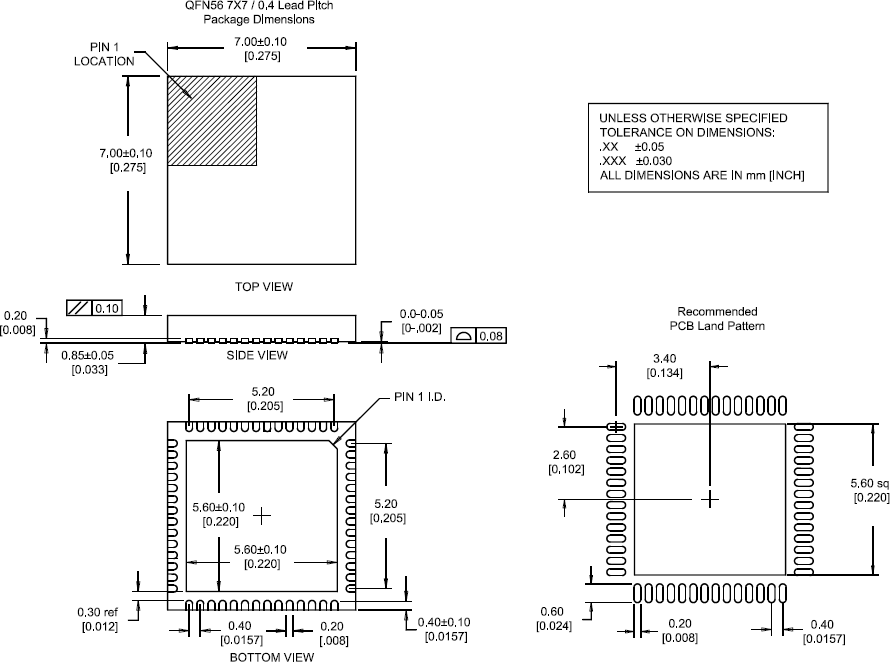
**PART # ASSEMBLER (A)/DATE(YWW)/MARKING CODE(X)**

**LOT CODE (ENG MODE - MIN. LAST 5 DIGITS OF EATI #) (PROD MODE – 4 DIGIT SPN CODE)**

**Figure 66: Package Marking**

# PACKAGE INFORMATION

QFN 7x7mm, 56-pin



**Figure 67: Package Dimensions**

# ENVIRONMENTAL QUALIFICATIONS

|  |  |  |  |
| --- | --- | --- | --- |
| **Qualification Level**  **Moisture Sensitivity Level** | | Industrial | |
| QFN package | MSL2 |
| **ESD** | **Machine Model** | JESD22-A115-A | |
| **Human Body Model** | JESD22-A114-E | |
| **Charged Device Model** | JESD22-C101-C | |
| **Latch-up** | JESD78 | |
| **RoHS Compliant** | | Yes | |

† Qualification standards can be found at International Rectifier web site: [http://www.irf.com](http://www.irf.com/)

†† Exceptions to AEC-Q101 requirements are noted in the qualification report.

Data and specifications subject to change without notice. This product will be designed and qualified for the Industrial market. Qualification Standards can be found on IR’s Web site.



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