***8/7/6/5/4/3/2/1-Phase Synchronous-Rectified Buck Controller***

***with SMBus Digital Interface***

## General Description

The uP9512 is an 8/7/6/5/4/3/2/1-phase PWM controller specifically designed to provide high-precision output voltage system for next generation GPUs. The uP9512 provides programmable output voltage and active voltage positioning functions to adjust the output voltage as a function of the load current, so it is optimally positioned for a load current transient.

The uP9512 supports NVIDIA Open Voltage Regulator type 4i+ with PWMVID feature. The PWMVID input is buffered and filtered to generate accurate reference voltage and the output voltage is precisely regulated to the reference input. The integrated SMBus interface provides user the flexibility to optimize the performance and efficiency.

The uP9512 supports Advanced DrMOS power module with current reporting function (DrMOS) application. The REFOUT provides an input reference voltage for DrMOS’s REFIN pin. The uP9512 uses the current reporting signal of DrMOS for channel current balancing. The uP9512 also provides hardware setting to adjust the operating phase number in different load current state.

Other features include adjustable soft-start, channel current limit, under voltage protection, over voltage protection and power good output. The uP9512 is available in a VQFN5x5- 40L package.

## Ordering Information

|  |  |  |
| --- | --- | --- |
| Order Number | Package | Top Marking |
| uP9512PQGJ | VQFN5x5 - 40L | uP9512P |

Note:

1. Please check the sample/production availability with uPI representatives.

## Features

* + **Support NVIDIA’s Open VReg Type 4i+ PWMVID Technology**
  + **SMBus Interface for Performance and Efficiency Optimization**
    - **Dynamic Programmable VR Parameters**
    - **Programmable Protection Thresholds**
    - **VR Output Reporting**
  + **Selectable 8/7/6/5/4/3/2/1-Phase Operation by Hardware Setting**
  + **Support up to 2MHz Operation Frequency**
  + **REFOUT Reference Voltage for Advanced DrMOS Power Module with Current Reporting Function (DrMOS)**
  + **Auto-Phase Shedding**
  + **Adjustable Soft-Start Time**
  + **Power State Input (PSI)**
  + **Power Good Indication**
  + **Channel Current Limit Protection**
  + **Total Output Over Current Protection**
  + **Over/Under Voltage Protection**
  + **Over Temperature Protection**
  + **RoHS Compliant and Halogen Free**

## Pin Configuration

**ADDR/FSW**

1. uPI products are compatible with the current IPC/ JEDEC J-STD-020 requirements. They are halogen-free, RoHS compliant and 100% matte tin (Sn) plating that are suitable for use in SnPb or Pb-free soldering processes.

**COMP**

**EAP**

**DAC**

**VINMON**

**IMON**

**LPC**

**REFOUT**

**CSPSUM**

**CSNSUM**

# Applications

### Middle-High End GPU Core Power Supplies

**FB**

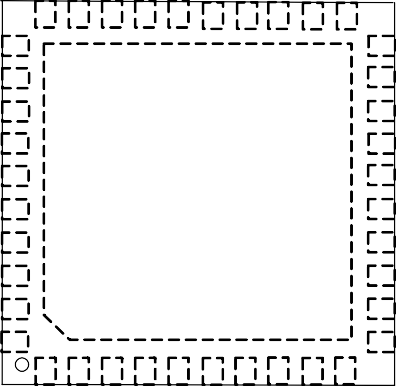
**FBRTN TSENSE**

**SDA SCL**

**EN PSI PGOOD**

**CSP1 CSP2 CSP3 CSP4**

**CSP5 CSP6**



**30 29 28 27 26 25 24 23 22 21**

**31 20**

**32 19**

**33 18**

**34 17**

**35**

**41**

**GND**

**16**

**36 15**

**37 14**

**38 13**

**39 12**

**40 11**

**1 2 3 4 5 6 7 8 9 10**

**CSP7 CSP8**

**VID 5VCC**

**REFADJ PWM1 / LL**

**REFIN**

**VREF**

**CH\_OC**

**PWM8 / T\_RAMP**

**PWM7 / RMP\_SLP**

**PWM6 / APL4**

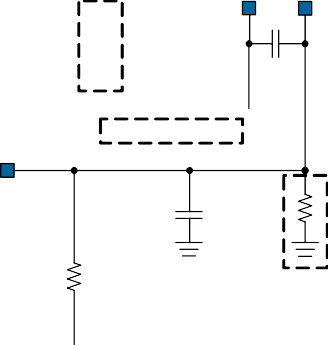
**PWM5 / APL3**

**PWM4 / APL2**

**PWM3 / APL1**

**PWM2 / APL\_HYS / MID\_BUF**

## Typical Application Circuit



VINMON

EN

5VCC

VIN

91k

27

Note :

Repeat to 8

10k

36

Depends on the impedance of DrMOS's EN,

additional circuit may be required.

From uP9512's EN

VIN

12

5V

24 LPC

TSENSE PWMx

5V

33

4~11

VCC

EN

PVCC TOUT

IOUT

PWM

DrMOS

PHASE SW

VIN

VOUT

REFIN

BOOT

VOUT

26 ADDR / FSW

CSPx

13~20

Note :

PWM strap setting

5V

CH\_OC REFOUT 23

3

Note : Reserved for Phase Disable

1. SDA
2. SCL

CSNSUM 21

RSUM

Note :

Reserved for REFOUT sink

Note to PWM strap setting function: Make sure the PWM input impedance of DrMOS is in high impedance state when DrMOS is disabled if uP9512 PWM strap setting function is used. If the PWM pin input impedance of DrMOS is not in high impedance state when it is disabled,

CSPSUM 5VCC

please disable the PWM strap setting function.

FBRTN

GPIO

5VCC

1.8V

38 PGOOD

37 PSI

2 VREF

1 REFIN

40 REFADJ

39 VID

GND

COMP 30

FB 31

FBRTN 32

28

DAC

EAP 29

IMON 25

VOUT

VOUT\_SNS

VGND\_SNS

GND

41

|  |  |  |
| --- | --- | --- |
| **No.** | **Name** | **Pin Function** |
| 1 | REFIN | **Reference Input.** Connect this pin to an external reference voltage through a resistor or connect to the output of the REFADJ circuit. |
| 2 | VREF | **Reference Voltage.** 2V LDO voltage output pin. Connect an at least 1 uF decoupling capacitor between this pin and GND. |
| 3 | CH\_OC | **Channel Current Limit.** Connect a resistor from this pin to GND to set the per- channel current limit threshold. |
| 4 | PWM8/T\_RAMP | **Phase 8 PWM Output and Soft-Start Time.** It outputs a PWM logic signal for external MOSFET driver and it is also used to set the soft-start time. Connect this pin to the PWM input of external MOSFET driver. Connect a resistor from this pin to GND to set the soft-start time. The resistor value should be greater than 15k |
| 5 | PWM7/RMP\_SLP | **Phase 7 PWM Output and RAMP Slope.** It outputs a PWM logic signal for external MOSFET driver and it is also used to set the slope of internal RAMP signal. Connect this pin to the PWM input of external MOSFET driver. Connect a resistor from this pin to GND to set the RAMP slope. The resistor value should be greater than 15k. |
| 6 | PWM6/APL4 | **Phase 6 PWM Output and Auto-Phase Shedding Threshold 4.** It outputs a PWM logic signal for external MOSFET driver and it is also used to set the auto-phase shedding threshold 4. Connect this pin to the PWM input of external MOSFET driver. Connect a resistor from this pin to GND to set the auto-phase shedding threshold 4. The resistor value should be greater than 15k |
| 7 | PWM5/APL3 | **Phase 5 PWM Output and Auto-Phase Shedding Threshold 3.** It outputs a PWM logic signal for external MOSFET driver and it is also used to set the auto-phase shedding threshold 3. Connect this pin to the PWM input of external MOSFET driver. Connect a resistor from this pin to GND to set the auto-phase shedding threshold 3. The resistor value should be greater than 15k |
| 8 | PWM4/APL2 | **Phase 4 PWM Output and Auto-Phase Shedding Threshold 2.** It outputs a PWM logic signal for external MOSFET driver and it is also used to set the auto-phase shedding threshold 2.Connect this pin to the PWM input of external MOSFET driver. Connect a resistor from this pin to GND to set the auto-phase shedding threshold 2. The resistor value should be greater than 15k |
| 9 | PWM3/APL1 | **Phase 3 PWM Output and Auto-Phase Shedding Threshold 1.** It outputs a PWM logic signal for external MOSFET driver and it is also used to set the auto-phase shedding threshold 1.Connect this pin to the PWM input of external MOSFET driver. Connect a resistor from this pin to GND to set the auto-phase shedding threshold 1. The resistor value should be greater than 15k |
| 10 | PWM2/APL\_HYS/ MID\_BUF | **Phase 2 PWM Output, Hysteresis of Auto-Phase Shedding and PWM Middle State Mode Control.** It outputs a PWM logic signal for external MOSFET driver and it is also used to set the hysteresis of auto-phase shedding and PWM middle state mode selection. Connect this pin to the PWM input of external MOSFET driver.  Connect a resistor from this pin to GND to set the hysteresis of auto-phase shedding and selects the PWM middle state mode. The resistor value should be greater than 15k |
| 11 | PWM1/LL | **Phase 1 PWM Output and Load Line**. It outputs a PWM logic signal for external MOSFET driver and it is also used to program the DC load line enable threshold. Connect a resistor from this pin to GND to set the DC load line enable threshold**.** The resistor value should be greater than 15k |

# Functional Pin Description

|  |  |  |
| --- | --- | --- |
| **No.** | **Name** | **Pin Function** |
| 12 | 5VCC | **Supply Input for the IC.** Connect this pin to a 5V voltage source with RC filter. Connect this pin to a 5V supply and decouple with a ceramic capacitor of 1uF minimum**.** |
| 13 | CSP8 | **CSP8.** Connnet this pin to the current monitor output of DrMOS to sense phase8 output current. Keep the maximum differential voltage between CSP8 to REFOUT lower than 400mV. |
| 14 | CSP7 | **CSP7.** Connnet this pin to the current monitor output of DrMOS to sense phase7 output current. Keep the maximum differential voltage between CSP7 to REFOUT lower than 400mV. |
| 15 | CSP6 | **CSP6.** Connnet this pin to the current monitor output of DrMOS to sense phase6 output current. Keep the maximum differential voltage between CSP6 to REFOUT lower than 400mV |
| 16 | CSP5 | **CSP5.** Connnet this pin to the current monitor output of DrMOS to sense phase5 output current. Keep the maximum differential voltage between CSP5 to REFOUT lower than 400mV. |
| 17 | CSP4 | **CSP4.** Connnet this pin to the current monitor output of DrMOS to sense phase4 output current. Keep the maximum differential voltage between CSP4 to REFOUT lower than 400mV. |
| 18 | CSP3 | **CSP3**. Connnet this pin to the current monitor output of DrMOS to sense phase3 output current. Keep the maximum differential voltage between CSP3 to REFOUT lower than 400mV. |
| 19 | CSP2 | **CSP2.** Connnet this pin to the current monitor output of DrMOS to sense phase2 output current. Keep the maximum differential voltage between CSP2 to REFOUT lower than 400mV. |
| 20 | CSP1 | **CSP1.** Connnet this pin to the current monitor output of DrMOS to sense phase1 output current. Keep the maximum differential voltage between CSP1 to REFOUT lower than 400mV. |
| 21 | CSNSUM | **Inverting Input of Total Current Sense Amplifier.** |
| 22 | CSPSUM | **Non-Inverting Input of Total Current Sense Amplifier.**Pull this pin up to 5VCC with 100k for internal CSP1 ~ CSP8 current summing. |
| 23 | REFOUT | **Reference Output Votlage.** This pin provides an reference voltage for DrMOS. Connect this pin to the REFIN pin of DrMOS. Depends on application, a resistor from this pin to GND is allowed to help to sink the current from DrMOS. |
| 24 | LPC | **Low Phase Count.** Connect a voltage divider from 5VCC to this pin to set the operation phase number of Warm Boot and Cold Boot. **Do NOT** connect any decoupling capacitor to this pin. |
| 25 | IMON | **Output Current Monitor.** The output current of this pin is proportional to the total load current. The total load current is sensed and flows out of this pin, and a resistor from this pin to GND makes the IMON voltage proportional to the total output current. The IMON voltage is monitored for total output over current protection. A capacitor can be connected from IMON to GND to adjust the response time of IMON. |
| 26 | ADDR/FSW | **SMBus Device Address and Operation Frequency.** Connect a voltage divider from 5VCC to this pin to select the SMBus device address and operation frequency. **Do NOT** connect any decoupling capacitor to this pin. |

|  |  |  |
| --- | --- | --- |
| **No.** | **Name** | **Pin Function** |
| 27 | VINMON | **Power Stage Input Voltage Monitor.** Connect this pin to the power stage input VIN with a voltage divider. The controller senses the voltage on this pin for power stage input voltage VIN detection. It is recommended to use resistor divider with 1/10 dividing ratio from VIN. For example, use 91k/10k resistor divider is a good practice. |
| 28 | DAC | **DAC Output.** The output voltage of this pin is the reference votlage. |
| 29 | EAP | **Non-Inverting Input of the Error Amplifier**. Connect a resistor between this pin and DAC pin to set the droop (load line) function. |
| 30 | COMP | **Output of Control Loop Error Amplifier.** |
| 31 | FB | **Inverting Input of the Error Amplifier.** |
| 32 | FBRTN | **Output Voltage Feedback Return.** Inverting input to the differential voltage sense amplifier. FBRTN is the reference point in DAC output voltage measurement.Connect this pin directly to the GPU output voltage feedback return sense point. |
| 33 | TSENSE | **Temperature Monitoring Input.** Connect this pin to the temperature reporting pin of DrMOS. |
| 34 | SDA | **SMBus Data Input.** This pin is input or output of serial bus data signal. If the SMBus is not available, this pin can be a hardware setting pin for single phase operation mode selection. Find the detail description in "SMBus (SCL & SDA)" section. |
| 35 | SCL | **SMBus Clock Input.** This pin receives serial bus clock signal input. If the SMBus is not available, this pin can be a hardware setting pin for single phase operation mode selection. Find the detail description in "SMBus (SCL & SDA)" section. |
| 36 | EN | **Enable.** Connect a 10k resistor from this pin to ground to enable the PWM strap function and place this resistor close to the controller. To disable PWM strap function, use 24k instead. **Do NOT** use resistance values other than the value specified here**. Do NOT** connect any capacitor directly to this pin. Refer to the typical application circuit, it is recommended to use a MOSFET with its drain connected to EN pin without a pull-up resistor for power sequence control. **Do NOT** connect EN pin directly to a voltage source for sequence control. |
| 37 | PSI | **Power Saving Input.** An input pin receiving power saving control signal from GPU. |
| 38 | PGOOD | **Power Good Indication**. Connect this pin to a voltage source with a pull-up resistor. |
| 39 | VID | **VID.** PWMVID input pin. |
| 40 | REFADJ | **Reference Adjustment.** PWMVID output pin. Connect this pin with an RC integrator to generate REFIN voltage. |
| Exposed Pad | | **Ground.** The exposed pad is the ground of logic control circuits, it must be soldered to a large PCB and connected to GND. |

## Functional Block Diagram

**SDA SCL**

**5VCC EN VINMON**

**PSI**



EAP x 155%

OVP

S/H

UVP

EAP x 45%

S/H

ISEN(total)

Channel Current Limit

Current Balance

S/H

ISUM

RSEN

S/H

S/H

Linear Regulator

5VCC

S/H

5VCC

PWM

Control Logic

POR

RAMP1

SMBus/ADC

RAMP2

RAMP3

RAMP4

**Idroop**

RAMP5

S/H

RAMP6

RAMP7

RAMP8

**Idroop**

**ISUM**

S/H

Total OCP

2.1V

Linear Regulator

**LPC**

**TSENSE CH\_OC**

**ADDR/FSW PGOOD**

**DAC**

**REFIN**

**FBRTN COMP**

**FB EAP**

**IMON**

**CSNSUM**

**PWM1/LL**

**PWM2/APL\_HYS/MID\_BUF**

**PWM3/APL1**

**PWM4/APL2**

**PWM5/APL3**

**PWM6/APL4**

**PWM7/RMP\_SLP**

**PWM8/T\_RAMP**

**CSP1**

**CSP2**

**CSP3**

**CSP4**

**CSP5**

**CSP6**

**CSPSUM**

**CSP7**

**VREF**

**REFADJ**

**VID**

**CSP8**

**REFOUT**

**GND**

### Power On Reset (POR)

Figure 1 shows the power ready detection circuit. The 5VCC voltage is monitored for power on reset with typically 4.3V threshold at its rising edge. When 5VCC is ready, the controller waits for EN to start up. When EN pin is driven above 0.2V, the controller begins its start up sequence. When EN pin is driven below 0.1V, the controller will be turned off, and it will clear all fault states to prepare to next soft-start once the controller is re-enabled.

4.3V

0.2V

5VCC 

POR

EN 

Figure 1. Circuit of Power Ready Detection

### Power Input Monitor

VINMON is the power stage input voltage sense pin. Connect this pin to power stage input voltage (VIN) with a voltage divider and always keep VINMON as 1/10 of power stage input voltage. When VINMON less than typically 0.2V at POR, the uP9512 will force start up at single phase and disables the cold boot, warm boot, PSI and auto-phase function. Once this condition is triggered, it can only be reset by re-POR or EN restart.

### Enable Control

The EN pin controls the enable and disable of this device.

# Functional Description

### PWM Strap Function

The uP9512 implements PWM strap function that provides more functional programming in a limited pin out. The PWM strap function can be controlled by the REN resistor connected from EN pin to GND. Use REN=10k to activate the PWM strap function and use REN=24k for function disable. To ensure correct PWM strap function setting. The input impedance of PWM pin of companion DrMOS should be in high-impedance state during the initial setting period prior to soft-start (Figure 2). Otherwise all the function setting by PWM pins can only be done via SMBus interface.

### Soft Start and Power Up Sequence

The uP9512 features a programmable soft start function to limit the surge current from power supply input. Controller starts the soft-start process right on VEN > 0.2V with typical 550us initialization time (TINIT). The output voltage ramp up time (TRAMP) during soft start period is determined by the resistor RPWM8 connected from PWM8 pin to GND. Table1 shows the TRAMP time and recommended RPWM8 resistance.

Table 1. TRAMP Time and Recommended RPWM8

|  |  |
| --- | --- |
| RPWM8 | TRAMP |
| 39k | 160us |
| 100k | 320us |
| 150k | 1.28ms |
| unstuffed | 640us |

The resistor REN connected between EN pin to ground is used to implement this function. It is recommended to use

If R

PWM8

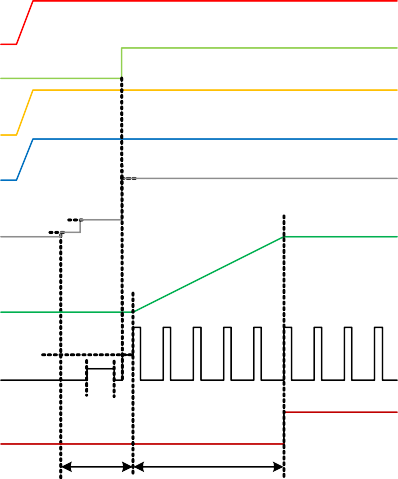
resistor is unstuffed, the output voltage ramp up

a small MOSFET with its drain connected to EN pin without pull up resistor for power sequence control as shown in Figure 2. Precaution should be taken while implementing the power sequence circuit to EN pin. **Do NOT** use other resistance value other than values specified in the PWM Strap section and **do NOT** connect EN pin directly to a voltage source. **Do NOT** connect EN pin directly to any sequencing circuit of the system. Make sure the slew rate of the gate signal (EN#) of Q1 is fast and not affected by any additional circuit. When VEN<0.1V and sustain 2us, the UVLO(Under Voltage Lock Out) event is triggered. Then, controller shuts down and reset all the hardware setting parameters.

time during soft-start period is typical 640us. If there is no

fault detected at the end of soft-start, the controller then asserts PGOOD when the output voltage reaches its target without delay. Figure 3 shows the power up sequence of the uP9512.

DrMOS's VCC DrMOS's EN



Note: DrMOS must be enabled and ready before 1st PWM.

**2.4V**

**0.6V**

**20uA x REN**

Mid

PWM

Setting

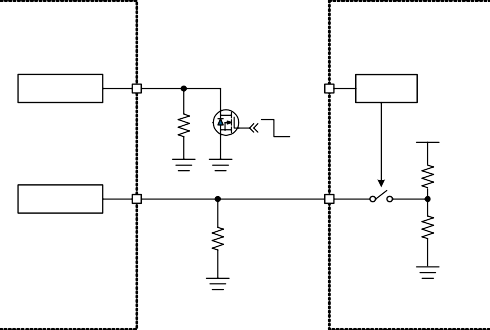
5VCC

VINMON

EN

VOUT

PWM



Enable Logic

EN

EN

EN\_POR

Q1

Disable

REN

EN#

Enable

VCC

PWM

IN

PWM Logic

RPWM

PWM Controller

DrMOS

PGOOD

TINIT TRAMP

Figure 3 Power Up Sequence

Figure 2. Enable Sequence Control

### PWMVID Function

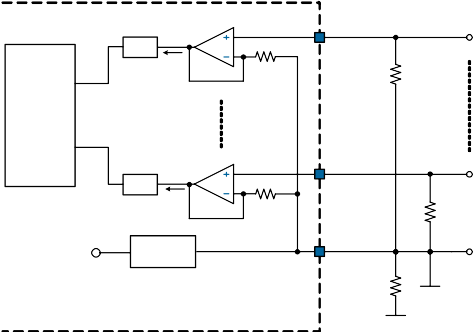
The PWMVID signal from GPU is applied to the VID pin, which is the input pin of the internal buffer. This buffer plays the role of level shifting, and the output of this buffer is injected into the external RC integrator to generate REFIN voltage, which can be calculated as:

*VREFIN* 

# Functional Description

### Channel Current Balance

IOUT1 (from DrMOS)



CSP1

S/H

ISEN1

R

SEN

Current Balance

CSP8

S/H

ISEN8

R

SEN

5VCC LDO

REFOUT

RSINK

1uF

IOUT8 (from DrMOS)

*R*2 //*R*3  *R*4  *R*5  *R*4  *R*5

*VVREF*  *D*  *R*1 *R*2 //*R*3  *R*4  *R*5 *R*3  *R*4  *R*5 

REFIN (from Dr.MOS)

*R*1//*R*3  *R*4  *R*5  *R*4  *R*5

*VVREF*  *R*2  *R*1//*R*3  *R*4  *R*5 *R*3  *R*4  *R*5

where VREFIN is the DC voltage of REFIN, VVREF is the voltage of VREF (typically 2V), and D is the duty cycle of PWMVID input. The VREF pin is an internal LDO, therefore an output decoupling capacitor is required. Recommend connecting at least a 1uF capacitor from VREF pin to local GND.

Figure 5. Current Balance Circuit

The uP9512 senses each phase current through CSPx pin for current balancing. The phase current signal is sampled and held when the low-side MOSFETs are turned on. The sensed current I can be determined by the following

### Boot Mode and Standby Mode

equation:

SENx

The PWMVID structure includes two operation modes: boot mode and standby mode. **During boot mode, controller ignores the PWMVID signal before PGOOD signal goes**

*VCSPx*

*SENx*

*R*



*I*

*SEN*

### high and the REFADJ pin enters high impedance state.

Where I

SENx

is the sampled and held phase current signal,

The REFIN voltage during boot mode can be calculated as:

*R*4  *R*5

VCSPx is the differential voltage between CSPx and REFOUT and the RSEN is internal sense resistor which is typical

*VREFIN* ,*BOOT*

 *VVREF*  *R*2  *R*3  *R*4  *R*5

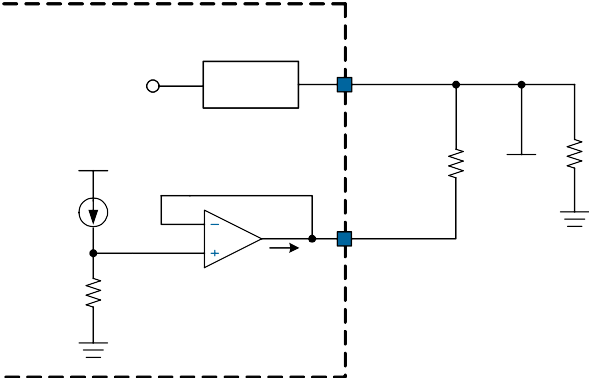
5k.The sensed current ISENx is mirrored to the current balance circuit, comparing between each other, and

During standby mode, other than GPU stopping the PWMVID transaction, an external system standby signal additionally controls the entry of standby mode. An additional external switch should be connected in parallel with the original PWMVID resistors as shown in Figure 4 to generate the standby mode voltage:

generating current adjusting signals for each phase. The current balance circuit increases the duty cycle of the phase whose phase current is smaller than others and decrease the duty cycle of the phase whose phase current is larger than others.

### Total Load Current Sense

*VREFIN* ,*STDBY* 



5VCC

LDO

REFOUT

RSUM

ISEN(total)

CSNSUM

ISUM

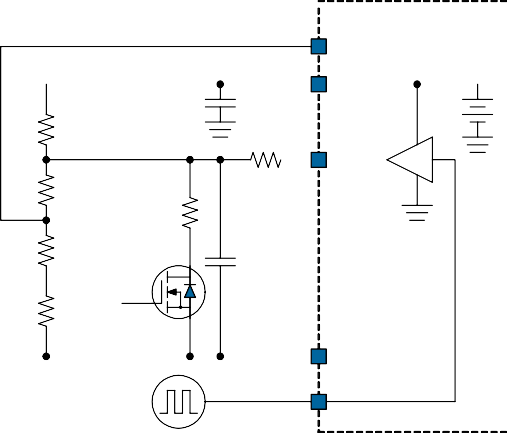
RSEN

*VVREF*

 *R*3  *R*4  *R*5// *RSTDBY R*2  *R*3  *R*4  *R*5// *RSTDBY*

  *R*4  *R*5 *R*3  *R*4  *R*5

RSINK



REFIN

VREF

2V

R2

R1 REFADJ

R3

RSTDBY

R4

C

R5

VSTDBY

FBRTN

VID

PWMVID

VSS\_SNS

Figure 6. Total Load Current Sense

Figure 4. PWMVID Structure

The uP9512 summed the ISENx current of each phase and generates a voltage on the positive input of the current sense amplifier (CSA), therefore the voltage on the CSNSUM pin can be written as:

*RSEN*

*V*  *I* 

*CSNSUM SEN* (*total* )

# Functional Description

amplifier respectively. The error amplifier modulates the COMP voltage (VCOMP) and the duty cycle of regulator to force VFB follows VEAP. The IDROOP current is mirrored to the EAP pin and creates a voltage at EAP pin as:

*VEAP*  *VDAC*  *IDROOP*  *RDROOP*

*I*  

8

*VCSPx*

*N*

*I DROOP*  *ISUM*  *ILLTH*

(if DC load line is activated)

*SEN* (*total* )

*x*1

*RSEN*

*IDROOP*  *ISUM*

(if AC load line is activated)

Where ISEN(total) is the summed current of ISEN of each phase,

Where V

is output of V , R

is an external resistor

*N* represents the actual operating phase number. The RSUM

DAC

REFIN DROOP

resistor connected between CSNSUM and REFOUT then

connected between DAC and EAP pins for adjusting load

generates the I

SUM

current. The ISUM

current represents the

line slope and IDROOP is a current source proportional to

output current when the DC load line function is activated.

total output current of the regulator, and it is directly used for droop function, total output current protection and auto-

C

phase shedding function. The I follows.

SUM

current is calculated as C

*ISUM*

 (*VCSNSUM* *VREFOUT* )

*RSUM*

RB CA

CB CD RC CE

### DC Load Line

The uP9512 implements DC load line with programmable enable threshold for user to optimize load transient performance. When DC load line is activated, the DC output voltage decreases as the output DC current increases. The

NVVDD\_GPU\_SENSE

Positive remote sense of GPU

RA

RDROOP

FB

EAP

DAC

Idroop

EA

Idroop

COMP

enable threshold of DC load line is set by a R

PWM1

resistor

CDAC

FBRTN

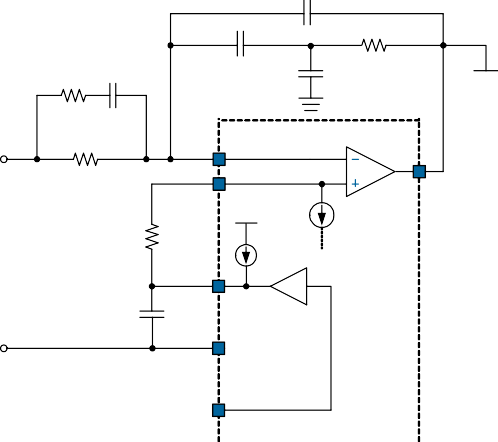
connected from PWM1 pin to GND. An ILLTH current is generated by a 2V voltage source and RPWM1 during TINIT time, it is calculated as :

NVVDD\_GND\_SENSE

Negative remote sense of GPU

REFIN

*I*  2*V*



*LLTH R*

*PWM* 1

Figure 7. Voltage Control Loop

If the ISUM current is greater than ILLTH current, controller then activates the DC load line function. The ILLTH current must in the range of 10uA to 80uA (RPWM1=200k to 25k), out of the specified range should be avoided.

### AC Load Line

The AC load line function is used to improve the load transient response. This function only takes effect in the load transient condition when the output voltage has instantaneous change due to transient load current. It does not affect the output DC voltage when the load current is in DC condition. Connect a 16k resistor (or resistance range from 15k to 18k) from PWM1 to GND to enable the AC load line function. The response time of AC load line is typically 80us, and the voltage drop is generated by the RDROOP resistor (see “Voltage Control Loop” section for details). The AC load line function & the response time can also be programmed via SMBus interface.

### Voltage Control Loop

Figure 7 illustrates the voltage control loop of the uP9512. FB and EAP are negative and positive inputs of the error

### Output Voltage Differential Sense

The uP9512 uses differential sense by a high-gain low offset error amplifier for output voltage differential sense as shown in Figure 7. The GPU voltage is sensed by the FB and FBRTN pins. FB pin is connected to the positive remote sense pin NVVDD\_GPU\_SENSE of the GPU via the resistor RFB.FBRTN pin is connected to the negative remote sense pin NVVDD\_GND\_SENSE of GPU directly.

### Power Saving Mode

The uP9512 provides power saving features for platform designers to program platform specific power saving configuration. There are three operation modes: Full-Phase mode, Auto-Phase Shedding mode, and Low-Phase mode. The uP9512 switches between these three operation modes according to the input voltage level of the PSI pin. Figure 8 shows typical PSI application circuit, and Table 2 shows recommended PSI setting voltage level of the three operation modes. In low-phase mode, it can separate into Cold Boot Mode and Warm Boot Mode. The operation phase number of Cold Boot Mode and Warm Boot Mode is

determined by LPC pin. In auto-phase shedding mode, the

# Functional Description

if VAPL2< VIMON < VAPL3, uP9512 operates in four phase;

operation phase number will auto increase/decrease

according to output loading. In Full-Phase mode, the

if V

APL3

< VIMON

< VAPL4

, uP9512 operates in six phase;

maximum phase number of operation is determined by checking the status of CPSx pins when POR.

**1.8V**



PSI

Power State Selection

**H-L Logic**

Figure 8. PSI Application Circuit

Table 2. Operation Mode and Recommended VPSI

|  |  |
| --- | --- |
| Operation Mode | Recommended Voltage Setting at PSI |
| Full-Phase CCM Mode | 1.8V |
| Auto-Phase Shedding Mode | 1V |
| Low-Phase Mode | GND |

### Auto-Phase Shedding

The uP9512 provides Auto-Phase Shedding function to reduce the switching and conduction losses at light load condition and enable high efficiency over a wide range of output current. Auto-Phase Shedding function is activated by two conditions:

1. PSI voltage stays at “Auto-Phase Shedding Mode”.
2. After PGOOD goes high, VID pin received the PWM-VID input signal from GPU.

Once the Auto-Phase Shedding function is activated, the uP9512 compares the VIMON with APL1/APL2/APL3/APL4 threshold to decide the operation phase number

dynamically. The APL1/APL2/APL3/APL4 threshold and the hysteresis can be programmed through SMBus interface. It also can be programmed by the resistor which is connected from PWM3~PWM6 pins to GND. The APL1 ~ APL4 threshold can be calculated as:

VAPL1 = (10uA x RPWM3) / 4

if VIMON >VAPL4, uP9512 operates in eight phase.

The uP9512 always keeps all-of-phase interleaved operation. **When setting the operating phase number of each current zone, always keep**

 **APL1 <** **APL2 <** **APL3 <** **PL4.**

### Violating this rule, controller will be forced into full phase operation mode.

The hysteresis of APLx level and the PWM middle state mode can be programmed by a resistor connected from PWM2 pin to GND. When the PWM middle state is enabled, the uP9512 drives the PWM middle state voltage by itself. Otherwise, the PWM output of the controller is in high-impedance state, and then the PWM middle state voltage is determined by DrMOS. Table 3 lists the recommended RPWM2 value for APL hysteresis and the PWM middle state mode.

Table 3. APL Hysteresis and Recommended RPWM2 Value

VAPL2

= (10uA x R

PWM4) / 2

VAPL3 = (10uA x RPWM5) VAPL4 = (10uA x RPWM6)

|  |  |  |
| --- | --- | --- |
| Recommended RPWM2(k) | APL\_Hys | PWM Middle State |
| 15 | 140mV | Disable |
| 24 | 120mV |
| 36 | 100mV |
| 56 | 80mV |
| 68 | 60mV |
| 82 | 40mV |
| 100 | 20mV |
| 150 | 20mV | Enable |
| 169 | 40mV |
| 180 | 60mV |
| 200 | 80mV |
| 215 | 100mV |
| 232 | 120mV |
| 280 | 140mV |

If VIMON < VAPL1, uP9512 operates in single phase;

if VAPL1< VIMON < VAPL2, uP9512 operates in dual phase;

### Operation Frequency and SMBus Device Address

The uP9512 features a multi-function pin (ADDR/FSW) to provide 5 SMBus device address and 8 operation frequency selection. Connect ADDR/FSW pin to 5VCC with a resistor divider (Figure 9) to set the operation frequency and SMBus device address. Table 4 shows the recommended RUP and RDW resistance of the resistor divider.

# Functional Description

**5VCC**



ADDR / FSW

SMBus Device Address &

Operation Frequency

RUP

RDW

Figure 9. ADDR/FSW Pin Connection

Table 4. Operation Frequency and SMBus Device Address

|  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| VADDR/FSW =  % of 5VCC | Operation Frequency (Hz) | SMBus Device Address (Unit: k) | | | | | | | | | |
| 0x48 | | 0x4A | | 0x4C | | 0x4E | | 0x40 | |
| RUP | RDW | RUP | RDW | RUP | RDW | RUP | RDW | RUP | RDW |
| 40.63% | 200k | 4.92 | 3.37 | 24.61 | 16.84 | 44.3 | 30.32 | 73.84 | 50.53 | 147.67 | 101.06 |
| 46.88% | 300k | 4.27 | 3.77 | 21.33 | 18.83 | 38.4 | 33.89 | 63.99 | 56.48 | 127.99 | 112.95 |
| 53.13% | 400k | 3.76 | 4.27 | 18.82 | 21.34 | 33.88 | 38.4 | 56.47 | 64.01 | 112.93 | 128.01 |
| 59.38% | 500k | 3.37 | 4.92 | 16.84 | 24.62 | 30.31 | 44.31 | 50.52 | 73.86 | 101.04 | 147.71 |
| 65.63% | 600k | 3.05 | 5.82 | 15.24 | 29.1 | 27.43 | 52.37 | 45.71 | 87.29 | 91.42 | 174.57 |
| 71.88% | 1000k | 2.78 | 7.11 | 13.91 | 35.56 | 25.04 | 64.01 | 41.74 | 106.69 | 83.47 | 213.37 |
| 78.13% | 1500k | 2.56 | 9.14 | 12.8 | 45.72 | 23.04 | 82.3 | 38.4 | 137.17 | 76.8 | 274.35 |
| 84.38% | 2000k | 2.37 | 12.8 | 11.85 | 64.02 | 21.33 | 115.24 | 35.55 | 192.06 | 71.11 | 384.12 |

### Phase Number of Operation (Hardware Programming)

The uP9512 supports 8/7/6/5/4/3/2/1-phase operation. The maximum phase number of operation is determined by checking the status of CSPx pins when power on reset. Please follow Table 5 for the phase disable. The maximum phase number of operation is decided and latched at each POR rising edge. The unused PWMx pins can be left floating only if PWM strap function is disabled.

Table 5. Operation Phase Number Settings

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Configuration | Pin Configuration, Pull High to Target | | | | | | | |
| CSP8 | CSP7 | CSP6 | CSP5 | CSP4 | CSP3 | CSP2 | CSP1 |
| 8-phase | -- | -- | -- | -- | -- | -- | -- | -- |
| 7-phase | 5VCC | -- | -- | -- | -- | -- | -- | -- |
| 6-phase | X | 5VCC | -- | -- | -- | -- | -- | -- |
| 5-phase | X | X | 5VCC | -- | -- | -- | -- | -- |
| 4-phase | X | X | X | 5VCC | -- | -- | -- | -- |
| 3-phase | X | X | X | X | 5VCC | -- | -- | -- |
| 2-phase | X | X | X | X | X | 5VCC | -- | -- |
| 1-phase | X | X | X | X | X | X | 5VCC | -- |
| Note 1: "--" denotes normal connection. Note 2: "x" denotes floating.  Note 3: Use 100k pull up resistor when pull up to 5VCC  Note 4: Strictly follow the table for phase disable. Incorrect pin pull up /down connection may cause catastrophic fault during start up. | | | | | | | | |

### Cold Boot and Warm Boot

The uP9512 features programmable operation phase number of Cold Boot Mode and Warm Boot Mode. When PSI=Low and uP9512 first boots up (first time of 5VCC and EN goes high), controller will enter to Cold Boot Mode. Exclude the first boot up condition, when PSI=Low state and controller power up by EN control, then uP9512 will enter to Warm Boot Mode. Connect LPC pin to 5VCC with a voltage divider (Figure 10) to set the operation phase number of Cold Boot Mode and Warm Boot Mode. Figure 11 shows all the power states of uP9512 under each combination of 5VCC/EN/ PSI/VID signal. Table 6 shows the recommended resistance of the voltage divider.

# Functional Description

**5VCC**



R

LPC

R

Low Phase Mode

TOP

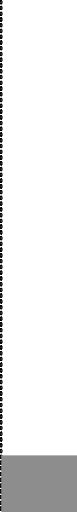
BOT

Figure 10. LPC Pin Connection

Table 6. Recommended Resistance of Cold Boot Mode and Warm Boot Mode

|  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| VLPC = % of 5VCC | Cold Boot Phase Count | Warm Boot Phase Count (Unit: k) | | | | | | | | | |
| 1-phase | | 2-phase | | 3-phase | | 4-phase | | 5-phase | |
| RTOP | RBOT | RTOP | RBOT | RTOP | RBOT | RTOP | RBOT | RTOP | RBOT |
| 40.63% | 1-phase | 4.92 | 3.37 | 24.61 | 16.84 | 44.3 | 30.32 | 73.84 | 50.53 | 147.67 | 101.06 |
| 46.88% | 2-phase | 4.27 | 3.77 | 21.33 | 18.83 | 38.4 | 33.89 | 63.99 | 56.48 | 127.99 | 112.95 |
| 53.13% | 3-phase | 3.76 | 4.27 | 18.82 | 21.34 | 33.88 | 38.4 | 56.47 | 64.01 | 112.93 | 128.01 |
| 59.38% | 4-phase | 3.37 | 4.92 | 16.84 | 24.62 | 30.31 | 44.31 | 50.52 | 73.86 | 101.04 | 147.71 |
| 65.63% | 5-phase | 3.05 | 5.82 | 15.24 | 29.1 | 27.43 | 52.37 | 45.71 | 87.29 | 91.42 | 174.57 |
| 71.88% | 6-phase | 2.78 | 7.11 | 13.91 | 35.56 | 25.04 | 64.01 | 41.74 | 106.69 | 83.47 | 213.37 |
| 78.13% | 7-phase | 2.56 | 9.14 | 12.8 | 45.72 | 23.04 | 82.3 | 38.4 | 137.17 | 76.8 | 274.35 |
| 84.38% | 8-phase | 2.37 | 12.8 | 11.85 | 64.02 | 21.33 | 115.24 | 35.55 | 192.06 | 71.11 | 384.12 |

**5VCC**



High

Tri-state

Low

**Full-Phase**

**Cold-Boot OFF Warm-Boot Full-Phase Warm-Boot OFF Cold-Boot Full-Phase Auto-Phase**

**OFF**

**EN**

**PSI**

**VID**

Figure 11. Power States of uP9512

### Channel Current Limit (CH\_OC)

The uP9512 adopts channel peak current limit function to avoid catastrophic damage to power stage components.

The uP9512 monitors the sensed current (in the form of voltage) from DrMOS. If the sensed voltage of any phase exceeds the channel current limit threshold, the channel current limit function activates. The resistor RCH\_OC connected between CH\_OC pin and GND determines the channel current limit threshold. The channel current limit threshold can be calculated as:

# Functional Description

Figure 12. Total Output Current Protection

The uP9512 provides total OCP as shown in Figure 12. A resistor RIMON is connected from IMON pin to GND. Adding a capacitor to the IMON pin can adjust the IMON response time. The sensed current ISUM is mirrored internally and fed to IMON pin. This current flows through the resistor RIMON creating voltage across it. As the total load current increases, the voltage on IMON pin (VIMON) increases proportionally. When the IMON pin voltage is greater than 2.1V, the total OCP will be triggered. The total OCP level (2.1V) is usually designed for the voltage regulator that is

*IOUT* ( *PEAK* )

 *RCH* \_ *OC*  20*uA* 6  *GCS*

operated in full phase condition by hardware setting. The actual operating phase number is controlled by the PSI signal or the SMBus Auto Phase setting. When the

Where I R

OUT(PEAK)

is the per-phase inductor peak current,

operating phase number is decreased, the total OCP level

is decreased as well. The total OCP level is changed per

CH\_OC is the resistor connected between CH\_OC pin and

GND. The RCH\_OC must be at least 10k. GCS (mV/A) is the current sense gain of DrMOS. Once the per-phase current exceeds the setting threshold, the per-phase output inductor current is limited to an average current. A continuous over load event will cause the output voltage drop and eventually trigger under voltage protection and shuts down the uP9512.

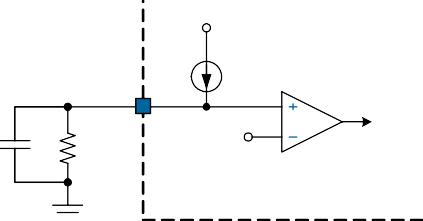
### Total Output Current Protection

actual operating phase number. Table 7 shows the

relationship between total OCP ratio per actual operating phase number and the hardware configuration.

Once the total OCP is triggered. The uP9512 will turn off both high-side and low-side MOSFETs of all channels. The total OCP function is a latch-off function and only EN restart or 5VCC re-POR can release the latch.

CIMON



ISUM

IMON

CMP

RIMON

2.1V

Total OCP

Table 7. Total OCP and Operating Phase Number

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Total Output OCP Ratio | | Operating Condition | | | | | | | |
| 8-phase | 7-phase | 6-phase | 5-phase | 4-phase | 3-phase | 2-phase | 1-phase |
| Hardware Configuration | 8-phase | 1 | 7/8 | 3/4 | 5/8 | 1/2 | 3/8 | 5/16 | 2/8 |
| 7-phase | -- | 1 | 7/8 | 3/4 | 5/8 | 1/2 | 3/8 | 5/16 |
| 6-phase | -- | -- | 1 | 3/4 | 5/8 | 1/2 | 3/8 | 5/16 |
| 5-phase | -- | -- | -- | 1 | 3/4 | 5/8 | 1/2 | 3/8 |
| 4-phase | -- | -- | -- | -- | 1 | 3/4 | 1/2 | 3/8 |
| 3-phase | -- | -- | -- | -- | -- | 1 | 3/4 | 1/2 |
| 2-phase | -- | -- | -- | -- | -- | -- | 1 | 3/4 |
| 1-phase | -- | -- | -- | -- | -- | -- | -- | 1 |

### Ramp Slope Setting

The ramp slope of the oscillator for PWM modulation can

# Functional Description

frequency, operating phase number, and load line according to the total load current. This function is referred to Auto

be adjusted and is determined by the resistor R setting for ramp slope and recommended R

PWM7. The

Phase, and it provides user the maximal flexibility in the

platform design to maximize voltage regulator’s efficiency

is shown in the table below.

|  |  |
| --- | --- |
| RPWM7 | Ramp Slope |
| 39k | 50% |
| 100k | 75% |
| 150k | 100% |
| unstuffed | 125% |

### Thermal Protection (TSENSE)

PWM7 resistance

and performance as well. The SMBus interface default is locked, it can be ”read only” before it is unlocked. Writes 94h value in the register 0x39h to unlock the SMBus and writes 87h value to lock the SMBus interface. The SMBus provides one time lock/unlock mechanism. Once it is unlocked and locked, it cannot be unlocked again. It can only be reset by 5VCC re-cycle.

If the SMBus interface is not available in the platform design, the SDA and SCL pins can also be the hardware programming pins to program the operation mode when controller is working in single phase operation. The uP9512 detects the state of SCL and SDA pins right on power on

The uP9512 features a TSENSE pin to monitor the thermal condition of regulator. For multiple phases application, ties all the DrMOS’s TMON together and connects it to uP9512’s TSENSE pin directly. The controller senses the voltage (VTSENSE ) on TSENSE pin(which from DrMOS’s TMON)

then converts and stores the information in the SMBus

register 0x25h(VR\_SHDN) with a 8mV/LSB resolution. As regulator temperature rises, the VTSENSE increases. Therefore the controller detects the VTSENSE to obtain regulator thermal information. The controller shuts down when VTSENSE is

higher than 2.032V(FEh). To disable the thermal protection function, set the SMBus register 0x25h value to 2.04V(FFh).

### Over Voltage Protection (OVP)

reset (POR) to recognize whether the SMBus is used or SCL and SDA becomes hardware programming pins. If SCL pin is ”high” when POR, it becomes SMBus programming pins and the controller latched at CCM operation mode when controller is working in single-phase operation. If the SCL pin is ”low” when POR, it becomes hardware programming pins and the controller latched at DCM mode when controller is working in single phase operation. Then, the SDA pin is used to program the PWM output behavior of DCM operation mode as the following table**.**

The OVP is triggered if VFB > 1.5x VEAP sustained 5us.When

|  |  |  |
| --- | --- | --- |
| SCL | SDA | Single Phase Operation Mode |
| 0 | 0 | Controller Controlled ZCD |
| 0 | 1 | DrMOS Controlled ZCD |
| 1 | x | Forced CCM Mode |
| "0": Denotes the voltage is lower than 1V "1": Denotes the voltage is higher than 1.2V "x": Don't care | | |

OVP is activated, the uP9512 turns on all low-side MOSFETs and turns off all high-side MOSFETs. The over voltage protection is a latch-off function and can only be reset by 5VCC re-POR or EN restart.

### Under Voltage Protection (UVP)

The under voltage protection is triggered if VFB < 0.5 x VEAP

sustained 5us. When UVP is activated, the uP9512 turns off all high-side and low-side MOSFETs. The under voltage protection is a latch-off function and can only be reset by 5VCC re-POR or EN restart.

### Over Temperature Protection (OTP)

The uP9512 monitors the temperature of itself. If the temperature exceeds typical 160oC, the uP9512 is forced into shutdown mode. The over temperature protection is a latch-off function and can only be reset by 5VCC re-POR or EN restart.

### SMBus (SCL & SDA)

The uP9512 features an SMBus interface to allow user to adjust various operating parameters. The supported operating parameters that can be adjusted through the SMBus are summarized as Table 8. The main function is to dynamically change the offset voltage, switching

When SCL=0 and SDA=0, the zero current detection (ZCD) is controlled by controller uP9512. When the zero inductor current is detected, the controller sets the PWM output from low to high impedance state or sets PWM output to middle state level (depends on PWM2 setting) and turns off the low side MOSFET, then the controller runs in discontinuous conduction mode (DCM).

When SCL=0 and SDA=1, the zero current detection is controlled by DrMOS itself. The uP9512 sets the PWM output from high to middle state level after a effective PWM duty cycle. When the companion DrMOS receives the PWM middle voltage from controller uP9512, the DrMOS decides the discontinuous conduction mode (DCM) or continuous conduction mode (CCM) by itself according to output loading.

### APL1, APL2, APL3, APL4 : (Reg0x01 ~ Reg0x04)

Define the thresholds for five load current states (LCS0, LCS1, LCS2, LCS3 and LCS4). The controller compares the APL1, APL2, APL3 and APL4 content with VIMON voltage to determine which load current state should be entered and executes the corresponding operating parameter settings (frequency, offset, operating phase number and load line).

LCS0 : VIMON> APL4, highest load current state. LCS1 : APL4 > VIMON > APL3

LCS2 : APL3 > VIMON > APL2

LCS3 : APL2 > VIMON > APL1

LCS4 : APL1 > VIMON, lowest load current state. **APL\_Hys1, APL\_Hys2, APL\_Hys3, APL\_Hys4 : (Reg0x05~Reg0x06)**

Define the hysteresis voltage of APL1, APL2, APL3 and APL4. 8-bits content setting with 20mV/step

### IICP0, IICP1, IICP2, IICP3, IICP4 : (Reg0x07 ~ Reg0x09)

Define the operating phase number in each load current state. The operating phase number can be full-phase to single phase.

### VOFS0, VOFS1, VOFS2, VOFS3, VOFS4:

**(Reg0x0A~Reg0x0C)**

Define the offset voltage in each load current state. 4-bits content setting with 10mV/step.

### IICF0, IICF1, IICF2, IICF3, IICF4 : (Reg0x0D ~ Reg0x0F)

Define the switching frequency in each load current state. The switching frequency is defined as the ratio to current operation frequency setting.

### Current Balance Gain Adjustment : (Reg0x12 ~ Reg0x19)

The uP9512 provides the current balance gain adjustment for user to optimize the performance in the system application.The current balance gain adjustment is defined as the ratio to default setting.

### Current Balance Offset Adjustment : (Reg0x1A ~ Reg0x1D)

uP9512 features the current balance offset adjustment for user the optimize the performance in the system application.3-bits content setting with 0.4uA/step.

### Channel Current Limit (CH\_OC) : (Reg0x22)

For per-channel current limit threshold adjustment. 8-bits content setting with 10mV/step.

### Total OCP : (Reg0x23)

For total output current protection level adjustment. 8-bits content setting with 10mV/step. The total output current protection adjustment is defined as the ratio to default setting.

### T\_OCP/UV/OV : (Reg0x24)

T\_OCP programs the delay time of total OCP. UV/OV is used for the threshold adjustment of UVP and OVP respectively.

# Functional Description

### VR\_SHDN : (Reg0x25)

Thermal shut down threshold adjustment, 8-bits content setting with 8mV/step. Once the voltage on TSENSE pin exceeds the voltage set in VR\_SHDN register, then uP9512 is forced in shut down mode.

### GCOMP : (Reg0x26)

For OTA transconductance setting for voltage control loop. It is defined as the ratio to the default value of 1960uA/V. **SL\_RAMP: (Reg0x3A)**

The slope adjustment of the RAMP signal. It is defined as the ratio to the default setting.

### IOUT : (Reg0x2C)

This register reports total output current that is converted by internal ADC with 10mV/step.

### VOUT : (Reg0x2D)

This register reports total output voltage that is converted by internal ADC with 10mV/step.

### TEMP : (Reg0x2E)

This register reports highest temperature of DrMOS that is converted by internal ADC with 8mV/step.

### Data Validity

The data on the SDA line must be stable during the HIGH period of the SCL, unless generating a START or STOP condition. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW. Refer to the figure below.

SDA

SCL

### START and STOP Conditions

SDA stable Data Valid

Change of SDA allowed

A START (S) condition is a HIGH to LOW transition of SDA while SCL is HIGH. The STOP (P) condition is a LOW to HIGH transition of SDA while SCL is HIGH. A STOP condition must be sent before each START condition.

SDA

SCL

START(S) STOP(P)

### Acknowledge

Each address and data transmission uses 9 clock pulses. The ninth pulse is the acknowledge bit (A). After the start condition, the master sends 7 slave address bits and a R/W bit during the next 8 clock pulses. During the ninth clock pulse, the device that recognizes its own address pulls SDA low to acknowledge. The acknowledge bit is also used by both the master and the slave to acknowledge receipt of register addresses and data.

SDA

MSB

LSB

1

8

9

SCL

### Read and Write Protocol

Write to a Single Register

START(S)

ACK(A)

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| S | slave\_addr+W | AS | reg\_addr | AS | reg\_data | AS | P |

Read from a Single Register

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| S | slave\_addr+W | AS | reg\_addr | AS | S | slave\_addr+R | AS | reg\_data | NA | P |

S = START, P = STOP, AS = ACK from slave, AM = ACK from master, NA = No ACK

Table 8. SMBus Configuration Register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Register Address** | **Register Name** | **Access** | **Default** | **Description** |
| 0x01 | APL1[7:0] | R/W | 00h | Set Auto Phase Shedding Threshold 1. 0V ~ 630mV. (10mV / step)  VIMON < VAPL1=> LCS4 (lowest load current state) |
| 0x02 | APL2[7:0] | R/W | 00h | Set Auto Phase Shedding Threshold 2. 0V ~1.27V. (10mV / step)  VAPL1 < VIMON < VAPL2 => LCS3 |
| 0x03 | APL3[7:0] | R/W | 00h | Set Auto Phase Shedding Threshold 3. 0V ~ 2.55V. (10mV / step)  VAPL2 < VIMON < VAPL3 => LCS2 |
| 0x04 | APL4[7:0] | R/W | 00h | Set Auto Phase Shedding Threshold 4. 0V ~ 2.55V. (10mV / step)  VAPL3 < VIMON < VAPL4 => LCS1  VIMON > VAPL4 => LCS0 (highest load current state) |
| 0x05 | PWM\_Mid[7] APL\_Hys1[6:4] APL\_Hys2[2:0] | R/W | 55h | Bit[3]: Don't care.  PWM\_Mid[7] : Controller driving PWM middle state voltage "0" : Disable (default)  "1" : Enable  APL\_Hys1[6:4] : Hysteresis of APL1 threshold. 0mV ~ 140mV. (20mV / step)  APL\_Hys2[2:0] : Hysteresis of APL2 threshold. 0mV ~ 140mV. (20mV / step) |
| 0x06 | APL\_Hys3[6:4] APL\_Hys4[2:0] | R/W | 55h | Bit[7] & Bit[3] : Don't care.  APL\_Hys3[6:4] : Hysteresis of APL3 threshold. 0mV ~ 140mV. (20mV / step)  APL\_Hys4[2:0] : Hysteresis of APL4 threshold. 0mV ~ 140mV. (20mV / step) |
| 0x07 | IICP0[6:4] IICP1[2:0] | R/W | 75h | Bit[7] & Bit[3] : Don't care.  IICP0[6:4] : Operation phase number of LCS0. Default = 8-phase  IICP1[2:0] : Operation phase number of LCS1. Default = 6-phase  000 : 1 phase ; 001 : 2 phase ; 010 : 3 phase ; 011 : 4 phase  100 : 5 phase ; 101 : 6 phase ; 110 : 7 phase ; 111 : 8 phase |
| 0x08 | IICP2[6:4] IICP3[2:0] | R/W | 31h | Bit[7] & Bit[3] : Don't care.  IICP2[6:4] : Operation phase number of LCS2. Default = 4-phase  IICP3[2:0] : Operation phase number of LCS3. Default = 2-phase  000 : 1 phase ; 001 : 2 phase ; 010 : 3 phase ; 011 : 4 phase  100 : 5 phase ; 101 : 6 phase ; 110 : 7 phase ; 111 : 8 phase |
| 0x09 | IICP4[6:4] | R/W | 00h | Bit[7] & Bit[3:0] : Don't care.  IICP4[6:4] : Operation phase number of LCS4. Default = 1-phase  000 : 1 phase ; 001 : 2 phase ; 010 : 3 phase ; 011 : 4 phase  100 : 5 phase ; 101 : 6 phase ; 110 : 7 phase ; 111 : 8 phase |
| 0x0A | IICV0[7:4] IICV1[3:0] | R/W | 00h | IICV0[7:4] : Voltage offset of LCS0.  0mV ~ 150mV( 10mV / step ). Default = 0mV IICV1[3:0] : Voltage offset of LCS1.  0mV ~ 150mV( 10mV / step ). Default = 0mV |

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| **Register Address** | **Register Name** | **Access** | **Default** | **Description** |
| 0x0B | IICV2[7:4] IICV3[3:0] | R/W | 00h | IICV2[7:4] : Voltage offset of LCS2.  0mV ~ 150mV( 10mV / step ). Default = 0mV IICV3[3:0] : Voltage offset of LCS3.  0mV ~ 150mV( 10mV / step ). Default = 0mV |
| 0x0C | IICV4[7:4] | R/W | 00h | Bit[3:0]: Don't care.  IICV4[7:4] : Voltage offset of LCS4.  0mV ~ 150mV( 10mV / step ). Default = 0mV |
| 0x0D | IICF0[7:4] IICF1[3:0] | R/W | 88h | IICF0[7:4] : Operation frequency of LCS0. IICF1[3:0] : Operation frequency of LCS1.  0000 : 60% ; 0001 : 65% ; 0010 : 70% ; 0011 : 75% ;  0100 : 80% ; 0101 : 85% ; 0110 : 90% ; 0111 : 95% ;  1000 : 100% (default) ; 1001 : 125% ; 1010 : 150% ;  1011 : 175% ;1100 : 200% ; 1101 : 225% ; 1110 : 250% ;  1111 : 275% |
| 0x0E | IICF2[7:4] IICF3[3:0] | R/W | 88h | IICF2[7:4] : Operation frequency of LCS2. IICF3[3:0] : Operation frequency of LCS3.  0000 : 60% ; 0001 : 65% ; 0010 : 70% ; 0011 : 75% ;  0100 : 80% ; 0101 : 85% ; 0110 : 90% ; 0111 : 95% ;  1000 : 100% (default) ; 1001 : 125% ; 1010 : 150% ;  1011 : 175% ;1100 : 200% ; 1101 : 225% ; 1110 : 250% ;  1111 : 275% |
| 0x0F | IICF4[7:4] IICLL0[2:0] | R/W | 84h | Bit [3]: Don't care.  IICF4[7:4] : Operation frequency of LCS4.  0000 : 60% ; 0001 : 65% ; 0010 : 70% ; 0011 : 75% ;  0100 : 80% ; 0101 : 85% ; 0110 : 90% ; 0111 : 95% ;  1000 : 100% (default) ; 1001 : 125% ; 1010 : 150% ;  1011 : 175% ; 1100 : 200% ; 1101 : 225% ; 1110 : 250% ;  1111 : 275%  IICLL0[2:0] : Load line setting of LCS0.  000 : 0% ; 001 : 25% ; 010 : 50% ; 011 : 75% ;  100 :100%(default) ; 101 : 125% ; 110 : 150% ; 111 : 175% |
| 0x10 | IICLL1[6:4] IICLL2[2:0] | R/W | 44h | Bit[7] & Bit[3] : Don't care.  IICLL1[6:4] : Load line setting of LCS1. IICLL2[2:0] : Load line setting of LCS2.  000 : 0% ; 001 : 25% ; 010 : 50% ; 011 : 75%;  100 :100%(default) ; 101 : 125% ; 110 : 150% ; 111 : 175% |
| 0x11 | IICLL3[6:4] IICLL4[2:0] | R/W | 44h | Bit[7] & Bit[3] : Don't care.  IICLL3[6:4] : Load line setting of LCS3. IICLL4[2:0] : Load line setting of LCS4.  000 : 0% ; 001 : 25% ; 010 : 50% ; 011 : 75%;  100 :100%(default) ; 101 : 125% ; 110 : 150% ; 111 : 175% |
| 0x12 | CB\_EN[7] PH8\_IGAIN[6:2] | R/W | BCh | Bit[1:0]: Don't care.  CB\_EN[7] : On/Off control of current balance function, default = ON.  "0" = OFF (current balance function is disabled) "1" = ON (current balance function is enabled)  PH8\_IGAIN[6:2] : PHASE8 current balance gain adjustment. PH8\_IGAIN = 243.75% - Bit[6:2] x 6.25%, default = 150%. |
| 0x13 | PH7\_IGAIN[6:2] | R/W | 3Ch | Bit[7] & Bit[1:0]: Don't care.  PH7\_IGAIN[6:2] : PHASE7 current balance gain adjustment. PH7\_IGAIN = 243.75% - Bit[6:2] x 6.25%, default = 150%. |
| 0x14 | PH6\_IGAIN[6:2] | R/W | 3Ch | Bit[7] & Bit[1:0]: Don't care.  PH6\_IGAIN[6:2] : PHASE6 current balance gain adjustment. PH6\_IGAIN = 243.75% - Bit[6:2] x 6.25%, default = 150%. |

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| **Register Address** | **Register Name** | **Access** | **Default** | **Description** |
| 0x15 | PH5\_IGAIN[6:2] | R/W | 3Ch | Bit[7] & Bit[1:0]: Don't care.  PH5\_IGAIN[6:2] : PHASE5 current balance gain adjustment. PH5\_IGAIN = 243.75% - Bit[6:2] x 6.25%, default = 150%. |
| 0x16 | PH4\_IGAIN[6:2] | R/W | 3Ch | Bit[7] & Bit[1:0]: Don't care.  PH4\_IGAIN[6:2] : PHASE4 current balance gain adjustment. PH4\_IGAIN = 243.75% - Bit[6:2] x 6.25%, default = 150%. |
| 0x17 | PH3\_IGAIN[6:2] | R/W | 3Ch | Bit[7] & Bit[1:0]: Don't care.  PH3\_IGAIN[6:2] : PHASE3 current balance gain adjustment. PH3\_IGAIN = 243.75% - Bit[6:2] x 6.25%, default = 150%. |
| 0x18 | PH2\_IGAIN[6:2] | R/W | 3Ch | Bit[7] & Bit[1:0]: Don't care.  PH2\_IGAIN[6:2] : PHASE2 current balance gain adjustment. PH2\_IGAIN = 243.75% - Bit[6:2] x 6.25%, default = 150%. |
| 0x19 | PH1\_IGAIN[6:2] | R/W | 3Ch | Bit[7] & Bit[1:0]: Don't care.  PH1\_IGAIN[6:2] : PHASE1 current balance gain adjustment. PH1\_IGAIN = 243.75% - Bit[6:2] x 6.25%, default = 150%. |
| 0x1A | PH8\_IOS[6:4] PH7\_IOS[2:0] | R/W | 00h | Bit[7] & Bit[3] : Don't care.  PH8\_IOS[6:4] : PHASE8 current balance offset adjustment, default = 0uA.  PH7\_IOS[2:0] : PHASE7 current balance offset adjustment, default = 0uA.  000 : 0uA ; 001 : 0.4uA ; 010 : 0.8uA ; 011 : 1.2uA ;  100 : 1.6uA ; 101 : 2.0uA ; 110 : 2.4uA ; 111 : 2.8uA |
| 0x1B | PH6\_IOS[6:4] PH5\_IOS[2:0] | R/W | 00h | Bit[7] & Bit[3] : Don't care.  PH6\_IOS[6:4] : PHASE6 current balance offset adjustment, default = 0uA.  PH5\_IOS[2:0] : PHASE5 current balance offset adjustment, default = 0uA.  000 : 0uA ; 001 : 0.4uA ; 010 : 0.8uA ; 011 : 1.2uA ;  100 : 1.6uA ; 101 : 2.0uA ; 110 : 2.4uA ; 111 : 2.8uA |
| 0x1C | PH4\_IOS[6:4] PH3\_IOS[2:0] | R/W | 00h | Bit[7] & Bit[3] : Don't care.  PH4\_IOS[6:4] : PHASE4 current balance offset adjustment, default = 0uA.  PH3\_IOS[2:0] : PHASE3 current balance offset adjustment, default = 0uA.  000 : 0uA ; 001 : 0.4uA ; 010 : 0.8uA ; 011 : 1.2uA ;  100 : 1.6uA ; 101 : 2.0uA ; 110 : 2.4uA ; 111 : 2.8uA |
| 0x1D | PH2\_IOS[6:4] PH1\_IOS[2:0] | R/W | 00h | Bit[7] & Bit[3] : Don't care.  PH2\_IOS[6:4] : PHASE2 current balance offset adjustment, default = 0uA.  PH1\_IOS[2:0] : PHASE1 current balance offset adjustment, default = 0uA.  000 : 0uA ; 001 : 0.4uA ; 010 : 0.8uA ; 011 : 1.2uA ;  100 : 1.6uA ; 101 : 2.0uA ; 110 : 2.4uA ; 111 : 2.8uA |
| 0x1E | POCGAIN8[7:4] POCGAIN7[3:0] | R/W | BBh | POCGAIN8[7:4] : PHASE8 channel current limit gain adjustment, default = 100%.  POCGAIN7[3:0] : PHASE7 channel current limit gain adjustment, default = 100%.  0000 : 237.5% ; 0001 : 225% ; 0010 : 212.5% ;  0011 : 200% ; 0100 : 187.5% ; 0101 : 175% ;  0110 : 162.5% ; 0111 :150% ; 1000 : 137.5% ;  1001 : 125% ; 1010 : 112.5% ; 1011 : 100% ;  1100 : 87.5% ; 1101 : 75% ; 1110 : 62.5% ; 1111 : 50% |

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| **Register Address** | **Register Name** | **Access** | **Default** | **Description** |
| 0x1F | POCGAIN6[7:4] POCGAIN5[3:0] | R/W | BBh | POCGAIN6[7:4] : PHASE6 channel current limit gain adjustment, default = 100%.  POCGAIN5[3:0] : PHASE5 channel current limit gain adjustment, default = 100%.  0000 : 237.5% ; 0001 : 225% ; 0010 : 212.5% ;  0011 : 200% ; 0100 : 187.5% ; 0101 : 175% ;  0110 : 162.5% ; 0111 :150% ; 1000 : 137.5% ;  1001 : 125% ; 1010 : 112.5% ; 1011 : 100% ;  1100 : 87.5% ; 1101 : 75% ; 1110 : 62.5% ; 1111 : 50% |
| 0x20 | POCGAIN4[7:4] POCGAIN3[3:0] | R/W | BBh | POCGAIN4[7:4] : PHASE4 channel current limit gain adjustment, default = 100%.  POCGAIN3[3:0] : PHASE3 channel current limit gain adjustment, default = 100%.  0000 : 237.5% ; 0001 : 225% ; 0010 : 212.5% ;  0011 : 200% ; 0100 : 187.5% ; 0101 : 175% ;  0110 : 162.5% ; 0111 :150% ; 1000 : 137.5% ;  1001 : 125% ; 1010 : 112.5% ; 1011 : 100% ;  1100 : 87.5% ; 1101 : 75% ; 1110 : 62.5% ; 1111 : 50% |
| 0x21 | POCGAIN2[7:4] POCGAIN1[3:0] | R/W | BBh | POCGAIN2[7:4] : PHASE2 channel current limit gain adjustment, default = 100%.  POCGAIN1[3:0] : PHASE1 channel current limit gain adjustment, default = 100%.  0000 : 237.5% ; 0001 : 225% ; 0010 : 212.5% ;  0011 : 200% ; 0100 : 187.5% ; 0101 : 175% ;  0110 : 162.5% ; 0111 :150% ; 1000 : 137.5% ;  1001 : 125% ; 1010 : 112.5% ; 1011 : 100% ;  1100 : 87.5% ; 1101 : 75% ; 1110 : 62.5% ; 1111 : 50% |
| 0x22 | CH\_OC[7:0] | R/W | -- | CH\_OC[7:0] : Channel current limit threshold adjustment. VCH\_OC = Bit[7:0] x 10mV |
| 0x23 | Total\_OCP[2:0] | R/W | 00h | Bit [7:3] : Don't care.  Total\_OCP[2:0] : Total output current protection threshold adjustment.  000 : 100% (default) ; 001 : 001% ; 010 : 120% ; 011 : 130%  100 : 140% ; 101 : 150% ; 110 : 160% ; 111 : 170% |
| 0x24 | T\_OCP[7:6] UV[5:3]  OV[2:0] | R/W | 1Bh | T\_OCP[7:6] : Total output current protection delay time adjustment.  00 : 20us (default) ; 01 : 10us ; 10 : 6.67us ; 11: 5us UV[5:3] : Under voltage protection threshold adjustment. 000 : 30% ; 001: 35% ; 010 : 40% : 011 : 45% (default) ;  100 : 50% ; 101 : 55% ; 110 : 60% ; 111 : 65%  OV[2:0] : Over voltage protection threshold adjustment.  000 : 140% ; 001: 145% ; 010 : 150% : 011 : 155% (default)  100 : 160% ; 101 : 165% ; 110 : 170% ; 111 : 175% |
| 0x25 | VR\_SHDN[7:0] | R/W | FEh | VR\_SHDN[7:0] : Thermal shutdown threshold adjustment. 0V ~ 2.04V, default = 2.04V(8mV/step) |
| 0x26 | GCOMP[3:0] | R/W | 00h | Bit[7:4] : Don't care.  GCOMP[3:0] : OTA Gm value selection, default = 1960uA/V. 000 : 1960uA/V ; 001: 2300uA/V ; 010 : 2610uA/V ;  011 : 2890uA/V ; 100 : 3380uA/V ; 101 : 1580uA/V ;  110 : 1150uA/V ; 111 : 636uA/V |

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| **Register Address** | **Register Name** | **Access** | **Default** | **Description** |
| 0x2A | Misc2[6:2] | R/W | 20h | Bit[7] & Bit[1:0]: Internal testing bit. Keep these bit values = "0"  Bit[6]: Output voltage offset enable control "0" = Disable Offset(default)  "1" = Enable Offset  Bit[5] : Auto Phase H/W setting enable control "0" = Ignore H/W setting  "1" = Follow H/W setting (default)  Bit[4]: Auto Phase enable control (when Bit[5]=0)  "0" = Disable Auto Phase (forced full phase operation) (default)  "1" = Enable Auto Phase  Bit[3]: DCM enable control when in 1-phase operation "0" = Disable DCM (default)  "1" = Enable DCM  Bit[2]: Forced full phase operation when channel OCL is triggered at APS Mode.  "0" = Disable (default) "1" = Enable |
| 0x2C | IOUT[7:0] | RO | -- | Total output current reporting, ADC result of IMON voltage  .(10mV/step) |
| 0x2D | VOUT[7:0] | RO | -- | Output voltage reporting. (sense FB voltage)(10mV/step) |
| 0x2E | TEMP[7:0] | RO | -- | Temperature reporting, reports highest temperature of DrMOS. (8mV/step) |
| 0x33 | ZC\_OFFSET[7:5] T\_PH\_DW[4:2] OTP[1] | R/W | 26h | Bit[0]: Internal testing bit. Keep this bit value = "0".  ZC\_OFFSET[7:5]: ZC offset adjustment.  000:0mV; 001: 2mV(default); 010: 4mV; 011: 6mV;  100: 8mV; 101: 10mV; 110: 12mV; 111: 14mV  T\_PH\_DW[4] : Down phase delay control. "0" : Disable (default)  "1" : Enable  T\_PH\_DW[3:2] : Down phase delay time 00=10us 01=20us(default) 10=40us 11=80us OTP[1] : OTP protection control.  "0" : Disable  "1" : Enable (default) |
| 0x35 | PROT\_IND2[7:0] | RO | 00h | Each channel OCL indicator.  Bit[7] : PHASE8 channel OCL indicator Bit[6] : PHASE7 channel OCL indicator Bit[5] : PHASE6 channel OCL indicator Bit[4] : PHASE5 channel OCL indicator Bit[3] : PHASE4 channel OCL indicator Bit[2] : PHASE3 channel OCL indicator Bit[1] : PHASE2 channel OCL indicator Bit[0] : PHASE1 channel OCL indicator "0" = Not Active  "1" = Active |

# Functional Description

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| **Register Address** | **Register Name** | **Access** | **Default** | **Description** |
| 0x37 | PWM1\_H\_Mid[2] BF[1] | R/W | 02h | Bit[7:3] & Bit[0]: Internal Testing Bit. Keep these bit values = "0"  PWM1\_H\_Mid[2] : PWM1 output switching behavior control. Once it is enabled, only PWM1 output switching behavior changes from "High -> Low" to "High -> Middle", other PWM outputs keep "High -> Low" switching behavior.  "0" : Disable (default) "1" : Enable  BF[1]: Beat Frequency Function "0" : Disable  "1" : Enable (default) |
| 0x38 | ACLL[7:5] V\_OCL\_MIN[4:2] IOUT\_AVG\_SR[1:0] | R/W | 2Ch | Bit[7]: AC load line control.  "0" : Follow HW setting (default) "1" : Enable AC Load Line  Bit[6:5]: AC load line response time  00=40us 01=80us(default) 10=120us 11=160us Bit[4]: OCL disable if REFIN < V\_OCL\_Min  "0" = Disable(default)  "1" = Enable  Bit[3:2]: OCL disable if REFIN voltage reaches below threshold.  "00"=0.3V ; "01"=0.4V ; "10"=0.5V ; "11"=0.6V(default)  Bit[1:0]: Sample rate of IOUT\_AVG.  "00"=50us(default) ; "01"=200us ; "10"=800us ; "11"=3200us |
| 0x39 | SMBus\_Lock[7:0] | R/W | 00h | SMBus\_Lock[7:0] : SMBus register security lock.  SMBus register default is locked, all the registers are "read only" and cannot be modified before unlock. Once the SMBus unlock and lock again, it needs VCC re-POR to reset.  Bit[7:0] = "94h" , unlock SMBus Bit[7:0] = "87h" , lock SMBus |
| 0x3A | SL\_RAMP[7:6] | R/W | C0h | Bit [5:0]: Don't care.  SL\_RAMP[7:6] :RAMP slope adjustment.  00 : 50% ; 01 : 75% ; 10 : 100% ; 11 : 125%(default) |
| 0x3B | PROT\_IND[7:3] OP\_PH\_MON[2:0] | RO | 00h | Protection indication, indicating which protection is triggered.  Bit[7] : OTP indicator "0" = Not Active  "1" = Active  Bit[6] :Total OCP Indicator "0" = Not Active  "1" = Active  Bit[5] :Channel OCL indicator "0" = Not Active  "1" = Active  Bit[4] : OVP Indicator "0" = Not Active  "1" = Active  Bit[3] : UVP Indicator "0" = Not Active  "1" = Active  Bit[2:0] : Operating Phase Number Monitor  000 : 1 phase ; 001 : 2 phase ; 010 : 3 phase ; 011 : 4 phase  100 : 5 phase ; 101 : 6 phase ; 110 : 7 phase ; 111 : 8 phase |

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| **Register Address** | **Register Name** | **Access** | **Default** | **Description** |
| 0x3C | Misc1[3:0] | R/W | 0Fh | Bit [7:5]: Don't care.  Bit [4]: Internal testing bit. Keep this bit value = "0".  Bit[3]: Total OCP control  "0" = Disable Total OCP function  "1" = Enable Total OCP function(default)  Bit[2]: Channel OCL Control  "0" = Disable Channel OCL function  "1" = Enable Channel OCL function(default)  Bit[1]: OVP Control  "0" = Disable OVP function  "1" = Enable OVP function(default)  Bit[0]: UVP Control  "0" = Disable UVP function  "1" = Enable UVP function(default) |
| 0x3D | IOUT\_AVG[7:0] | RO | -- | Average output current report, ADC result of VIMON. (10mV/step) |
| 0x27 | Vendor ID | RO | 00h |  |
| 0x28 | Device ID | RO | 2Bh |  |

(Note 1)

Supply Input Voltage, 5VCC

## Absolute Maximum Rating

-0.3V to +6V

Other Pins 0.3V to +6V

Storage Temperature Range -65OC to +150OC

Junction Temperature 150OC

Lead Temperature (Soldering, 10 sec) 260OC

ESD Rating (Note 2)

HBM (Human Body Mode) 2kV

# Thermal Information

Package Thermal Resistance (Note 3)

VQFN5x5 - 40L JA 36oC/W

VQFN5x5 - 40L JC 3oC/W

Power Dissipation, PD @ TA = 25oC

VQFN5x5 - 40L 2.78W

# Recommended Operation Conditions

(Note 4)

Operating Junction Temperature Range Operating Ambient Temperature Range

-40oC to +125oC

-40oC to +85oC

Supply Input Voltage, 5VCC 4.5V to 5.5V

Power Stage Input Voltage, VIN 3V to 20V

**Note 1.** Stresses listed as the above *Absolute Maximum Ratings* may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

**Note 2.** Devices are ESD sensitive. Handling precaution recommended.

**Note 3.** JA is measured in the natural convection at TA = 25oC on a low effective thermal conductivity test board of

JEDEC 51-3 thermal measurement standard.

**Note 4.** The device is not guaranteed to function outside its operating conditions.

(5VCC = 5V, TA = 25oC, unless otherwise specified)

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| **Parameter** | **Symbol** | **Test Conditions** | **Min** | **Typ** | **Max** | **Unit** |
| **Supply Input** | | | | | | |
| 5VCC POR Threshold | POR5VCC | 5VCC rising | 4 | 4.3 | 4.5 | V |
| 5VCC POR Hysteresis | HYS5VCC\_POR |  | -- | 300 | -- | mV |
| Quiescent Current | IQ | EN = high , No switching | -- | 7 | -- | mA |
| Shutdown Current | ISD | EN = 0V | -- | 300 | -- | uA |
| **Power Stage Input Voltage Monitoring** | | | | | | |
| VINMON Monitoring Range |  |  | 0.3 | -- | 2.4 | V |
| VINMON Rising Threshold | VVINMON |  | -- | 0.2 | -- | V |
| VINMON Hysteresis | VVINMON\_HYS |  | -- | 100 | -- | mV |
| **Enable Control** | | | | | | |
| Logic Low | VIL\_EN |  | -- | -- | 0.1 | V |
| Logic High | VIH\_EN |  | 0.2 | -- | -- | V |
| **PWMVID Interface (VREF, VID, REFADJ, REFIN)** | | | | | | |
| VREF Voltage Accuracy | VREF |  | 1.98 | 2 | 2.02 | V |
| VREF Sourcing Current | IREF\_SRC | VREF short to GND | 10 | -- | -- | mA |
| REFIN Disable Threshold | VREFIN\_DSB |  | -- | 0.1 | -- | V |
| External Reference Voltage Range | VREFIN |  | 0.2 | -- | 2 | V |
| VID Input Low | VIL\_VID |  | -- | -- | 0.6 | V |
| VID Input High | VIH\_VID |  | 1.2 | -- | -- | V |
| VID Tri-state Voltage | VTRI\_VID |  | -- | 0.9 | -- | V |
| VID Tri-state Delay | TTRI\_VID | VID from High to Tri-state; VID from Low to Tri-state | -- | 100 | -- | ns |
| REFADJ Source Resistance | RBF\_SRC | ISRC = 1mA | -- | 20 | -- |  |
| REFADJ Sink Resistance | RBF\_SNK | ISINK = 1mA | -- | 20 | -- |  |
| **DAC Voltage Accuracy** | | | | | | |
| DAC Output Accuracy | VDAC | Load Line Disabled | -1 | -- | 1 | mV |
| **Oscillator** | | | | | | |
| Operation Frequency Range | FSW | Per-phase operation frequency | 200 | -- | 2000 | kHz |
| Frequency Accuracy |  | Frequency setting to 300kHz | 270 | 300 | 330 | kHz |
| Maximum Duty Cycle | DMAX | Ramp slope setting to 100% | -- | 45 | -- | % |
| Minimum PWM Pulse Width | TPWM\_MIN | Guaranteed by design | -- | 40 | -- | ns |

# Electrical Characteristics

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| **Parameter** | **Symbol** | **Test Conditions** | **Min** | **Typ** | **Max** | **Unit** |
| **Soft-Start** | | | | | | |
| Output Ramp Up Time | TRAMP | RPWM8 = unstuffed | -- | 640 | -- | us |
| Initialization Time | TINIT | EN go high to Vout start up from 0V | -- | 550 | -- | us |
| **Error Amplifier** | | | | | | |
| Offset Voltage | VOS(EA) |  | -1 | -- | 1 | mV |
| Input Bias Current | IEA | Guaranteed by design | -10 | -- | 10 | nA |
| Open Loop DC Gain | AO | Guaranteed by design | -- | 70 | -- | dB |
| Gain-Bandwidth Product | GBW | Guaranteed by design | -- | 10 | -- | MHz |
| Trans-conductance | GM |  | -- | 1960 | -- | uA / V |
| COMP Source Current | ICOMP\_SRC |  | -- | 300 | -- | uA |
| COMP Sink Current | ICOMP\_SNK |  | -- | 300 | -- | uA |
| **FBRTN** | | | | | | |
| FBRTN Current | IFBRTN | EN = 1.8V, normal operation | -- | -- | 100 | uA |
| **Current Summing Amplifier** | | | | | | |
| Input Offset Voltage | VOFF\_CSA | Guaranteed by design | -1 | -- | 1 | mV |
| Max Sourcing Current | ISRC\_CSA |  | 300 | -- | -- | uA |
| **Current Sense Amplifier ( CSP1~CSP8 )** | | | | | | |
| Input Offset Voltage | VOFF\_CSA | Guaranteed by design | -1 | -- | 1 | mV |
| **REFOUT** | | | | | | |
| REFOUT Output Voltage | VREFOUT |  | -- | 1.2 | -- | V |
| REFOUT Sink Resistor | RREFOUT | EN=0V, REFOUT=2.4V | -- | 240 | -- | k |
| **PWM Output (PWM1~PWM8)** | | | | | | |
| Output Low Voltage | VPWM\_L | ISNK = 4mA | -- | -- | 0.2 | V |
| Output Hight Voltage | VPWM\_H | ISOURCE = 4mA | 4.7 | -- | -- | V |
| High Impedance State Leakage |  | VPWM = 0V | -1 | -- | 0 | uA |
| VPWM = 5V | 0 | -- | 1 | uA |
| Source Current | IPWMx | REN = 10k;  during TINIT time | -- | 10 | -- | uA |
| **Power Saving Input (PSI)** | | | | | | |
| Power Saving Mode Logic | VPSI | Full-Phase Mode | 1.4 | -- | -- | V |
| Auto-Phase Shedding Mode | 0.8 | -- | 1.2 |
| Low-Phase Mode | -- | -- | 0.4 |

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **Parameter** | **Symbol** | **Test Conditions** | **Min** | **Typ** | **Max** | **Unit** |
| **DC Load Line** | | | | | | |
| DC Load Line Enable Threshold |  | PWM1 resistor strap to GND | 25 | -- | 200 | k |
| DC Load Line Always Functional |  |  | 250 | -- | -- | k |
| **IMON** | | | | | | |
| Current Mirror Accuracy |  | From ISUM to IEAP or IMON | 95 | 100 | 105 | % |
| **Protection** | | | | | | |
| Channel Current Limit Setting Current | ICH\_OC |  | -- | 20 | -- | uA |
| Total Over Current Protection (OCP) Threshold | VOCP | Measure IMON voltage | -- | 2.1 | -- | V |
| Total Over Current Protection (OCP) Delay | TOCP | VIMON > VOCP | -- | 20 | -- | us |
| Under Voltage Protection (UVP) Threshold | VUVP |  | 40 | 45 | 50 | % |
| Under Voltage Protection (UVP) Delay | TUVP |  | -- | 5 | -- | us |
| Over Voltage Protection (OVP) Threshold | VOVP | VFB/VREFIN | 150 | 155 | 160 | % |
| Over Voltage Protection (OVP) Delay | TOVP |  | -- | 5 | -- | us |
| Over Temperature Protection (OTP) Threshold | TOTP | Guaranteed by design | -- | 160 | -- | oC |
| **Power Good Indicator** | | | | | | |
| PGOOD Output Low Level | VPG | ISINK = 4mA | -- | -- | 0.3 | V |
| PGOOD Leakage Current | IPG\_Leak | VPGOOD = 5V | -- | -- | 0.1 | uA |
| **SMBus Interface (SCL & SDA)** | | | | | | |
| Input Low Voltage | VIL\_SMBus | Guaranteed by design | -- | -- | 0.4 | V |
| Input High Voltage | VIH\_SMBus | Guaranteed by design | 1.6 | -- | -- | V |
| Pull Down Resistance | RPULL\_SMBus | Guaranteed by design | -- | 8 | -- |  |
| **Thermal Monitoring (TSENSE)** | | | | | | |
| ADC Voltage Range | VADC | 8mV/step | 0 | -- | 2.04 | V |
| Thermal Shutdown Threshold |  |  | -- | 2.032 | -- | V |

### Power On from EN

Time : 200us/Div

VIN = 12V, VOUT = 0.81V, IOUT = 0A

### PSI = 0V⮀1.8V

Time : 100us/Div

VIN = 12V, VOUT = 0.81V(offset), IOUT = 0A

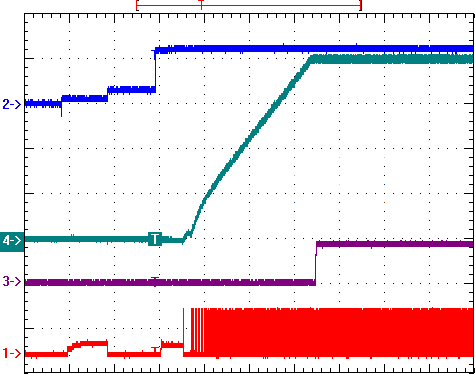
### VID = Low to High

Time : 40us/Div

VIN = 12V, VOUT = 0.81V, IOUT = 0A, CDAC = 100nF

# Typical Operation Characteristics

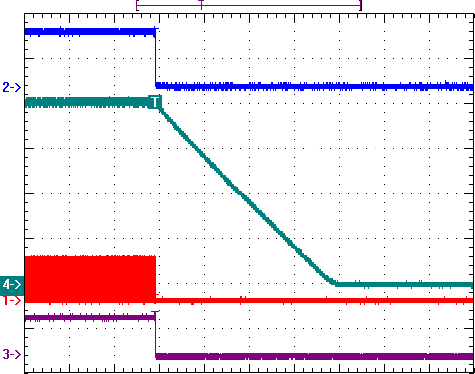
### Power Off from EN



EN(2V/Div)

VOUT(200mV/Div) PGOOD(2V/Div)

PWM1(5V/Div)



EN(2V/Div)

VOUT(200mV/Div)

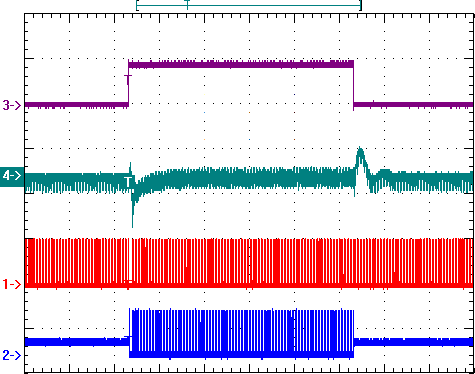
PWM1(5V/Div)

PGOOD(2V/Div)

Time : 200us/Div

VIN = 12V, VOUT = 0.81V, IOUT = 1A

### PSI = 1V⮀1.8V

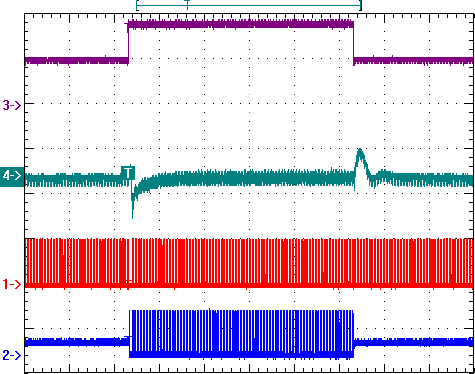


PSI(2V/Div)

VOUT(50mV/Div)

PWM1(5V/Div)

PWM8(5V/Div)



PSI(1V/Div)

VOUT(50mV/Div)

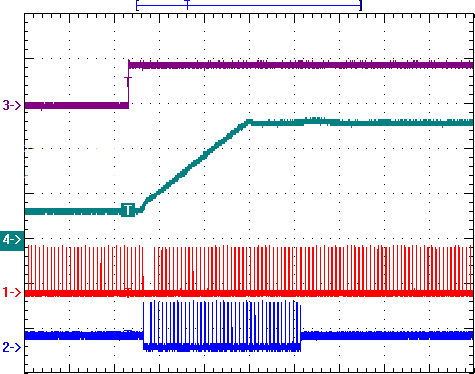
PWM1(5V/Div)

PWM8(5V/Div)

Time : 100us/Div

VIN = 12V, VOUT = 0.81V(offset), IOUT = 0A

### VID = High to Low

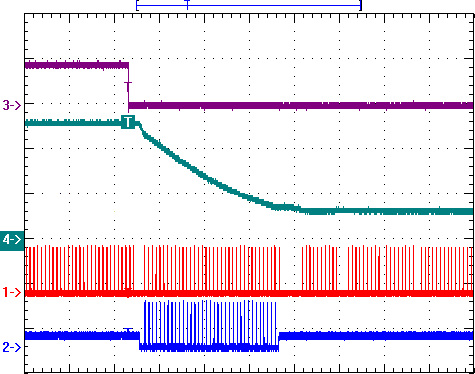


VID(2V/Div)

VOUT(500mV/Div)

PWM1(5V/Div)

PWM8(5V/Div)



VID(2V/Div)

VOUT(500mV/Div)

PWM1(5V/Div)

PWM8(5V/Div)

Time : 40us/Div

VIN = 12V, VOUT = 0.81V, IOUT = 0A, CDAC = 100nF

### Load Transient - Undershoot

Time : 40us/Div

VIN = 12V, VOUT = 0.81V(offset), IOUT = 1A to 150A

### Auto Phase Shedding

Time : 40us/Div

VIN = 12V, VOUT = 0.81V, VIMON = 0V to 2V

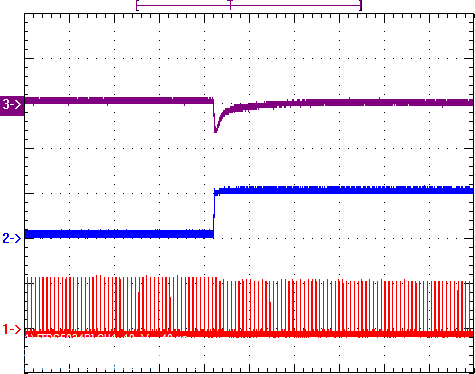
### Under Voltage Protection

Time : 4us/Div

VIN = 12V, VOUT = 0.81V, IOUT = 0A

# Typical Operation Characteristics

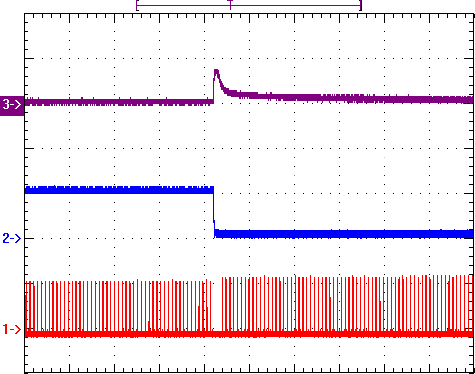
### Load Transient - Overshoot



VOUT(200mV/Div)

IOUT(133A/Div)

PHASE1(10V/Div)



VOUT(200mV/Div)

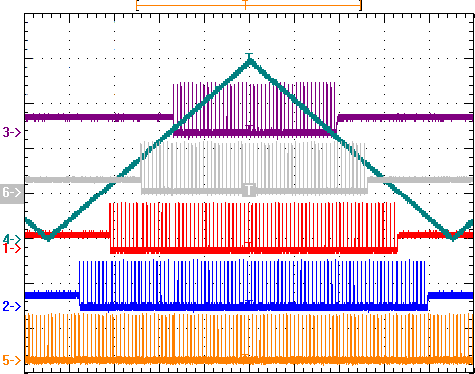
IOUT(133A/Div)

PHASE1(10V/Div)

Time : 40us/Div

VIN = 12V, VOUT = 0.81V(offset), IOUT = 1A to 150A

### Over Current Protection



IMON(500mV/Div)

PWM8(5V/Div)

PWM6(5V/Div)

PWM2

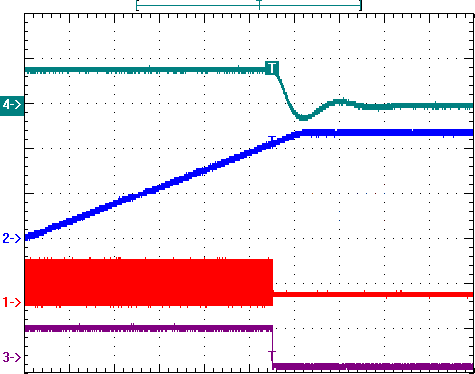
(5V/Div)

PWM4

(5V/Div)

PWM1

(5V/Div)



VOUT(1V/Div)

IMON(1V/Div)

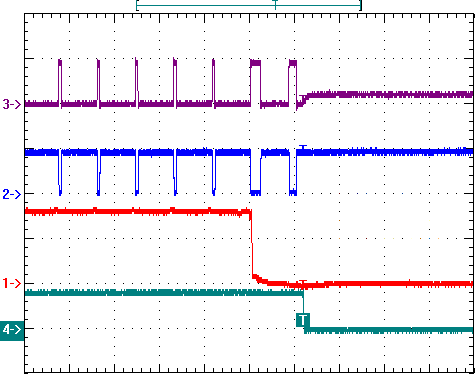
PWM1(5V/Div)

PGOOD(2V/Div)

Time : 200us/Div

VIN = 12V, VOUT = 0.81V, VIMON = 0V to 2.4V

### Over Voltage Protection

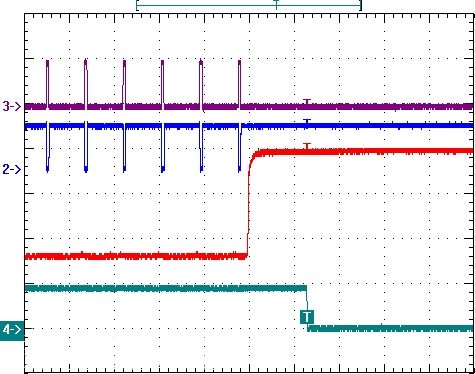


PWM(5V/Div)

LG(5V/Div)

FB(500mV/Div)

PGOOD(2V/Div)



PWM(5V/Div)

LG(5V/Div)

FB(500mV/Div)

PGOOD(2V/Div)

Time : 4us/Div

VIN = 12V, VOUT = 0.81V, IOUT = 0A

## Package Information

VQFN5x5 - 40L

0.30 - 0.50

3.20 - 3.80

0.15 - 0.25

3.20 - 3.80

4.90 - 5.10

Bottom View - Exposed Pad



4.90 - 5.10

Pin 1 mark

0.80 - 1.00



0.0 - 0.05 0.20 REF

Note

1. Package Outline Unit Description:

BSC: Basic. Represents theoretical exact dimension or dimension target MIN: Minimum dimension specified.

MAX: Maximum dimension specified.

REF: Reference. Represents dimension for reference use only. This value is not a device specification. TYP. Typical. Provided as a general value. This value is not a device specification.

1. Dimensions in Millimeters.
2. Drawing not to scale.
3. These dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm.

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