

CE391 Lab 2 Report

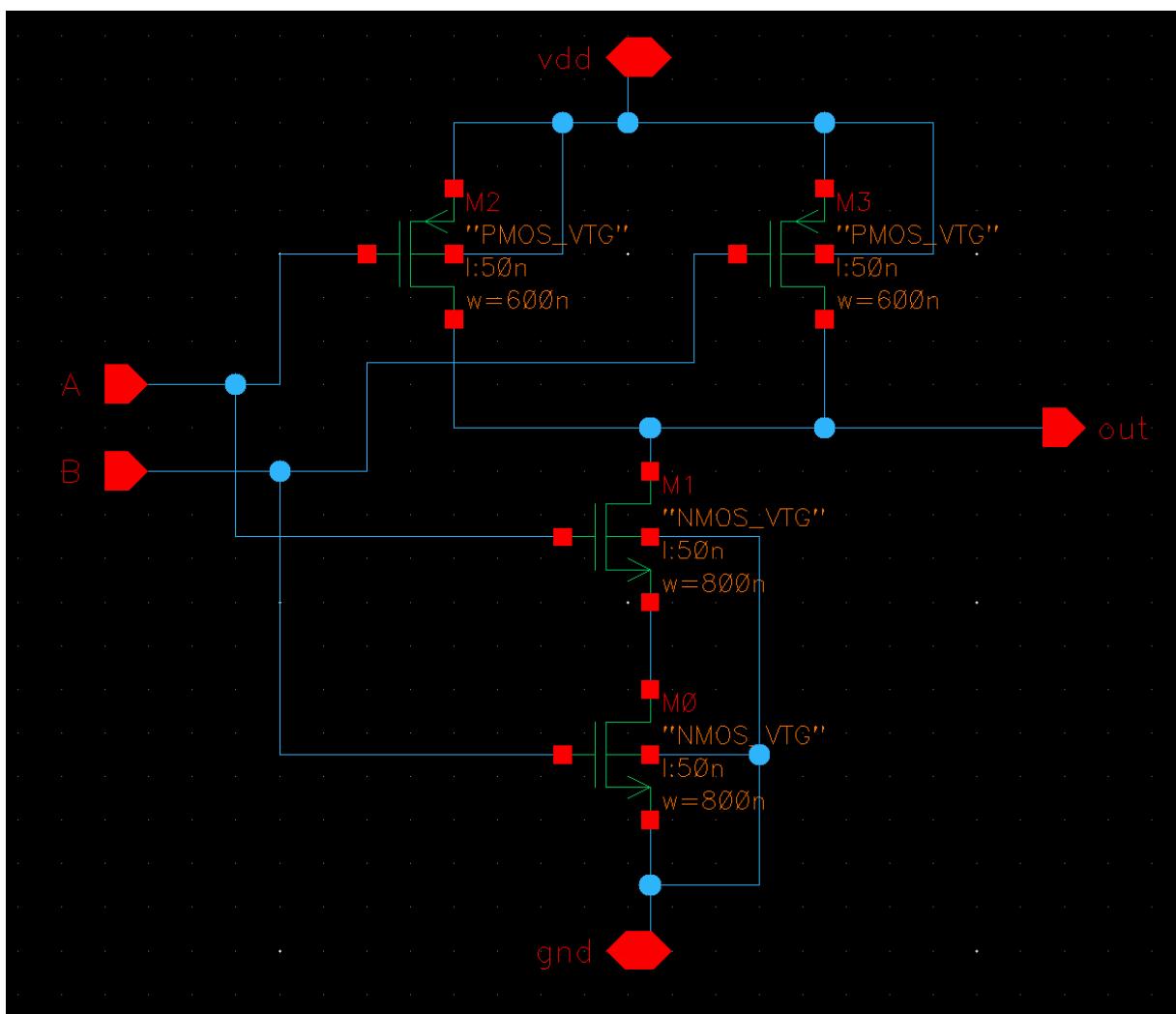
Luc Ah-Hot, Yuqing Wang, Giovanni Michel

NAND2

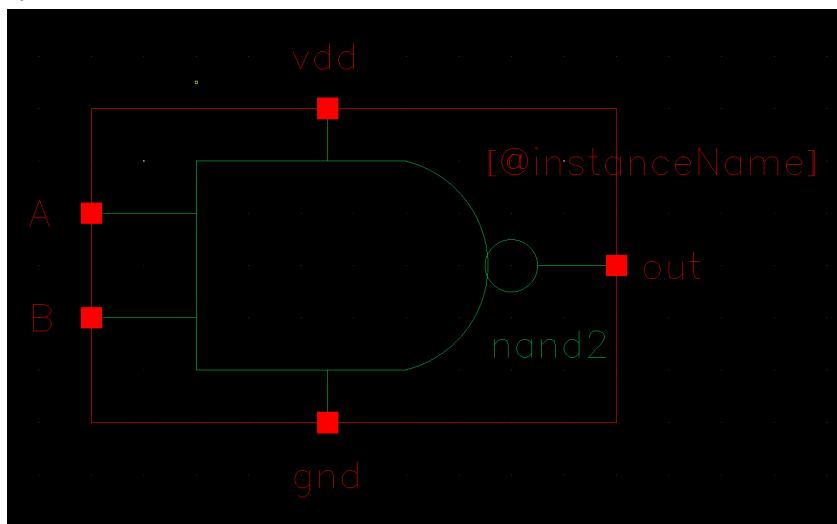
PMOS width = 600nm

NMOS width = 800nm

Schematic:

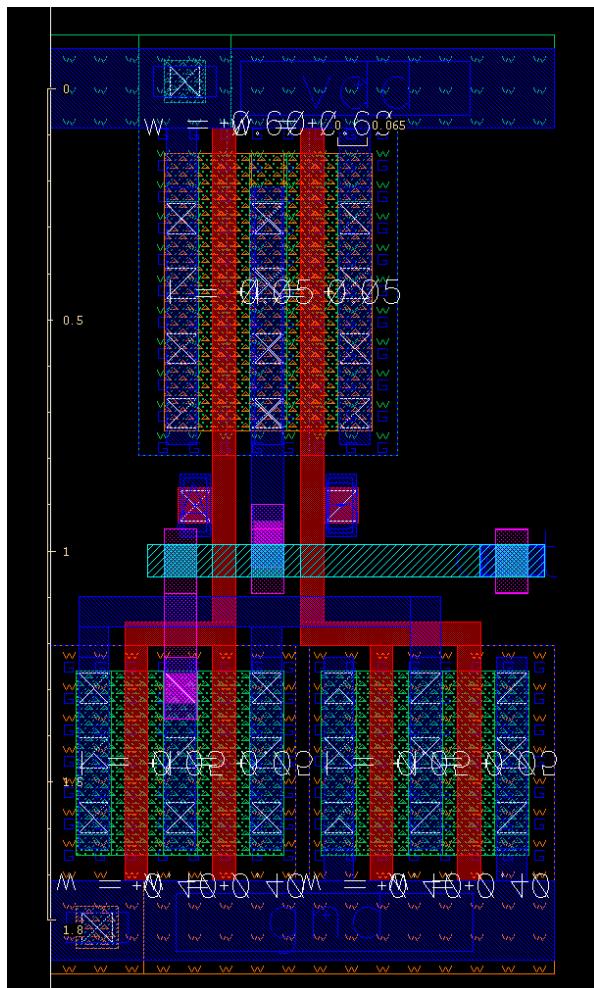


Symbol:



Layout:

Used 2-fingered NMOS transistors that were 400nm wide each to create a 800nm wide NMOS.



DRC Report:

Calibre - RVE v2011.4_35.27 : nand2.drc.results

File View Highlight Tools Window Setup Help

Topcell nand2, 0 Results (in 0 of 167 Checks) Show All

Cell / Check

- Cell nand2
 - Check Well.1
 - Check Well.2
 - Check Well.4
 - Check Poly.1
 - Check Poly.2
 - Check Poly.3
 - Check Poly.4
 - Check Poly.5
 - Check Poly.6
 - Check Active.1
 - Check Active.2
 - Check Active.3
 - Check Active.4
 - Check Implant.1
 - Check Implant.2
 - Check Implant.3

LVS Report:

Calibre - RVE v2011.4_35.27 : svdb nand2

File View Highlight Tools Window Setup Help

Navigator Comparison Results

Results Extraction Results Comparison Results Reports Rules File Extraction Report LVS Report View Info Finder Schematics Setup Options

Comparison Results

Layout Cell / Type	Source Cell	Nets	Instances	Ports
nand2	nand2	5L, 5S	1L, 1S	5L, 5S

Cell nand2 Summary (Clean)

CELL COMPARISON RESULTS (TOP LEVEL)

```

      #      #####
      #      #####
      #      #   CORRECT   #
      #      #      #
      #      #####
  
```

LAYOUT CELL NAME: nand2
SOURCE CELL NAME: nand2

INITIAL NUMBERS OF OBJECTS

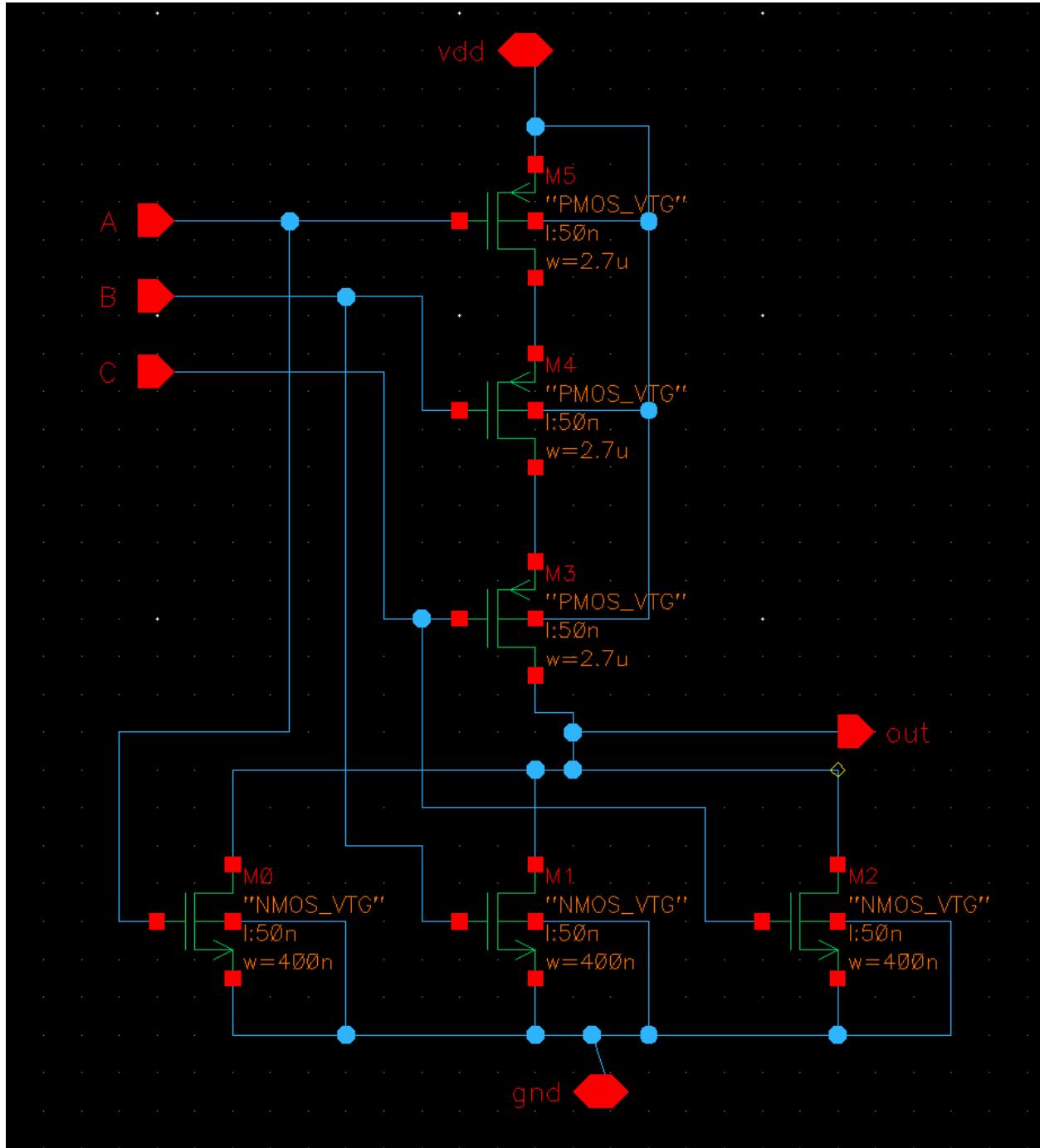
	Layout	Source	Component Type
Ports:	5	5	
Nets:	6	6	
Instances:	4	2	MN (4 pins)
	2	2	MP (4 pins)
Total Inst:	6	4	

NOR3

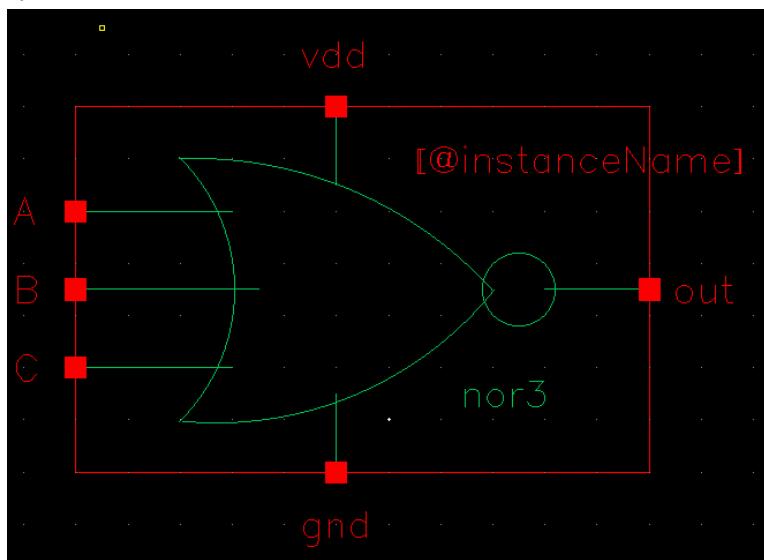
PMOS width = 2.7um

NMOS width = 400nm

Schematic:

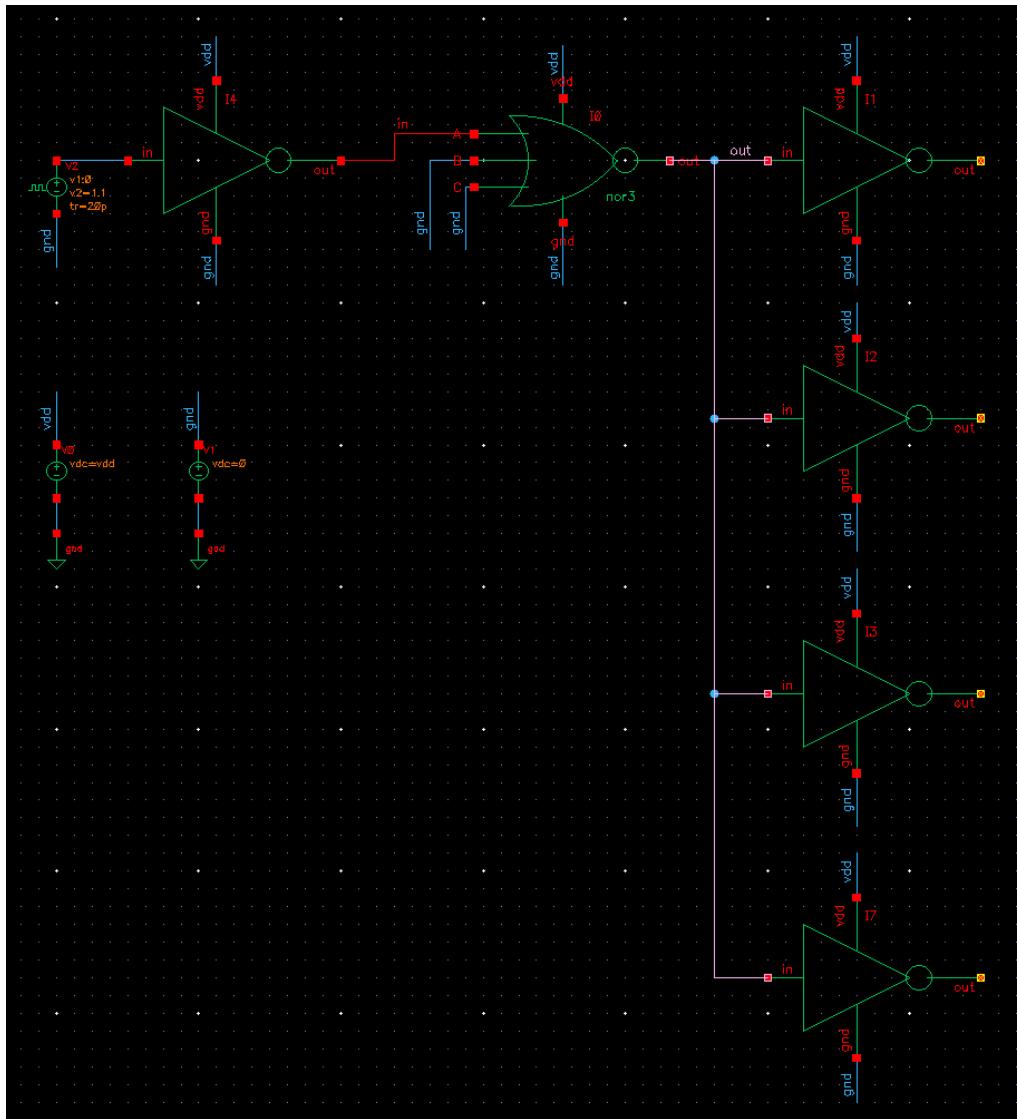


Symbol:



Sim_NOR3 Schematic:

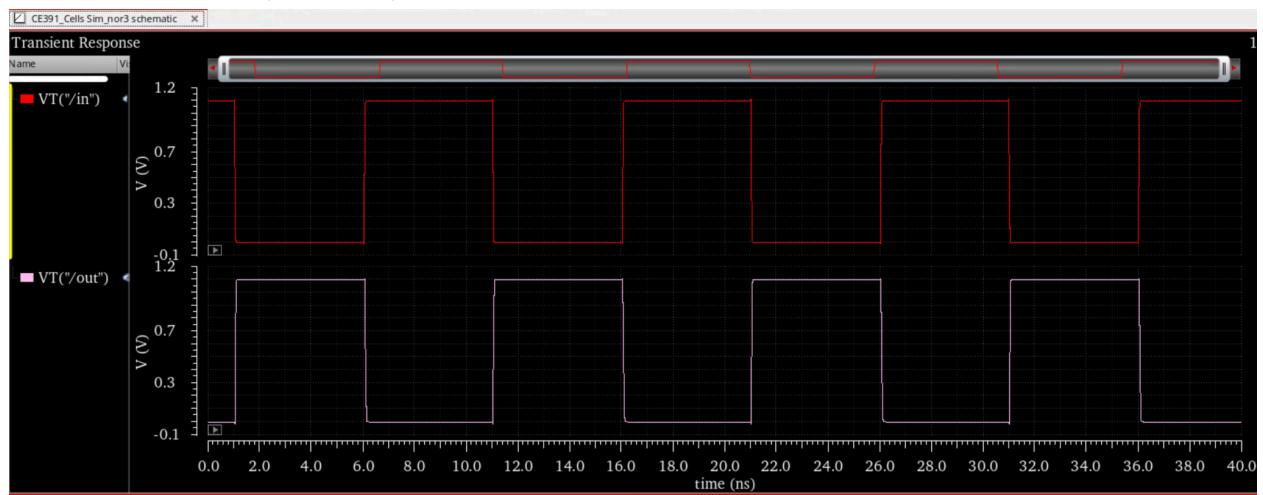
Switching A 0->1 and 1->0 for both worst-case rising and falling delay.



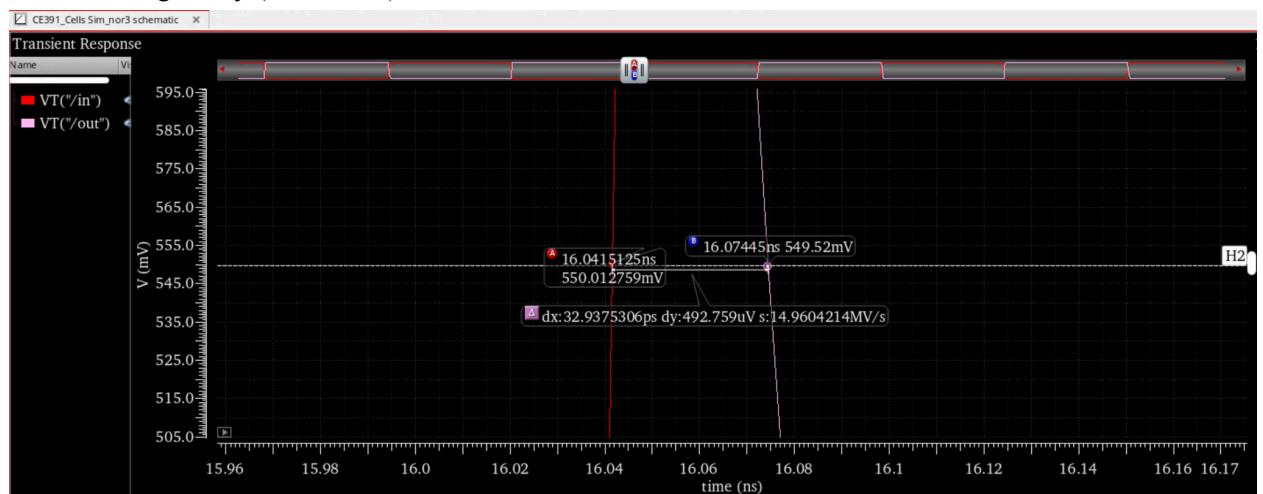
NOR3 Outputs (Schematic):

Outputs		Value	Plot	Save	Save Options
1	in		<input type="checkbox"/>	<input checked="" type="checkbox"/>	allv
2	I0/vdd		<input type="checkbox"/>	<input checked="" type="checkbox"/>	yes
3	delay_rise	15.17p	<input checked="" type="checkbox"/>	<input type="checkbox"/>	
4	delay_fall	32.91p	<input checked="" type="checkbox"/>	<input type="checkbox"/>	
5	energy_rise_fall	25.83f	<input checked="" type="checkbox"/>	<input type="checkbox"/>	

NOR3 Transient Plot (Schematic):



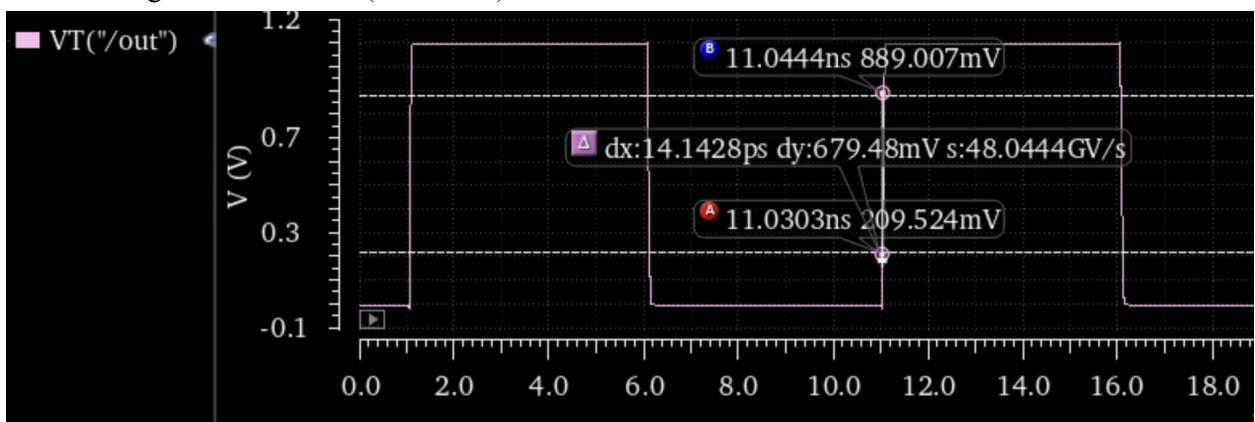
NOR3 Falling Delay (Schematic):



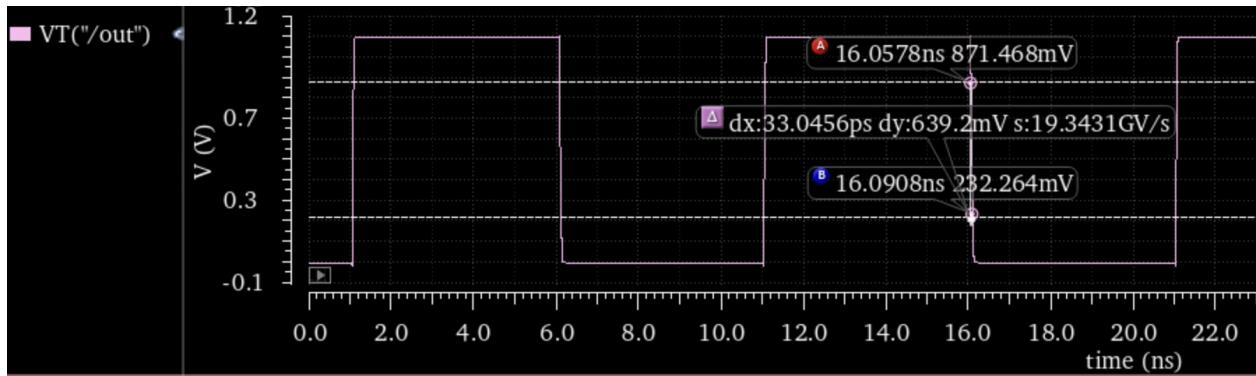
NOR3 Rising Delay (Schematic):



NOR3 Rising Transition Time (Schematic):

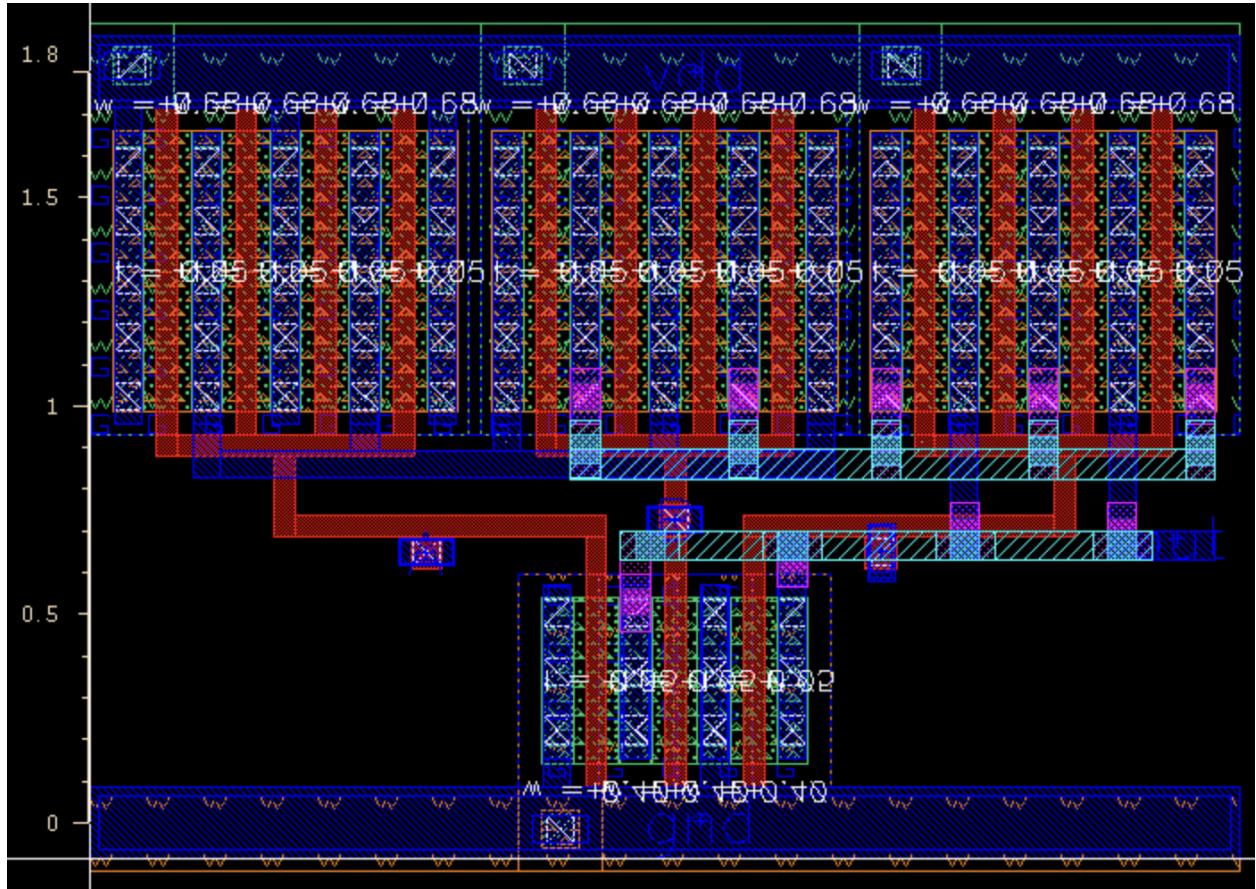


NOR3 Falling Transition Time (Schematic):



Layout:

Used 4-fingered PMOS transistors that were 675nm wide each to create a 2.7um wide PMOS.



DRC:

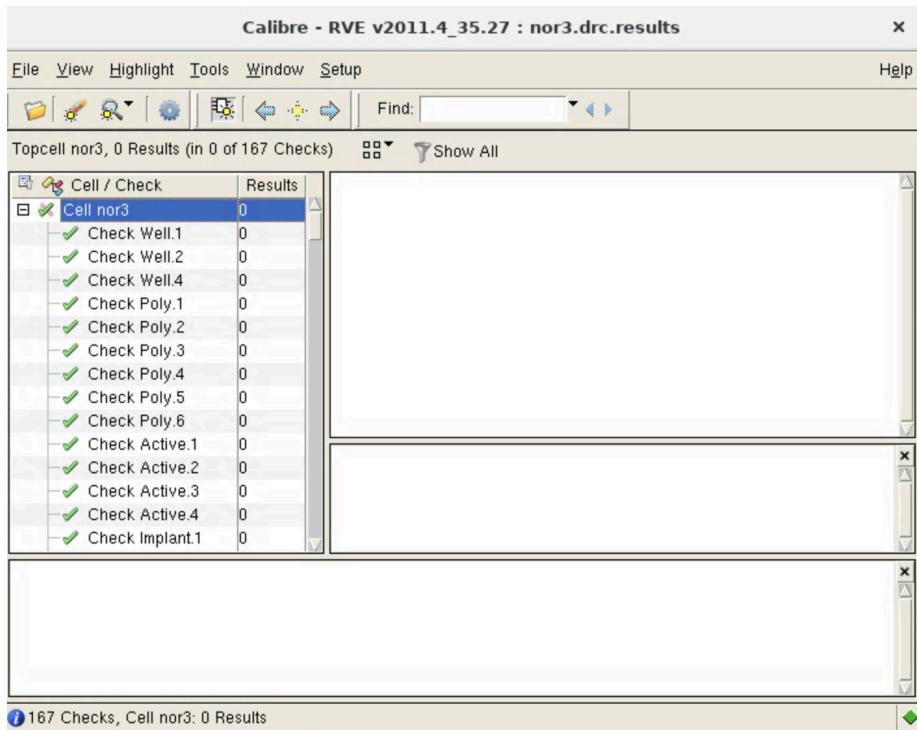
Calibre - RVE v2011.4_35.27 : nor3.drc.results

File View Highlight Tools Window Setup Help

Topcell nor3, 0 Results (in 0 of 167 Checks) Show All

Cell / Check	Results
Cell nor3	0
Check Well.1	0
Check Well.2	0
Check Well.4	0
Check Poly.1	0
Check Poly.2	0
Check Poly.3	0
Check Poly.4	0
Check Poly.5	0
Check Poly.6	0
Check Active.1	0
Check Active.2	0
Check Active.3	0
Check Active.4	0
Check Implant.1	0

167 Checks, Cell nor3: 0 Results



LVS:

Calibre - RVE v2011.4_35.27 : svdb nor3

File View Highlight Tools Window Setup Help

Navigator

Results

- Extraction Results
- Comparison Results

Reports

- Rules File
- Extraction Report
- LVS Report

View

- Info
- Finder
- Schematics

Setup

- Options

Comparison Results

Layout Cell / Type	Source Cell	Nets	Instances	Ports
nor3	nor3	6L, 6S	1L, 1S	6L, 6S

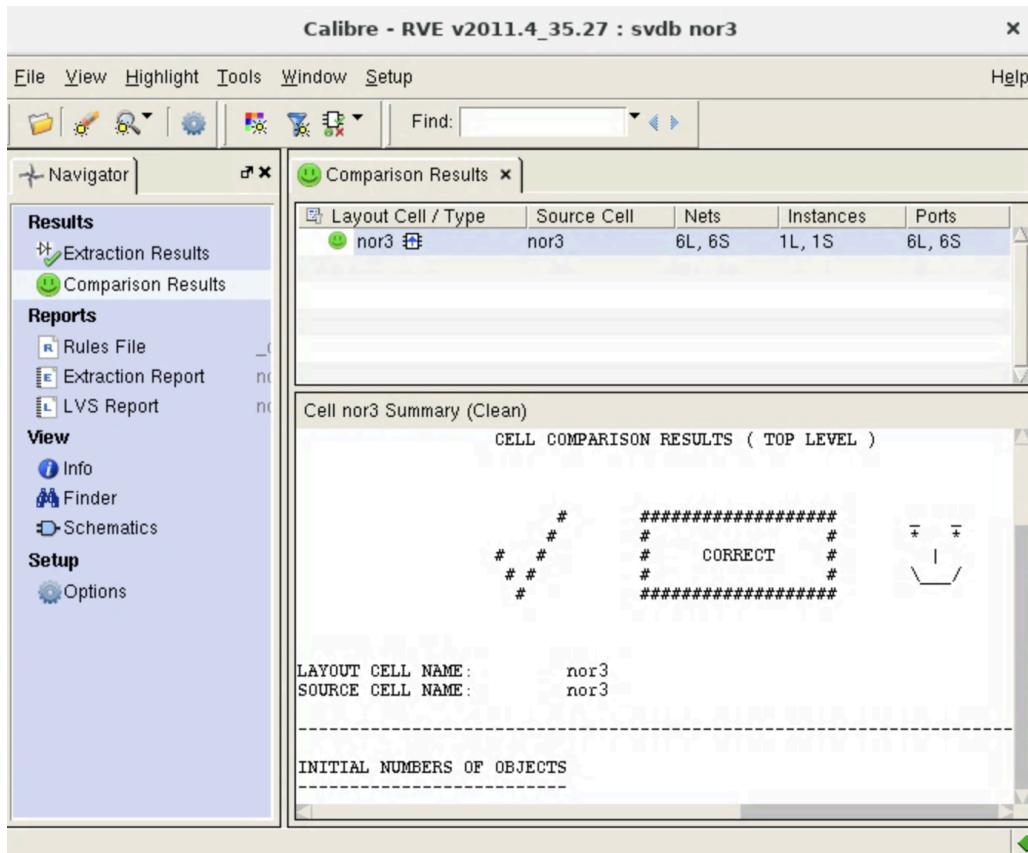
Cell nor3 Summary (Clean)

CELL COMPARISON RESULTS (TOP LEVEL)

CORRECT
#####

LAYOUT CELL NAME: nor3
SOURCE CELL NAME: nor3

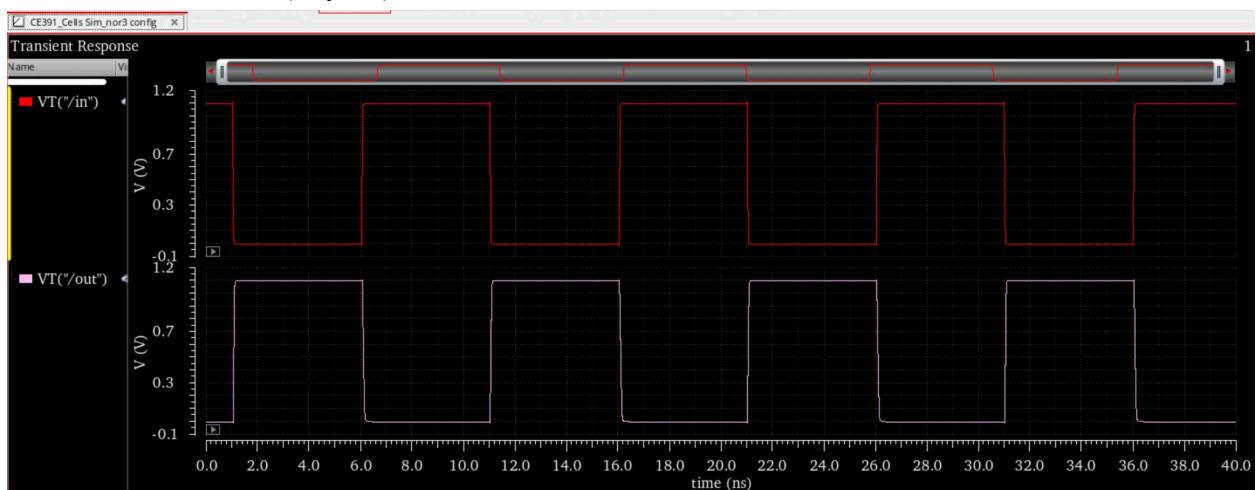
INITIAL NUMBERS OF OBJECTS



NOR3 Outputs (Layout):

Name/Signal/Expr	Value	Plot	Save	Save Options
1 in		<input type="checkbox"/>	<input checked="" type="checkbox"/>	allv
2 10/vdd		<input type="checkbox"/>	<input checked="" type="checkbox"/>	yes
3 delay_rise	24.6p	<input checked="" type="checkbox"/>	<input type="checkbox"/>	
4 delay_fall	46.81p	<input checked="" type="checkbox"/>	<input type="checkbox"/>	
5 energy_rise_fall	35.48f	<input checked="" type="checkbox"/>	<input type="checkbox"/>	

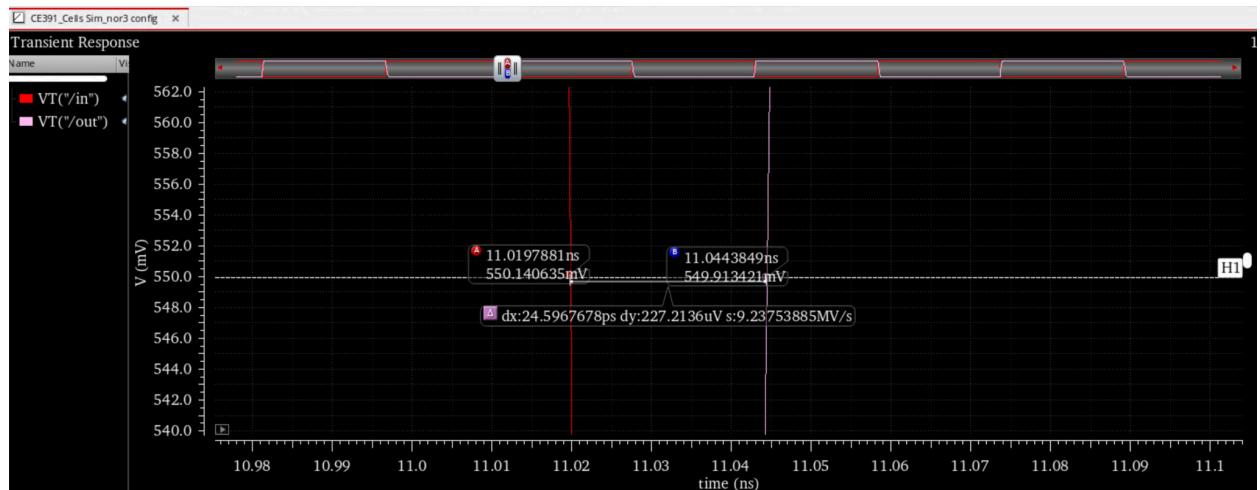
NOR3 Transient Plot (Layout):



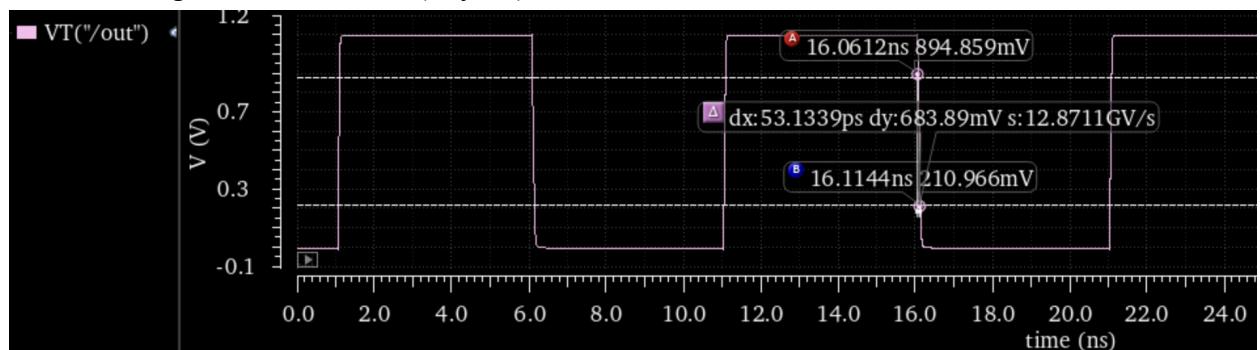
NOR3 Falling Delay (Layout):



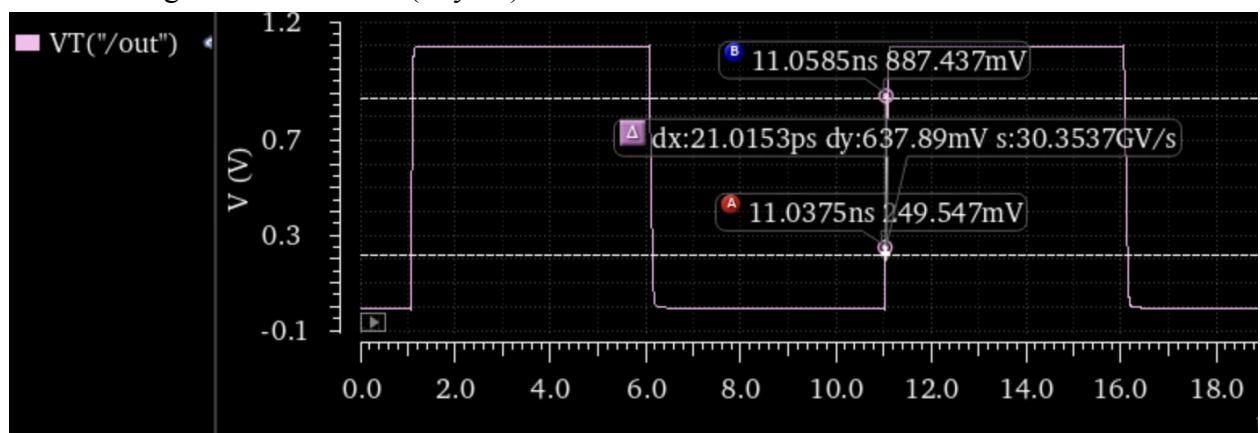
NOR3 Rising Delay (Layout):



NOR3 Falling Transition Time (Layout):



NOR3 Rising Transition Time (Layout):

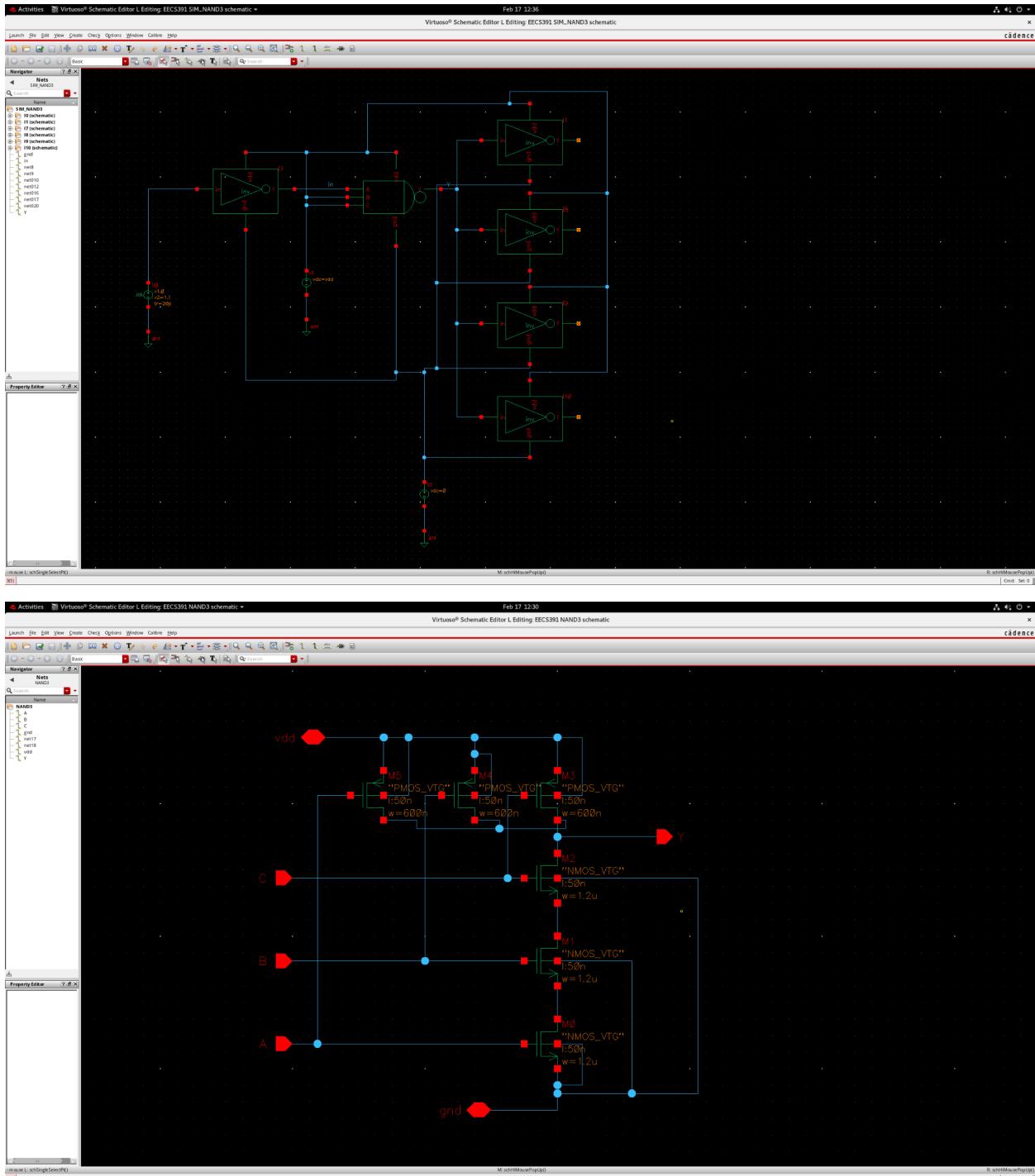


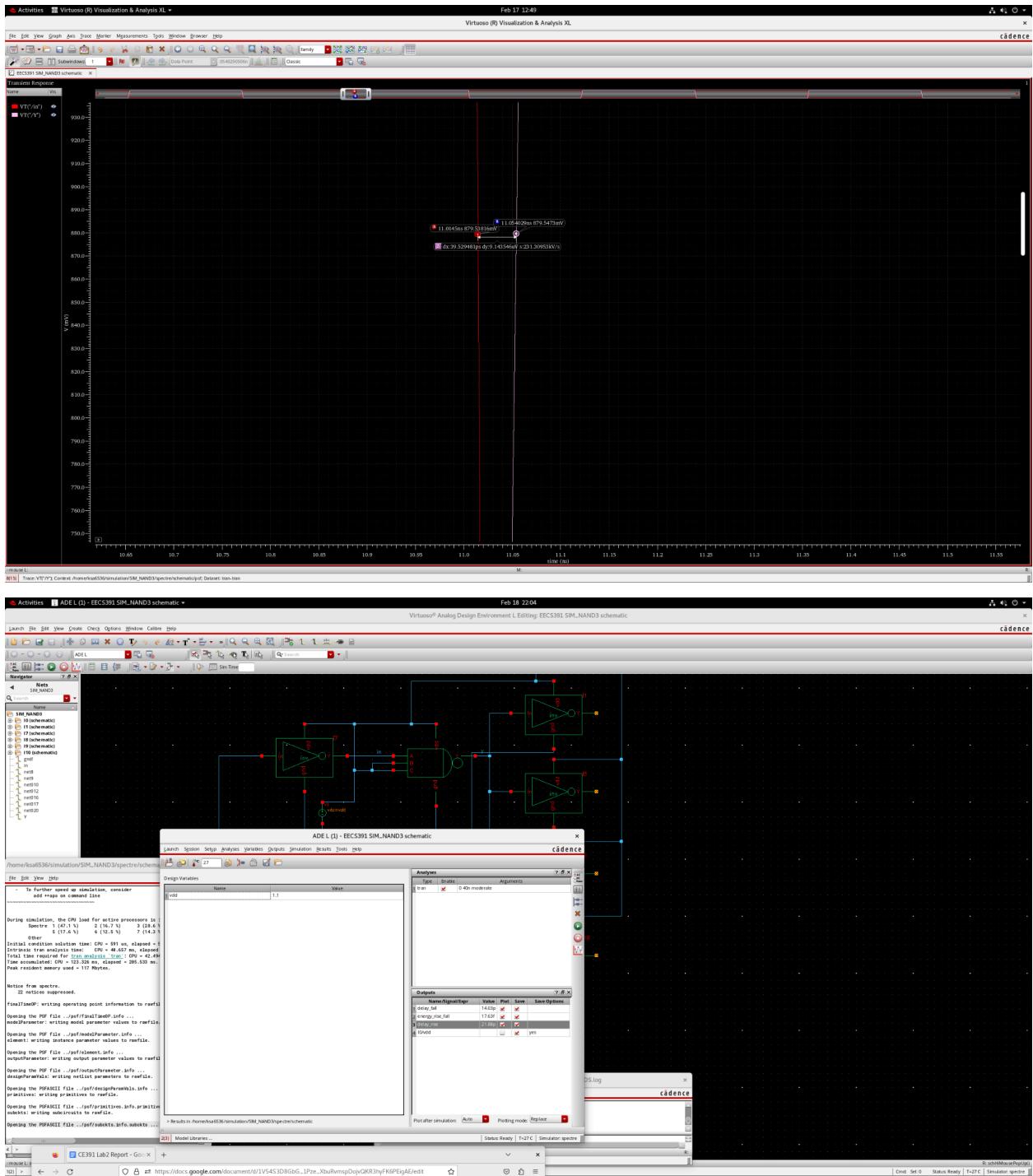
NOR3 Schematic vs. Layout Comparison Table:

	Schematic	Layout
Rising Delay (ps)	15.17	24.60
Falling Delay (ps)	32.91	46.81
Rising Transition Time (ps)	14.14	21.01
Falling Transition Time (ps)	33.05	53.13
Energy Rise Fall (fJ)	25.83	35.48

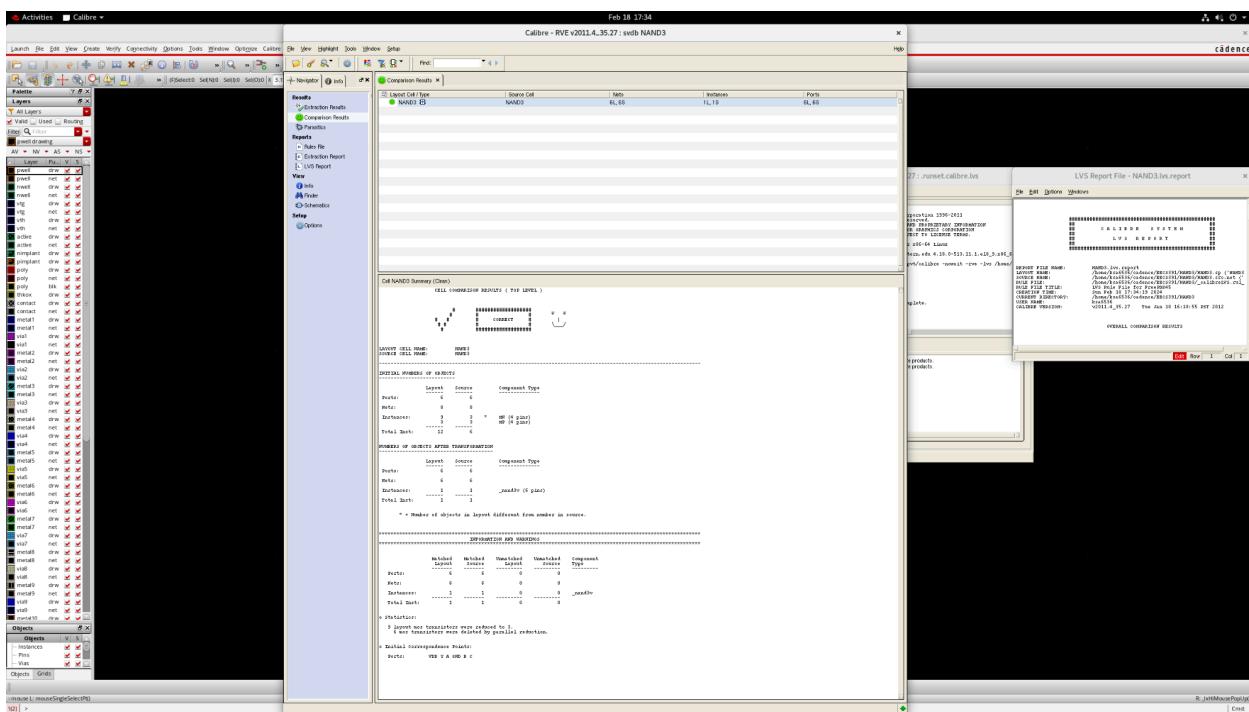
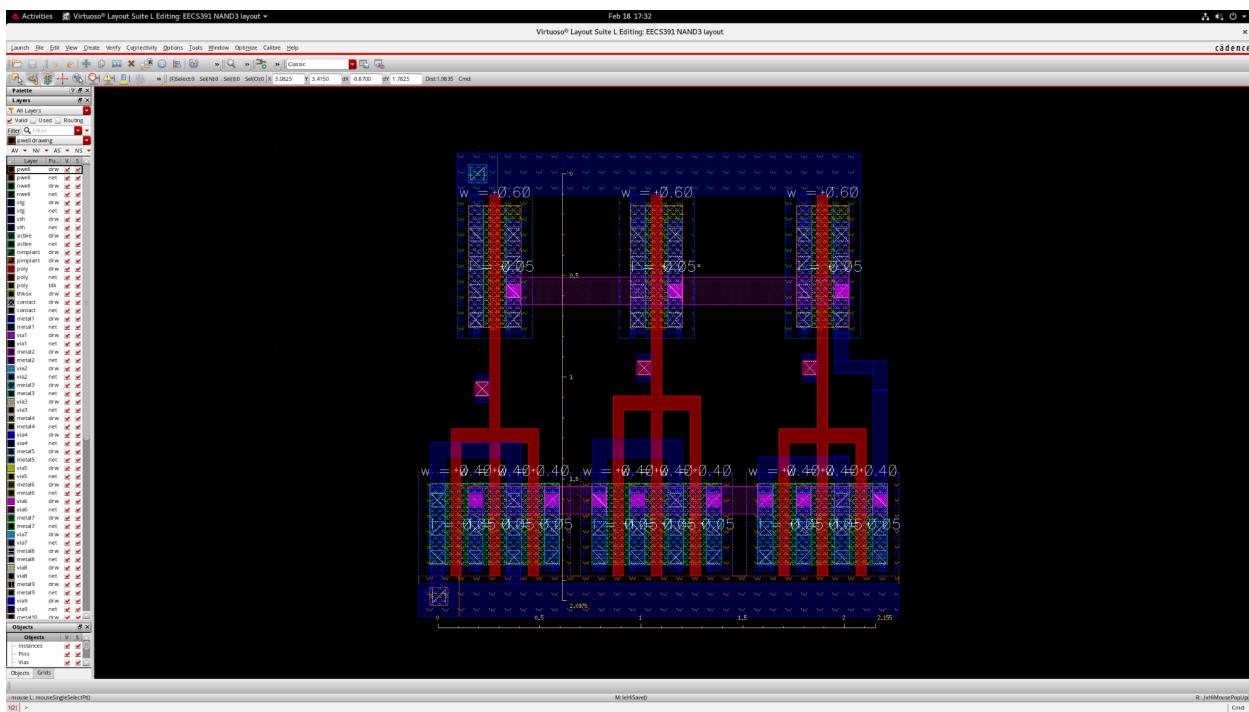
Above calculations for the worst-case delay which is when B and C are grounded and A is the input switching; A going from 0 to 1 causes the falling delay, and A going from 1 to 0 causes the rising delay.

NAND3 Schematic & Testbench





LVS Results and Layout:



DRC Results:

Calibre - RVE v2011.4_35.27 : NAND3.drc.results

DRC Summary Report - NAND3.drc.summary

Topcell NAND3, 0 Results (in 0 of 167 Checks) Show All

Check / Cell	Results
✓ Check Well.1	0
✓ Check Well.2	0
✓ Check Well.4	0
✓ Check Poly.1	0
✓ Check Poly.2	0
✓ Check Poly.3	0
✓ Check Poly.4	0
✓ Check Poly.5	0
✓ Check Poly.6	0
✓ Check Active.1	0
✓ Check Active.2	0
✓ Check Active.3	0
✓ Check Active.4	0
✓ Check Implant.1	0
✓ Check Implant.2	0
✓ Check Implant.3	0
✓ Check Implant.4	0
✓ Check Implant.5	0
✓ Check Contact.1	0
✓ Check Contact.2	0
✓ Check Contact.3	0
✓ Check Contact.4	0
✓ Check Contact.5	0
✓ Check Contact.6	0
✓ Check Metal1.1	0
✓ Check Metal1.2	0
✓ Check Metal1.3	0
✓ Check Metal1.4	0
✓ Check Val1.1	0
✓ Check Val1.2	0
✓ Check Val1.3	0
✓ Check Val1.4	0
✓ Check Metal2.1	0
✓ Check Metal2.2	0
✓ Check Metal2.3	0
✓ Check Metal2.4	0
✓ Check Via2.1	0
✓ Check Via2.2	0
✓ Check Via2.3	0
✓ Check Via2.4	0
✓ Check Metal3.1	0
✓ Check Metal3.2	0
✓ Check Metal3.3	0

```
Rule File In Use: /home/joc1147/cadence/lab_2/NAND3/calibre08c.vcl
Well1 and Well2 must not overlap

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-- NVLZCHECK RESULTS STATISTICS (BY CELL)  

---  

--- SUMMARY  

TOTAL CPU TIME: 0  

TOTAL REAL TIME: 0  

TOTAL LAYER Semantics: 0 (0)  

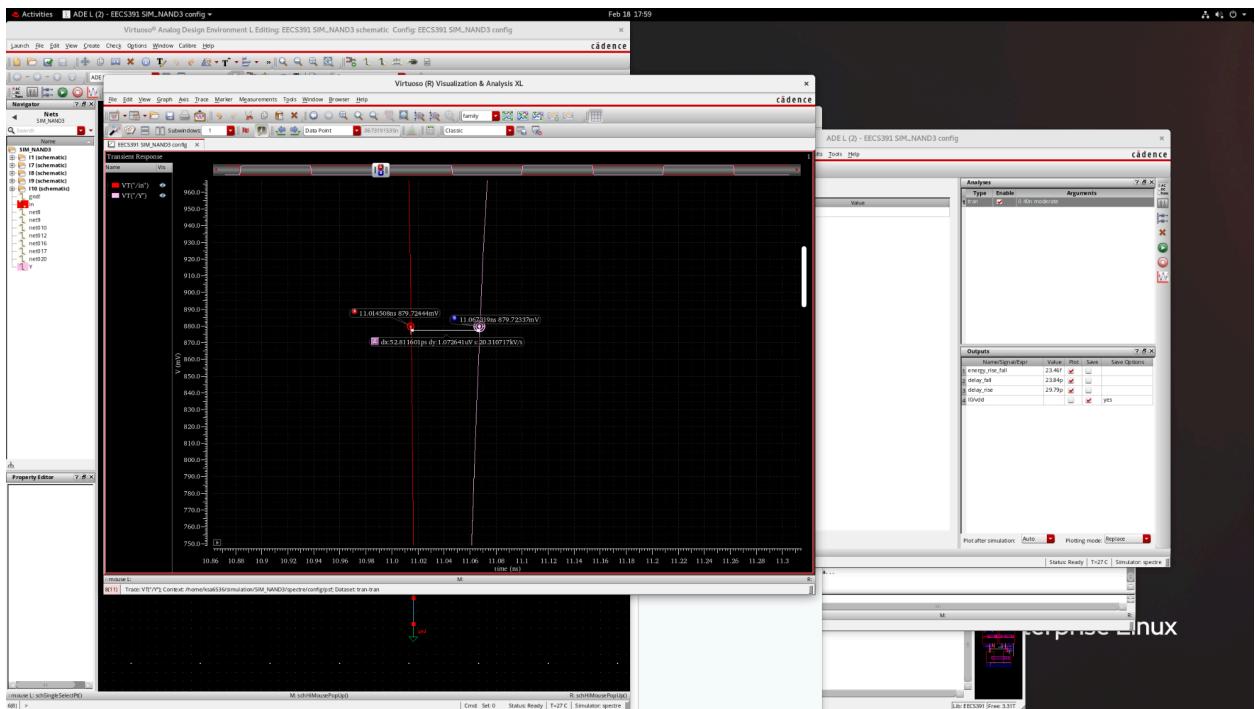
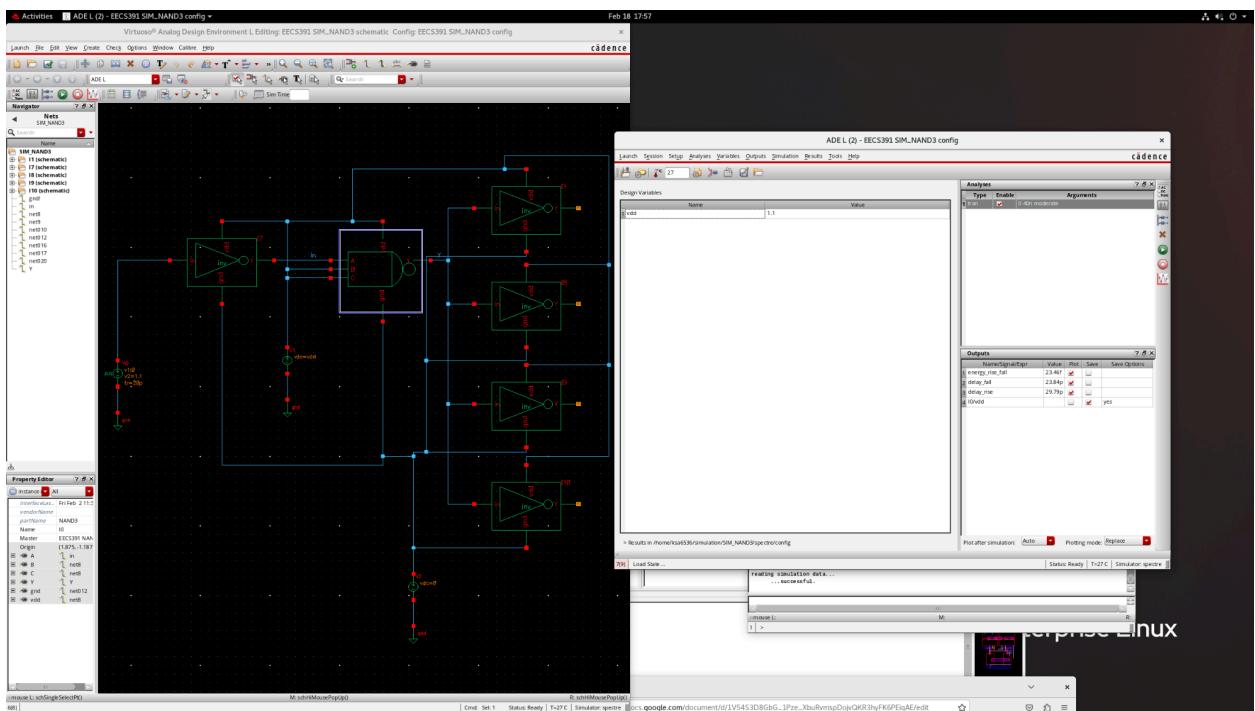
TOTAL DRC Rulechecks Executed: 167  

TOTAL DRC Results Generated: 0 (0)  

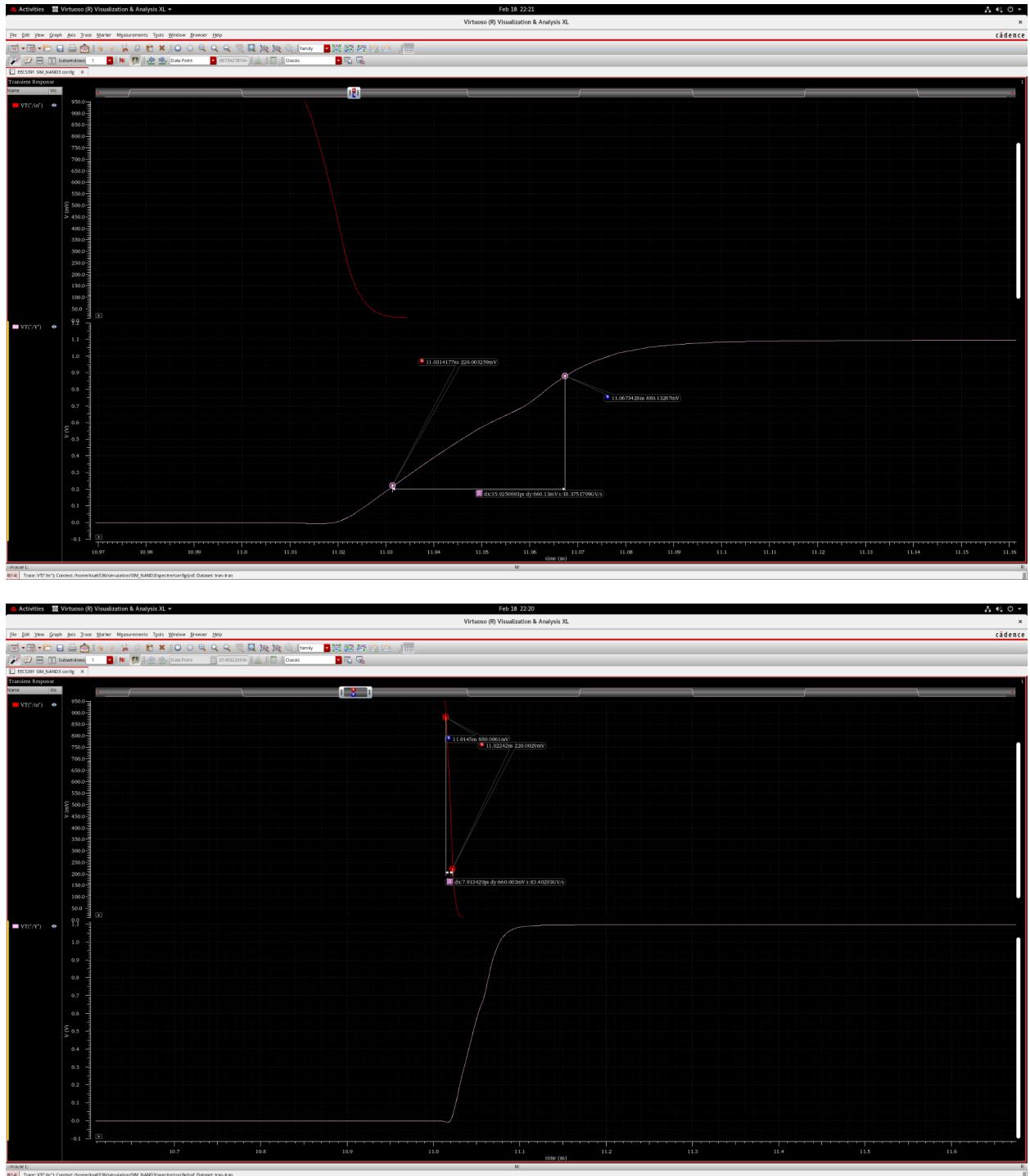
-----
```

Check Well.1, 0 Cells, 0 Results

Extracted Simulation Results:



Extracted Layout Transition Times:



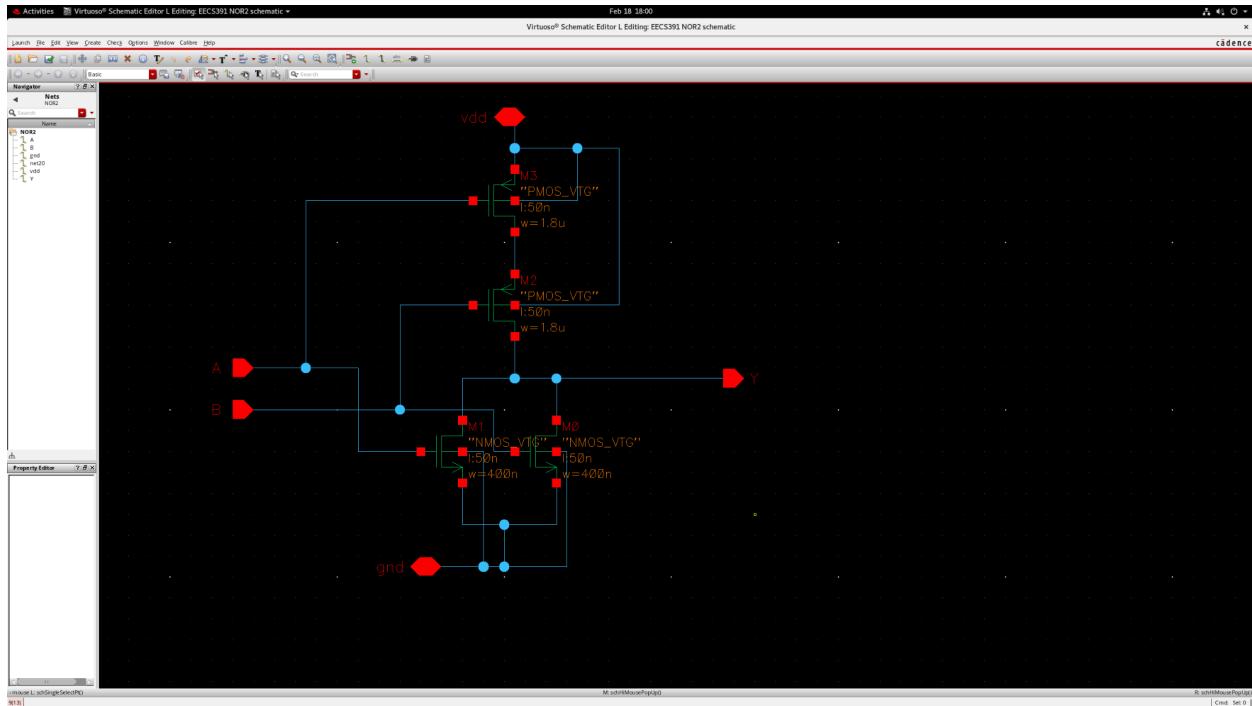
NAND3 Schematic vs. Layout Comparison Table:

	Schematic	Layout
Rising Delay (ps)	21.88p	29.79p
Falling Delay (ps)	14.03p	23.84
Rising Transition Time (ps)	25.35ps	35.91ps
Falling Transition Time (ps)	7.39ps	7.913
Energy Rise Fall (fJ)	17.65f	23.46f

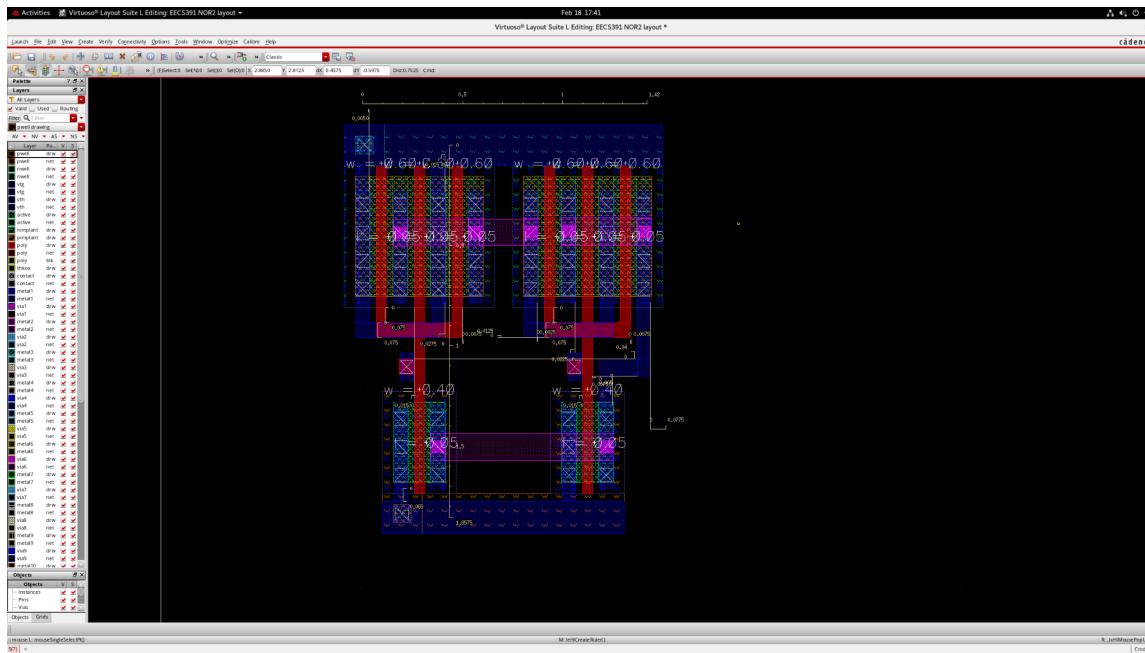
Above calculations for the worst-case delay which is when B and C are connected to VDD and A is the input switching; A going from 0 to 1 causes the falling delay, and A going from 1 to 0 causes the rising delay.

NOR2

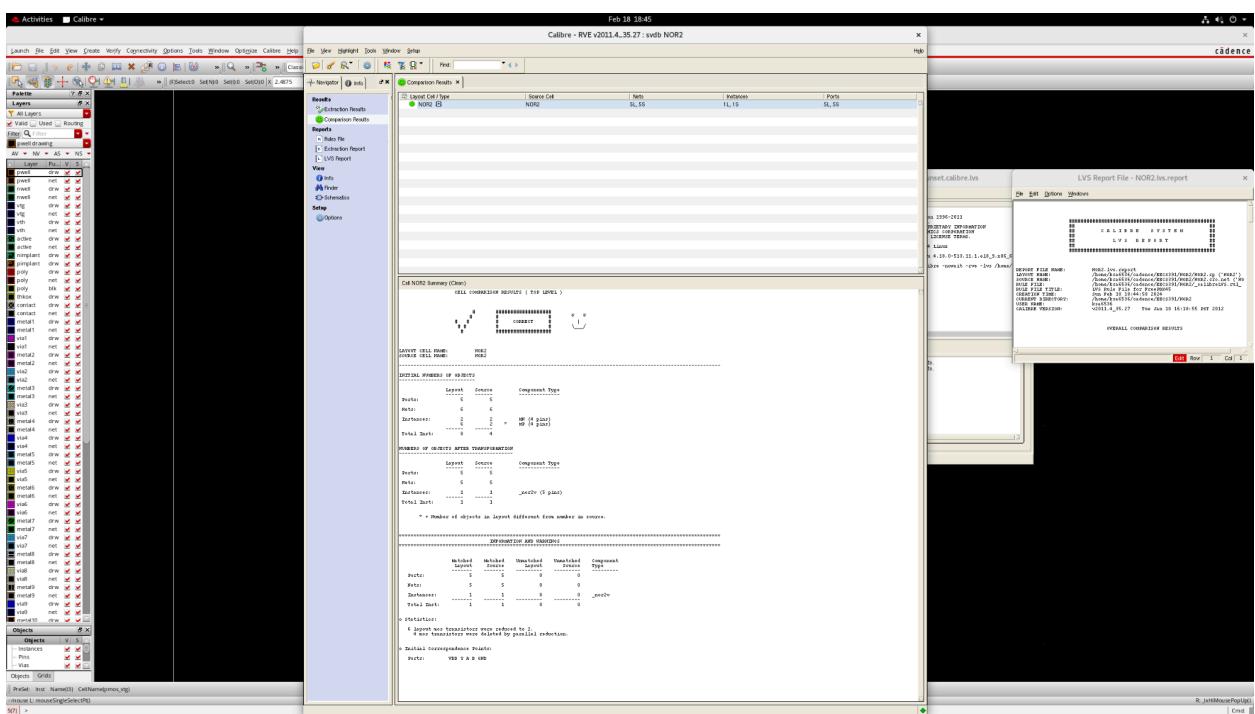
Schematic:



Layout:



LVS Simulation Results:



DRC Results:

Calibre - RVE v2011.4_35.27 : NAND3.drc.results

DRC Summary Report - NAND3.drc.summary

File Edit Options Windows

Topcell NAND3, 0 Results (in 0 of 167 Checks)

Check / Cell Results

- Check Well.1 0
- Check Well.2 0
- Check Well.4 0
- Check Poly.1 0
- Check Poly.2 0
- Check Poly.3 0
- Check Poly.4 0
- Check Poly.5 0
- Check Poly.6 0
- Check Active.1 0
- Check Active.2 0
- Check Active.3 0
- Check Active.4 0
- Check Implant.1 0
- Check Implant.2 0
- Check Implant.3 0
- Check Implant.4 0
- Check Implant.5 0
- Check Contact.1 0
- Check Contact.2 0
- Check Contact.3 0
- Check Contact.4 0
- Check Contact.5 0
- Check Contact.6 0
- Check Metal1.1 0
- Check Metal1.2 0
- Check Metal1.3 0
- Check Metal1.4 0
- Check Val1.1 0
- Check Val1.2 0
- Check Val1.3 0
- Check Val1.4 0
- Check Metal2.1 0
- Check Metal2.2 0
- Check Metal2.3 0
- Check Metal2.4 0
- Check Val2.1 0
- Check Val2.2 0
- Check Val2.3 0
- Check Val2.4 0
- Check Metal3.1 0
- Check Metal3.2 0
- Check Metal3.3 0

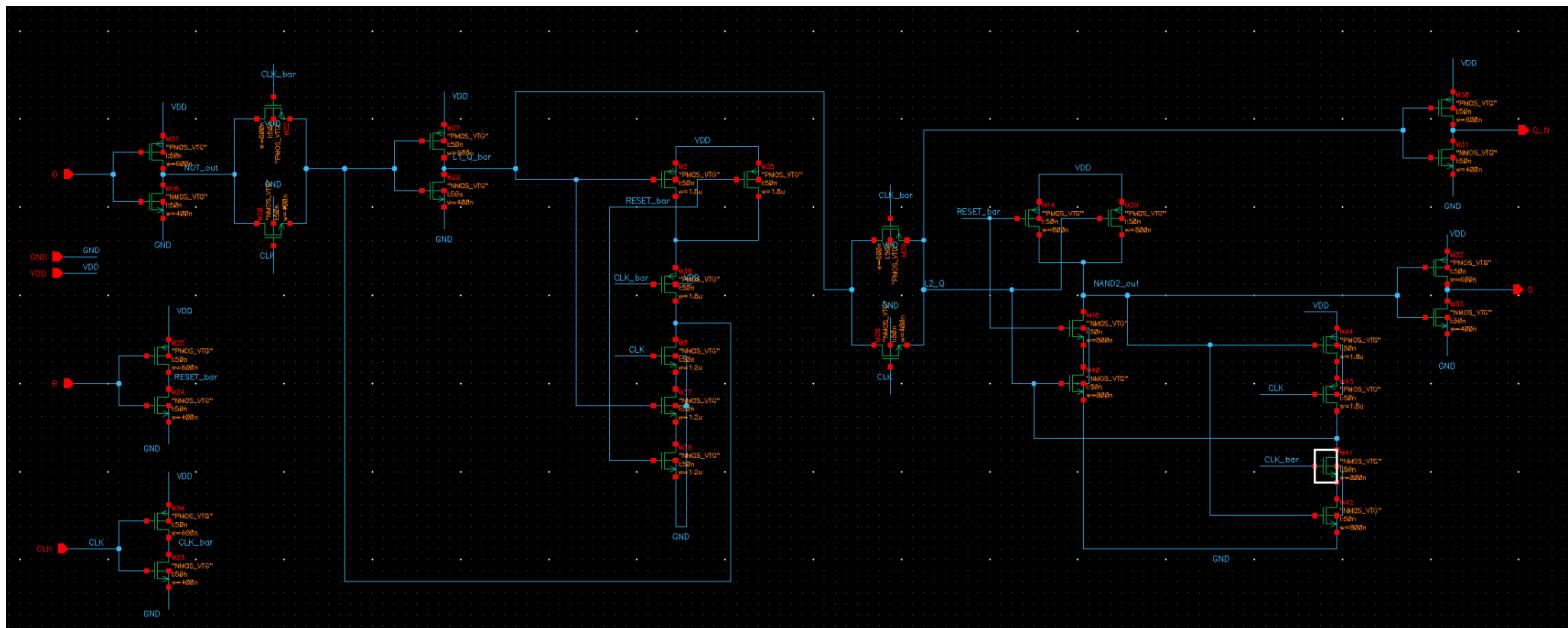
Rule File Pathname: /home/jcc1147/evidence/lab_2/90053/_calibre08c.rvl
Rvll and Prell must not overlap

```

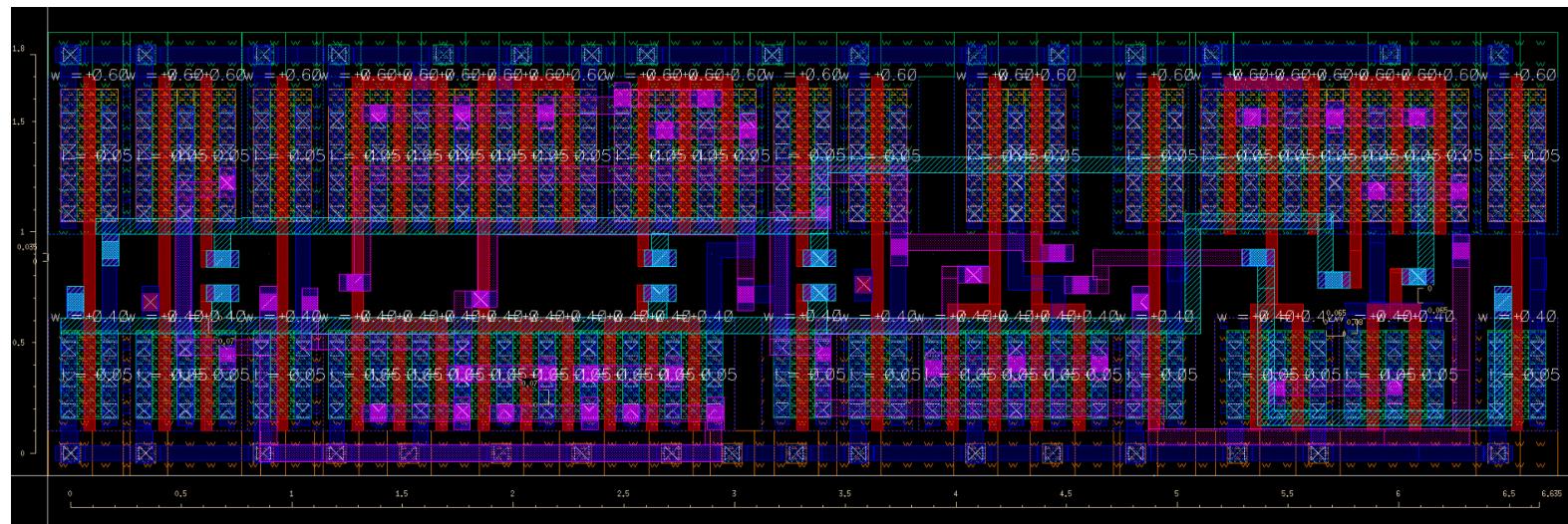
Rule DRC Statistics (BY CELL)
=====
--- RULECHECK RESULTS STATISTICS (BY CELL)
=====
===== SUMMARY =====
=====
TOTAL CPU TIME: 0
TOTAL EXEC TIME: 0
TOTAL Layer geometries: 132 (262)
TOTAL DRC Rulechecks Executed: 167
TOTAL DRC Results Generated: 0 (0)

--- RULECHECK RESULTS STATISTICS (BY CELL)
=====
```

D-Flip Flop schematic



Layout Dimensions: 1.8um x 6.85um



Calibre - RVE v2011.4_35.27 : DFF.drc.results

File View Highlight Tools Window Setup Help

Topcell DFF, 0 Results (in 0 of 167 Checks) Show All

Check / Cell

- ✓ Check Well.1
- ✓ Check Well.2
- ✓ Check Well.4
- ✓ Check Poly.1
- ✓ Check Poly.2
- ✓ Check Poly.3
- ✓ Check Poly.4
- ✓ Check Poly.5
- ✓ Check Poly.6
- ✓ Check Active.1
- ✓ Check Active.2
- ✓ Check Active.3
- ✓ Check Active.4
- ✓ Check Implant.1
- ✓ Check Implant.2
- ✓ Check Implant.3
- ✓ Check Implant.4

Rule File Pathname: /home/krr2464/cadence/EEC5493/inverter/_calibreDRC.rul_

Mwell and Pwell must not overlap

Check Well.1, 0 Cells: 0 Results

Calibre - RVE v2011.4_35.27 : svdb DFF

File View Highlight Tools Window Setup Help

Navigator Comparison Results Extraction Results

Results Extraction Results Comparison Results

Reports Rules File Extraction Report LVS Report

View Info Finder Schematics

Setup Options

Layout Cell / Type Source Cell Nets Instances Ports

DFF	DFF	14L, 14S	15L, 15S	7L, 7S
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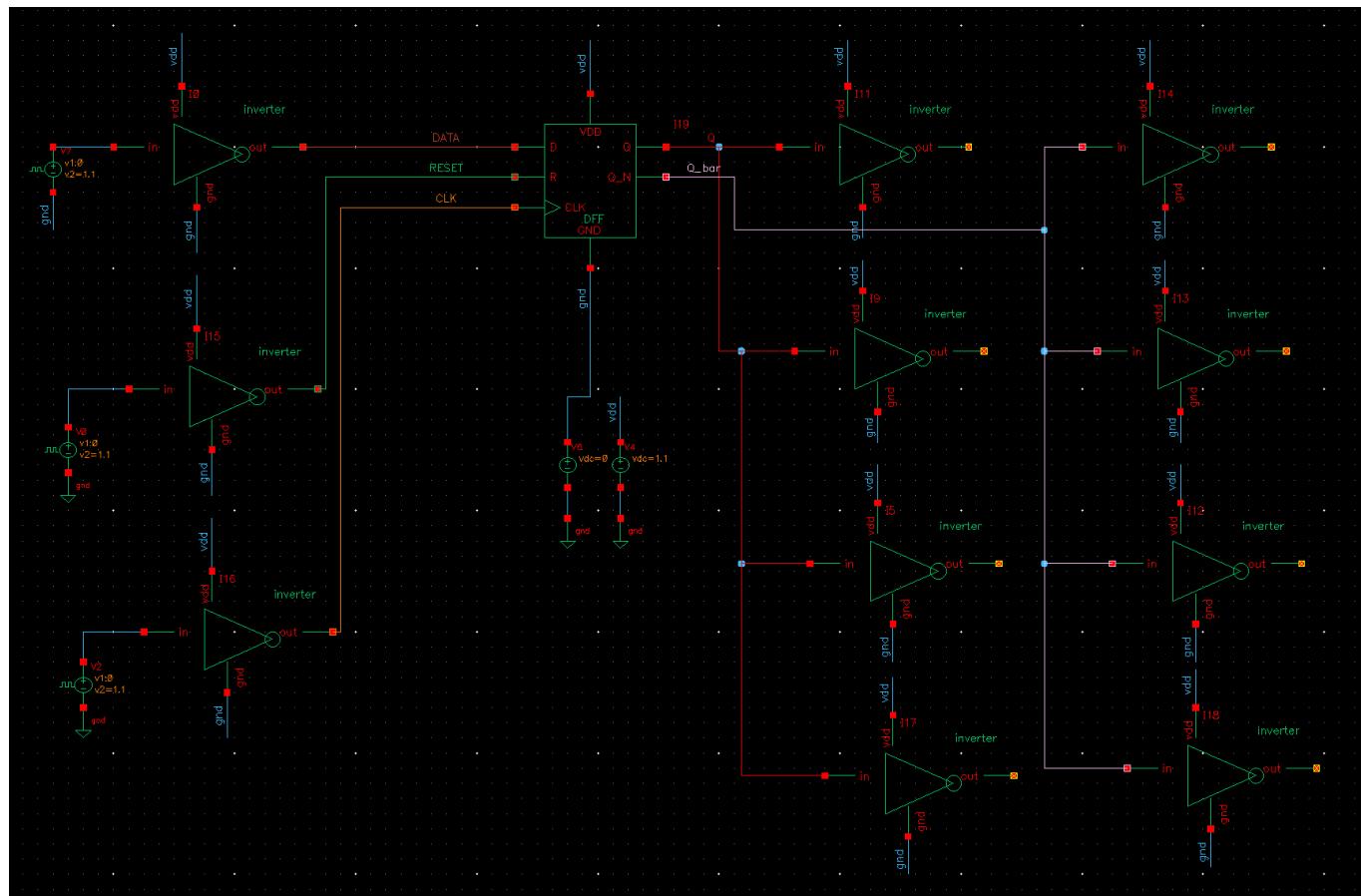
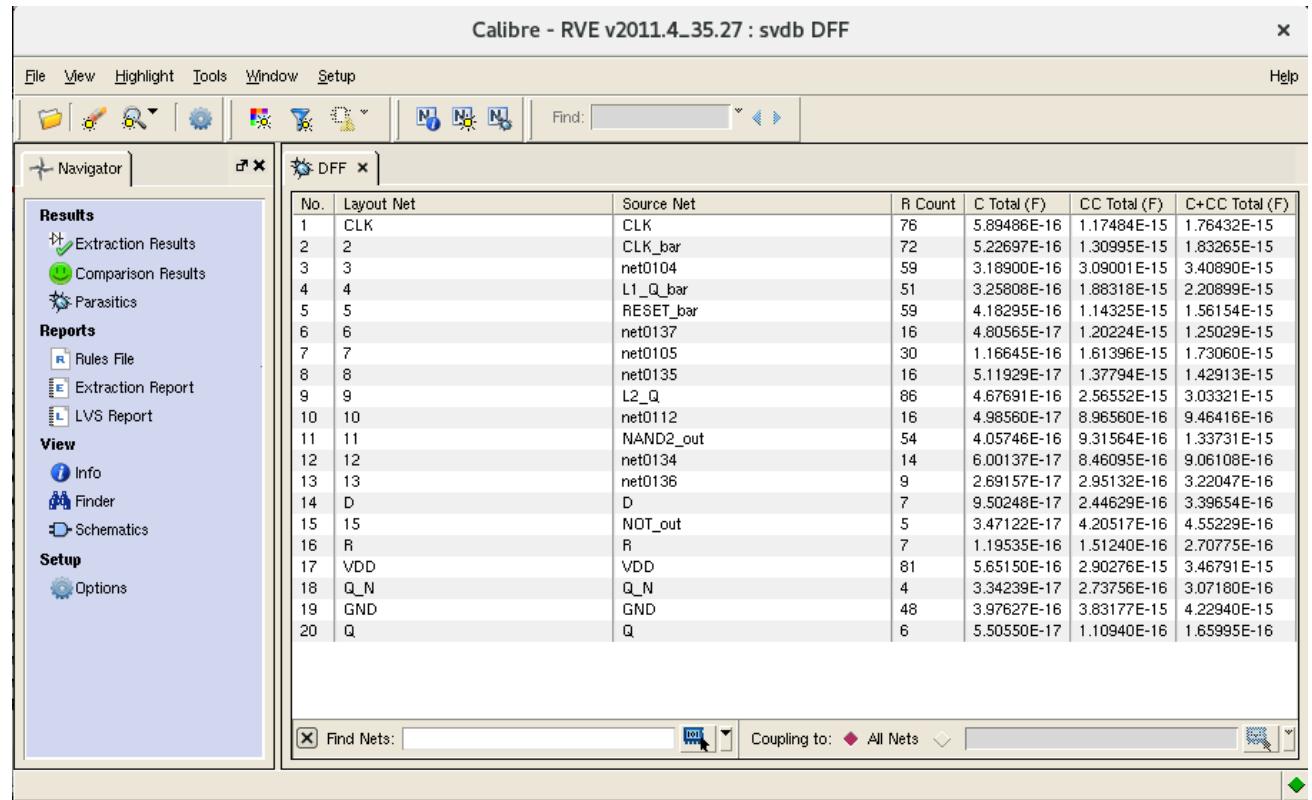
Cell DFF Summary (Clean)

CELL COMPARISON RESULTS (TOP LEVEL)

LAYOUT CELL NAME: DFF
SOURCE CELL NAME: DFF

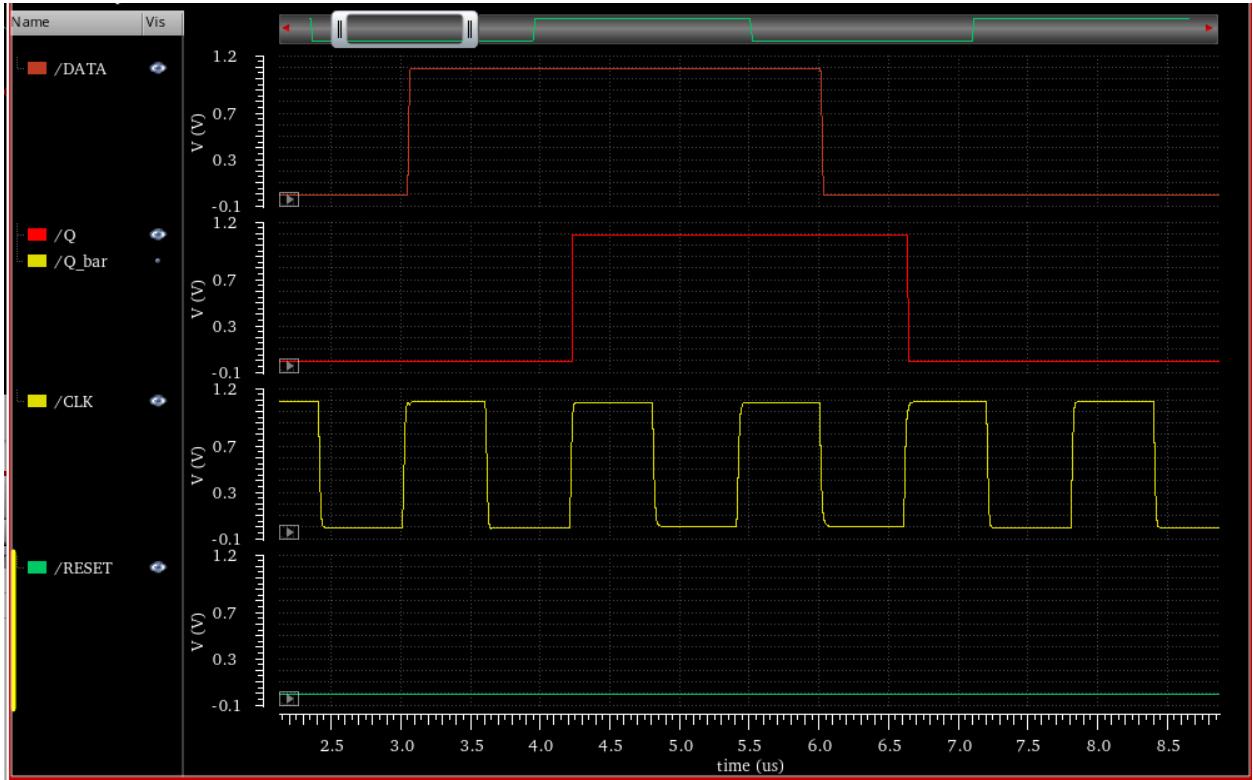
INITIAL NUMBERS OF OBJECTS

	Layout	Source	Component Type
Ports:	7	7	
Nets:	20	20	

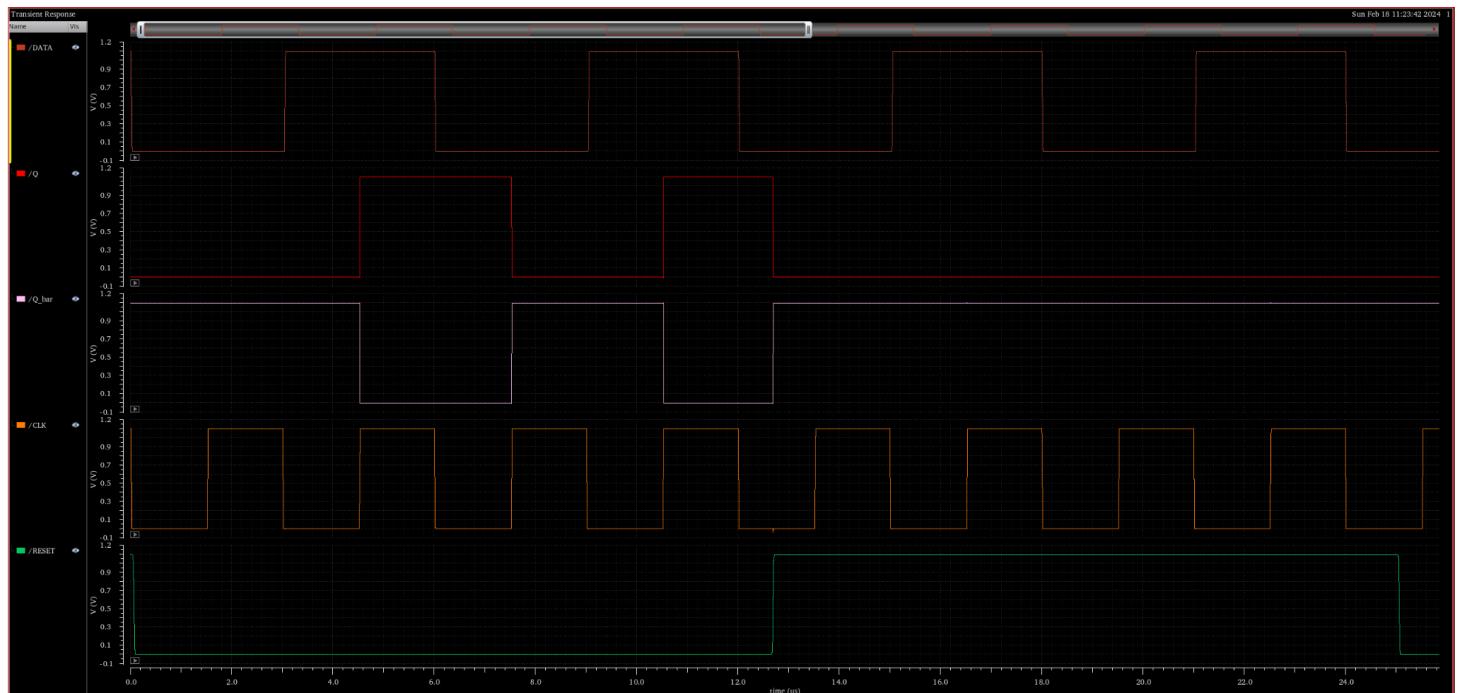


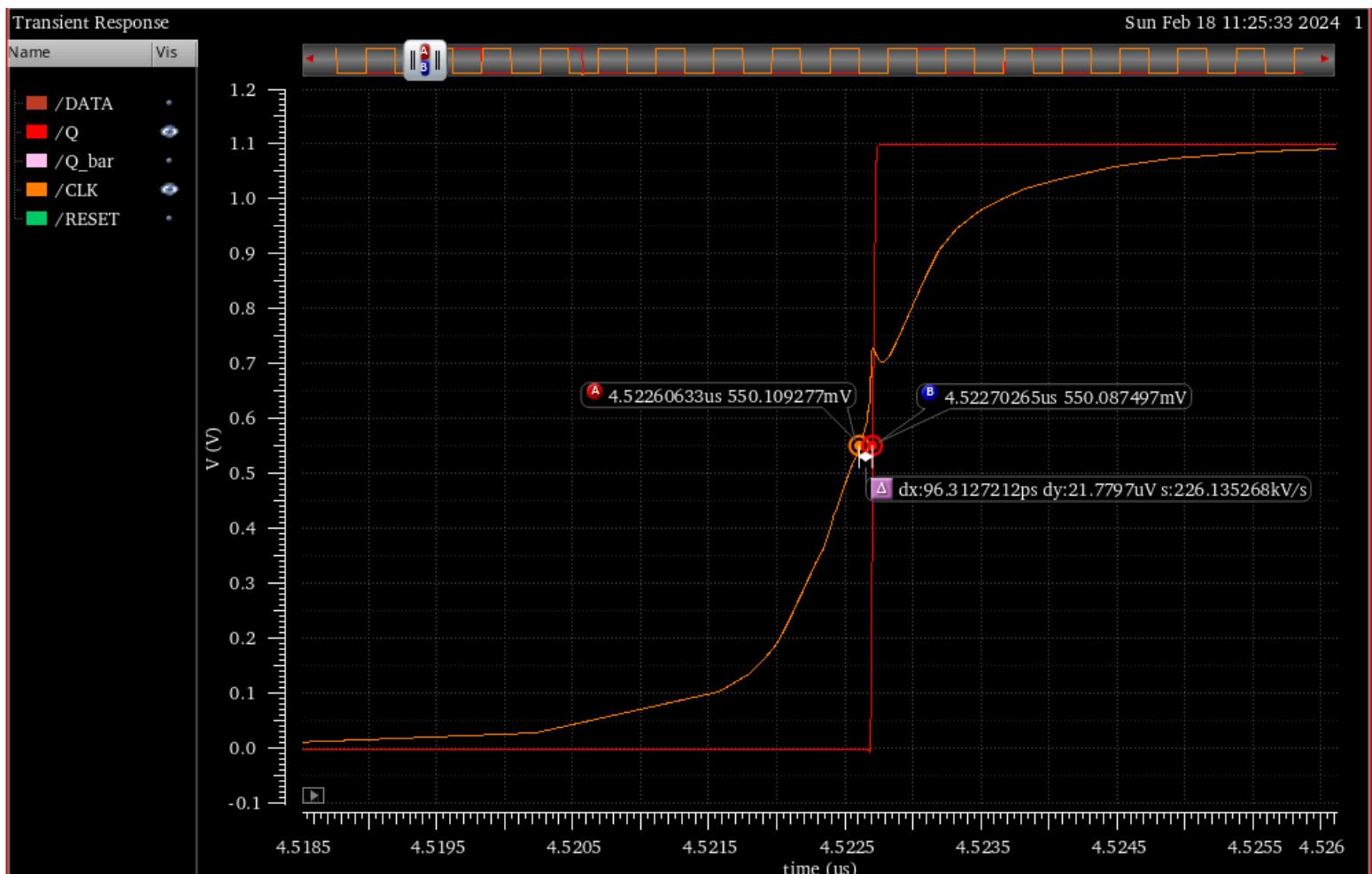
Schematic Simulations

Q Changing triggered by CLK to reflect D

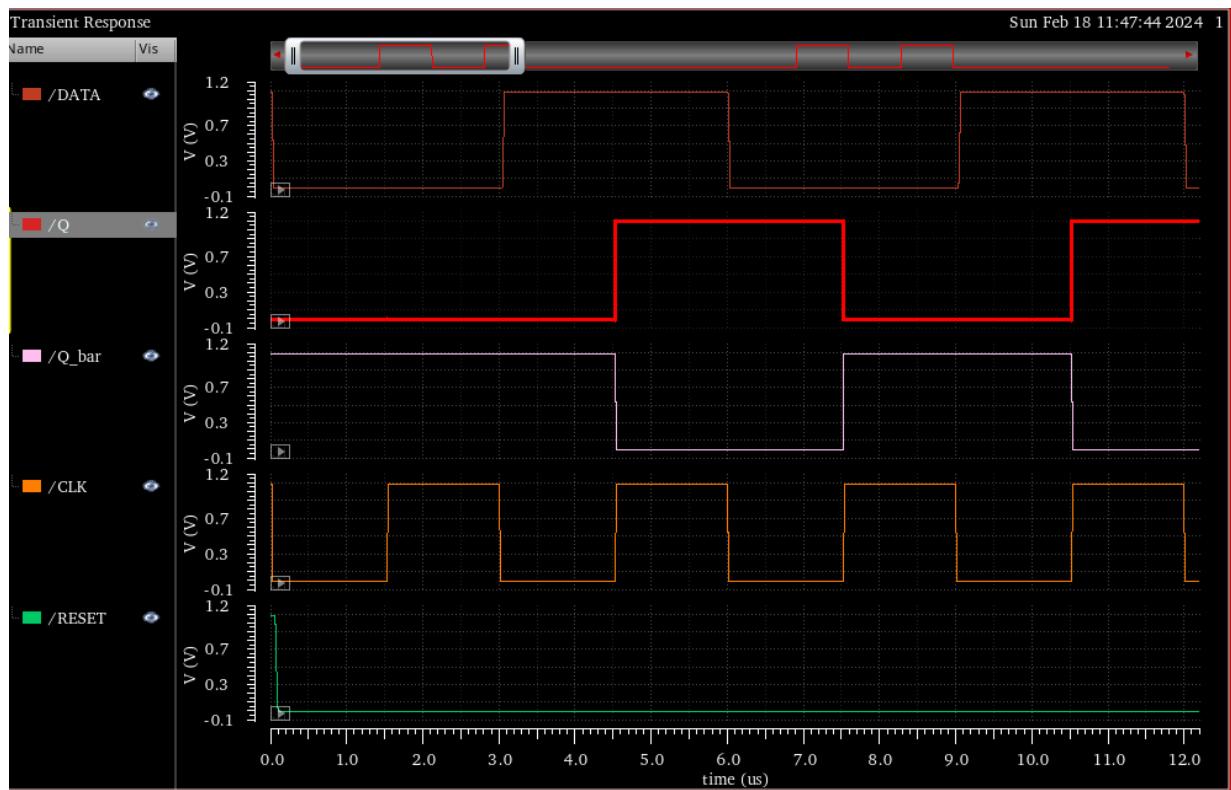
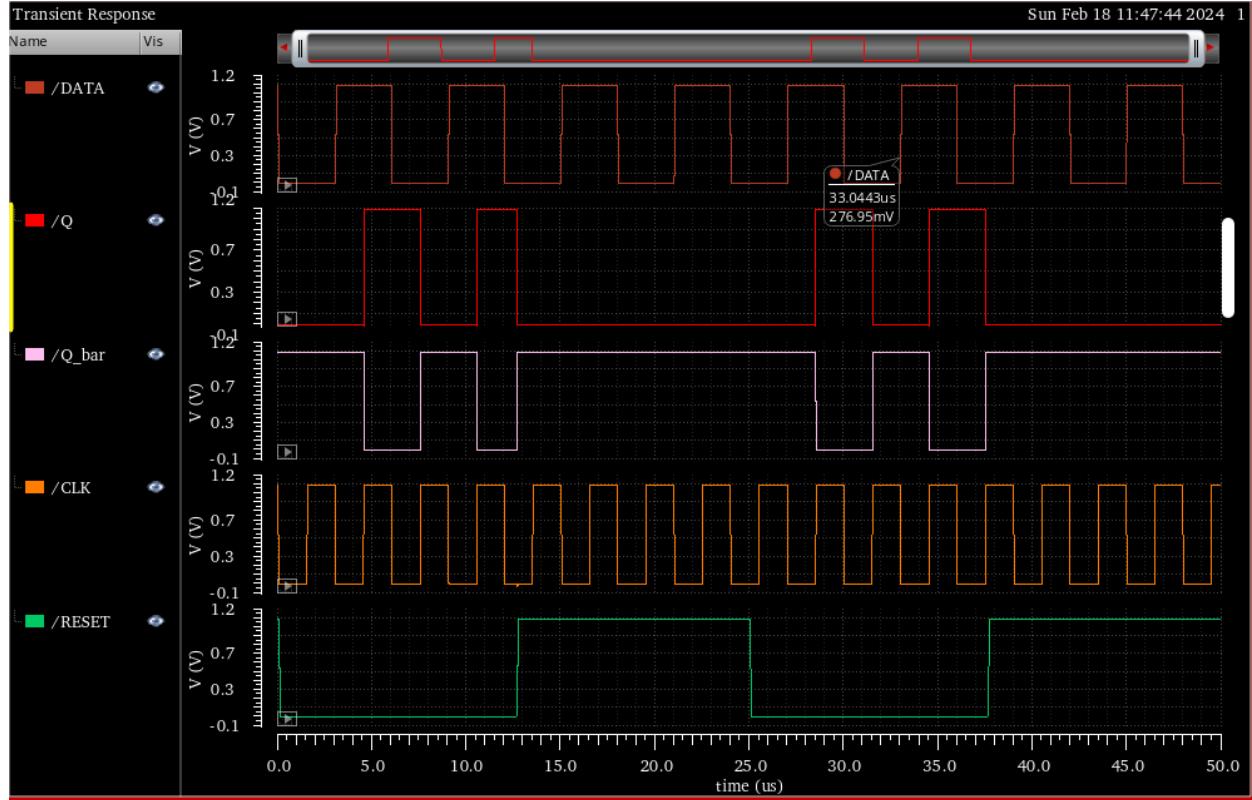


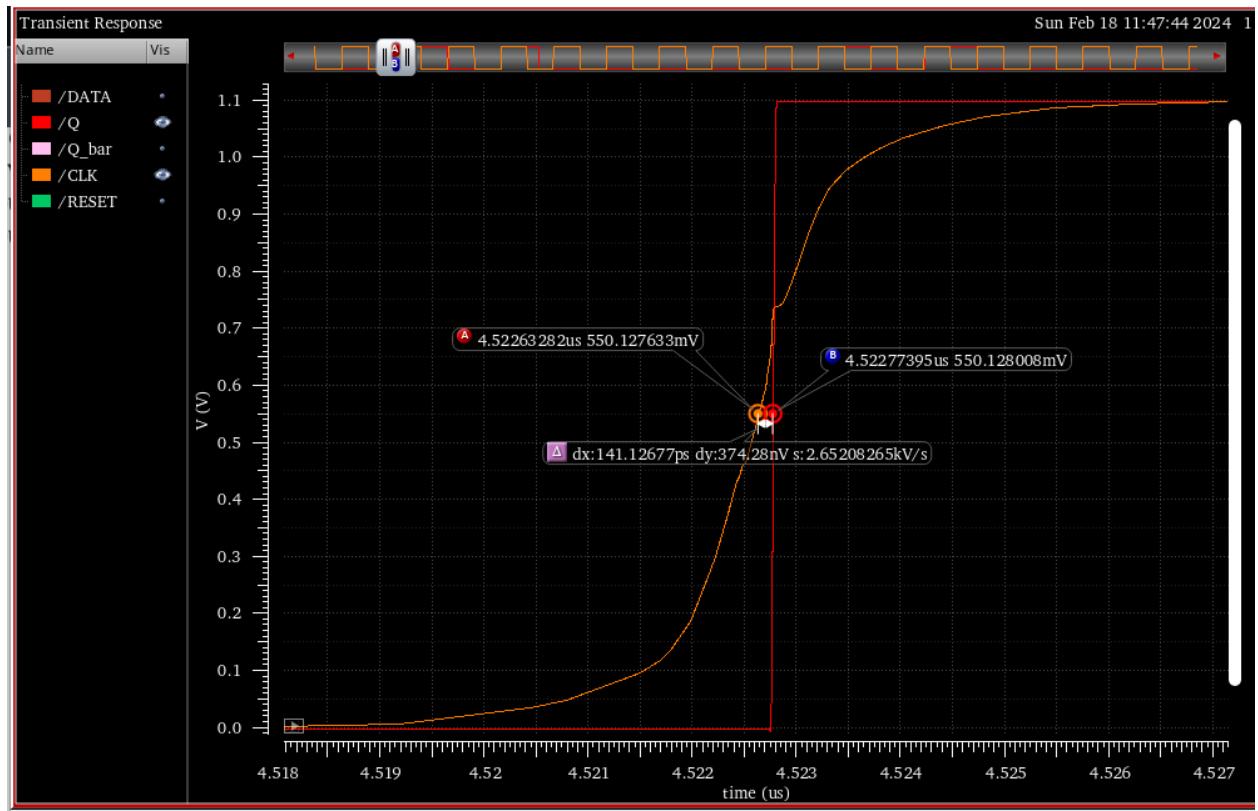
Full waveform showing Reset functionality





Extraction Simulation





CLK-to-Q Delay

Schematic	Extracted Layout
96.31ps	141.126ps