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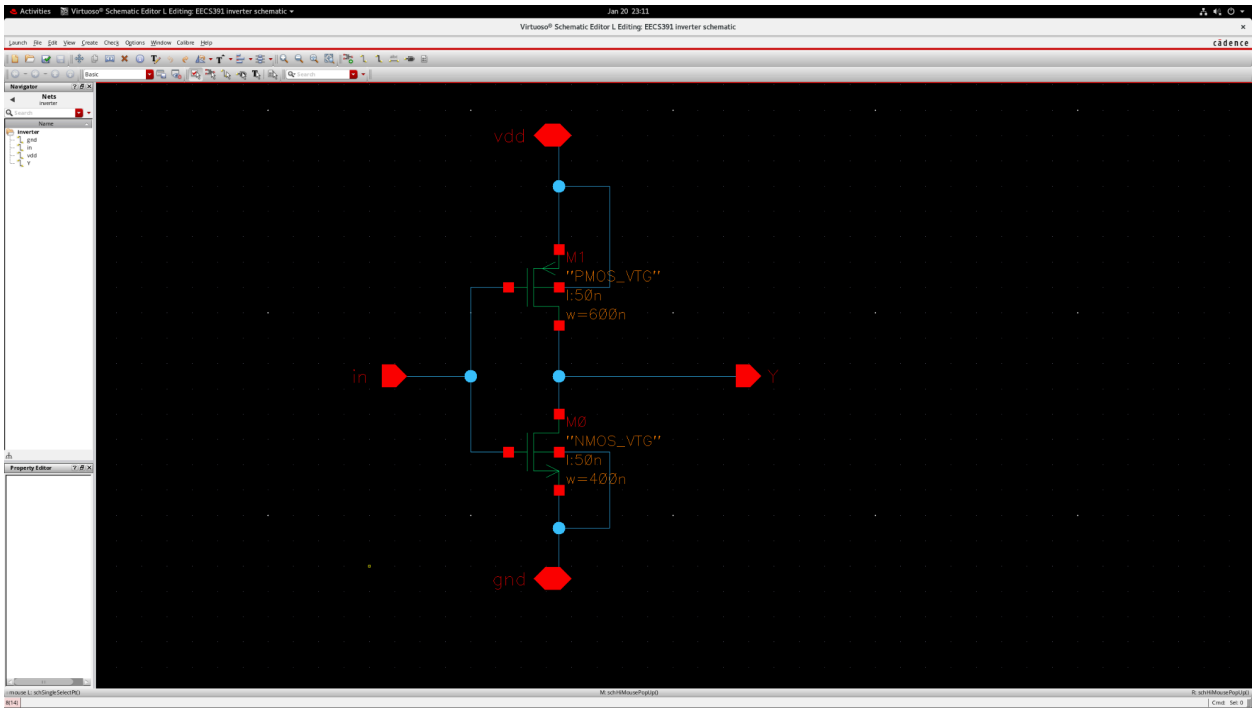
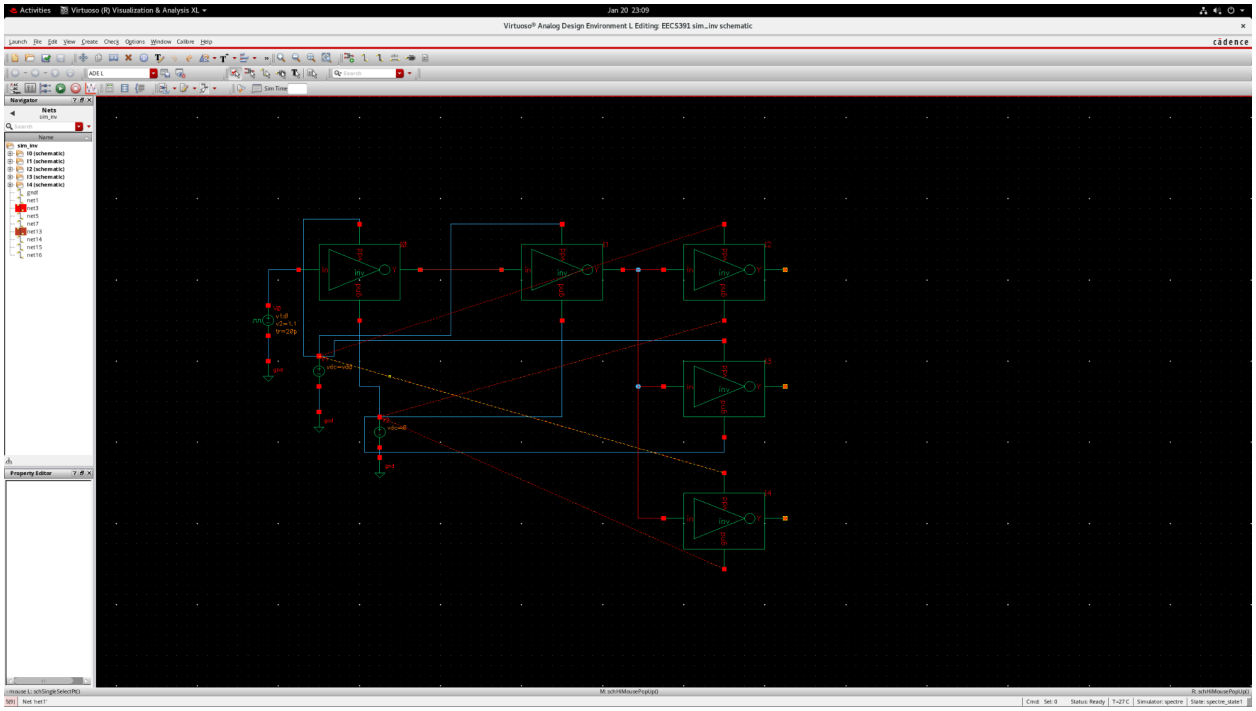
01/24/24
Student iD:3503394

1. Snapshot of your schematics, both inverter and testbench.

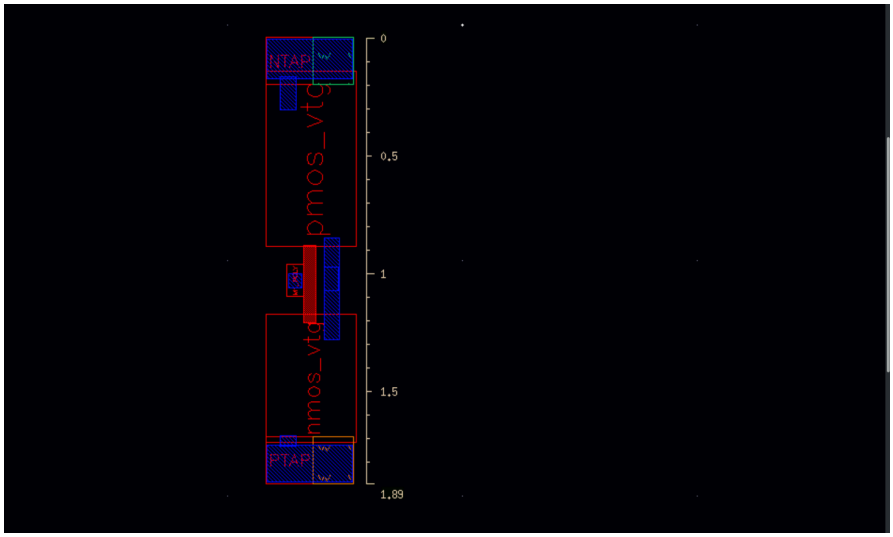
- Here is the snapshot of the schematic I made for the inverter. This is including the connections of the in,out,vdd,and gnd pins.

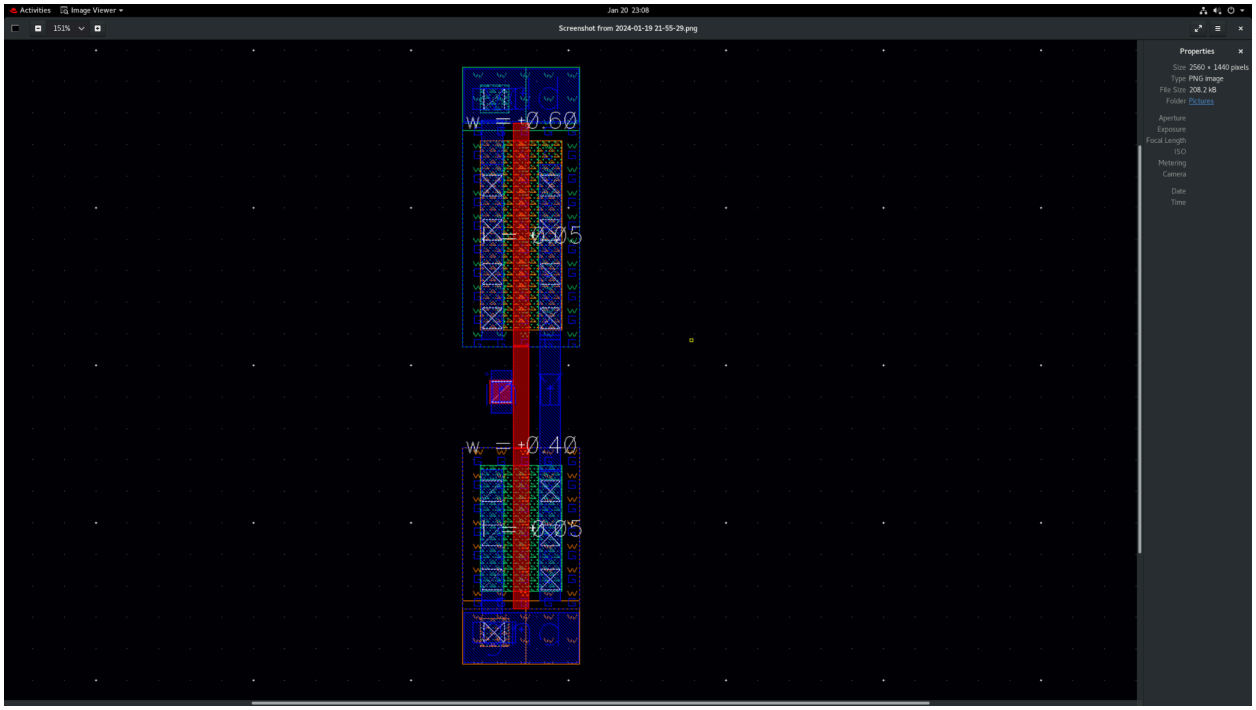


- Here is the snapshot of the testbench I made to simulate my design.

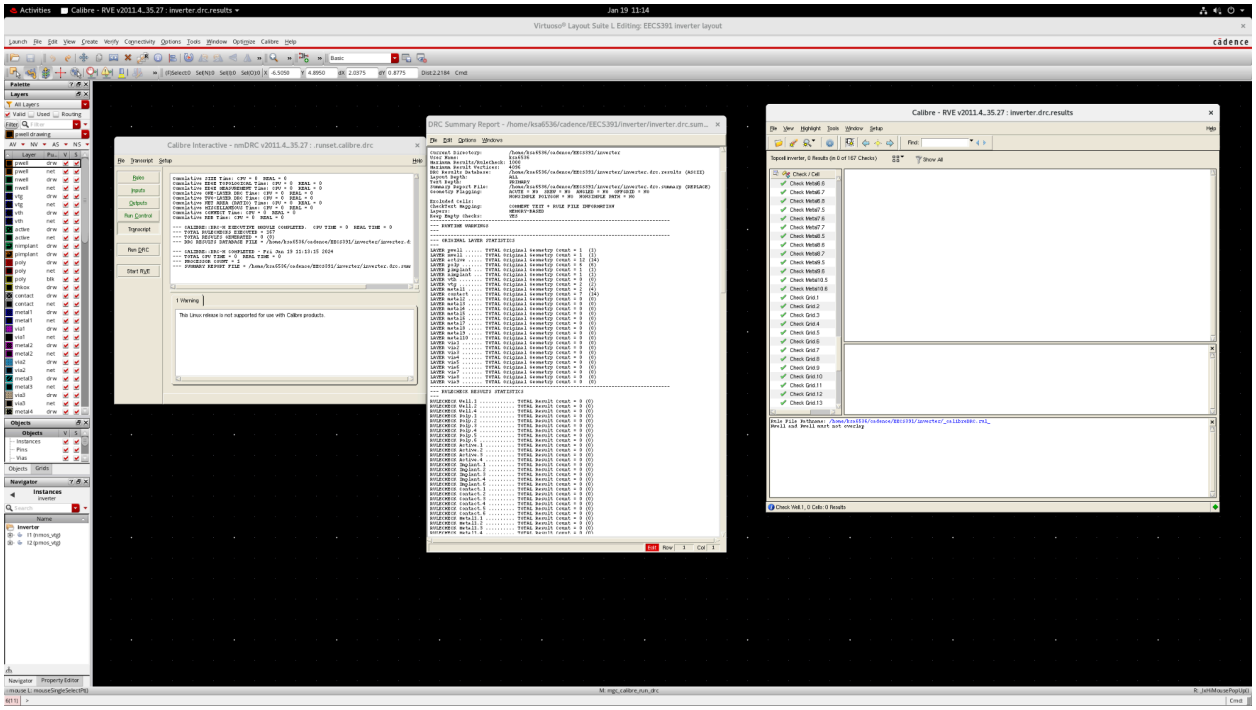


2. Snapshot of your layout of single inverter (use ruler shortcut key “k” to show the size of the circuit (from top to bottom, from left to right).



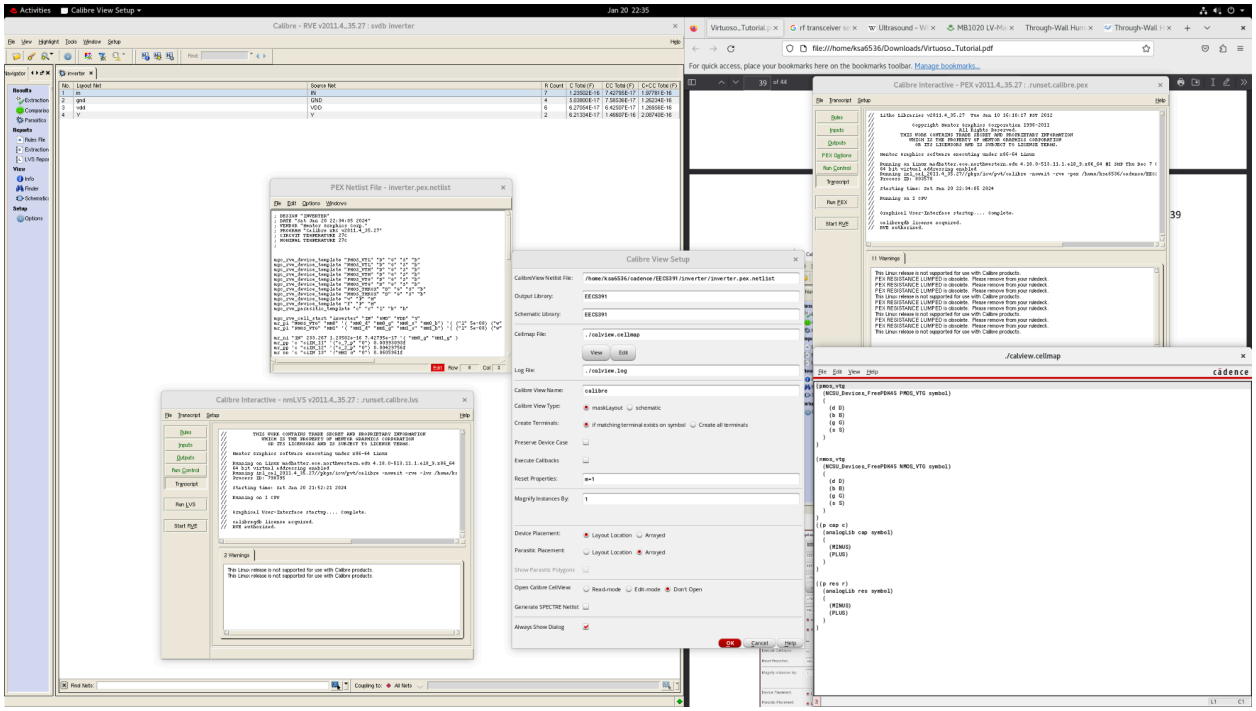


3. Snapshot of DRC results showing you are DRC clean.



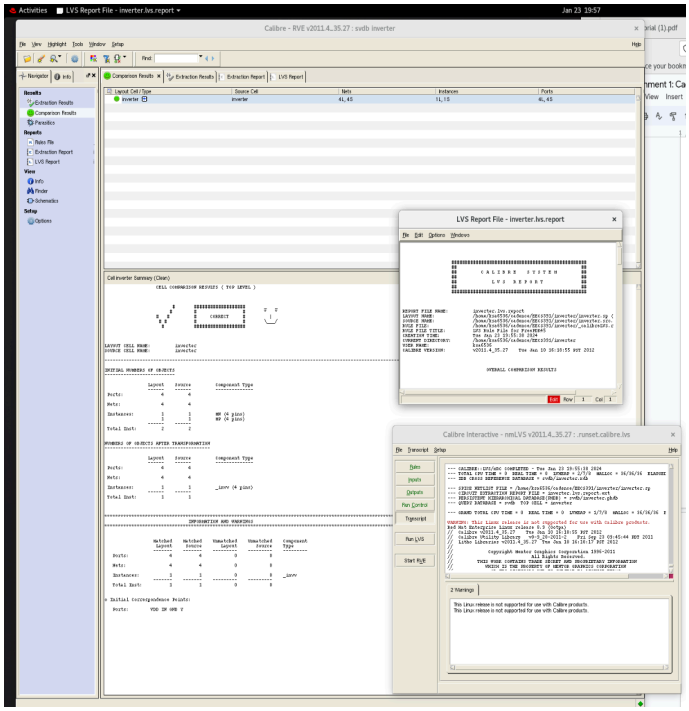
4. Snapshot of LVS results showing you are LVS clean.

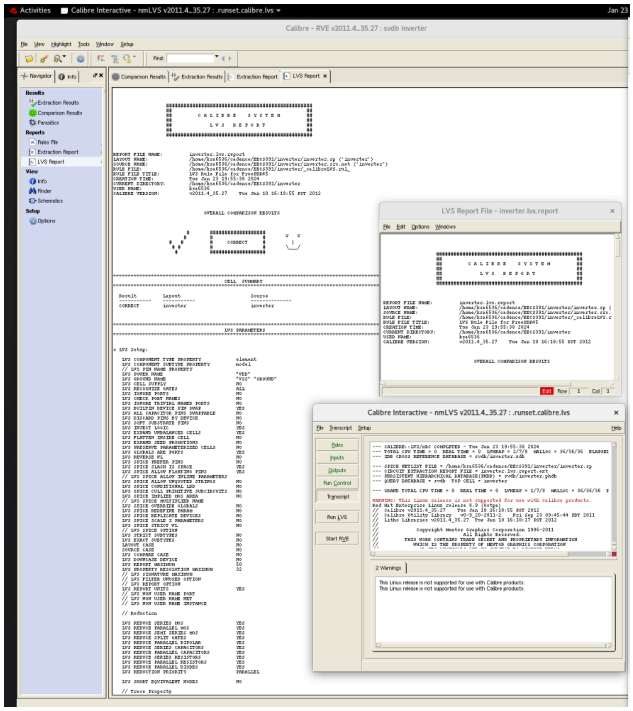
This snapshot shows the LVS and PEX results after doing the simulations successfully.



5. Snapshot of Layout extraction summary.

Here I show the layout extraction summary for LVS.

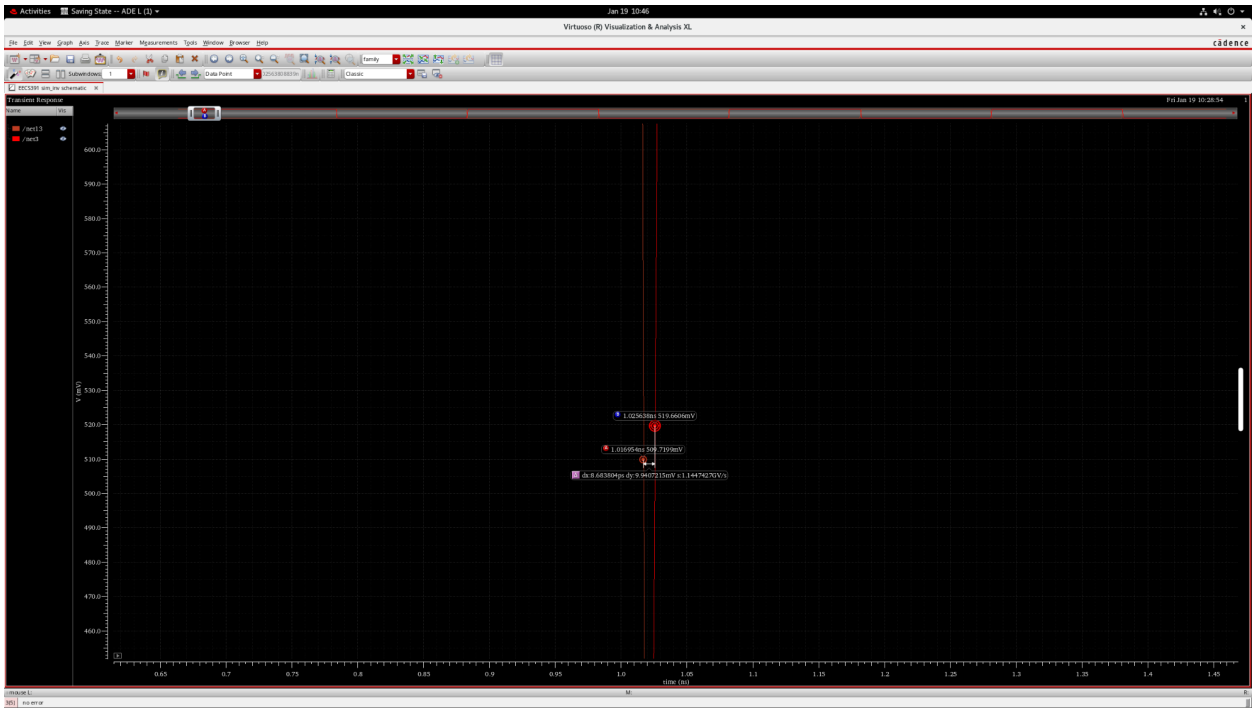




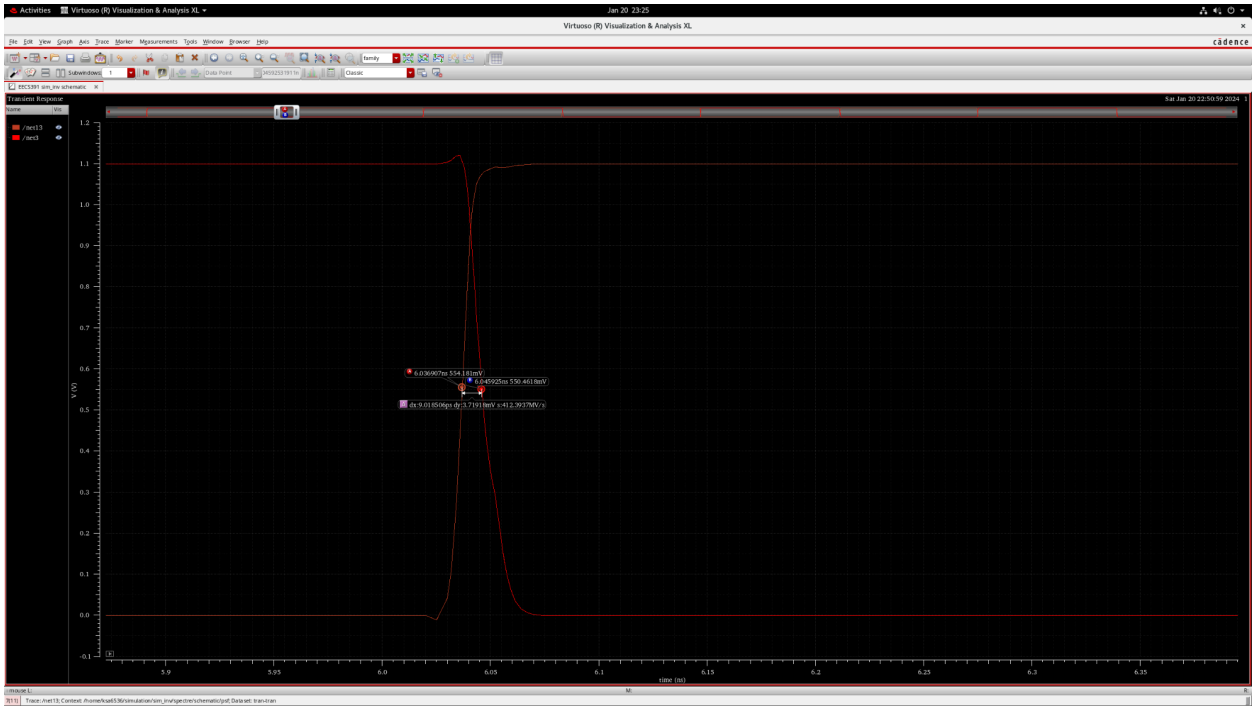
6. Both schematic simulation and layout extraction simulation waveforms of the inverter testbench showing input and output transitions. (Use shortcut key “a” and “b” in the waveform window to measure the delay from the input signal to output signal at 50%

transition points.

Here is the schematic simulation first:

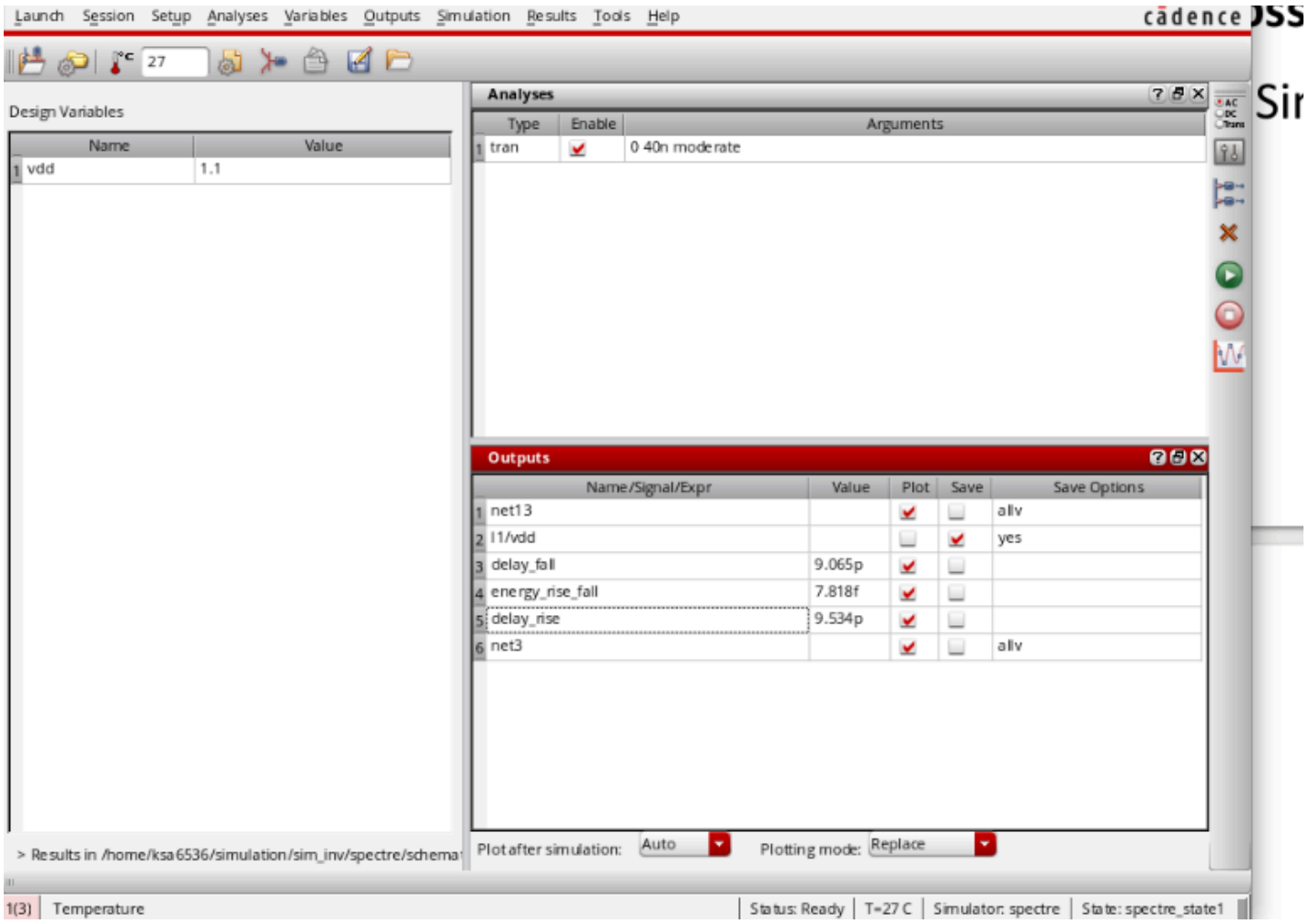


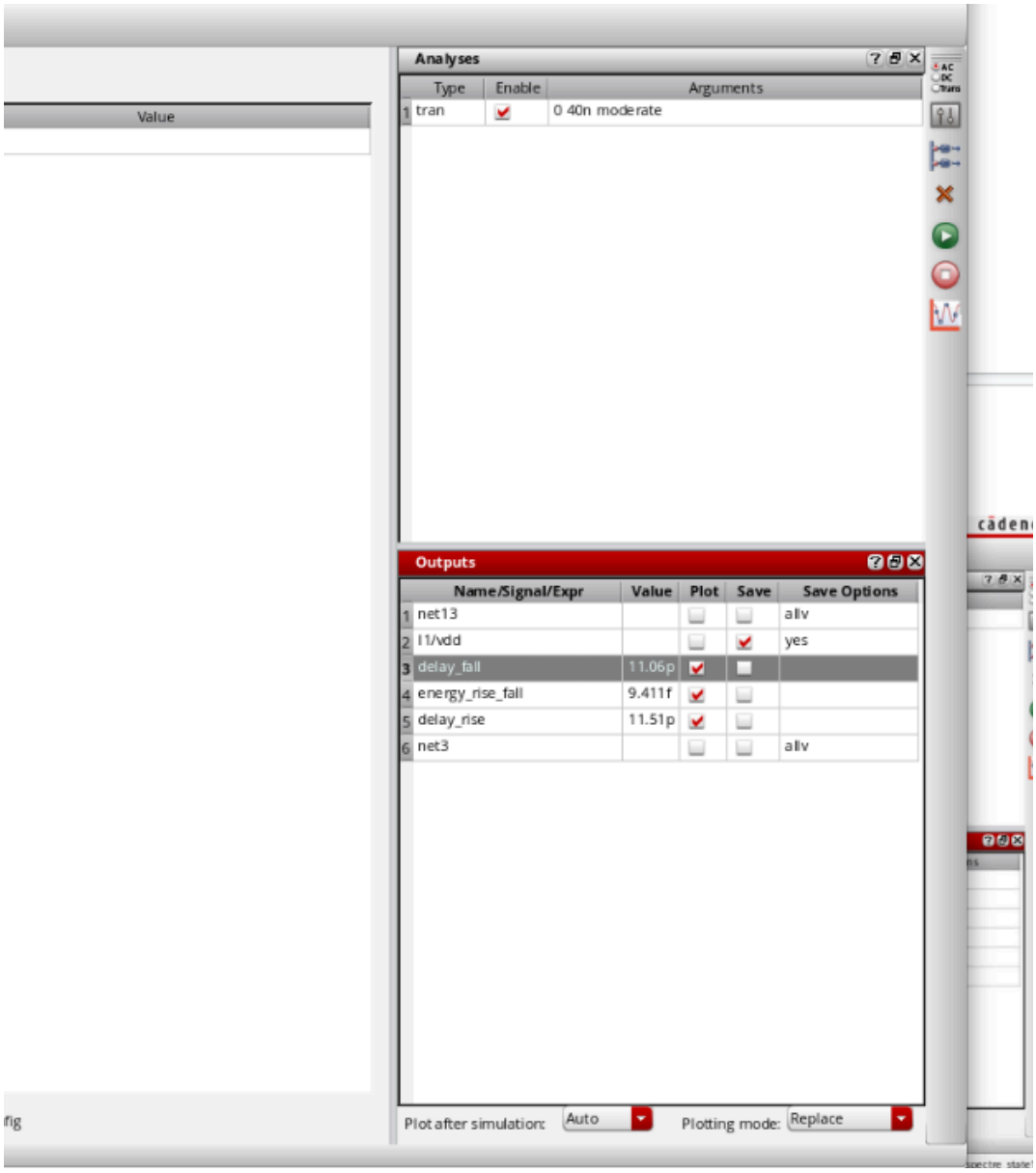
Here is the layout extraction simulation:

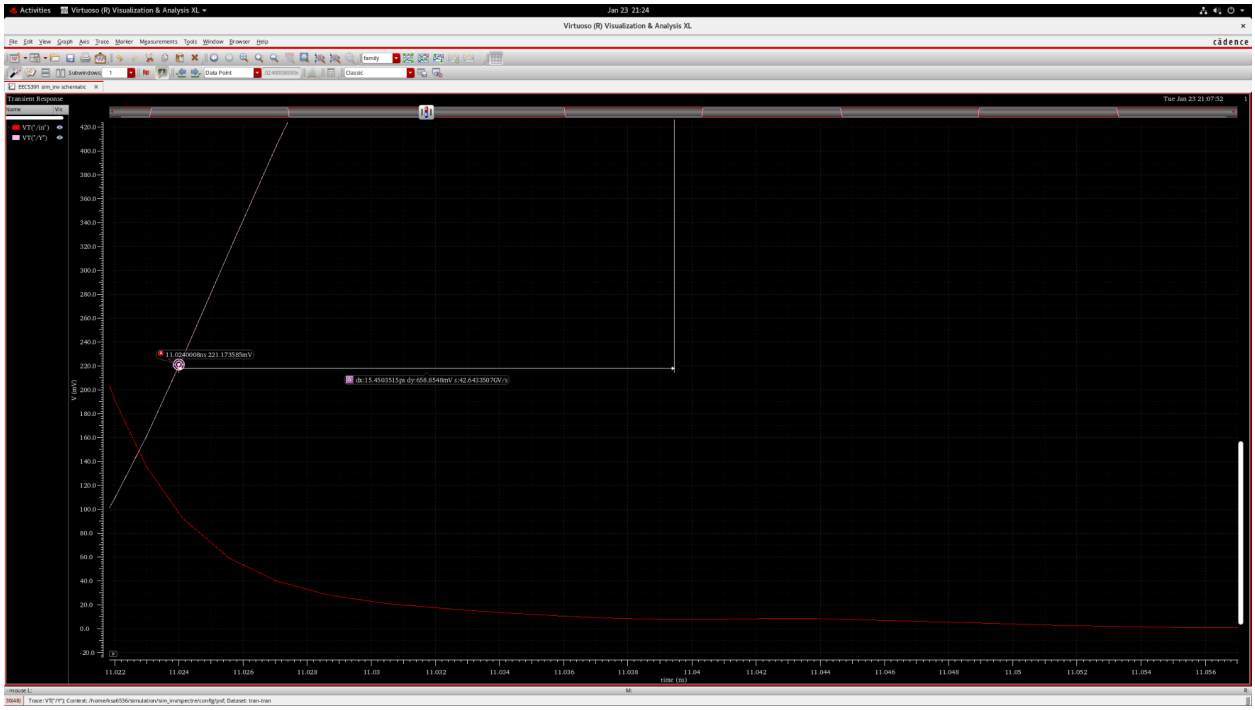


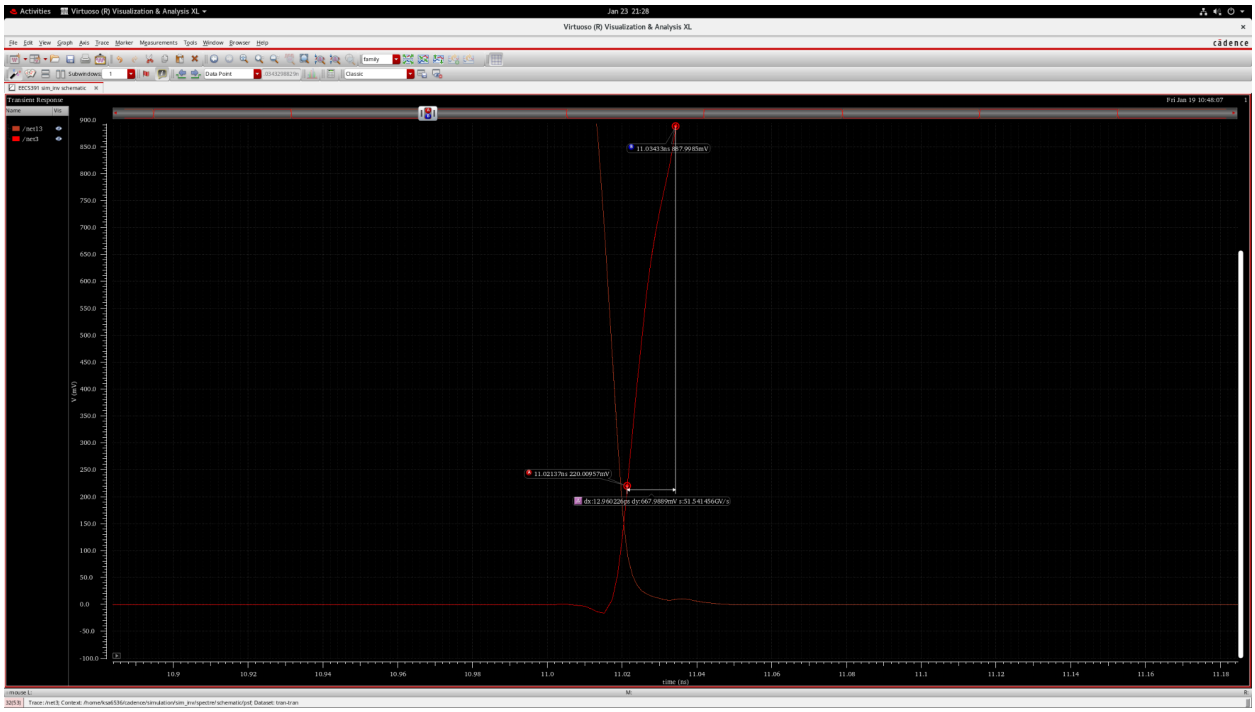
7. A simulation result table comparing (1) delay time (both rising and falling), (2) transition time (slew rate) from 20% to 80% for both rising and falling, (3) energy during rise and fall transition of the inverter from both schematic and layout extracted simulation.

	Simulated	LVS
Delay Rise	9.065p (Rise)	11.51p
Delay Fall	9.535p (Fall)	11.06p
Energy	7.818f	9.411f
Slew Rate	51.541GV/s	42.643GV/s


Launch Session Setup Analyses Variables Outputs Simulation Results Tools Help
cadence
27
Design Variables
Name Value
1 vdd 1.1
Analyses
Type Enable Arguments
1 tran 0 40n moderate
Outputs
Name/Signal/Expr Value Plot Save Save Options
1 net13 allv
2 I1/vdd yes
3 delay_fall 9.065p
4 energy_rise_fall 7.818f
5 delay_rise 9.534p
6 net3 allv
> Results in /home/ksa6536/simulation/sim_inv/spectre/schema
Plot after simulation: Auto
Plotting mode: Replace
1(3) Temperature
Status: Ready
T=27 C
Simulator: spectre
State: spectre_state1


Value
Analyses
Type
Enable
Arguments
1 tran
0 40n moderate
Outputs
Name/Signal/Expr
Value
Plot
Save
Save Options
1 net13
allv
2 I1/vdd
yes
3 delay_fall
11.06p
4 energy_rise_fall
9.411f
5 delay_rise
11.51p
6 net3
allv
Plot after simulation:
Auto
Plotting mode:
Replace


Activities
Virtuoso (R) Visualization & Analysis XL
Jan 23 21:24
Virtuoso (R) Visualization & Analysis XL
cadence
Transient Response
Tue Jan 23 21:07:52
VT("/in")
VT("/F")
11.034000ns 221.173585mV
dx:15.4503515ps dy:658.8548mV s:42.643507GV/s
V (mV)
time (ns)


Activities
Virtuoso (R) Visualization & Analysis XL
Jan 23 21:28
Virtuoso (R) Visualization & Analysis XL
cadence
Transient Response
Fri Jan 19 10:48:07
/net13
/net3
11.034338ns 887.998835mV
11.021378ns 220.009578mV
dx:12.960226ps dy:667.9889mV s:51.541456GV/s
V (mV)
time (ns)