Cryogenic Characterization of 28-nm FD-SOI Ring Oscillators With Energy Efficiency Optimization

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***Abstract*— Extensive electrical characterization of ring oscillators (ROs) made in high-κ metal gate 28-nm fully depleted silicon-on-insulator technology is presented for a set of temperatures between 296 and 4.3 K. First, delay per stage (τ_P), static current (I_{STAT}), and dynamic current (I_{DYN}) are analyzed for the case of the increase of threshold voltage (V_{TH}) observed at low temperature. Then, the same analysis is performed by compensating V_{TH} to a constant, temperature-independent value through forward body biasing (FBB). Energy efficiency optimization is proposed for different supply voltages (V_{DD}) in order to find an optimal operating point combining both high RO frequencies and low-power dissipation. We show that the Energy-Delay product can be significantly reduced at low temperature by applying an FBB voltage (V_{FBB}). We demonstrate that outstanding performance of RO in terms of speed ($\tau_P = 37$ ps) and static current (7nA/stage) can be achieved at 4.3 K with V_{DD} reduced down to 0.325 V.**

***Index Terms*— 28-nm fully depleted silicon-on-insulator (FD-SOI), body biasing, cryogenic electronics, quantum computing, ring oscillator (RO), ultralow power.**

I. Introduction

SINCE the famous proposal for quantum computing with quantum dots [1], significant progress in Si spin qubits has been reported [2]–[5]. The first two-qubit logic gate in isotopically enriched Si was demonstrated [3], and a foundry-compatible CMOS SOI platform was used to demonstrate a hole spin qubit functionality [4], [5]. These major achievements on the basic building block of a quantum computer are paving the way for the implementation of a large number of qubits individually controlled with tunable nearest-neighbor couplings. However, scaling up these systems in complex quantum computing architectures can be extremely challenging. In addition to fundamental advances in physical understanding and material development needed for spin qubits, a consistent engineering work should be made to propose a means of controlling, interacting, and reading out a large number of qubits in parallel.

In recent years, hardware interfaces based on advanced CMOS technologies that operate at cryogenic temperature so as to ensure proximity to qubits have been proposed and discussed [6]–[9]. Bulk Si MOSFET [10]–[13] and some circuits such as ring oscillators (ROs) [11] and a field-programmable gate array [14] were characterized down to 4 K. Despite a significant reduction of subthreshold swing and improvement of carrier mobility at low temperature, some limitations have been raised on bulk Si MOSFETs. Nonideal kink behavior and hysteresis in the characteristics are induced by the bulk current generated by impact ionization at the drain combined with increased resistivity from the freeze out of charge carriers [15]. Moreover, the increase of drive current from the enhanced carrier mobility at low temperature is partially mitigated by the increase of threshold voltage which can be hardly compensated by body biasing in bulk technologies.

In this paper, an alternative to bulk Si CMOS technologies is proposed in order to provide more flexibility to designers for optimizing both high-performance and low power cryogenic electronics. Undoped thin-planar 28-nm fully depleted silicon-on-insulator (FD-SOI) devices offer an excellent short-channel electrostatic control, low leakage current, and immunity to random dopant fluctuations. More flexibility is brought to the circuit through an extremely effective body biasing allowing to switch dynamically between high performance mode [forward body biasing (FBB)] and ultralow leakage mode [reverse body biasing (RBB)] [16]. We thus propose to study the low temperature characterization of 28-nm FD-SOI ROs down to 4.3 K. The RO performance in terms of delay per stage (τ_P), dynamic

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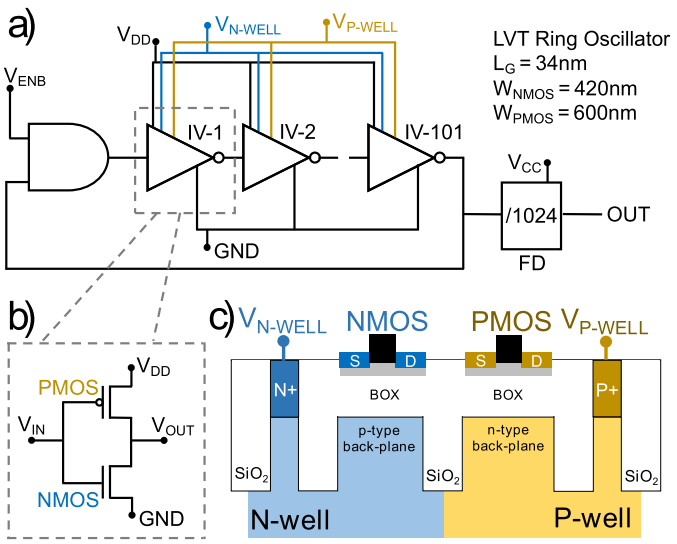

Fig. 1. (a) Schematic layout of 101-stages RO with 1024-FD. (b) Single inverter stage composed of NMOS and PMOS. (c) Illustration of LVT transistors in the flip-well configuration. V_{CC} is the supply voltage of the clock divider polarized with +1 V. V_{ENB} controls the AND gate that enables the oscillations ($V_{ENB} = V_{DD}$ was kept during all the measurements). For more details on the measurement protocol, see Table I.

(I_{DYN}), and static (I_{STAT}) currents is studied from 296 down to 4.3 K for V_{DD} ranging between 0.325 and 1.2 V. Cryogenic effects on the RO performance are investigated without and with FBB in order to compensate the shift of threshold voltage (V_{TH}) at low temperature. In addition, an energy efficiency optimization using FBB is proposed. We show that V_{DD} can be reduced down to 0.325 V while maintaining an ultralow Energy-Delay product (EDP).

This paper is organized as follows: a brief review of 28-nm FD-SOI is given in Section II. Low temperature characterization of FD-SOI ROs and their energy efficiency optimization are discussed in Section III. Finally, the main conclusions are drawn in Section IV.

II. Brief Review of 28-nm FD-SOI Technology

The GO1 FD-SOI transistors are fabricated with a gate-first high-κ metal gate using STMicroelectronics technology [17], [18]. They are processed on 300-mm (100) SOI wafers with a buried oxide (BOX) thickness of 25 nm. The equivalent oxide thickness is 1.55 nm for NMOS and 1.7 nm for PMOS. Low-threshold-voltage (LVT) transistors are used with the flip-well architecture: N-WELL (resp. P-WELL) with p-type (resp. n-type) back-plane doping for NMOS (resp. PMOS).

A 34-nm gate length (L_G) is considered for both NMOS and PMOS transistors of width W_{NMOS} = 420 nm and W_{PMOS} = 600 nm. The schematic layout of RO in the flip-well configuration is shown in Fig. 1. The RO consists of 101 identical stages together with an enabling two-way AND gate. The output is fed to a frequency divider (FD) to lower its frequency in the sub-megahertz regime. The parameters and the measurement protocols used in this paper are summarized in Table I.

TABLE I
RO and MOSFET Parameters, Units, Description, and the Measurement Protocol

Parameter	*Unit*	*Description*	*Measurement protocol*
f	Hz	RO frequency	V_{ENB}=V_{DD}, V_{CC} = 1V and measure OUT.
τ_P	ps	RO delay per stage	= 1/(f×2×101×1024).
I_{DYN}	µA/ stage	Dynamic current per stage in oscillating state	V_{ENB}=V_{DD}, V_{CC} = GND and measure OUT.
I_{STAT}	nA/ stage	Static current per stage in non-oscillating state	V_{ENB} = V_{CC} = GND and measure OUT.
I_{EFF}	µA	Effective drive current of FD-SOI transistor [19]	I_{EFF} = 1/(1/ I_{EFF-N} + 1/ I_{EFF-P}) $I_{EFF-N(P)}$ = (I_H+ I_L)/2 where I_H = I_{DS} (V_{GS} = V_{DD}, V_{DS} = V_{DD}/2) I_L = I_{DS} (V_{GS} = V_{DD}/2, V_{DS} = V_{DD}) where V_{GS}, V_{DS}, and I_{DS} are MOSFET gate voltage, drain voltage and drain current.
$G(I_{EFF})$	%	I_{EFF} enhancement at low temperature	= [I_{EFF} (T) - I_{EFF} (296K)] / I_{EFF} (T)
$G(\tau_P)$	%	τ_P enhancement at low temperature	= [τ_P (T) - τ_P (296K)] / τ_P (T)
EPT	fJ	Energy per transition	=101 × τ_P × (I_{DYN} - I_{STAT}) ×V_{DD}
EDP	fJ×ps	Energy-Delay product	= τ_P × EPT

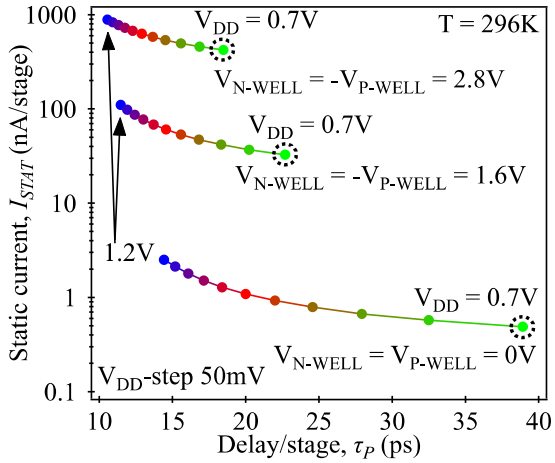

Fig. 2. Static current versus delay per stage for a set of V_{DD} from 0.7 to 1.2 V (ΔV_{DD} = 50 mV). Three different pairs of FBB voltages are considered. I_{STAT} is significantly increased at high V_{FBB} illustrating that ROs are well optimized for room temperature with V_{FBB} = 0 V.

III. Results and Discussion

A. RO Performance at Room Temperature

In contrast to usual bulk technology, ultrathin FD-SOI enables an extended body-bias range from −3V (RBB/FBB for NMOS and resp. PMOS) up to +3V (FBB/RBB for NMOS and resp. PMOS), thanks to the thin BOX providing either high-performance or low-power transistors [20]. In order to compensate the increase of V_{TH} at low temperature this paper is focused on LVT transistors

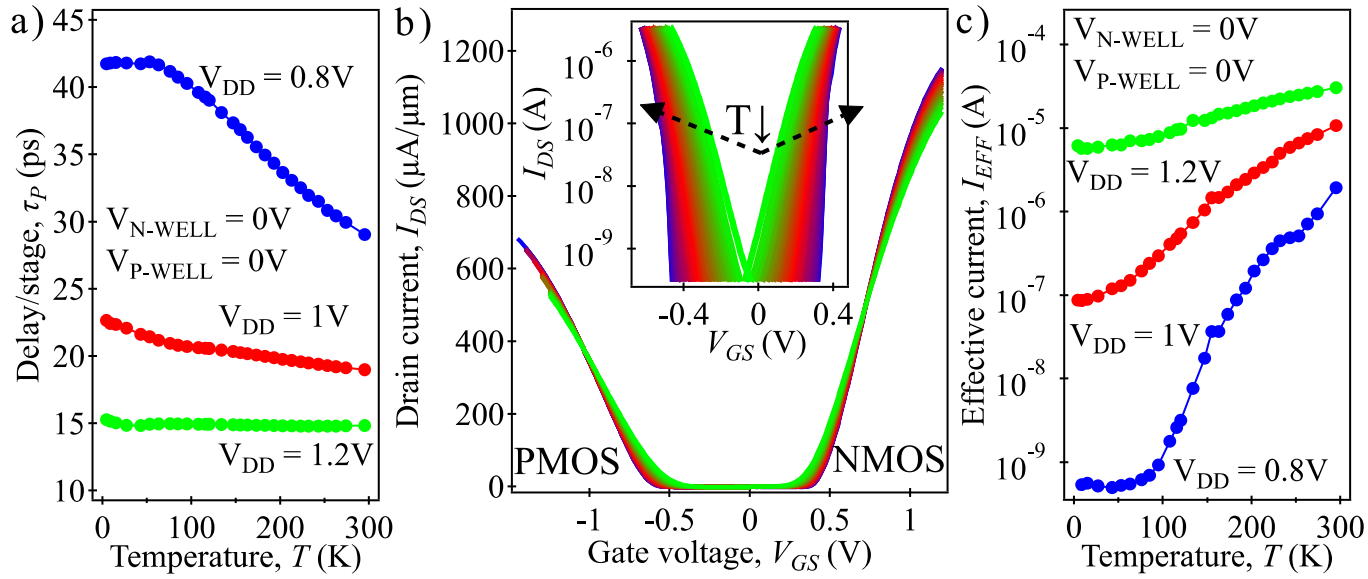

Fig. 3. (a) Delay per stage versus temperature for V_{DD} = 0.8, 1, and 1.2 V showing the RO slowing down due to the increase of V_{TH} at low temperature. (b) I_{DS}–V_{GS} curves recorded at V_{DD} = 1 V plotted in linear scale. Inset shows the subthreshold regime where current is plotted in logarithmic scale. Green (resp. blue) corresponds to room temperature (resp. 4.3 K). (c) Effective current versus temperature for different V_{DD}. The procedure used to calculate I_{EFF} is described in Table I.

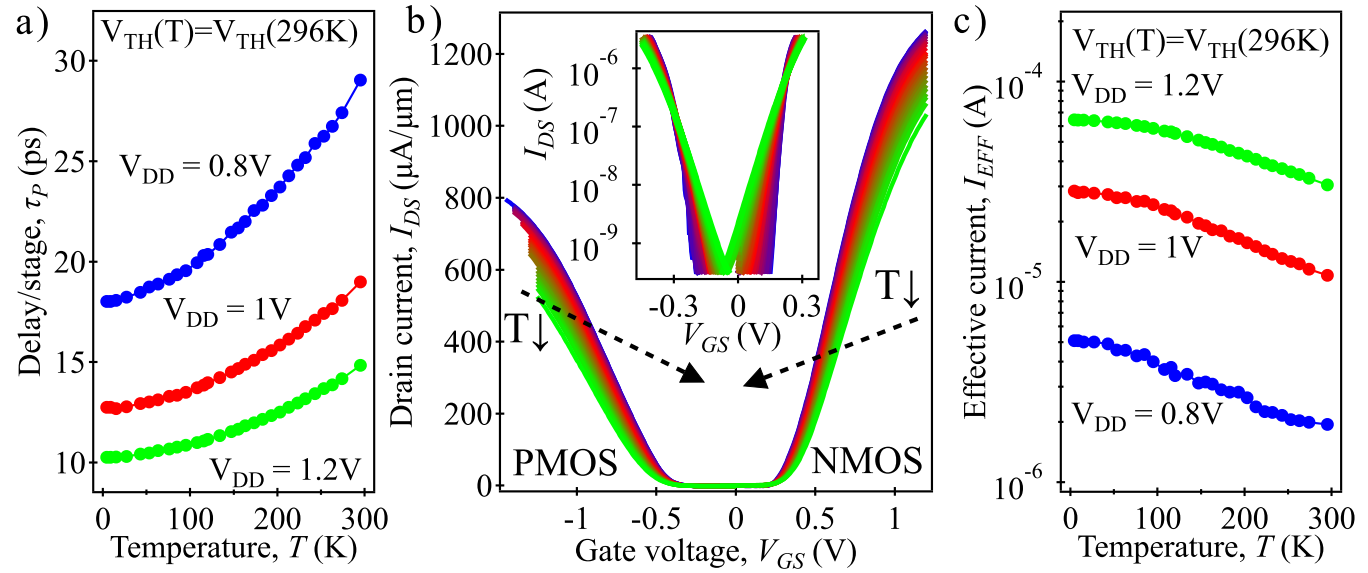

Fig. 4. (a) Delay per stage versus temperature for V_{DD} = 0.8, 1, and 1.2 V in the case of compensated V_{TH}. The RO speeds up at low temperature due to the carrier mobility enhancement. (b) I_{DS}–V_{GS} curves recorded at V_{DD} = 1 V plotted in linear scale. Inset shows the subthreshold behavior with current plotted in logarithmic scale. V_{TH_PMOS} and V_{TH_NMOS} are constant within the whole temperature range and can be found in Table II. Green (resp. blue) corresponds to room temperature (resp. 4.3 K) (c) Effective current versus temperature for different V_{DD}. As it can be seen in (b), the effective current increases at any stage of cooling down.

which enable a strong improvement in the switching speed thanks to FBB (body factor of 85 mV/V) at the cost of a higher leakage current. When no input is provided on the AND logic gate, I_{STAT} and then static power consumption occur due to the flow of leakage from supply to ground. For the room temperature data in Fig. 2, the static current of 101-stages RO is plotted as a function of the delay per stage for a set of different V_{DD} and V_{FBB}. Let us note that the delay of CMOS inverter can be approximated by $\tau_P = C_{LOAD} \times V_{DD}/I_{EFF}$ [21] with I_{EFF} the effective current (defined in Table I) and C_{LOAD} the load capacitance including the inversion capacitance, the parasitic capacitances and the wiring capacitance of back-end-of-line. Hence, lowering the supply voltage V_{DD} to achieve lower static power dissipation (i.e., lower I_{STAT}) degrades the RO performance giving higher delay per stage. This frequency reduction can be balanced by using FBB voltage. The efficiency of FBB for the τ_P reduction and improved performance is well observed in Fig. 2. For the RO operating at V_{DD} = 1 V, a τ_p reduction of 33% is achieved (at V_{FBB} = 2.8 V) at the expense of a significant

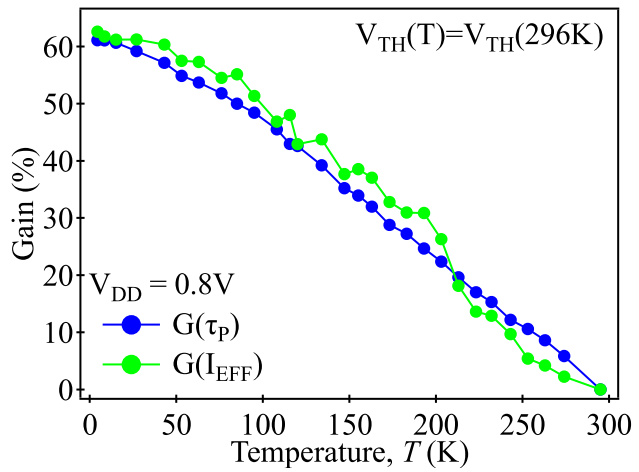

Fig. 5. Relative enhancement of I_{EFF} and τ_p at V_{DD} = 0.8 V for temperatures between 296 and 4.3 K. FBB is applied to compensate the increase of V_{TH} at low temperatures. Note that both relative gains are well correlated within the whole temperature range.

enhancement of static current (i.e., static power dissipation). Thus, a compromise in terms of power dissipation and speed should be carefully considered. Maintaining the body biasing efficiency at very low temperature is crucial to ensure accuracy and speed in the control and readout of qubits while using comparatively less power dissipation to perform the calculations.

B. RO Performance Without FBB Down to 4.3 K

Operation of FD-SOI transistors at cryogenic temperatures was already reported in [18], [22], and [23]. Since the scattering of charge carriers with phonons is sufficiently weak and can be neglected at liquid helium temperature, electron and hole mobilities are enhanced and should lead to a smaller τ_p at lower temperature for a given V_{DD}. However, despite a significant increase of drive current expected at low temperature [18], the RO slows down as it can be seen in Fig. 3(a). This increase in delay per stage is explained by the V_{TH} shift at lower temperatures [Fig. 3(b)] for both NMOS and PMOS transistors. Consequently, the effective current is strongly reduced at lower temperatures due to a lower overdrive current for the gate voltage. This I_{EFF} reduction becomes especially important at low V_{DD}. Hence, without FBB ($V_{N\text{-WELL}} = V_{P\text{-WELL}} = 0$ V) the enhanced carrier mobility at low temperature does not improve the effective current which becomes strongly limited by the V_{TH} increase. The I_{EFF} reduction shown in Fig. 3(c) is then directly responsible for the observed increase of τ_P. The degradation of RO performance becomes even more important at low V_{DD}. Therefore, without FBB used to compensate the V_{TH} shift it may be difficult to work with an optimized cryogenic digital control electronics combining the demands of both high-performance and low-power consumption.

C. RO Performance by Applying FBB Down to 4.3 K

In order to preserve the benefit of higher carrier mobility and thus, higher driving current at low temperatures, the V_{TH} shift should be compensated. The ability to adjust V_{TH} through body biasing was already successfully demonstrated down to 4.3 K using 28-nm FD-SOI transistors [18]. In this paper, the threshold voltages of NMOS and PMOS transistors as well as the body factors ($\Delta V_{TH}/\Delta V_{FBB}$) were systematically extracted over a wide range of V_{FBB} from 0 up to 3 V. Then, by adjusting $V_{N\text{-WELL}}$ and $V_{P\text{-WELL}}$ for each temperature, the V_{TH} shift was compensated (in order to keep V_{TH} measured at 296 K) and thus, V_{TH_PMOS} and V_{TH_NMOS} were kept constant in temperature, as shown in Fig. 4(b). In contrast to the previous results (without FBB), a significant speedup for different V_{DD} is now observed when threshold voltages were settled to $V_{TH}(T) = V_{TH}$ (296 K) within the full temperature range [Fig. 4(a)]. By reducing the temperature from room temperature down to 4.3 K, the delay per stage is decreased by 38% at V_{DD} = 0.8 V, 33% at V_{DD} = 1 V, and 31% at V_{DD} = 1.2 V. The τ_P reduction can be explained by the increase of I_{EFF} shown in Fig. 4(c). By monitoring the enhancement of $G(I_{EFF})$ and $G(\tau_P)$ at low temperature (down to 4.3 K) we observe a good correlation between the relative variations in the I_{EFF} increase and the τ_P reduction for V_{DD} = 0.8 V, as shown in Fig. 5. Hence, the load capacitance seems to be weakly dependent on temperature since the I_{EFF} increase is mainly responsible for the speedup of RO at low temperature.

Besides the low-temperature behavior of τ_P, other critical parameters such as dynamic current (I_{DYN}) and static current (I_{STAT}) were monitored for the evaluation of the power dissipation in oscillating and sleeping mode. As shown in Fig. 6, I_{DYN} naturally increases as the temperature is reduced due to the I_{EFF} enhancement, which leads to the increase of active power dissipation. Indeed, by applying FBB for the V_{TH} compensation, the effective current is improved due to higher carrier mobility at low temperature, and then I_{DYN} is enhanced. In comparison to the room temperature case, the I_{DYN} enhancement normalized by V_{DD} is about 34% at 4.3 K.

TABLE II
COMPARISON OF RO PERFORMANCE AT 296 AND 4.3 K BETWEEN THE CASES UNCOMPENSATED AND COMPENSATED V_{TH}

T (K)	V_{DD} (V)	V_{TH_NMOS} (V) / V_{TH_PMOS} (V)	$V_{N\text{-WELL}}$ (V) / $V_{P\text{-WELL}}$ (V)	τ_P (ps)	I_{DYN} (nA/stage)	I_{STAT} (nA/stage)
296	0.8	0.224 / -0.376	0 / 0	27	497	0.67
	1	0.216 / -0.363	0 / 0	18	885	1.29
	1.2	0.208 / -0.352	0 / 0	14	1308	1.9
4.3	0.8	0.391 / -0.549	0 / 0	42	363	0.002
		0.224 / -0.376	1.65 / -2.75	18	717	0.002
	1	0.384 / -0.531	0 / 0	22	812	0.007
		0.216 / -0.363	1.65 / -2.65	13	1182	0.01
	1.2	0.375 / -0.518	0 / 0	15	1281	0.037
		0.208 / -0.352	1.62 / -2.62	10	1669	0.29

The set of $V_{N\text{-WELL}}$ and $V_{P\text{-WELL}}$ used for different V_{DD} is chosen to compensate the corresponding V_{TH}-shift at 4.3K.

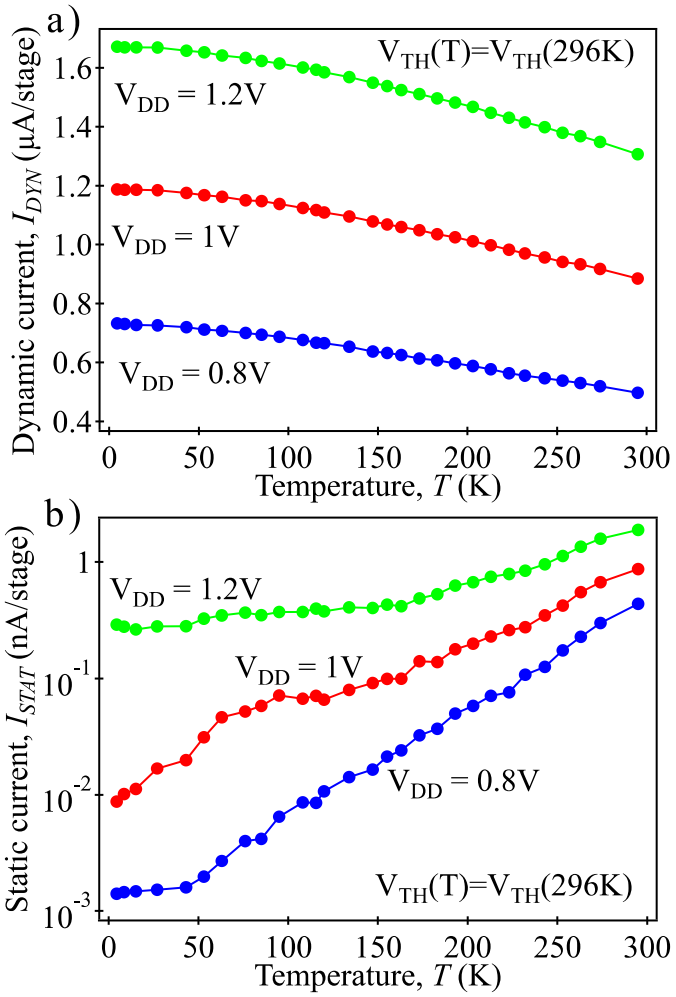

Fig. 6. (a) Dynamic current and (b) static current as a function of temperature for different V_{DD} in the case of compensated V_{TH}. Note that I_{STAT} continuously decreases and reaches 2.3 pA/stage for V_{DD} = 0.8 V at 4.3 K.

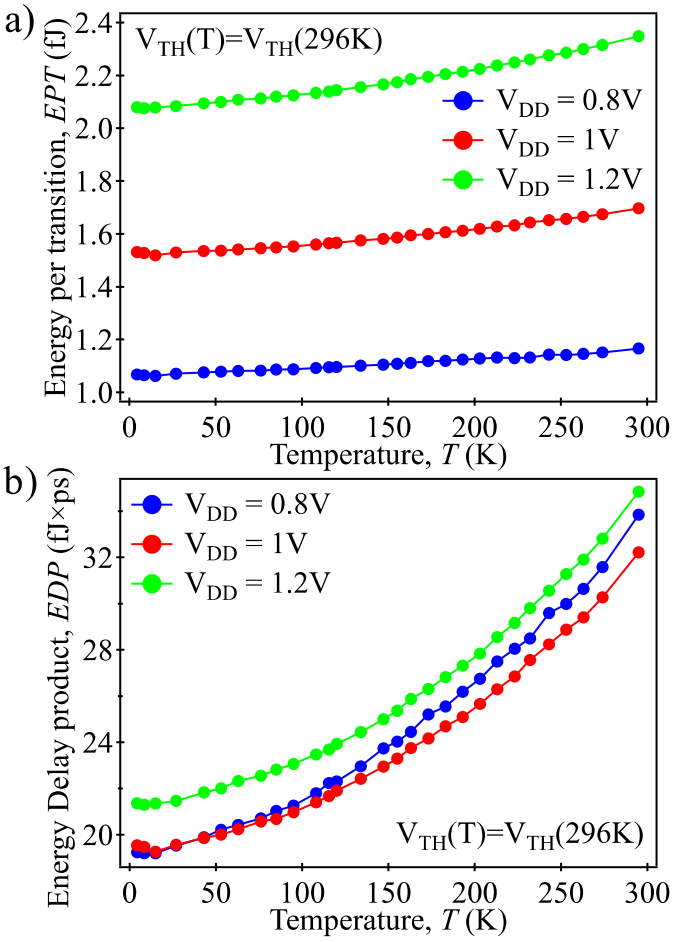

Fig. 7. (a) EPT versus temperature for three different V_{DD}. Note that the decrease of EPT for all V_{DD} at cryogenic temperature is mainly due to an important τ_P reduction. (b) EDP versus temperature for V_{DD} = 0.8, 1, and 1.2 V. The lowest EDP indicates the optimal V_{DD}.

At the same time a significant reduction in static current [Fig. 6(b)] and thus, in static power dissipation is observed thanks to the decrease of subthreshold swing at low temperature [18].

As compared to room temperature, the calculated static power dissipation $P_{STAT} = I_{STAT} \times V_{DD}$ at 4.3 K is reduced by a factor of 1600 (V_{DD} = 0.8 V), 100 (V_{DD} = 1 V), and 6.5 (V_{DD} = 1.2 V). The RO performance in terms of τ_P, I_{DYN}, and I_{STAT} measured at 4.3 and 296 K with and without FBB is summarized in Table II.

D. Energy Efficiency Optimization Down to 4.3 K

Wiring up large qubit arrays today is a key issue across all qubit platforms. Indeed, a large number of qubits must be read out periodically and rapidly processed to check whether errors occur along the way and to correct them. Furthermore, the energy efficiency of a cryogenic platform for the classical control of a scalable quantum computer is essential. Low-power dissipation is required, down to few watts at 4 K [24] to enable the operation of thousands of cryogenic fault-tolerant loops in existing refrigerators. The adoption of FD-SOI technology to reduce power consumption while keeping high speed of operation can be a promising solution for the future implementations of large-scale quantum computers. Then, ensuring that control signals produce minimal dissipation will be essential at the lowest temperature stage of the refrigerator. We thus propose to deal with the energy consumption per transition and more specifically with the Energy-Delay metric to translate the more and more stringent constraint on the speed, while not disregarding the energy dissipation. The temperature dependence of energy per transition (EPT) for different V_{DD} is shown in Fig. 7(a). As in Section III-C, FBB is applied to correct the V_{TH} shift at low temperatures. One can notice that despite an increase of I_{DYN} [shown in Fig. 6(a)], the significant decrease of delay per stage at low temperature [Fig. 4(a)] results in EPT becoming smaller and smaller during the cooling down to 4.3 K. Lowering V_{DD} at liquid helium temperature also leads to a significant reduction of EPT at the expense of performance with a lower RO frequency. To achieve the best possible performance, the Energy-Delay metric [21], [25] defined in Table I can be used. Smaller Energy-Delay values imply a lower energy consumption at the same level of performance corresponding to a more energy-efficient design. At 296 K, the lowest EDP is obtained for V_{DD} = 1 V as shown in Fig. 7(b). However, as the RO is cooled down, we see that the

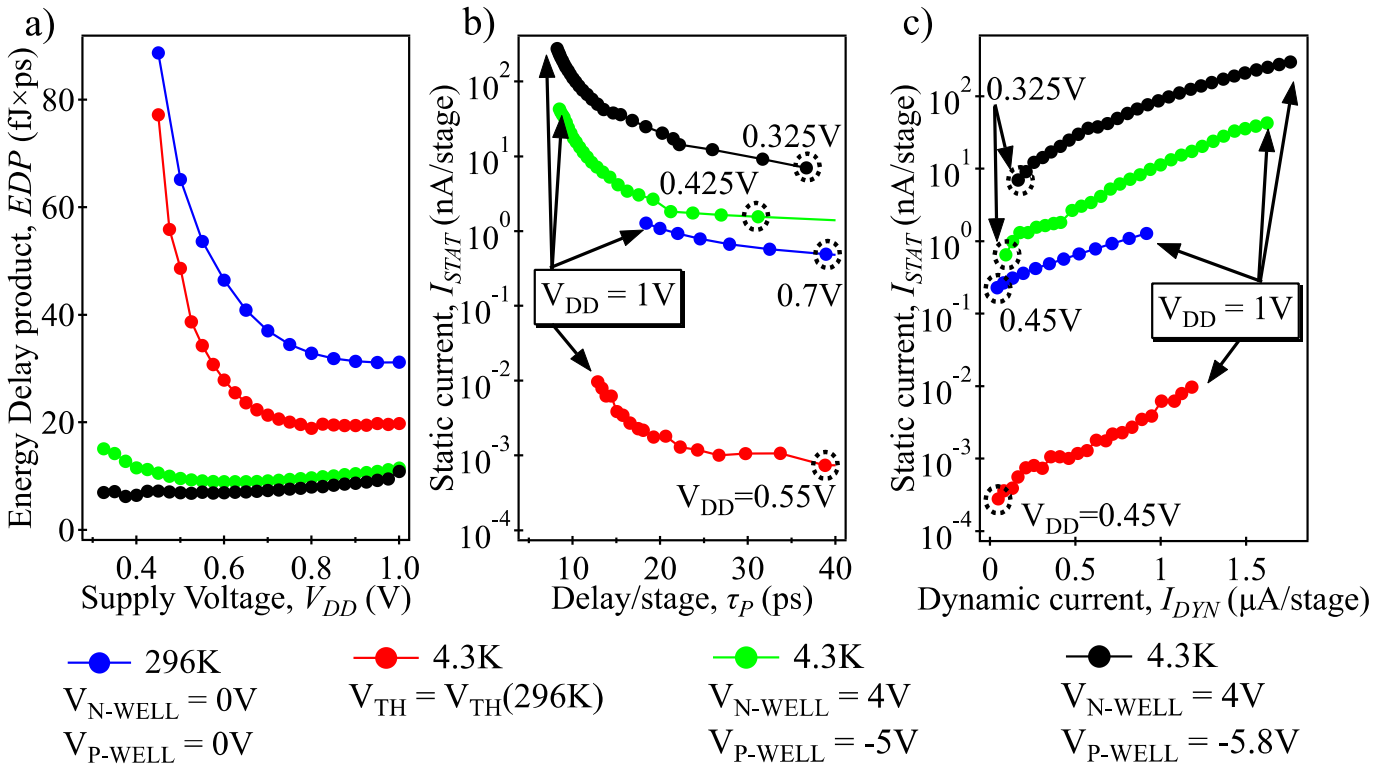

Fig. 8. (a) Comparison of EDP versus V_{DD} at room temperature and 4.3 K with different FBB conditions. Note that for the case of very high V_{FBB} ($V_{N\text{-WELL}} = 4$ V and $V_{P\text{-WELL}} = -5.8$ V) no minimum is observed down to $V_{DD} = 0.325$ V. (b) Static current versus delay/stage metric measured at RT and 4.3 K for different V_{DD}. (Initial and final values for the studied V_{DD} interval are given.) (c) Static current versus dynamic current for different V_{DD} at 296 and 4.3 K. Note that depending on FBB voltage, I_{DYN} between 30 nA/stage and 1.76 μA/stage can be achieved. Initial and final values for the studied V_{DD} interval are given.

optimal V_{DD} can be lowered. At 4.3 K, the minimal EDP is now obtained at $V_{DD} = 0.8$ V. V_{DD} dependence on the EDP is shown in Fig. 8(a) at 4.3 and 296 K. At 4.3 K, FBB is first used to keep the same V_{TH} as that obtained at room temperature. Then, higher V_{FBB} was applied in order to maximize the energy efficiency. As expected, EDP is minimal for $V_{DD} = 1$ V at 296 K. However, a strong increase is observed at low V_{DD} due to the rise of τ_P as shown in Fig. 3(a). At 4.3 K, the V_{TH} compensation allows to reduce τ_P [see Fig. 4(a)] and leads to the decrease of EDP with a minimal value close to $V_{DD} = 0.8$ V. However, once again, the EDP remains strongly enhanced at lower V_{DD}. The best FBB configuration minimizing EPT while keeping high RO speed is obtained for $V_{N\text{-WELL}} = 4$ V and $V_{P\text{-WELL}} = -5.8$ V. This FBB configuration was chosen such as no minimum is observed in EDP even at V_{DD} as low as 0.325 V. The combination of LVT transistors with high FBB allows to further reduce V_{TH} and then to obtain a lower τ_P for a given V_{DD}. In Fig. 8(b), we show the static current versus τ_p for different V_{DD} in order to highlight the advantage of FBB on LVT FD-SOI transistors. At 4.3 K, low delay operation can be achieved without suffering from an excessive increase of static power. However, if high FBB voltages ($V_{N\text{-WELL}} = 4$ V and $V_{P\text{-WELL}} = -5.8$ V) are applied to reduce V_{TH} close to 0 V, I_{STAT} is significantly increased. Nevertheless, excellent RO performance with $\tau_P = 37$ ps and $I_{STAT} = 7$ nA/stage are demonstrated at $V_{DD} = 0.325$ V. This static current can be further reduced by a factor 10 if $V_{P\text{-WELL}}$ is lowered from -5.8 to -4.8 V while keeping $V_{N\text{-WELL}} = 4$ V. In addition, as shown in Fig. 8(c), ultralow I_{DYN} current of 92 nA/stage (at $V_{DD} = 0.325$ V) can be of great importance if low-power dissipation in oscillating mode at moderate speed ($\tau_P = 71$ ps) is required. It should be noted that the RO performance for different FBB configurations can be further optimized depending on targeted applications.

TABLE III
ENERGY EFFICIENCY OPTIMIZATION FOR ULTRALOW SUPPLY VOLTAGE UNDER FBB AT 4.3 K

V_{DD} (V)	$V_{N\text{-WELL}}$ (V) / $V_{P\text{-WELL}}$ (V)	τ_P (ps)	I_{DYN} (nA/stage)	I_{STAT} (nA/stage)
0.325	4 / -5.8	37	170	7
	4 / -4.8	71	92	0.7
0.5	4 / -5.8	17	518	30
	4 / -4.8	21	426	1.6

The data reported in Table III are given to illustrate the tremendous versatility of 28-nm FD-SOI technology for both ultralow power and high-performance applications at highly reduced V_{DD} at 4.3 K. This highlights the possible tradeoffs between the delay and the static/dynamic power dissipation. For instance, in case of $V_{N\text{-WELL}} = 4$ V and $V_{N\text{-WELL}} = -4.8$ V, we obtain highly improved delay of 31 ps with

I_{DYN} = 271 nA/stage and I_{STAT} = 1.56 nA/stage if V_{DD} is increased to 0.425 V.

IV. Conclusion

This paper describes, for the first time, electrical characterization of 28-nm FD-SOI ROs down to 4.3 K. The unique capability of body biasing in the development of fast power-efficient peripheral circuitry for qubits is shown through the analysis of delay per stage, static, and dynamic currents of the ROs. Also, the tradeoff between energy consumption and delay per stage is discussed for a large range of supply voltage (V_{DD} from 0.325 to 1.2 V). It is demonstrated that by properly balancing the energy consumption and delay, the maximum benefit in terms of speed and energy consumption can be derived at a very low supply voltage of V_{DD} = 0.325 V only. At 4.3 K and high FBB voltage ($V_{N\text{-WELL}}$ = 4 V and $V_{P\text{-WELL}}$ = −5.8 V), a very small EPT of 0.186 fJ with τ_P = 37 ps and EDP = 6.9 fJ·ps are achieved at V_{DD} = 0.325 V. These achievements prove that the 28-nm FD-SOI platform provides significant opportunities toward optimizing highly efficient and ultralow-power cryogenic circuits for large-scale quantum computing. Based on the promising results in this paper, other applications such as low-temperature sensors, low power neuromorphic circuits [26], or space electronics can be envisioned.

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Authors' photographs and biographies not available at the time of publication.