

GIOVANNI MICHEL

Electrical Engineering

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EDUCATION

Master of Science in Electrical Engineering Northwestern University, Evanston, IL. Graduation date: May 2025	Cumulative GPA: 3.4
Master of Science in Artificial Intelligence Florida Atlantic University, Boca Raton, FL. Graduation date: August 2023	Cumulative GPA: 3.7
Bachelor of Science in Computer Engineering Florida Atlantic University, Boca Raton, FL. Graduation date: August 2022	Cumulative GPA: 3.4

TECHNICAL SKILLS

Programming Languages: C/C++, C#, MATLAB, Python, VHDL, System Verilog, JavaScript
Skills & Technologies: ROS, Oscilloscopes, DMM, Soldering, PCB Design, Linux, Genus, Virtuoso, Quartus, PSPICE, SolidWorks
Controllers: TI MSP430, ARM Cortex-M3, Raspberry Pi, Nexys4 DDR FPGA, Intel Loihi

PROFESSIONAL EXPERIENCE

Graduate Research Assistant, Los Alamos National Laboratory Los Alamos, NM <i>Conduct research, design, and development towards training spiking networks on the Intel neuromorphic research processor, Loihi.</i> <ul style="list-style-type: none">Investigate reinforcement learning and deep reinforcement learning algorithm design for neuromorphic processors.Developed and implemented sparse encoding methods for physical dynamics in control theory to train spiking networks on neuromorphic systems.	April 2022 – Present Day
Graduate Research Assistant, Grayson Group Evanston, IL <i>Conduct experiments to model the dynamics of various electronic devices at cryogenic temperatures down to 1.5K.</i> <ul style="list-style-type: none">Designed experiments to analyze signal stability and temperature dependence for Voltage-Controlled Oscillators (VCOs) by modeling mod. Allan variance, power spectral density, and phase noise.Investigated the temperature dependence of voltage thresholds, Fermi energy, leakage current, and insulator capacitance through meticulously designed experimental procedures.	December 2023 – Present Day
Software Engineer (Internship), GRUBBRR Boca Raton, FL <i>Performed QA automation for unit and functional tests as assigned by Project Management, ensuring product quality and reliability.</i> <ul style="list-style-type: none">Implemented standardized QA processes, improving efficiency in product testing and the design of end-to-end product releases.Contributed to onsite coordination, progress tracking, planning, closeout, and quality control to support project development.Collaborate with client integration teams using technical communication skills and Scrum/Agile methodologies, driving successful project outcomes.	September 2021 – February 2022

PUBLICATIONS

- Michel, G.**, Nesbit, S., Sornborger, A. (2024, December). Closed-loop Q-learning Control with Spiking Neuromorphic Network. LA-UR-24-32562. Association for Computing Machinery. **Paper** (In review, submitted 12/1/24).
- Michel, G.**, Renner, A., Kunde, G., Sornborger, A. (2023, August). Towards Q-Learning-based control using a spiking neuromorphic network and sparse encoding. LA-UR-23-283336. Association for Computing Machinery. **Poster**.
- Michel, G.**, Pulido, J., Turton, T. (2022, August). Database Visualization for the Data Science Infrastructure Project. **Poster**.

RELEVANT PROJECTS

NFC Wireless Temperature Sensor VLSI Group Project <ul style="list-style-type: none">Designed schematics for an integrated circuit (IC) to convert analog temperature input into digital output, powered via Near Field Communication (NFC).Developed and tested schematics and testbenches for key components, including a temperature sensor, low-dropout regulators, power rectifier, and demodulation rectifier.Engineered and validated a power-harvesting component, creating multistage rectifiers integrated with a bandgap reference circuit to generate a stable signal.Gained expertise in RC response, impedance matching, and analog-to-digital converter (ADC) design through project implementation.	June 2024
4x4 6T SRAM VLSI Project <ul style="list-style-type: none">Designed schematics and testbench for a 4x4 6T SRAM array, including sense amplifiers, bitline precharge, and write circuits for each column.Created a 6T SRAM layout with dimensions of $1.495\mu\text{m} \times 0.3825\mu\text{m} = 0.5718375\mu\text{m}^2$, successfully passing all DRC and LVS tests.Developed layouts for the sense amplifier, write circuit, and precharging circuit to ensure functionality and integration.Optimized energy consumption, achieving $34.31\mu\text{W}$ (schematic) and $45\mu\text{W}$ (layout) for complete read/write operations of the 16-bit SRAM, equivalent to $2.14\mu\text{W}$ and $2.81\mu\text{W}$ per single-bit read/write.	March 2024

Leadership

VP Society of Hispanic Professional Engineers (SHPE) FAU	August 2022 – August 2023
Marketing Chair Machine Perception Cognition Robotics Lab (MPCR) FAU	August 2022 – August 2023