GIOVANNI MICHEL

Computer & Electrical Engineer

U.S. Citizen | Willing to relocate

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EDUCATION

Master of Science in Electrical Engineering **Cumulative GPA: 3.5**
Northwestern University, Evanston, IL. Graduation date: June 2025

Master of Science in Artificial Intelligence **Cumulative GPA: 3.8**
Florida Atlantic University, Boca Raton, FL. Graduation date: August 2023

Bachelor of Science in Computer Engineering **Cumulative GPA: 3.4**
Florida Atlantic University, Boca Raton, FL. Graduation date: August 2022

TECHNICAL SKILLS

Programming Languages: C/C++, C#, SQL, HTML, Python, VHDL, SystemVerilog, VLSI, PSpice, JavaScript, CUDA
Tools & Technologies: ROS/ROS2, Cadence Virtuoso, Genus, Quartus, FreeRTOS, Nsight Systems, SLAM
Controllers: TI MSP430, STM32, Raspberry Pi, Nexys4 DDR FPGA, ESP32

EXPERIENCE

Graduate Research Assistant, Los Alamos National Laboratory | Los Alamos, NM **August 2022 – June 2025**

- Developed a sparse-coding algorithm in Python for Q-Learning; trained a Python-based neural network to balance an inverted pendulum on robotic cart, then deployed the learned weights onto a neuromorphic FPGA using a two-layer spiking neural network —demonstrating equivalent real-time performance and proof of concept for neuromorphic Machine Learning algorithms.
- Built a modular Python framework for on-chip learning for neuromorphic Machine Learning, enabling simulation, and rapid prototyping of spiking neural networks.
- Designed a learning algorithm for training and validating spiking neural networks in reinforcement learning and control by implementing a Software-In-The-Loop (SITL) framework to interact with OpenAI Gym.

Software Engineer (Internship), Los Alamos National Laboratory | Los Alamos, NM **May 2022 – August 2022**

- Built the Data Science Infrastructure (DSI) prototype for the Common Model Framework (CMF) – designed a SQL-backed schema that captures simulation, filesystem, and performance metadata, turning multi-day HPC runs into a searchable, permanent knowledge database for analysis and visualization.
- Built a full-stack analytics layer for CMF—authored and optimized backend APIs/SQL for in-database analytics, dataset comparison, and metadata visualizations, and developed interactive browser dashboards (with a parallel-coordinates viewer) that let scientists explore results in real time, eliminating manual post-processing.
- Evaluated GUI front ends and set reproducibility standards – benchmarked ModelDB, Apache Superset, Trame and MLflow, and defined logging of parameters, code versions and environment configs to guarantee experiment repeatability and secure collaboration.

Software Engineer (Internship), GRUBBRR | Boca Raton, FL **September 2021 – February 2022**

- Optimized previous QA processes by 30%, by writing custom Java code to automate red team testing for Android kiosk products which lead to increased efficiency in product testing and design from idea to product releases. Followed CI/CD software development with version control.
- Performed QA automation for unit and functional tests assigned by Project Management, ensuring product quality and reliability.
- Contributed to onsite coordination, progress tracking, planning, closeout, and quality control to support project development.
- Collaborated with client integration teams to engage in insightful discussions. Tracked and raised issues along product life cycle through Jira using Scrum and Agile methodologies.

Relevant Projects

NFC Wireless Temperature Sensor| VLSI Group Project **June 2024**

- Designed schematics for an integrated circuit (IC) to convert analog temperature input into digital output, powered via Near Field Communication (NFC).
- Designed schematics and testbenches for key components, including a temperature sensor, low-dropout regulators, power rectifier, and demodulation rectifier.
- Engineered and validated a power-harvesting component, creating multistage rectifiers integrated with a bandgap reference circuit to generate a stable signal.

4x4 6T SRAM| VLSI Project **March 2024**

- Designed schematics and testbench for a 4x4 6T SRAM array, including sense amplifiers, bit-line pre-charge, and write circuits for each column.
- Created a 6T SRAM layout with dimensions of 1.495µm x 0.3825µm = 0.5718375µm², successfully passing all DRC and LVS tests.
- Developed layouts for the sense amplifier, write circuit, and bit-line pre-charge circuit to ensure functionality and integration.
- Optimized energy consumption, achieving 34.31µW (schematic) and 45µW (layout) for complete read/write operations of the 16-bit SRAM, equivalent to 2.14µW and 2.81µW per single-bit read/write.

Digilent Nexys 4 DDR FPGA Projects with VHDL | Design of Digital Systems **May 2022**

- Built Register Files with 8 and 16 registers on Xilinx Vivado.
- Built an ALU and a Parameterized Carry Save Multiplier on Xilinx Vivado.
- Built a Vending Machine Subsystem using a Finite State Machine and Arithmetic State Machine on Xilinx Vivado.
- Conducted research for different ASICs, FPGAs, BIST, Timing Analysis, and Critical Path related to VHDL FPGA design.