

GIOVANNI MICHEL

ELECTRICAL AND COMPUTER ENGINEERING

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Education

Master of Science Electrical and Computer Engineering **Cumulative GPA: 3.4**
Northwestern University, Evanston, IL. Graduation date: August 2025

Master of Science in Artificial Intelligence **Cumulative GPA: 3.8**
Florida Atlantic University, Boca Raton, FL. Graduation date: August 2023

Bachelor of Science in Computer Engineering **Cumulative GPA: 3.2**
Florida Atlantic University, Boca Raton, FL. Graduation date: August 2022

Technical Skills

Programming Languages: C/C++, C#, MATLAB, Simulink, Python, VHDL, Verilog, VLSI, PSPICE, Cadence Virtuoso, Quartus
Tools & Technologies: ROS, Microsoft Office Suite (Word, Excel, PowerPoint), Oscilloscopes, DMM, Soldering, PCB Design, Linux, Cryogenics Cryostat, Machine Learning, Mixed Signal Design, Data Analysis

Professional Experience

Graduate Research Assistant, Los Alamos National Laboratory | Los Alamos, NM **April 2022 – Present Day**
Engage in Research, Design and Development for Spiking Neural Networks on Neuromorphic Architectures on Intel Loihi FPGA.

- Designed, developed, and test software for spiking neural networks, for various Machine Learning mission critical applications.
- Designed neuronal circuit for implementation of RL algorithms to solve cartpole balancing problem.
<https://github.com/GiovanniThysMichel/SNN-for-RL-with-LANL>
- Designed and implemented encoding methods for SNN on Intel Loihi FPGA.

Undergraduate Research Assistant, Connected Autonomy Lab at FAU | Boca Raton, FL **December 2021 – April 2022**
Worked with Connected Autonomy lab to develop Wireless Navigation Algorithms for autonomous robots and drones.

- Designed and implemented machine learning algorithms for integration with ROS robots for wireless navigation.
- Collaborated with cross-functional teams to meet NSF deadlines and requirements. Worked with PhD students to contribute to publications for wireless navigation.

Software Engineer (Internship), GRUBBRR | Boca Raton, FL **September 2021 – February 2022**
Responsible for performing Q&A automation duties for unit test and functional test assigned by Project Management.

- Implemented standardized processes for Q&A group, which lead to efficient product testing for and design of end-to-end product release.
- Engage in onsite coordination, progress, planning, closeout, & quality control to add support to project development.
- Led teams for client integrations using technical communications skills, Scrum, and Agile methodologies.

Lab Assistant, Florida Atlantic University | Boca Raton, FL **October 2020 – August 2021**
Responsible for packaging and distributing Lab kits for College of Engineering and Computer Science. Worked with Professors and building managers to meet deadlines.

- Engage with students and professors for scheduling events, managing inventory, and lab supplies.
- Performed System troubleshooting for oscilloscopes, power supplies, DMMs, various controllers and microprocessors.

Relevant Projects

Cadence Virtuoso Projects | CMOS VLSI **March 2024**
Designed a 4x4 SRAM array with 6T SRAM cells, simulated waveforms of critical wires, including word-line, bit-lines, clocks, and output signals.
both schematic and layout.

- Designed testbench, schematic and layout for 4x4 SRAM array.
- Built Bitline conditioning, built differential pair sense amplifiers to perform read and write operations for column multiplexing.
- Passed DRC, LVS test, and total area of 1.8um.

Autonomous Robot Manipulator | Undergraduate Senior Design Project **May 2022**

- Integration between Raspberry Pi and Arduino Mega for robotic car and robotic arm that would pick and place water bottles and cans.
- Developed obstacle avoidance and autonomous navigation algorithm using LIDAR, IMU, and ROS for navigating and avoiding obstacles while navigating to user dependent locations.

Digilent Nexys 4 DDR FPGA Projects with VHDL | Design of Digital Systems **May 2022**
Learned about different ASIC, FPGAs, BIST, Timing Analysis, and different architectures for VHDL FPGA design.

- Built Register Files with 8 and 16 registers on Xilinx Vivado.
- Built an ALU and a Parameterized Carry Save Multiplier on Xilinx Vivado
- Built a Vending Machine Subsystem using a Finite State Machine and Arithmetic State Machine on Xilinx Vivado.

Leadership

VP Society of Hispanic Professional Engineers (SHPE) | FAU **August 2022 – August 2023**
Marketing Chair Machine Perception Cognition Robotics Lab (MPCR) | FAU **August 2022 – August 2023**