GIOVANNI MICHEL

Electrical Engineering

US Citizen | Willing to relocate

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EDUCATION

Master of Science in Electrical Engineering **Cumulative GPA: 3.5**
Northwestern University, Evanston, IL. Graduation date: June 2025

Master of Science in Artificial Intelligence **Cumulative GPA: 3.8**
Florida Atlantic University, Boca Raton, FL. Graduation date: August 2023

Bachelor of Science in Computer Engineering **Cumulative GPA: 3.4**
Florida Atlantic University, Boca Raton, FL. Graduation date: August 2022

TECHNICAL SKILLS

Programming Languages: C/C++, MATLAB, Python, VHDL, System Verilog

Skills & Technologies: Neuromorphic Computing, Reinforcement Learning, Machine Learning, Deep Learning, Genus, Virtuoso, Quartus, PyTorch, ROS, Git, PCB Design, SolidWorks, Data Analysis, SR860-LOCKIN, Soldering, Digital Multimeter, Dilution refrigerator

PROFESSIONAL EXPERIENCE

Graduate Research Assistant, Los Alamos National Laboratory | Los Alamos, NM **April 2022 – June 2025**

Conduct research, design, and development towards training spiking networks on the Intel neuromorphic research processor, Loihi. ***Advised by Andrew Sornborger, Alpha Renner, and Gerd Kunde****.*

- Investigate reinforcement learning and deep reinforcement learning algorithm design for neuromorphic processors.
- Developed and implemented sparse encoding methods for physical dynamics in control theory to train spiking networks on neuromorphic systems.

Graduate Research Assistant, Grayson Group| Evanston, IL **December 2023 – February 2025**

Conduct experiments to model characteristics of Cryo-Thermoelectric MOSFET developed by Fermi Lab National Laboratory operating at ≈ 1.5K. ***Advised by Matthew Grayson and Davide Braga****.*

- Designed experiments to collect data from SR860-LOCKIN that was connected to a probe inserted into dilution refrigerator.
- Investigated the temperature dependence for drain current, threshold voltage, body well current, small signal transconductance, and body well current through meticulously designed experimental procedures.

Software Engineer (Internship), GRUBBRR | Boca Raton, FL **September 2021 – February 2022**

Performed QA automation for unit and functional tests assigned by Project Management, ensuring product quality and reliability.

- Implemented standardized QA processes, improving efficiency in product testing and the design of end-to-end product releases. Followed CI/CD software development with version control.
- Contributed to onsite coordination, progress tracking, planning, closeout, and quality control to support project development.
- Collaborate with client integration teams to engage in inciteful discussions. Tracked and raised issues along product life cycle through Jira using Scrum and Agile methodologies.

PUBLICATIONS | PEER REVIEWED

- **Michel, G**., Nesbit, S., Sornborger, A. (2024, December). Closed-loop Q-learning Control with Spiking Neuromorphic Network. LA-UR-24-32562. Association for Computing Machinery. **Paper**.
- **Michel, G**., Renner, A., Kunde, G., Sornborger, A. (2023, August). Towards Q-Learning-based control using a spiking neuromorphic network and sparse encoding. LA-UR-23-283336. Association for Computing Machinery. **Poster.**
- **Michel, G**., Pulido, J., Turton, T. (2022, August). Database Visualization for the Data Science Infrastructure Project. **Poster.**

RELEVANT PROJECTS

Cryo-Thermoelectric Modeling| Graduate Research Northwestern University **February 2025**

- Modeled cryogenic MOSFET operation from ≈4 K to 300 K: derived analytic expressions for the Fermi potential $\phi_F(T)$, scaling factor *n(T)*, threshold voltage $V_T(T)$, drain current $I_D(T)$ and others from sub-threshold-slope $SS(T)$ and depletion-capacitance $C_D(T)$ data.
- Reduced cryogenic MOSFET measurement time 5× by automating SR860-LOCKIN sweeps in Python.
- Collaborated with Fermi National Laboratory and Global Foundries for custom made low-t MOSFET.

NFC Wireless Temperature Sensor| VLSI Group Project **June 2024**

- Designed schematics for an integrated circuit (IC) to convert analog temperature input into digital output, powered via Near Field Communication (NFC).
- Designed schematics and testbenches for key components, including a temperature sensor, low-dropout regulators, power rectifier, and demodulation rectifier.
- Engineered and validated a power-harvesting component, creating multistage rectifiers integrated with a bandgap reference circuit to generate a stable signal.
- Gained expertise in RC response, impedance matching, and analog-to-digital converter (ADC) design through project implementation.

4x4 6T SRAM| VLSI Project **March 2024**

- Designed schematics and testbench for a 4x4 6T SRAM array, including sense amplifiers, bit line pre-charge, and write circuits for each column.
- Created a 6T SRAM layout with dimensions of 1.495µm x 0.3825µm = 0.5718375µm², successfully passing all DRC and LVS tests.
- Developed layouts for the sense amplifier, write circuit, and pre-charge circuit to ensure functionality and integration.
- Optimized energy consumption, achieving 34.31µW (schematic) and 45µW (layout) for complete read/write operations of the 16-bit SRAM, equivalent to 2.14µW and 2.81µW per single-bit read/write.