Depletion-Mode GaN HEMT Q-Spoil Switches for MRI Coils

Jonathan Y. Lu*, *Student Member, IEEE*, Thomas Grafendorfer, Tao Zhang, Shreyas Vasanawala, Fraser Robb, *Member, IEEE*, John M. Pauly, *Member, IEEE*, and Greig C. Scott, *Member, IEEE*

***Abstract*— Q-spoiling is the process of decoupling an MRI receive coil to protect the equipment and patient. Conventionally, Q-spoiling is performed using a PIN diode switch that draws significant current. In this work, a Q-spoiling technique using a depletion-mode Gallium Nitride HEMT device was developed for coil detuning at both 1.5 T and 3 T MRI. The circuits with conventional PIN diode Q-spoiling and the GaN HEMT device were implemented on surface coils. SNR was measured and compared for all surfaces coils. At both 1.5 T and 3 T, comparable SNR was achieved for all coils with the proposed technique and conventional Q-spoiling. The GaN HEMT device has significantly reduced the required power for Q-spoiling. The GaN HEMT device also provides useful safety features by detuning the coil when unpowered.**

***Index Terms*— Q-spoiling, GaN HEMT, depletion mode, receive coils.**

I. Introduction

Q-SPOILING is the process of decoupling and detuning an MRI receive coil during transmit mode to prevent induced currents that can compromise patient and equipment safety. Conventionally, Q-spoiling is performed using PIN diode switches [1], [2] which require high bias currents of 50 to 100 mA, though many other RF switch technologies exist [3]–[9]. PIN diode switches are often accompanied by passive crossed diodes [10]–[12] on the coil for additional safety. However, interest is growing in lightweight wearable arrays with optical or wireless data streaming. Present MRI receive chains can consume over 1 W per channel. A fully autonomous battery or wireless powered system will require lower power receive chains especially as the channel count of arrays rises. In addition, they must be safe for patients during unexpected power failures. Finding an alternative lower power replacement for PIN diodes would be an important first step toward realizing wearable and wireless arrays.

Manuscript received April 22, 2016; revised June 17, 2016; accepted June 25, 2016. Date of publication June 28, 2016; date of current version November 29, 2016. *Asterisk indicates corresponding author.*

*J. Y. Lu is with the Department of Electrical and Computer Engineering, Stanford University, Stanford, CA 94305 USA (e-mail: jonylu97@stanford.edu).

T. Grafendorfer is with Advanced Coils, GE Healthcare Inc., Stanford, CA 94305 USA.

T. Zhang, J. M. Pauly, and G. C. Scott are with the Department of Electrical and Computer Engineering, Stanford University, Stanford, CA 94305 USA.

S. Vasanawala is with the Department of Radiology, Stanford University, Stanford, CA 94305 USA.

F. Robb is with Advanced Coils, GE Healthcare Inc., Aurora, OH 44202 USA.

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TMI.2016.2586053

One possibility for the Q-spoiling switch is a field effect transistor (FET). Semiconductor technology has made great strides in high power FET devices with saturation currents exceeding several amperes while having small parasitic capacitance. Historically, Gallium Arsenide (GaA) devices [13], [14] have been commonplace as RF switches but did not have adequate power handling for use as a Q-spoiling switch. Now, Gallium Nitride (GaN) devices [15]–[18] offer the higher current, and lower on-resistance and off-capacitance requirements needed for power RF switches [19]–[29].

Though FET RF switches for MRI Q-spoiling have been proposed [30], [31], they were only recently demonstrated for 1.5 T with enhancement mode GaN (eGaN) FETs [32], [33] but these devices have a large off-capacitance (42 pF), which leads to greater circuit complexity and performance degradation at 3 T. Second, enhancement-mode devices do not perform Q-spoiling when the device is unpowered, creating safety concerns during power faults. Q-spoiling has also been demonstrated using MEMs switches [34]–[38], but these devices have limited commercial availability and require additional DC-DC boost converters to reach the 70-80 V control voltages. Phase-change Germanium Telluride (GeTe) switches [39], [40] are another up-and-coming technology. While promising, GeTe switches require improvements in speed, reliability, and availability.

In this work, we propose depletion-mode GaN FET Q-spoil switches, extending upon our initial efforts [41], [42]. We demonstrate 1.5 T and 3 T GaN High-Electron-Mobility Transistor (HEMT) based Q-spoiling circuits for surface coil loops using microwave power HEMT devices of three different power handling capabilities. The blocking impedances of these Q-spoiling circuits are compared with conventional PIN diode Q-spoiling circuits. SNR performance of these low power Q-spoiling surface coils is also compared with conventional PIN diode and crossed diode Q-spoiling coils. In addition, the image artifacts of the unpowered coils, mimicking power faults, are explored.

II. Q-Spoiling Tank

In MRI, Q-spoiling activates a parallel LC resonant tank within the receive loop using a switch in series with an inductor. This combination is then placed in parallel with a capacitor (Fig. 1). The quality factor of the LC circuit determines the blocking impedance of the tank. This blocking impedance reduces the induced current at a narrowband

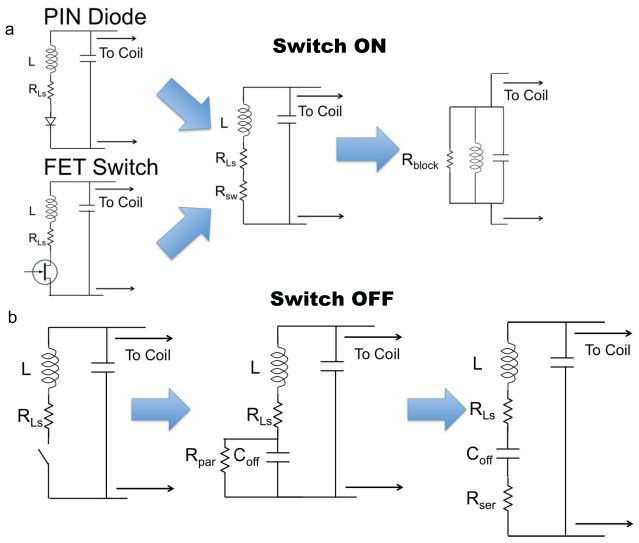

Fig. 1. Q-spoiling using PIN diode and FET switch. The FET switch is voltage actuated, and the PIN diode current actuated. The inductor and switch on-resistance limit the blocking impedance of the tank. In the off state, the parasitic off-resistance contributes small losses to the resonating coil capacitor.

frequency within the receive loop during transmit, preventing Q-spoiling artifacts in images while protecting the patient and the coil components. Insufficient blocking impedance may result in significant transmit B1 distortion near the receive coil, altering the intended flip angle of the pulse sequence [43], [44]. During receive mode, the switch is off and can be modelled as a capacitor and an equivalent large parallel resistance. As long as C_{off} is small relative to the coil capacitor (e.g. 10x), the equivalent parallel resistance adds a minor loss to the coil resulting in a small degradation in image SNR.

The switch (PIN or FET) must support a high circulating current in the tank circuit during transmit mode. This will require RF power FET devices having high drain saturation current I_{dss}. By Faraday's law, the induced EMF, and therefore induced current in the receive coil, is directly proportional to the coil area A, the B_1 pulse amplitude, and the Larmor frequency ω, as

$$V = \frac{d(A|B_1|e^{j\omega t})}{dt} = j\omega e^{j\omega t} A|B_1| \quad (1)$$

$$|V| = \omega A|B_1|. \quad (2)$$

For example, using a loop coil of area 150 cm^2, and B_1 magnitude of 20 μT at 1.5 T ($\omega = 4 \times 10^8$ rad/s), the loop EMF reaches 120 V. If the blocking impedance reached 5 $k\Omega$, and tank Q were 100, the current in the main coil would only be 24 mA by Ohm's law, but the RF current circulating in the tank is Q-multiplied yielding 2.4 A! At 3 T MRI, the tank current would double to 4.8 A for similar blocking impedances, peak B_1 and Q.

Thus, if we were to insert a FET device in a Q-spoiling circuit, it must be able to handle several Amperes of RF current. Figure 2 shows an IV curve acquired for a 25 W GaN FET device. The FET "safe operating zone" of the IV curve is the high slope region, indicating a small resistance. Outside this region, the drain current begins to saturate. The switch

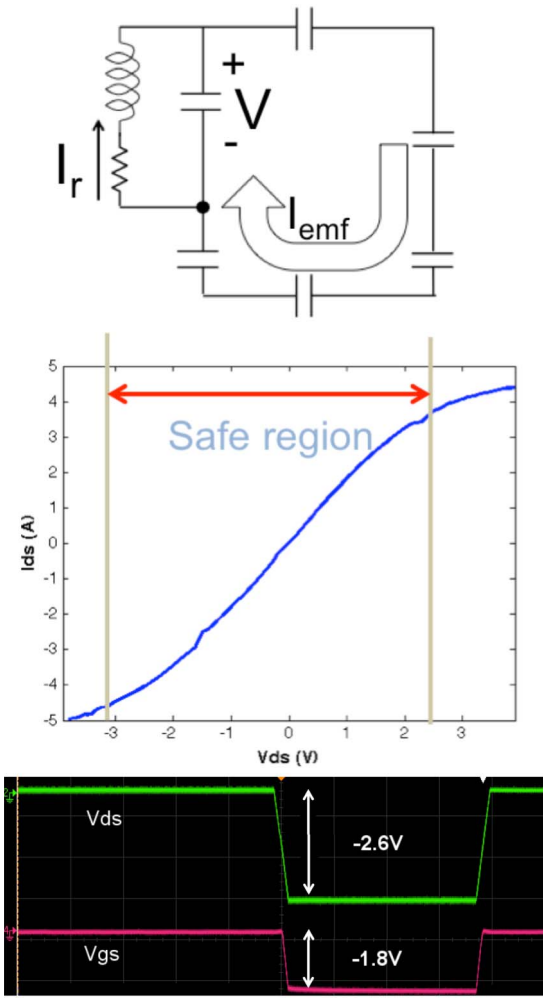

Fig. 2. Top: An induced EMF causes high current to flow through the FET switch. Middle: The FET switch must operate within a designated safe zone of its IV curve to continually function as a closed switch (low resistance). Bottom: When the voltage of the drain swings negative (V_{ds}), the gate (V_{gs}) will track the drain.

no longer acts like a small resistance, and the device fails to perform Q-spoiling. If the current approaches saturation, the drain-to-source voltage V_{ds} can now swing to large values. For a negative swing, the gate to drain diode will forward bias, and the FET gate will track the drain leading to a breakdown [45], [46] between the gate-source junction in devices with low V_{gs} limit. Therefore, it is important to select a device of sufficient size to avoid excursions into current saturation during the induced EMF levels from the transmit field.

III. FET Switch Size for Power Levels

FET Q-spoiling belongs to the class of low voltage control switched LC resonant tank circuits [47], [48]. We tested three depletion-mode GaN HEMT devices from Cree: a CGHV1J025D (25 W, DC-18GHz), a CGHV60040D (40 W, DC-6GHz), and a CGHV60075D (75 W, DC-6GHz), each with its stated saturated power limit and maximum operating frequency. Table I outlines select parameters according to the data-sheets and our own measurements. These devices all

TABLE I
DIFFERENT FET DEVICES AND DATASHEET VALUES FOR SELECT PARAMETERS

	EPC8004 [33]	PIN -15V, 30/100mA	CGHV1J025D (25 W)	CGHV60040D (40 W)	CGHV60075D (75 W)
V_{ds} breakdown (V)	48	-100	100	150	150
I_{DSS} (A)	>7.5	-	3.8	4.2	8
R_{on} (Ω)	0.08-0.11	0.4/0.15	0.6	0.56	0.28
$C_{off}(V_{ds} = 0)$ (pF)	42	1.9	3.1	3.5	7.05
V_{to} (V)	1.4	-	-3.8	-3.8	-3.8
FOM = $R_{on} \cdot C_{off}$ ($\Omega \cdot$ pF)	3.36-4.62	0.76/0.29	1.86	1.96	1.974

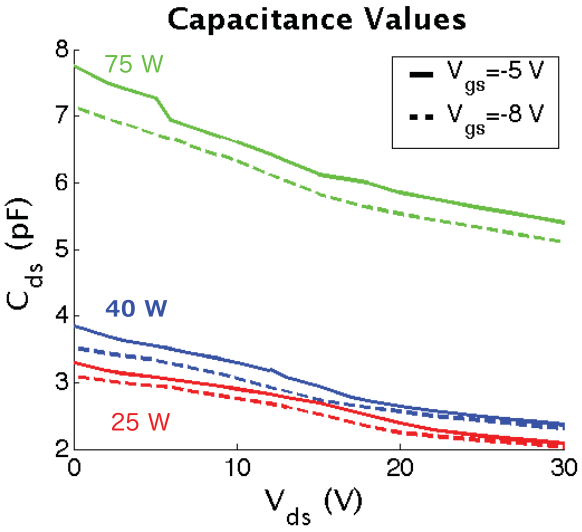

Fig. 3. The drain-to-source off-capacitance for the 25 W, 40 W, and 75 W FET devices at -5 V (solid) and -8 V (dashed) bias.

supported the expected peak circulating currents of several amperes in a Q-spoil tank circuit. A larger device has higher current limit and smaller on-resistance, but also larger off-capacitance that could alter the tuned frequency of the coil. FET switches are compared by the figure-of-merit (FOM) product [23]:

$$FOM = R_{on} \cdot C_{off} \tag{3}$$

with lower FOM being superior.

A second concern is the device off-capacitance behavior near zero drain-to-source and gate-to-source voltage. The datasheets listed C_{off} for amplifier conditions of $V_{gs} = -8$ V and $V_{ds} = 50$ V, as 1.2 pF, 1.6 pF, and 3.2 pF for the 25 W, 40 W, and 75 W parts respectively. However, the capacitance at 0 V_{ds} is more relevant for a Q-spoil switch. The off-capacitance of each device was measured as a function of applied voltage using a network analyzer. Figure 3 shows that off-capacitance values are higher with 0 V applied across the drain and source. For $V_{gs} = -8$ V, and $V_{ds} = 0$ V, the 25 W part is approximately 3.1 pF; the 40 W FET is approximately 3.5 pF; and the 75 W FET is 7.05 pF. Based on device capacitance and the $R_{on} \cdot C_{off}$ figure of merit, the depletion-mode GaN HEMT devices have better performance than the enhancement mode eGaN FETs used in [32], [33].

IV. BIASING CIRCUITRY FOR FET SWITCH

The depletion mode GaN FET bias for Q-spoiling (Fig. 4) can be performed in two ways: adjust the gate voltage and fix the source voltage, or fix the gate voltage and bias the FET source. With minor modifications, both schemes were implemented using the GE Signa RX coil bias which imposes −15 V during receive mode and +5 V during transmit mode. The source-biased configuration (Fig. 4 c) enables coil reception with a positive voltage and disables (Q spoils) with 0 volts which is well suited for single supply (e.g. battery) operation. However, for its demonstration in-bore, an auxilliary bias supply and BJT were inserted to act as a voltage/logic inverter. A diode is placed at the base of the BJT for protection. When a positive voltage is applied to the base, the collector voltage of the BJT goes low, leaving the FET switch on and activating Q-spoiling. When a negative voltage is applied to the base of the BJT, the collector of the BJT is pulled high to the source voltage level and creates a negative gate-to-source voltage across the FET to place the coil into receive mode.

The second FET bias scheme applies RX control voltage directly to the gate of the FET (Fig. 4 d). Depending on the control voltage of the scanner, one can create a voltage divider such that −5 V is applied between the FET gate and source to switch it off during receive mode. When a positive voltage is applied during transmit mode, the FET is on and Q-spoiling is activated. In fact, the gate-source diode will be slightly forward biased which could further lower the switch resistance [28]. This bias scheme is ideal for scanners that apply a negative coil bias to enable receive. Importantly, for both schemes, the FET switches would be on by default during a power or cable interruption, and Q-spoiling would occur. This provides an inherent safety benefit.

V. MATERIALS AND METHODS

A. Q-Spoiling Schematics and Coil Construction

We constructed identical coils on printed circuit board (PCB) for 1.5 T and 3 T with different Q-spoiling circuits for comparison. Each coil was approximately 11 cm by 14 cm including chamfered corners, with loop areas of 146 cm^2. For 1.5 T, we implemented the following Q-spoil circuits: conventional active PIN diode Q-spoiling (Fig. 4 a), crossed diode Q-spoiling (Fig. 4 b), 25 W FET Q-spoiling with the "source-controlled configuration" (Fig. 4 c) and finally 25 W, 40 W and 75 W FET Q-spoiling with the "gate-controlled configuration" (Fig. 4 d). For 3 T, only the PIN scheme

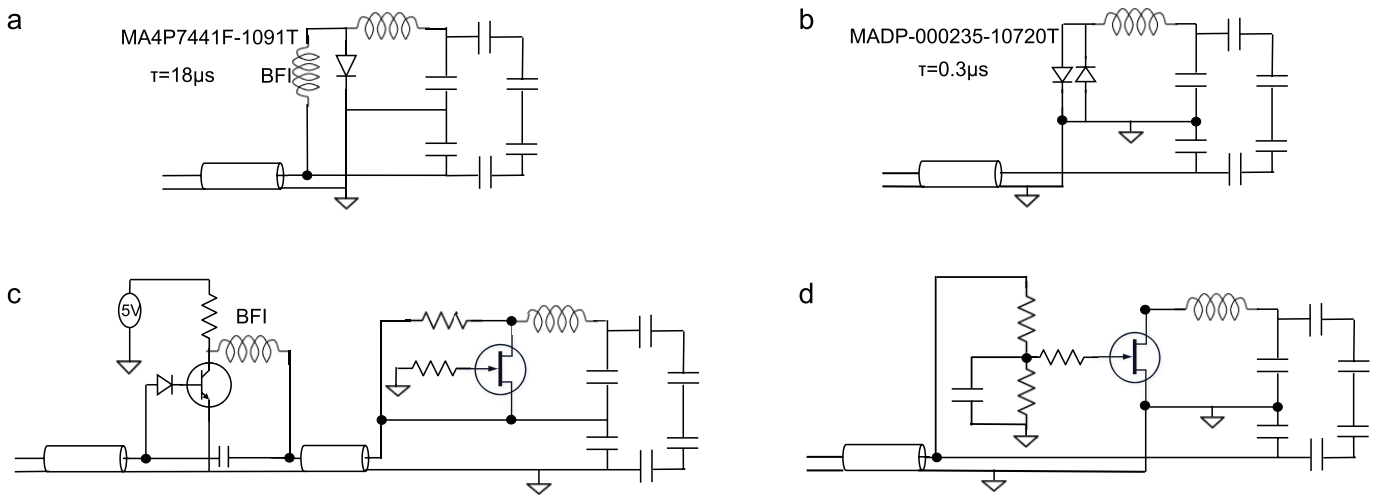

Fig. 4. Schematics showing (a) PIN Diode Q-spoiling (b) Cross Diode Q-Spoiling (c) Source-Controlled FET Q-spoiling (d) Gate-Controlled FET Q-spoiling.

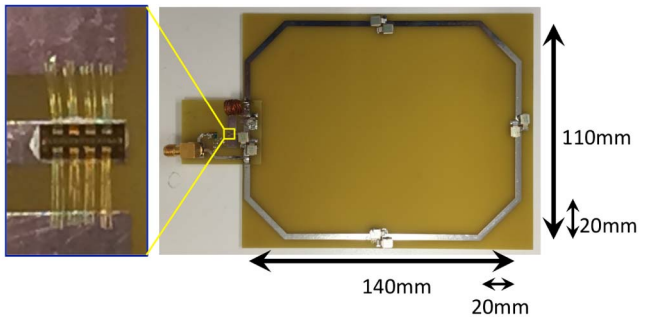

Fig. 5. Magnified picture the 25 W HEMT die (left) on our PCB fabricated coil (right).

and gate-controlled FET biases were constructed. Since all packaged parts sold by Cree were magnetic, the parts were purchased in die form and gold wire bonded in-house onto the PCB boards (Fig. 5).

The PIN diode Q-spoiling employed the Macom MA4P7441F-1091T (max 0.5 Ω, 0.15 Ω typ. at 100 mA) (Fig. 4 a). The crossed diode passive blocking (Fig. 4 b) [10]–[12] employed faster switching diodes (MADP-000235-10720T) to activate the LC tank. This passive decoupling is commonly built in as a safety precaution for most receive coils but alone is known to be susceptible to certain artifacts in MRI scans if the diodes do not turn on completely [49]. For FET bias schematic (Fig. 4 c), a control voltage of 0 or +5 V is applied to the source of the HEMT device. This required the additional BJT bias circuit in front. The bias schematic of Fig. 4 d uses a voltage divider with resistor values of 5 kΩ and 10 kΩ to convert the +5/-15V control voltages from the MRI scanner to +1.8/-5V at the gate of the HEMT device (the gate is slightly forward biased by a diode drop in transmit mode). Since the FET is biased on during high RF power intervals, the low drain-source impedance prevents high RF voltages at the device terminals, unless Idsat is approached. A bypass capacitor was added in the resistive divider to short high frequency signals coupling indirectly to the gate, although this increases the RC switch time constant. An additional 10 kΩ resistor was placed at the FET gate for current limiting protection and to provide dc control source isolation [50].

B. Impedance Blocking Measurements

For the 1.5 T coil prototypes, the blocking circuit employed a nominal 43 pF capacitor in parallel with a 130 nH inductor. The 3 T prototypes used a nominal 10 pF in parallel with 140 nH inductance. We tuned and matched our loaded coils to similar impedances and $|S_{11}|$ quantities. We matched the loaded coils to $|S_{11}| \leq -20$ dB. We maintained consistency in $|S_{11}|$ value between coils within the same SNR comparison scan test. We then performed bench top measurement to examine the blocking impedance of the PIN diode Q-spoiling circuit as a function of DC bias current to compare with our FET coils. Using analyses from previous works [43], [44], we calculated that we need 2.3 kΩ to achieve a maximum of 5% transmit B1 perturbation with our coils at 1.5 T, and at least 4.7 kΩ to achieve a maximum of 5% distortion at 3 T. In Eqn. (4), A is the area of the coil, and f_0 is the Larmor frequency.

$$\frac{|Z_{blocking}|}{A\,[cm^2]} \approx \frac{1}{4} f_0[MHz] \tag{4}$$

The impedance blocking measurements of the PIN diode 1.5 T and 3 T Q-spoiling circuit were made in a lab bench-top setting using an HP network analyzer E5071C (Keysight Technologies, Santa Clara, CA, USA) while adjusting the PIN diode bias current from a power supply. Similar blocking impedance measurements were made with the FET Q-spoil circuits.

C. Q-Measurements for 1.5 T Coils

We measured the loaded and unloaded Q values for a 1.5 T coil with no switch, the PIN diode coil, and the three FET (25 W, 40 W, 75 W) coils. For the unloaded Q measurement, we applied a battery control voltage to the coil to turn the switch off, and probed the coil using an overlapped sniffer

loop pair connected to the HP E5071C network analyzer. This measurement gives an understanding of the off-switch resistive loss contributions for the FET devices compared with the PIN diodes. Resistive chokes (100 $k\Omega$) were added to decouple the impedance of the battery from affecting the Q measurement for the PIN diode coil. To perform the same measurement with the FET coils without altering the control bias voltage of the resistor divider, the receive line was opened between the FET bias resistors and the input matching capacitor. The battery voltage was then directly applied to the resistor divider. For the loaded Q measurement, we continued the same procedure while loading the coils with the phantom. The unloaded-to-loaded Q ratios were also calculated.

D. SNR Comparison Studies

1) FET Gate Versus Source Biasing at 1.5 T: The source-control bias (Fig. 4 c) and gate-control bias (Fig. 4 d) schemes were tested for SNR differences using the 25 W GaN FET in two coils at 1.5 T. Scans were performed using a 1.5 T GE system (GE Healthcare, Waukesha, Wisconsin, USA). The experimental surface coils were placed underneath a 26.5 cm by 20 cm by 7 cm deep Copper-Sulfate doped saline gel phantom. We performed FSE scans (TR= 450 ms, TE= 15 ms, BW= $\pm$15.63 kHz, FOV = 20 cm x 20 cm, 4 echoes) for comparison. Cable traps were inserted in the BJT supply path for the source scheme to insure common mode RF did not impact SNR and tuning. These schemes ultimately yielded similar SNR, hence subsequent tests employed only the "gate-controlled" configurations.

2) FET Versus Diode Q-Spoiling at 1.5 T: The FET coils, built with the "gate-controlled" bias (Fig. 4 d) for the 25 W, 40 W, and 75 W devices were compared to the diode Q-spoiled coils. Here we examined the impact of different blocking impedances and parasitic capacitances on the coil performance. Two different pulse sequences were performed: a gradient echo sequence (GRE) scan for 60° flip angles (TR= 50 ms, TE= 3.2 ms, BW= $\pm$31.25 kHz, FOV= 20 cm x 20 cm) and a fast spin echo (FSE) scan (TR= 500 ms, TE= 12 ms, BW= $\pm$15.63 kHz, FOV= 20 cm x 20 cm, 4 echoes) to compare SNR and artifacts. A GRE 60° demonstrates an average imaging sequence while the high-power FSE sequence tests the robustness of the FET devices in the Q-spoiled circuit and their current handling capability. We ensured that the coils and phantom were placed in identical positions.

3) Comparing FET Coils at 3 T: As a final test, the FET based Q-spoiling circuits were tested on surface coils tuned to 127.7 MHz for use in a GE 3 T Scanner (GE Healthcare, Wakesha, Wisconsin, USA). This determined whether the parasitic off-capacitance of the GaN FETs degrade the performance of the coils relative to conventional Q-spoiling methods at higher fields. In addition, the larger static magnetic field will double the EMF compared to 1.5 T for similar peak B_1. A set of coils were constructed: a conventional PIN diode coil, and FET based coils with gate-controlled bias (25 W, 40 W, and 75 W) and identical coil dimensions (140 mm by 110 mm) as with the 1.5 T case. These coils were then tuned and matched to have similar loaded coil $|S_{11}|$ return loss.

The phantom used for the scans was doped with both Nickel Chloride and Sodium Chloride and had dimensions of 15.5 cm x 15.9 cm x 37.5 cm. The single loop coils were placed underneath the phantom for SNR comparisons. We performed a GRE sequence of 60° flip angle (TR= 70 ms, TE= 4.0 ms, BW= $\pm$15.63 kHz, FOV= 24 cm x 24 cm) and a FSE sequence (TR= 500 ms, TE= 10 ms, BW= $\pm$15.63 kHz, FOV= 24 cm x 24 cm, 4 echoes). With each of the scan experiments, we aimed to maximize consistency in the hardware receive gain settings and phantom position between the different coils of that experiment.

E. Q-Spoil Power Fault Performance

A final experiment was performed to demonstrate Q-spoiling performance in case of a power fault. A scan was performed at 1.5 T with the conventional PIN coil connected to the scanner receive port. A second unpowered coil overlapped the PIN diode coil and the coil artifacts were observed in the scan. The coil conductor and saline were separated by only 5 mm to enhance any possible artifacts. For the unpowered coil, five different coils were substituted: a coil with no Q-spoiling, a coil with conventional PIN diode Q-spoiling, a coil with cross diode Q-spoiling, and 25 W source-controlled and gate-controlled FET coils. GRE images of 60° flip angle (TR= 50 ms, TE= 3.2 ms, BW= $\pm$31.25 kHz, FOV= 26 cm x 26 cm) were acquired.

VI. Results

A. Impedance Blocking Measurements

As expected, for the 1.5 T coils, higher blocking impedance was achieved with higher-power parts since larger devices have smaller on-resistance. The measured blocking impedances of the 1.5 T Q-spoiling circuits were 3.44 kΩ, 3.57 kΩ, and 4.9 kΩ for the 25 W, 40 W and 75 W FET parts respectively. These values were above the required 2.3 kΩ blocking impedance target, but are small signal values. To achieve equivalent blocking impedances of the 25 W, 40 W and 75 W parts using the PIN diode, we needed to supply 26 mA, 28 mA, and 70 mA respectively. At 100 mA, which matches the scanner coil bias, the blocking impedance reached 5.4 kΩ on the bench. At this bias, the MAP7441F-1091 PIN diode is rated at 0.5 Ω worst-case (0.15 Ω typical), and inductor Q likely limits the impedance.

For the 3 T Q-spoiling circuits, the measured blocking impedances were 5.8 kΩ, 5.9 kΩ, and 6.5 kΩ for the 25 W, 40 W, and 75 W circuits respectively, which were above the required 4.7 kΩ target. To achieve this with the PIN diode, we required 34 mA, 40 mA, and 76 mA respectively. With 100 mA bias current, the PIN diode blocking impedance reached 6.7 kΩ.

B. 1.5 T Loaded and Unloaded Coil Q Measurements

The unloaded Q of the coil with no switch had the highest Q of 319. The PIN diode coil and 40 W FET switch coil had

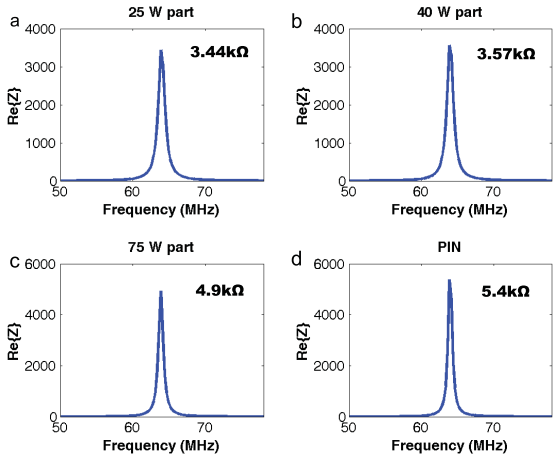

Fig. 6. Measured blocking impedances for the 1.5 T Q-spoiling circuits. The peaks of these plots are our measured blocking impedances. 3 T blocking impedances were measured by similar method, but their peaks shifted to 127.7 MHz.

TABLE II

UNLOADED AND LOADED Q VALUES AND RATIO FOR A COIL WITH NO SWITCH, THE PIN DIODE COIL, AND THE THREE FET COILS

	No Sw	PIN	25W FET	40W FET	75W FET
Q_u	319	298	260	292	276
Q_l	18.2	17.8	17.7	17.9	18.1
$\frac{Q_u}{Q_l}$	17.5	16.7	14.7	16.3	15.2

almost identical Q values greater than 290. The remaining FET switch coils had Q values greater than 260. The unloaded-to-loaded Q ratios of the different coils are all higher than 14 indicating large coupling between the coil and the samples (Table II).

C. 1.5 T Scan Tests: Impedance Matching and SNR

For the five different coils tested, we measured an $|S_{11}| \leq -20\,\text{dB}$. We ensured that the coils were placed at the same consistent location between the experiments. SNR comparisons are provided in Fig. 8 using box regions of Fig. 7. SNR quantities are averaged across two trials. In the GRE 60° sequence scans, the lower power 25 W FET, 40 W FET, and 75 W FET coils had a 0.2-0.4 dB SNR improvement over the PIN diode coil. The crossed diode coil had the same performance as the 25 W FET coil. During the FSE exams, the PIN diode and crossed diode coils had the same SNR performance and had a 0.4 dB improvement over the 25 W FET coil. The 40 W FET and 75 W FET coils had a 0.2-0.3 dB improvement over the PIN diode and crossed diode coils.

D. 1.5 T Scan Tests: FET Coil Bias Comparison

A similar SNR test compared the 25 W FET devices implementing the gate or source controlled bias. This examined whether the biasing circuit in the front of the source-controlled FET coil caused degradation in SNR performance. The coils were tuned and matched before measuring $|S_{11}| = -22.2\,\text{dB}$ and $|S_{11}| = -23.4\,\text{dB}$ for

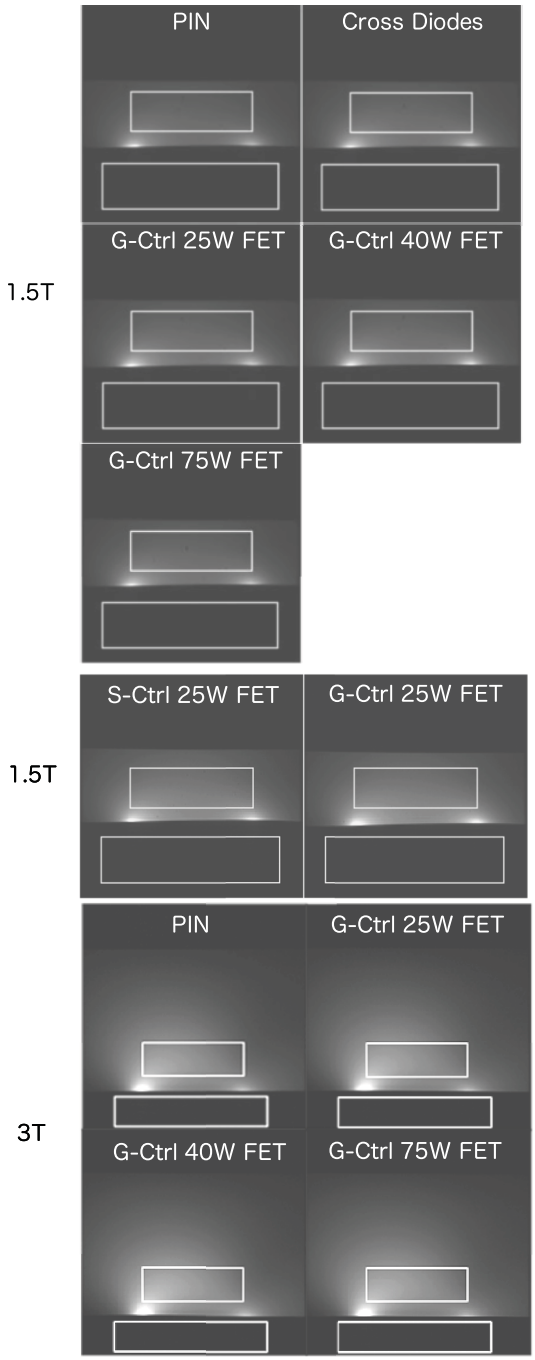

Fig. 7. Top: FSE images at 1.5 T. GRE sequence images look very similar. Middle: 1.5 T FSE Images between gate-controlled and source-controlled FET coil configurations. Both bias schemes yield similar performance in image quality and quantitative SNR. Bottom: FSE images at 3 T.

the gate-controlled and source-controlled FET configurations respectively (Fig. 7 middle row). The two trials yielded similar SNR performance to within 0.1dB, indicating both FET bias schemes provide comparable SNR performance.

E. SNR Comparison Tests at 3 T

The SNR results for the 3 T coils using PIN diode and 25, 40, and 75 W FETs are tabulated in Fig. 8 c. The loaded coil impedances achieved $|S_{11}| \leq -20\,\text{dB}$ in all cases. Since the field strength was now doubled, the induced EMF will be

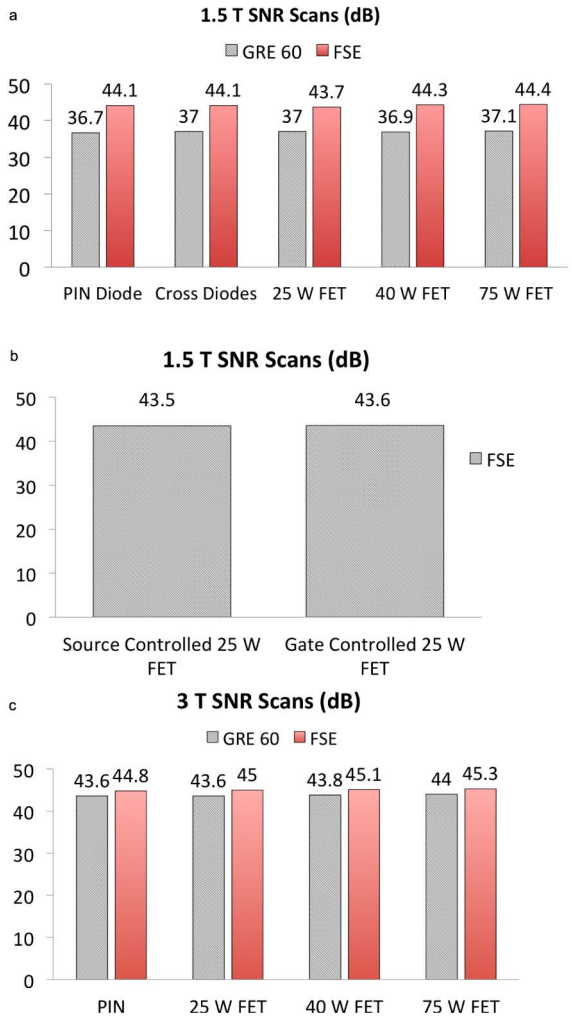

Fig. 8. SNR results from three different scan tests. The first two scan tests are at 1.5 T, and the third scan test is at 3 T.

double the 1.5 T value for the same pulse width and B_1 peak. The SNR was comparable for both GRE and FSE sequences. For the GRE 60°, the PIN diode and 25 W FET coil had the same SNR performance while the 40 W FET and 75 W FET coil were 0.2-0.4 dB higher. In the FSE scans, the 25 W part, 40 W part and 75 W part had at least 0.2 dB SNR improvement over the PIN diode coil. The FET coils themselves perform similarly and only slightly better than PIN diode coil. Overall, we conclude that that there is no noticeable degradation in SNR performance when using FET switches compared with the PIN diode switching in Q-spoiling.

F. Q-Spoil Power Fault Artifacts

Figure 9 shows the power fault overlay tests. When an unpowered coil overlaps a connected PIN diode coil, dark bands are generated by both the coil lacking Q-spoiling and the second disconnected PIN diode coil. On the other hand, these dark band artifacts are not present for the passive cross diode coils nor for the FET-based coils. One distinction between the passive cross diodes and the FET-based coils is that there is an inductively coupled bright sensitivity region above the cross diode coil while there is little sensitivity in the region above the FET-based coils.

VII. Discussions

The results demonstrate that depletion mode GaN FET HEMT devices are comparable to PIN diode Q-spoiling methods, yielding similar SNR values while consuming almost no power. The unloaded Q of the FET coils and PIN diode coils are comparable suggesting similar off-resistance switch values and low impact on SNR. In addition, the proximity between unloaded-to-loaded Q ratios of the PIN diode and FET coils indicate similar noise floor levels. Slight variations in SNR may be due to small mismatch differences and coil placement. Differences in SNR may also arise from the finite blocking impedances and slight tuning differences of the blocking networks. The latter can cause the phase of the residual coil current to differ with potential additive or subtractive effects, altering the scan profile. Lastly, local B1 changes can have a different impact on the SNR yields of GRE and FSE sequences.

PIN diode Q-spoil circuits still achieve somewhat larger blocking impedances at 100 mA bias, but in high channel count arrays, this can lead to substantial current drive, power consumption, and parasitic B_0 distortion near the diode DC bias chokes during transmit [30]. In contrast, depletion mode HEMT devices consume negligible power and current, and avoid bias chokes for resistors, which can greatly simplify bias distribution. Crossed diodes, while passive, leave all array elements active in receive but with the potential for unreliable isolation at low flip angles [49], whereas the FET biasing is robust over a wide range of flip angles and allows individual array elements to be selectively disabled during receive.

The FET switch operates much faster than PIN diodes which may benefit receiver recovery in ultra-short TE sequences. Typical PIN diode drive circuits allow switching times of 5-20 μs in most scanners though custom modifications can switch within 350 ns [51]. GaN HEMTs have switching speeds limited by the bias network resistors and gate input capacitance. In our case, we had included an RF bypass capacitor which slowed the RC switch time constant. If eliminated, FETs can theoretically switch at speeds of hundreds of nanoseconds without much optimization. Thus, FET switches show promise in applications that require imaging samples with short signal life times.

Q-spoiled blocking impedance measurements show that the series resistance of the inductor contributes along with the switch to determine blocking impedance of our Q-spoiling circuit. For example, with the 1.5 T tank circuit, an inductor Q of 160 was measured, corresponding to a series resistance of 0.4 Ω. With the tank circuit including the 25 W FET, the tank Q of 53 was observed, which corresponds to a blocking impedance of 3.37 kΩ. This value corresponded well with our measured blocking impedance.

An inherent advantage of the depletion-mode GaN HEMT device is its passive safety and bias flexibility. Without power, the device is fully conducting leaving the coil in it's Q-spoil state - a feature not possible with enhancement devices. Prostate coils are one example that would benefit

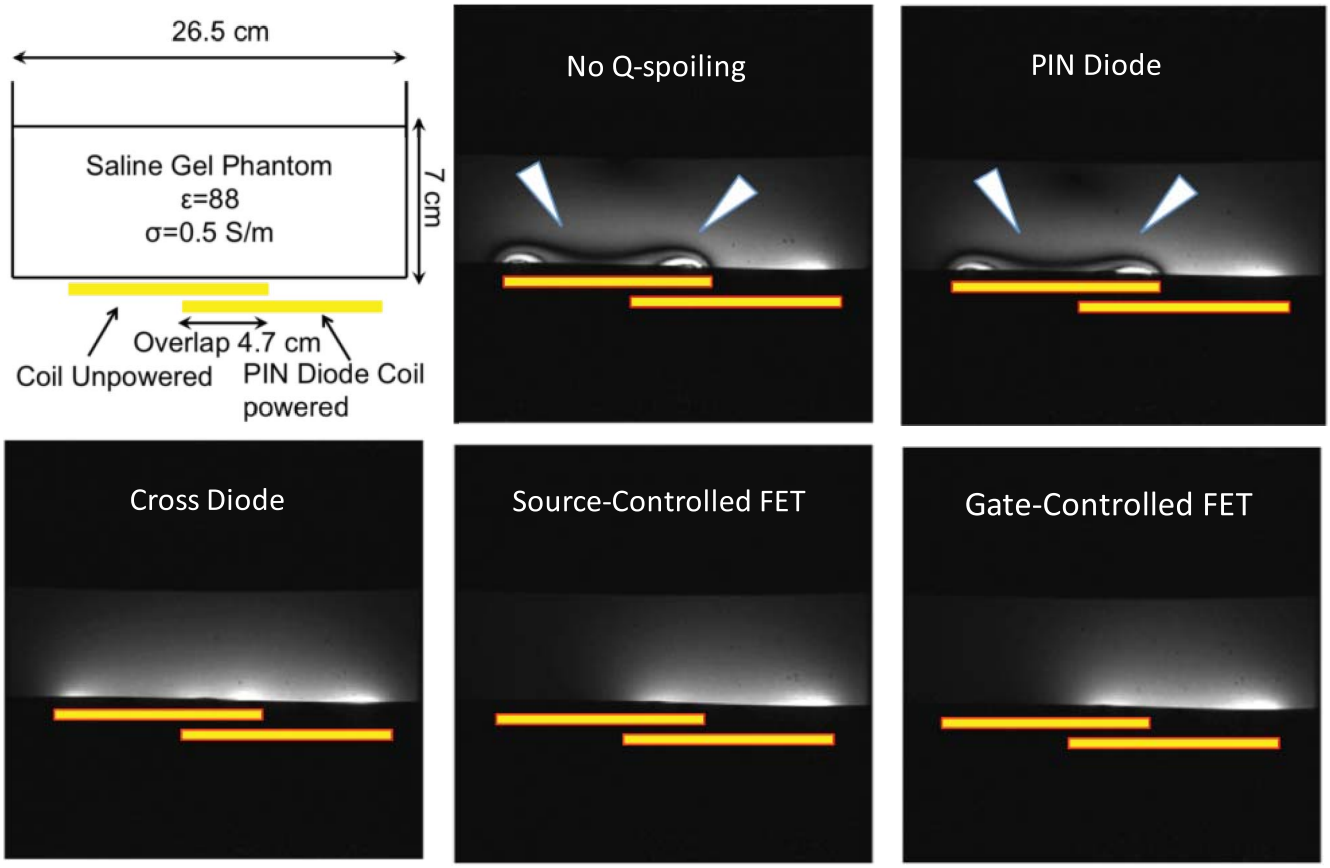

Fig. 9. A conventional PIN diode coil at 1.5 T is overlapped with an unpowered coil, chosen between a coil lacking blocking circuits, a second PIN coil, crossed-diode coil, or FET coils. Q-spoil artifacts are generated in both the coil lacking Q-spoiling and the PIN diode coil. The cross diode coil and FET coils exhibit no Q-spoiling artifacts but the cross-diode leaves the element active during receive, and the FET coils disable reception.

from this function in the case of connector faults. The overlay experiments demonstrated the typical Q-spoiling artifacts of alternating flip angles near the coil conductors when the PIN diode bias is cutoff, and the complete absence of such artifacts using the cross-diode and FET blocking circuits.

The GaN HEMT devices, upon failure, typically remain in a short circuit state, leaving the coil in a detuned state. Faults would then be immediately detectable by low SNR during prescans. We observed this during initial studies when the lower power Cree CGH60015D 15 W devices underwent catastrophic failure. This further supports the appeal of GaN HEMT devices from a safety aspect.

For the FET circuit, the receive mode is activated only by applying a negative gate-to-source voltage beyond the threshold cutoff. We tested two bias variants: applying a negative control voltage to the gate or a positive control voltage to the source. Both bias schemes yielded similar SNR performance. The negative gate bias is most amenable as a drop-in replacement for PIN diodes where dual polarity bias is typically employed in scanners. The source control scheme is better suited for single polarity control and could be used to simultaneously supply power to a preamp and enable receive mode. This would be useful if battery operated arrays become feasible as a step toward wireless systems.

Microwave RF FET switches are traditionally depletion mode devices with gate equidistant between source and drain. This is required for high voltage stand-off in the off state if the FET is a shunt element. In Q-spoiling, the switch need only support the high circulating currents within the blocking circuit in its on state while the off-state (receive mode) signals are miniscule. Consequently, GaN FETs intended for microwave amplification (asymmetric gate) were usable. Twieg et al [32], [33] took the alternate approach of enhancement eGaN power-conversion devices, demonstrating functionality at 1.5 T with 10° flip angles, but their performance deteriorated at 3 T. The devices were likely too large resulting in an unnecessarily low on-resistance and high off-capacitance. Consequently a more complex switch design entailing device stacking and inductor cancellation of switch capacitance was needed. The GaN HEMT devices had about 2x better FOM, and performed well in FSE sequences at 3 T with a very simple single transistor switch arrangement. Further testing will be needed to determine if the off-capacitance is low enough for 7 T operation.

Selection of the device power/current capability is very important. Initial studies had used the Cree CGH60015D 15 W device which worked for a 60° GRE sequence but was destroyed in a FSE pulse sequence at 1.5 T. We suspect the tank circuit current had approached saturation I_{dss}, at which point large drain-source voltage swings began. A possible breakdown occurred on a negative swing with the gate tracking the drain voltage (Fig. 2) leading to gate-source breakdown.

A corrective option is a hybrid of FET and diode, or cross diode much like a PIN-schottky limiter combination [52], [53] between drain and source to prevent these excursions, but at a cost of higher C_{off}. In our case, the higher power 25–75 W devices supported much higher saturation currents and were less likely to have a similar breakdown effect.

The cost of the FET devices approximately ranged from 40-50 USD while the PIN diode is less than 10 USD. However, we expect this to change overtime with technological advances.

A future goal is to simulate the nonlinear effects of induced voltages on the HEMT switches and assess the impact of intermodulation distortion on slice profiles near the coil. The ADS models for our specific devices provided by Cree were intended only for standard amplifier biasing and not switching applications. For instance, the p-n junction behavior between the gate and drain under the polarity reversal conditions was not taken into account. While the p-n junction of the drain and gate should result in the gate voltage being pulled down when drain voltage goes down, the model exhibited no such behavior. However, Cree has recently provided a generic FET switch model, whose parameters can be tuned to emulate any device for simulation studies. Another alternative solution would be to create a custom model (ie. based off the Curtice model [54], [55]) to more correctly mimic device behavior.

VIII. Conclusion

In this work, we prototyped, demonstrated, and compared a lower power Q-spoiling method using depletion-mode GaN HEMT devices at both 1.5 T and 3 T. The depletion-mode devices allow Q-spoiling by default, providing a useful safety feature. In addition, this method can yield large current savings and can be useful with growing interest in low-power wearable or even wireless arrays coils. These parts are easily accessible, require low control voltages, and have low off-capacitance and sufficiently low on-resistances to achieve acceptable blocking impedances.

Acknowledgment

The authors would like to thank Ronald Watkins of Stanford Radiology for helpful discussions. In addition, the authors would like to acknowledge the Stanford Graduate Fellowship, National Science Foundation, NIH Grant R01EB008108, P01CA15999, R01EB019241, GE Healthcare Research Support.

References

[1] R. F. Pierret, *Semiconductor Device Fundamentals*. Reading, MA, USA: Addison-Wesley, 1996.
[2] W. E. Doherty, Jr., and R. D. Joos, Eds., *The PIN Diode Circuit Designers' Handbook*, Artech, Watertown, MA, USA, 1992.
[3] I. Bahl, *Control Components Using Si, GaAs, and GaN Technologies*. Boston, MA, USA: Artech, 2014.
[4] R. Nelson, "RF switching options: The right fit might come with a loss," in *Proc. EDN*, Sep. 2009, pp. 31–36.
[5] R. Cory and D. Fryklund, "RF/microwave solid state switches," in *Microw. Products Dig.*, May 2009, pp. 1–7.
[6] R. Cory and D. Fryklund, "Solid state RF/microwave switch technology: Part 2," in *Microw. Products Dig.*, Jun. 2009, pp. 34–66.
[7] "Understanding RF/microwave solid state switches and their applications,"Agilent Technol.., Santa Clara, CA, USA, Appl. Note 5989-7618EN, Oct. 2009.
[8] P. Hindle, "The state of RF/microwave switch devices," *Microw. J.*, vol. 53, no. 11, p. 20, Nov. 2010.
[9] A. F. Berezniak and A. S. Korotkov, "Solid-state microwave switches: Circuitry, manufacturing technologies and development trends," *Radioelectron. Commun. Syst.*, vol. 56, no. 4, pp. 159–177, 2013.
[10] P. B. Roemer, W. A. Edelstein, C. E. Hayes, S. P. Souza, and O. M. Mueller, "The NMR phased array," *Magn. Reson. Med.*, vol. 16, no. 2, pp. 192–225, 1990.
[11] J. S. Hyde, R. J. Rilling, and A. Jesmanowicz, "Passive decoupling of surface coils by pole insertion," *J. Magn. Reson.*, vol. 89, no. 3, pp. 485–495, 1990.
[12] M. R. Bendall, A. Connelly, and J. M. Mckendry, "Elimination of coupling between cylindrical transmit coils and surface-receive coils for in vivo NMR," *Magn. Reson. Med.*, vol. 3, no. 1, pp. 157–163, 1986.
[13] A. Gopinath and J. B. Rankin, "GaAs FET RF switches," *IEEE Trans. Electron Devices*, vol. 32, no. 7, pp. 1272–1278, Jul. 1985.
[14] Y. Ayasli, "Microwave switching with GaAs FETs," *Microw. J.*, vol. 25, pp. 719–723, May 1982.
[15] V. Alleva *et al.*, "High power microstrip GaN-HEMT switches for microwave applications," in *Proc. 3rd Eur. Microw. Integr. Circuits Conf.*, 2008, pp. 194–197.
[16] U. K. Mishra, P. Parikh, and Y.-F. Wu, "AlGaN/GaN HEMTs—An overview of device operation and applications," *Proc. IEEE*, vol. 90, no. 6, pp. 1022–1031, Jun. 2002.
[17] M. A. Kahn, A. Bhattarai, J. N. Kuznia, and D. T. Olson, "High electron mobility transistor based on a GaN-Al_x Ga_{1-x} N heterojunction," *Appl. Phys. Lett.*, vol. 63, no. 9, pp. 1214–1215, 1993.
[18] R. Gaska *et al.*, "High-temperature performance of AlGaN/GaN HFETs on SiC substrates," *IEEE Electron Device Lett.*, vol. 18, no. 10, pp. 492–494, Oct. 1997.
[19] G. Simin *et al.*, "Novel approaches to microwave switching devices using nitride technology," *Int. J. High Speed Electron. Syst.*, vol. 20, no. 1, pp. 219–227, 2011.
[20] G. Simin *et al.*, "III-nitride microwave control devices and ICs," *Semicond. Sci. Technol.*, vol. 28, no. 7, p. 074008, Jul. 2013.
[21] A. Bettidi *et al.*, "High power GaN-HEMT SPDT switches for microwave applications," *Int. J. RF Microw. Comput.-Aided Eng.*, vol. 19, no. 5, pp. 598–606, 2009.
[22] N. V. Drozdovski and R. Caverly, "GaN-based high electron-mobility transistors for microwave and RF control applications," *IEEE Trans. Microw. Theory Tech.*, vol. 50, no. 1, pp. 4–8, Jan. 2002.
[23] R. Vetury, D. Hodge, D. Aichele, and J. Shealy, "High power and wideband GaN RF switch technology," presented at the Int. Conf. Nitride Semiconductors, 2011.
[24] R. S. Pengelly, S. M. Wood, J. W. Milligan, S. T. Sheppard, and W. L. Pribble, "A review of GaN on SiC high electron-mobility power transistors and MMICs," *IEEE Trans. Microw. Theory Tech.*, vol. 60, no. 6, pp. 1764–1783, Jun. 2012.
[25] M. Kameche and N. V. Drozdovski, "GaAs-, InP- and GaN HEMT-based microwave control devices: What is best and why," *Microw. J.*, vol. 48, no. 5, pp. 164–178, May 2005.
[26] T. Fujii *et al.*, "Over 200-W high isolation GaN-switch for L-band radar module," in *Proc. 8th Eur. Radar Conf.*, Manchester, U.K., Oct. 2011, pp. 25–28.
[27] H. Ishida *et al.*, "A high-power RF switch IC using AlGaN/GaN HFETs with single-stage configuration," *IEEE Trans. Electron Devices*, vol. 52, no. 8, pp. 1893–1899, Aug. 2005.
[28] J. M. Carroll, "Using GaN FETs for high power RF switches," in *Proc. IEEE Compound Semiconductor Integr. Circuits Symp. (CSICS)*, Monterey, CA, USA, Oct. 2008, pp. 1–4.
[29] R. Pengelly *et al.*, "Commercial GaN devices for switching and low noise applications," in *Proc. CS MANTECH Conf.*, Palm Springs, CA, USA, May 2011, pp. 1–6.
[30] M. Burl and M. X. Zou, "Transmit mode coil detuning for MRI systems," U.S. Patent 6850067, Feb. 1, 2005.
[31] A. Reykowski and R. Housen, "FET switch as detune circuit for MRI RF coils," U.S. Patent 2014 0070808 A1, Mar. 13, 2014.
[32] M. Twieg, M. D. Rooij, and M. A. Griswold, "Enhancement mode GaN on silicon (eGaN FETs) for coil detuning," *Proc. Int. Soc. Magn. Reson. Med.*, vol. 22, p. 926, 2014.
[33] M. Twieg, M. de Rooij, and M. A. Griswold, "Active detuning of MRI receive coils with GaN FETs," *IEEE Trans. Microw. Theory Tech.*, vol. 63, no. 12, pp. 4169–4177, Dec. 2015.
[34] D. Spence and M. Aimi, "Custom MEMs switch for MR surface coil decoupling," *Proc. Int. Soc. Magn. Reson. Med.*, vol. 23, p. 704, 2015.
[35] V. Choudhary and K. Iniewski, *MEMS: Fundamental Technology and Applications*. Boca Raton, FL, USA: CRC, 2013, pp. 203–204.

[36] G. M. Rebeiz and J. B. Muldavin, "RF MEMS switches and switch circuits," *IEEE Microw. Mag.*, vol. 2, no. 4, pp. 59–71, Dec. 2001.
[37] G. M. Rebeiz, "RF MEMS switches: Status of the technology," in *Proc. 12th Int. Conf. Solid-State Sens., Actuators Microsyst.*, Jun. 2003, pp. 1726–1729.
[38] M. Fuentes, E. Weber, S. Wilson, B. Li, and S. Crozier, "Micro-electromechanical systems (MEMS) based RF-switches in MRI—A performance study," *Proc. Int. Soc. Magn. Reson. Med.*, vol. 18, 2010.
[39] Y. Shim, G. Hummel, and M. Rais-Zadeh, "RF switches using phase change materials," in *Proc. MEMS*, Jan. 2013, pp. 237–240.
[40] N. El-Hinnawy *et al.*, "Improvements in GeTe-based inline phase-change switch technology for RF switching applications," in *Proc. CS MANTECH Conf.*, May 2014, pp. 401–403.
[41] J. Lu *et al.*, "Q-spoiling method using depletion mode gallium nitride (GaN) HEMT devices at 1.5 T," *Proc. Int. Soc. Magn. Reson. Med.*, vol. 23, p. 855, 2015.
[42] J. Lu *et al.*, "High powered GaN HEMT devices for low powered Q-spoiling at 3T MRI," *Proc. Int. Soc. Magn. Reson. Med.*, vol. 24, p. 2175, 2016.
[43] V. Taracila, P. Chan, and F. Robb, "Minimal acceptable blocking impedance for RF receive coils," *Proc. Int. Soc. Magn. Reson. Med.*, vol. 18, 2010.
[44] A. Kocharian, "Determination of appropriate RF blocking impedance for MRI surface coils and arrays," *Magn. Reson. Mater. Phys., Biol. Med.*, vol. 10, no. 2, pp. 80–83, 2000.
[45] G. Meneghesso, M. Meneghini, and E. Zanoni, "Breakdown mechanisms in AlGaN/GaN HEMTs: An overview," *Jpn. J. Appl. Phys.*, vol. 53, no. 10, p. 100211, Oct. 2014.
[46] M. D. Hodge, R. Vetury, and J. B. Shealy, "Fundamental failure mechanisms limiting maximum voltage operation in AlGaN/GaN HEMTs," in *Proc. IEEE Int. Rel. Phys. Symp. (IRPS)*, Apr. 2012, pp. 3D.2.1–3D.2.6.
[47] T. Tokumitsu, I. Toyoda, and M. Aikawa, "A low-voltage, high-power T/R-switch MMIC using LC resonators," *IEEE Trans. Microw. Theory Techn.*, vol. 43, no. 5, pp. 997–1003, May 1995.
[48] W. B. Kuhn, M. M. Mojarradi, and A. Moussessian, "A resonant switch for LNA protection in Watt level CMOS transceivers," *IEEE Trans. Microw. Theory Tech.*, vol. 53, no. 9, pp. 2819–2825, Sep. 2005.
[49] J. van Heteren and B. McCarten, "Computer modelling of passive decoupling circuits," in *Proc. 8th Soc. Magn. Reson. Med.*, 1989, p. 958.
[50] R. H. Caverly, *Microwave and RF Semiconductor Control Device Modeling*. Norwood, MA, USA: Artech, 2016.
[51] D. Brunner *et al.*, "A high speed, high power T/R switching frontend," *Proc. Int. Soc. Magn. Reson. Med.*, vol. 23, p. 496, 2016.
[52] "Schottky enhanced PIN limiter compact, low threshold and wideband," Avago Technol., San Jose, CA, USA, Appl. Note 5438.
[53] C.-L. Lim, "Recovery time of the Schottky-PIN limiter," *Microw. J.*, pp. 66–72, Nov. 2012.
[54] W. R. Curtice and M. Ettenberg, "A nonlinear GaAs FET model for use in the design of output circuits for power amplifiers," *IEEE Trans. Microw. Theory Tech.*, vol. MTT-33, no. 12, pp. 1383–1394, Dec. 1985.
[55] S. Maas, "Fixing the Curtice FET Model," *Microw. J.*, vol. 45, pp. 68–75, Mar. 2002.