Power Factor Correction in Cuk–SEPIC-Based Dual-Output-Converter-Fed SRM Drive

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***Abstract*—In this paper, a power factor correction (PFC)-based switched reluctance motor (SRM) drive is proposed. Generally, the SRM drive is fed with a simple diode bridge rectifier followed by a bulky capacitor, which draws peaky current at low power factor and high-input-current total harmonic distortion (THD). Here, a dual output converter is proposed to control the SRM and to provide power quality improvement as well. This converter is a combination of Cuk and SEPIC converters, which produces two equal output voltages with neutral point N, to feed a midpoint converter of the SRM drive. The converter is designed to operate in discontinuous conduction mode of operation to obtain inherent PFC at supply side. The motor control is attained by regulating dc link voltage over a wide range. Test results on a prototype of the SRM drive demonstrate the excellent performance with high power factor and reduced input current THD. The observed power quality indices depict the improved power quality as per the standard IEC 61000-3-2.**

***Index Terms*—Discontinuous conduction mode (DCM), midpoint converter, power factor correction (PFC), power quality, switch reluctance motor (SRM), total harmonic distortion (THD).**

I. Introduction

RECENT research in power converters has contributed to different dc–dc converter configurations, delivering regulated output voltages as per the end user requirement. However, at the same time, it has become the cause for power supply distortion. Therefore, the rapid increase in demand of power factor correction (PFC) converters prevails in the market [1]. These PFC converters not only provide the tight output voltage regulation however, at the same time, provide the inherent PFC.

Many PFC-based buck, boost, and buck–boost converters are proposed in the literature. These PFC converters provide PFC with regulated output voltages. Boost and buck converters are used widely for PFC, because an indirect transfer of energy is less which reduces the overall switching stress across the device [2]–[4], whereas the output voltage range is limited in boost and buck converters. Hence, buck–boost converters are highly recommended as they can operate in both buck and boost modes on the basis of duty cycle control [5], [6]. The only disadvantage of using of using buck–boost converter is high switching stress across the device as overall energy transferred to output, in switch OFF mode. To achieve active PFC, different control techniques are already implemented in [7] and [8].

Depending on the nature of the inductor current, these PFC converters can be designed to operate in three different modes of operation: discontinuous conduction mode (DCM), continuous conduction mode (CCM), and boundary between DCM and CCM, i.e., critical current mode [9]–[11]. In CCM, continuous inductor current leads to low root mean square current in the inductor and switch and low current ripples which result in low electromagnetic interference (EMI). Moreover, switch suffers from hard switching due to continuous inductor current, therefore, CCM is generally recommended for medium to high power operation, whereas in DCM, the inductor current exhibits discontinuous nature. This feature of DCM allows zero current switch ON and no reverse recovery in diode, whereas contrary to this, the discontinuous current also results in EMI-related issues. This restricts the DCM for low power applications.

To obtain inherent PFC in DCM of operation, the converter is required to operate at high switching frequency. Here, the converter switch is operated at switching frequency of 20 kHz. The key benefits of selecting high switching frequency are the reduced size of circuit components, such as inductors and capacitors as well as saving the board space and component cost. However, further increase in switching frequency increases switching losses and thus results in reduced converter efficiency. The switching loss during one switching period is multiplied by converter switching frequency to calculate total switching loss associated with the converter. Thus, power loss increases with an increase in switching frequency, which demands more board space, as required heat sink size increases to dissipate heat.

In order to achieve PFC, different converter topologies are proposed. Singh and Singh [12] have proposed PFC converter topologies for permanent brushless dc motor drives and suitable selection of converter on the basis of application and power rating. SEPIC and Cuk converters based PFC converters are proposed by Sabzali *et al.* [13] and Ismail [14] with reduced conduction and switching losses. Bridgeless configuration of both Cuk and SEPIC converters is also investigated on performance basis by them. Simonetti *et al.* [15] have given an inherent property of DCM of operation with correct selection of input and output side inductors in Cuk and SEPIC converters. The available PFC converter configurations provide the well-regulated dc output voltage with PFC. The requirement of dual-output

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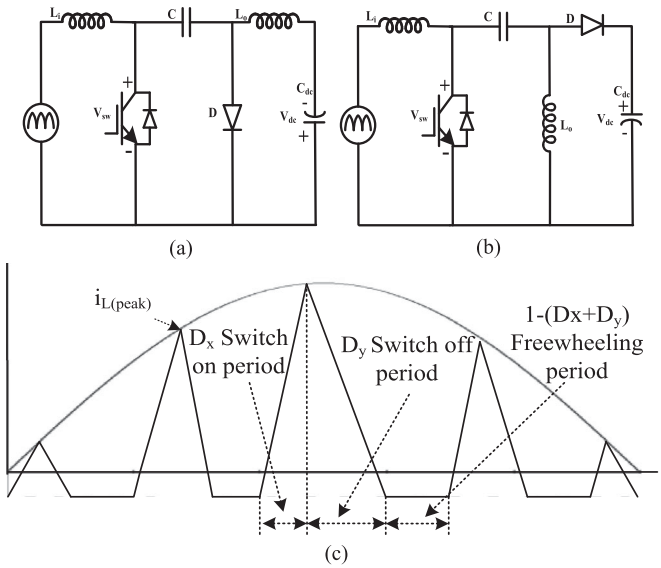


Fig. 1. (a), (b) Circuit diagram of conventional Cuk and SEPIC converter and (c) inductor current in DCM mode during switch ON period, switch OFF period, and freewheeling period.

voltage encourages the design and development of dual output converter.

The circuit topology comprises of Cuk and SEPIC converters which are shown in Fig. 1(a) and (b) [16], [17]. The output side inductors for both the converters are designed for DCM. Fig. 1(c) shows the nature of inductor current during DCM. The duty cycle during switch ON period is denoted by D_x whereas duty cycle during switch OFF period is given by D_y. The inductor is selected below the calculated value to ensure DCM of operation. The size of core for an inductor is selected accordingly to sustain peak flux density requirement without saturation at full load condition [18]. The selection of Cuk–SEPIC-based dual output converter is made because of these following significant features of the proposed converter.

1) Balanced dual output voltages without any additional voltage balance control.
2) The inverted output of Cuk converter and noninverted output of SEPIC converter are combined to generate two symmetrical dc voltages with a neural point N.
3) Single switch configuration of converter with reduced switching stress across the device due to available midpoint N.
4) High voltage conversion ratio as compared to available other buck–boost converter configuration.
5) Both the Cuk and SEPIC converters share common input side inductor, thus reducing the component count.

The switched reluctance motor (SRM) drives are drawing the interest of researchers as superior solution for low power application in household drives such as: vacuum cleaners, air conditioners, dryers, washing machines, food blending machines, refrigerators, etc. Today induction motor based drives rule the market, as these motors are already explored in the past few decades. In the process of learning and familiarization, the SRM appears as a low-cost machine with simple doubly salient construction. Winding free rotor with low inertia offers excellent performance at medium and high speed operation [19]–[21]. In case of SRM, additional power converter is required to excite the phases of SRM in synchronism with rotor position feedback. These converters topologies are discussed in [22] which decide the different voltage levels which should be applied to control the SRM. In order to improve reliability and reduced system cost, several sensor-less methods are developed and implemented in [23]. However, SRM is not widely accepted due to its high torque ripples. To deal with these torque ripples issues, many direct torque control techniques are developed in [24]. A four-phase, 8/6 pole SRM is selected (motor specification given in the Appendix), with simultaneous excitation of phases. The rotor position is estimated using shaft mounted optical encoder.

II. Proposed PFC Converter Fed SRM Drive

The converter proposed here utilizes a two conventional fourth order converters, i.e., SEPIC converter and Cuk converter as shown in Fig. 2. These two converters are similar in configuration at the input side, the only difference is the placement of the output side inductor and the diode. Hence, a combination of both converters is feasible with one common input structure and two output structures for dual output voltages. The voltage conversion ratio is the same for both Cuk and SEPIC converters; therefore, the converter can produce self-balancing dual output voltages. The derived converter is as per the requirement to feed a midpoint converter with neutral point N. The rectified output from diode bridge rectifier (DBR) is fed to the proposed converter utilizing single switch such that switch ON and switch OFF periods are the same for both the converters. Fig. 3(a) and (b) shows the proposed converter configuration split into SEPIC and Cuk converter separately. The output voltage of SEPIC converter and Cuk converter is denoted as V_{dc1} and V_{dc2}. The input side inductor L_i transfers its energy to intermediate capacitors C_1 and C_2. Furthermore, the stored energy of intermediate capacitor in each switch on period is transferred to two output side inductors L_{01} and L_{02} through two ultrafast diodes D_1 and D_2. The proposed converter has reduced switching stress as compared to conventional Cuk and SEPIC converters.

III. Operation of the Proposed Converter

The input side inductor L_i is the same for both the converters which is designed to operate in CCM, while the output side inductors L_{o1} and L_{o2} of both the converters are designed to operate in DCM [15]. The design of output side capacitors C_1 and C_2 is made such that capacitor voltage remains continuous throughout the switching period. The operating modes to understand working of proposed converter can be given as follows.

Mode I (Switch ON period t_2-t_1): The flow of current during turn ON period in both SEPIC and Cuk converter is shown in Fig. 4(a). The associated current and voltage waveforms during all the stated three modes of operation are shown in Fig. 5. Insulated gate bipolar transistor conducts during this mode. The input inductor starts charging with a slope of $V_m(t)/L_i$, whereas selection of L_i is made such that current always remains continuous through the inductor. The capacitors C_1 and C_2 of Cuk and

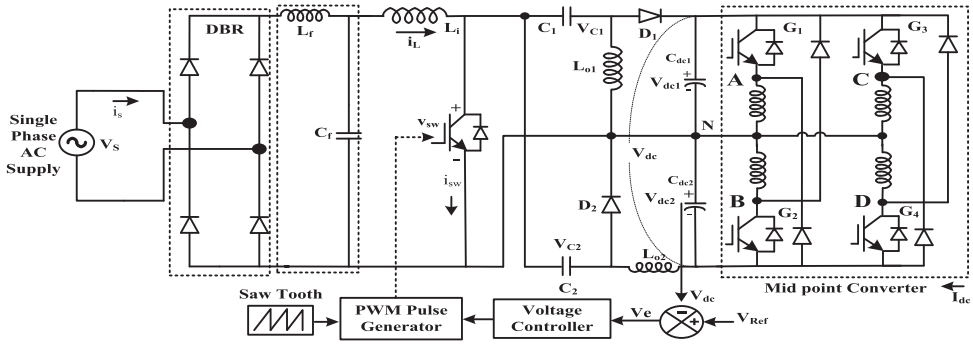


Fig. 2. Proposed Cuk–SEPIC-based dual output converter fed SRM drive.

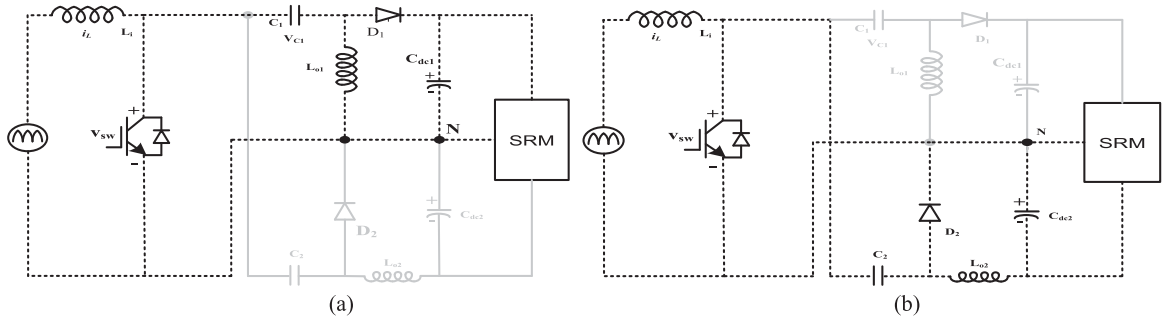


Fig. 3. Proposed circuit derived from combination of two basic circuit configuration: (a) SEPIC and (b) Cuk converter.

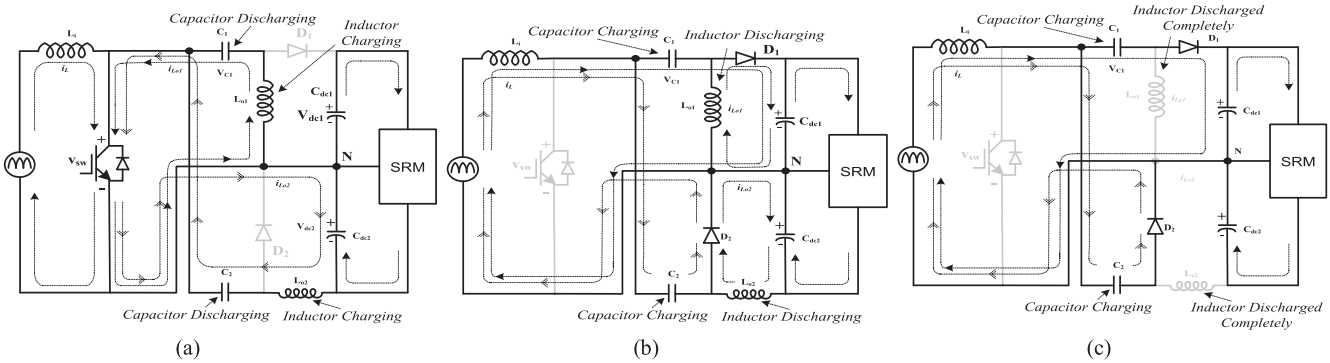


Fig. 4. Three different modes of operation of proposed converter (a) Mode I (Switch ON period $t_2 - t_1$), (b) Mode II (Switch OFF period $t_3 - t_2$), and (c) Mode III (DCM mode $t_3 - t_4$).

SEPIC converters configuration start discharging across output side inductors L_{o1} and L_{o2}. As diodes D_1 and D_2 do not conduct during this mode; the load current requirement is fulfilled by output capacitor. The peak switch current through single switch during this mode is given as $I_{\text{sw,peak}} = V_m D_x T_s / L_e$, where L_e is an equivalent inductance of circuit inductances, i.e., filter inductor L_f, input inductor L_i, and two output side inductors L_{o1} and L_{o2}. V_m is the peak value of ac voltage, D_x is the switch ON period, and T_s is the total switching period.

Mode II (Switch OFF period $t_3 - t_2$): This mode explains the switch OFF period of the switching cycle. In this mode, the capacitors C_1 and C_2 of both Cuk and SEPIC converters start charging through common input side inductor L_i and the load current requirement is fulfilled by the two output side inductors L_{o1} and L_{o2} as shown in Fig. 4(b). In this mode, both the ultrafast diodes D_1 and D_2 are forward biased; thus, capacitor charging current and output inductor discharging current are found in their path through these two diodes. The currents through output side inductors L_{o1} and L_{o2} can be given as $di_{Lo1}/dt = -V_{\text{dc1}}/L_{o1}$, $di_{Lo2}/dt = -V_{\text{dc2}}/L_{o2}$, where V_{dc1} and V_{dc2} are the output capacitor voltages for SEPIC and Cuk converters separately.

Mode III (DCM mode $t_3 - t_4$): During this mode, the currents through inductors L_{o1} and L_{o2} enter DCM as shown in Fig. 4(c). The diodes D_1 and D_2 provide the path for constant freewheeling current, as constant current flows through L_i, L_{o1}, and L_{o2}. The constant charging of capacitors C_1 and C_2 takes place through

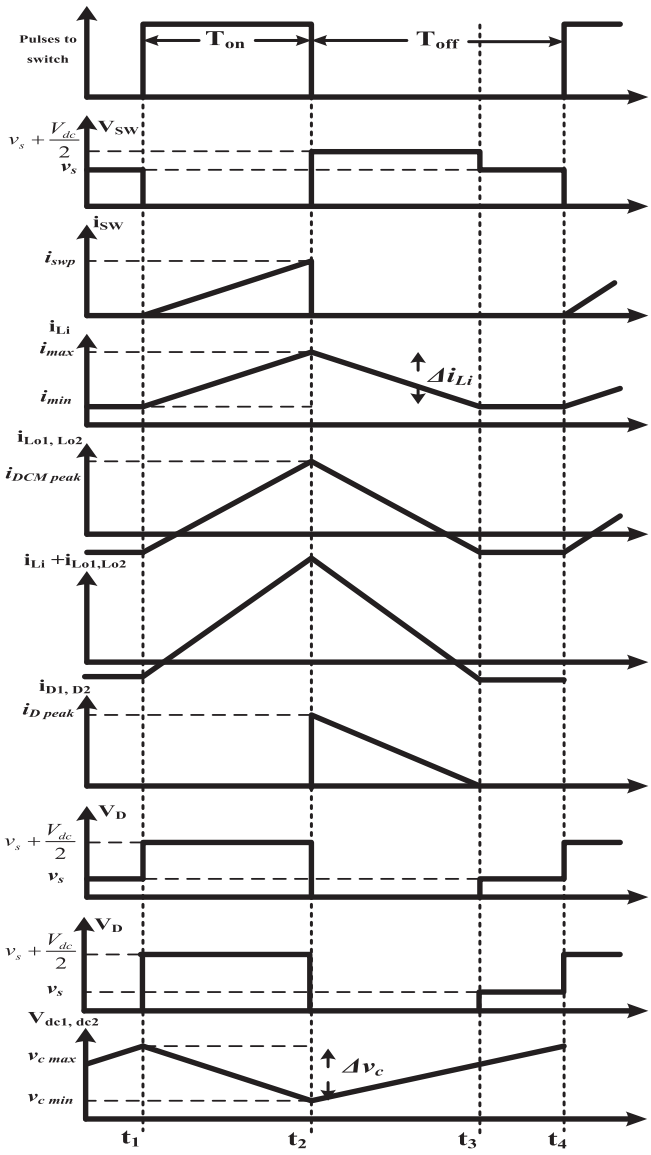


Fig. 5. Associated voltage and current waveform in three different modes of operation.

an input inductor. This mode lasts for until the next switching period. The time period for *mode III* can be given as

$$t_3 - t_4 = T_s - \{(t_2 - t_1) + (t_3 - t_2)\}.$$

The period of this mode directly depends on the size of output inductor, which is calculated for DCM operation. Further decreasing the inductor size, it increases the slope; thus, peak inductor current increases which increases the period for *mode III*.

IV. Design of the Proposed Converter

The design of proposed converter includes design of low-pass *LC* filter, input inductor (L_i), intermediate capacitors (C_1 and C_2), output inductors (L_{o1} and L_{o2}), and dc link capacitors (C_{dc1} and C_{dc2}). The SR motor rating is considered as 400 W, with 8 stator poles and 6 rotor poles. The calculations are made with supply voltage and frequency as 220 V and 50 Hz. As the motor control is proposed for regulated dc link voltage over wide range; therefore, dc link voltage variation is considered from $V_{dc\,min} = 100$ V to $V_{dc\,max} = 300$ V.

A. Design of Input Inductors (L_i) for CCM

The input inductor (L_i) is designed for continuous current which is common to both the converters, which can be given as [25]

$$\begin{aligned} L_i &= \frac{V_{in} D_x}{\eta I_{in} f_s} \\ &= \frac{R_{in} D_x}{\eta f_s} = \left(\frac{V_s^2}{P_i}\right)\frac{D_x}{\eta f_s} \\ &= \frac{1}{\eta f_s}\left(\frac{v_s^2}{P_{max}}\right)\left(\frac{V_{dc\,max}}{V_{dc\,max} + V_{in}}\right). \end{aligned} \tag{1}$$

R_{in} is considered as input resistance in the above-mentioned equation, whereas the duty cycle as D_x and switching frequency f_s is taken as 20 kHz. The maximum ripple through inductor is considered for rated converter output voltage and at supply voltage dip as $v_s = 170$ V. Thus, input inductor is calculated as

$$L_i = \frac{1}{0.4 \times 20\,000}\left(\frac{170^2}{400}\right)\left(\frac{300}{300 + 170\sqrt{2}}\right) = 5.01 \text{ mH}.$$

The current ripple (η) through this inductor is considered as 40%; therefore, selected value for L_i is 5 mH.

B. Design of Output Inductors (L_{o1} and L_{o2}) for DCM

The peak inductor current in DCM plays vital role in the design of an output side inductor. The inductor design should be considered such that the inductor does not saturate during any transient condition. Therefore, the calculation for inductor design can be given as [25]–[28]

$$\begin{aligned} L_{o1,o2} &= \frac{V_{dc}(1 - D_x)}{2 I_{Lo} f_s} \\ &= \frac{V_{dc} D_x}{2 I_{in} f_s} = \frac{R_{in} V_{dc} D_x}{2 V_{in} f_s} \\ &= \left(\frac{V_s^2}{P_i}\right)\frac{V_{dc}}{2 V_{in} f_s}\left(\frac{V_{dc}}{V_{in} + V_{dc}}\right). \end{aligned} \tag{2}$$

The calculation is made while considering the minimum load current at minimum dc link voltage as 100 V:

$$L_{o1,o2} = \left(\frac{v_s^2}{P_{max}}\right)\frac{V_{dc\,max}}{2\sqrt{2} v_s f_s}\left(\frac{V_{dc\,max}}{V_{dc\,max} + \sqrt{2} V_s}\right)$$

$$\begin{aligned} L_{o1,o2} &= \left(\frac{220^2}{120}\right)\frac{100}{2\sqrt{2} \times 220 \times 20\,000}\left(\frac{100}{100 + 220\sqrt{2}}\right) \\ &= 788.29\ \mu\text{H}. \end{aligned} \tag{3}$$

As per the given calculation, to ensure the discontinuous inductor current, inductors are selected as 250 μH each, i.e., up to 1/3 of the calculated value [15]. Here, E-type ferrite core is considered to design the inductor. The cores are provided with small air gap to avoid any chance of saturation during any transient condition.

C. Design of Intermediate Capacitors (C_1 and C_2) for Continuous Voltage

The intermediate capacitors both for Cuk and SEPIC converters are selected to operate in CCM. The calculation for capacitor design is given as [25]–[28]

$$C_{1,2} = \frac{V_{\rm dc} D_x}{\Delta V_{c1} f_s R_L} = \frac{V_{\rm dc} D_x}{\eta V_{c1} f_s R_L}. \tag{4}$$

The instantaneous voltage appearing across intermediate capacitors is the sum of input voltage at that instant and dc link voltage which is given as $V_{C1,2}(t) = \{V_{\rm dc} + V_{\rm in}(t)\}$. Consider the equivalent load resistance as R_L, which can be given as $R_L = V_{\rm dc}^2/P_i$, such that P_i denotes the input power to the drive. Substituting the value of capacitor voltage and load resistance in (4), the obtained expression is given as

$$C_{1,2} = \frac{V_{\rm dc}}{\eta\{V_{\rm dc} + V_{\rm in}\} f_s (V_{\rm dc}^2/P_i)} \left(\frac{V_{\rm dc}}{V_{\rm in} + V_{\rm dc}}\right) = \frac{P_{\max}}{\eta (V_{\rm dc\,max} + \sqrt{2} V_{s\,\max})^2 f_s}. \tag{5}$$

The intermediate capacitors are selected for rated supply voltage and output voltage conditions of the converter. The calculation for C_1 and C_2 with permissible ripple voltage as 10% can be given as

$$C_{1,2} = \frac{400}{0.1 \times 20\,000 \times \left(220\sqrt{2} + 300\right)^2} = 535 \text{ nF}.$$

Therefore, the value for C_1 and C_2 is selected as 880 nF.

D. Design of a DC-Link Capacitor

Output capacitors for the converter are estimated as [25]–[28]

$$C_{\rm dc} = \frac{I_{\rm dc}}{2\omega \Delta V_{\rm dc}} = \frac{P_i/V_{\rm dc}}{2\omega\delta V_{\rm dc}}. \tag{6}$$

As the converter output voltage varies from 100 to 300 V dc, therefore, the value of required output capacitor at C_{300} and C_{100} with permissible ripple voltage (δ) up to 5% is

$$C_{100} = \frac{P_{\min}}{2\omega\delta V^2_{\rm dc\,min}} = \frac{120}{2 \times 314 \times 0.03 \times 100^2} = 636.94\ \mu\text{F}$$

$$C_{300} = \frac{P_{\max}}{2\omega\delta V^2_{\rm dc\,max}} = \frac{400}{2 \times 314 \times 0.03 \times 300^2} = 235.90\ \mu\text{F}.$$

The dc link comprises of two capacitors connected in series, i.e., output capacitors of Cuk and SEPIC converters are connected in series with one common neutral point N. As per the calculation, two capacitors of 1000 μF are selected with voltage rating of 1000 V.

E. Design of DC Filter (L_f and C_f)

This *LC* filter attenuates switching frequency current harmonics, thus improving the input current total harmonic distortion (THD). Here, V_m and I_m denote the peak value of input voltage and current. Therefore, filter design can be given as [28]

$$C_{\max} = \frac{I_m}{\omega_L V_m}\tan(\theta) = \frac{\left(P_o\sqrt{2}/v_s\right)}{\omega_L V_m}\tan(\theta) = \frac{\left(400\sqrt{2}/220\right)}{314 \times 220\sqrt{2}}\tan(0.5^\circ) = 229.69 \text{ nF}. \tag{7}$$

Therefore, C_f is taken as 440 nF. $\omega = 2\pi f_L$ and f_L is the line frequency; however, θ is phase displacement between supply voltage and current. The calculation for filter inductor is made while considering the source inductance, which is considered as 4% of the base impedance of the system. Here, source inductor is denoted as (L_s) and filter inductor by (L_f); therefore, it is calculated as

$$L_f = L_{\rm req} + L_s \Rightarrow \frac{1}{4\pi^2 f_c^2 C_f} = L_{\rm req} + 0.04\left(\frac{1}{\omega_L}\right)\left(\frac{v_s^2}{P_i}\right)$$

$$L_{\rm req} = \frac{1}{4\pi^2 \times 2000^2 \times 440 \times 10^{-9}} - 0.03\left(\frac{1}{314}\right)\left(\frac{220^2}{400}\right) = 2.83 \text{ mH} \tag{8}$$

where f_c is the cut-off frequency and it is selected such that $f_L < f_c < f_s$; hence, it is taken as $f_s/10$. Thus, passive input filter is selected for suppression of higher order harmonics with inductor (L_f) as 3 mH and capacitor (C_f) as 440 nF. Moreover, the cut off frequency is considered as one-tenth of the switching frequency.

F. Boundary Condition for CCM and DCM

The continuous or discontinuous nature of inductor current depends on duty cycle for switch ON period D_x. Here, prerequisite condition for DCM operation is the size of inductor which is selected while considering the boundary condition to ensure the DCM operation at lower dc link voltage and low-speed operation. For switch ON period D_x and switch OFF period D_y, the condition for DCM operation is

$$D_x + D_y \le 1. \tag{9}$$

The dc voltage conversion ratio M is given as $M = V/V_{\rm in}$, where $V_{\rm in}$ represents dc input voltage and V represents dc output voltage. The dimensionless parameter K depends on equivalent inductance L_e, load resistance R, and switching period T_s; therefore, an expression for K can be given as

$$K = \frac{2L_e}{RT_s}. \tag{10}$$

For DCM operation $K < K_{\rm criti}$, such that $K_{\rm criti}$ depends on type of converter and the duty cycle D_x. Here, a combination of Cuk and SEPIC converter is considered; therefore, boundary condition for proposed converter is given as [10]

$$K_{\rm criti} = \frac{1}{2(M + (\sin\omega t))^2}. \tag{11}$$

V. Control of Dual-Output-Converter-Fed SRM Drive

The control of proposed drive is governed under two categories, i.e., control of the proposed converter and SR motor control. The converter control depends on sensed dc link voltage which is given to voltage follower loop to generate pulse width modulated (PWM) pulses, whereas control for SR motor is a function of rotor position feedback; thus, these two controls can be explained as follows.

A. Control of the Proposed Converter

The generated PWM pulses at a frequency similar to carrier frequency drive the converter switch to obtain dc bus voltage control. The dc bus voltage control is obtained by using voltage feedback loop. A voltage sensor is used to sense the converter output voltage ($V_{\rm dc}$), whereas required output voltage is set as reference dc link voltage ($V_{\rm ref}$). The error voltage (v_e) generated after comparing these two voltages serves as control signal for the switch as follows:

$$v_e(\kappa) = v^*_{\rm dc}(\kappa) - v_{\rm dc}(\kappa) \tag{12}$$

where "κ" is considered as sampling instant for comparing these two voltages. The proportional-integral controller is tuned for rated supply voltage and dc link voltage. While tuning, the gains are adjusted such that during dynamics conditions or sudden dc link voltage change, the output voltage peak sustains under permissible limit. The wrong selection of the controller parameters results in transient voltage to appear across device and may harm the device. Hence, controlled voltage can be given as

$$v_{\rm cdc}(\kappa) = v_{\rm cdc}(\kappa - 1) + \kappa_{\rm pv}\{v_e(\kappa) - v_e(\kappa - 1)\} + \kappa_{\rm iv} v_e(\kappa). \tag{13}$$

such that $\kappa_{\rm pv}$ are proportional integral gains of the system.

B. Inherent PFC Operation of the Proposed Converter in DCM

An inherent shaping of input current is obtained when the converter is operated in DCM with constant switching frequency. As in case of Cuk and SEPIC converters, DCM occurs when the current through output diodes becomes zero. During this period, sum of input and output inductor current becomes zero, and a constant current flows through the circuit. Because of this, constant current circuit appears as emulated resistor and hence line current follows the line voltage [29].

C. Control of SRM: Electronic Commutation

The encoder information is used to generate switching for a midpoint converter which is listed in Table I. These encoders are placed on stator periphery with slotted disk mounted on the rotor shaft. The control employing single phase excitation at a time results in discrete phase current which produces discontinuous torque, hence high torque ripples; therefore, simultaneous excitation of two phases is considered here to reduce high torque ripples [30], [31].

TABLE I
Switching Pulses With Respect to Rotor Position Feedback

Encoder Output		Pulses Sequence for Midpoint Converter Switches			
P_1	P_2	G_1	G_2	G_3	G_4
0	0	1	1	0	0
0	1	0	1	1	0
1	0	0	0	1	1
1	1	1	0	0	1

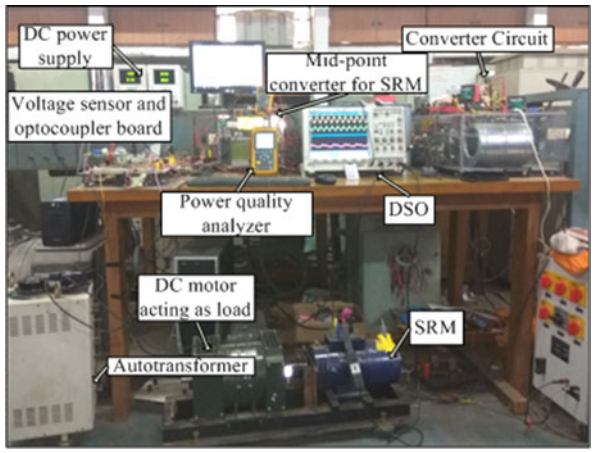


Fig. 6. Photograph of the developed prototype.

The switching pulses are accommodated by a midpoint converter with four switches to provide independent control of individual phases.

VI. Results and Discussion

The proposed SRM drive is experimentally examined using a prototype developed in the laboratory. The development of SRM drive prototype comprises of design and development of voltage sensor board and optocoupler board to provide pulses isolation. The voltage sensor used for sensing dc link voltage is provided with galvanized isolation. To provide optoisolation for converter switch and all the four switches of a midpoint converter, an optocoupler IC (6N136) is used. A digital signal processor (DSP) controller (dSPACE-1104) is used which can be replaced by low-cost DSP controller in future. Fig. 6 shows the photograph of the developed prototype. The encoder information and sensed dc link voltage are given to DSP, to generate the pulses for the midpoint converter switches and single switch of the PFC-based converter. Each SRM phase is provided with additional fuse to restrict the high phase current during faulty conditions. The obtained test results of the system are discussed as follows.

A. Steady-State Performance of the Proposed SRM Drive

On the basis of optical encoder information, the switching sequence of motor phase excitation is decided which is

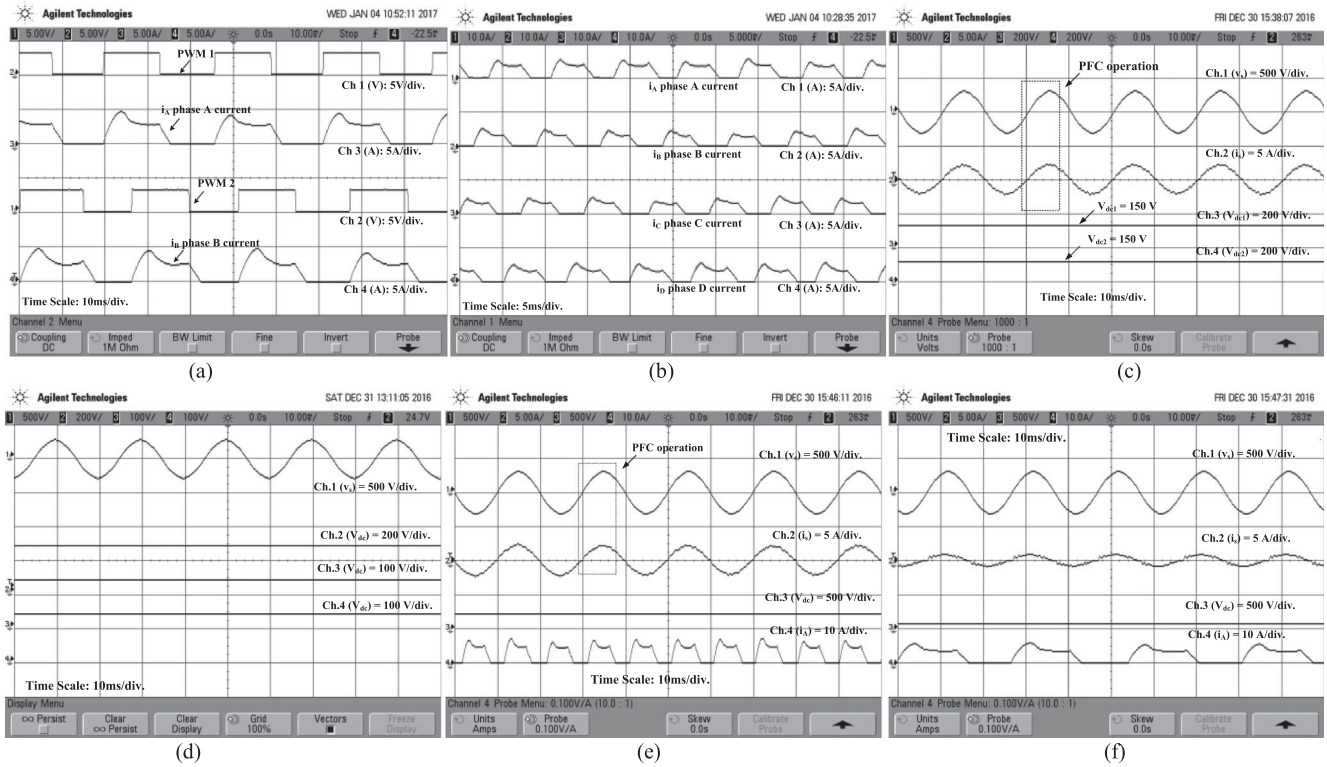


Fig. 7. Obtained test results when converters are operated at rated conditions. (a) Simultaneous excitation of two motor phases. (b) Current through all the four phases of the motor at rated condition. (c) Obtained PFC operation of proposed drive at rated dc link voltage as 300 V. (d) Two equal output voltages as 150 V and rated dc link voltage as a summation of two voltages as 300 V. (e), (f) Motor speed control with PFC at two different dc link voltages as 300 and 100 V.

presented in Table I. The simultaneous excitation of two phases with respect to given sequence and current to all the four phases of motor is shown in Fig. 7(a) and (b). Fig. 7(c) demonstrates the drive input voltage and current; the PFC operation with reduced input current THD as per the given standard has been observed. The balanced output voltages of the proposed converter are well depicted in Fig. 7(c) and (d). As the proposed drive does not require any physical speed sensor to control the motor speed; therefore, direct speed sensing is not possible in the proposed drive. Thus, the speed of the motor at different dc link voltages can be well observed from phase current frequencies which is well depicted in Fig. 7(e) and (f). The performance of proposed drive is evaluated at rated dc link voltage with rated speed which is shown in Fig. 7(e). Here, speed-dependent load is considered, i.e., to record motor performance at variable load conditions the motor is operated at different speeds. Therefore, test results obtained in Fig. 7(e) and (f) show the drive performance at 1500 r/min with dc link as 300 V and for reduced load condition with reduced speed as 500 r/min at low dc link voltage as 100 V.

B. Performance of the Proposed Dual Output Converter

The proposed converter is designed for single-phase household supply while considering the supply voltage fluctuation as 170–270 V ac. The converter is designed for two equal output voltages as 150 V each, across two dc link capacitor connected in series, with one neutral point N. Fig. 8(a) and (b) shows the current through circuit components in Cuk and SEPIC converters separately. The input inductor (L_i) which is common to both the converter is designed for continuous inductor current, which is well reflected in Fig. 8(c). Moreover, this figure also shows the continuous intermediate capacitor voltages V_{c1} and V_{c2}. Fig. 8(d) depicts the discontinuous current through output inductors L_{o1} and L_{o2}, with obtained PFC operation. The zoom in view of Fig. 8(d) clearly demonstrates large freewheeling period in every switching period, thus confirming DCM of operation. The device peak voltage across and current through stress of 420 V and 18 A are shown in Fig. 8(e).

C. Dynamic Performance of the Proposed SRM Drive

The performance of the proposed drive is evaluated under both steady-state and dynamic conditions. Test results reflect the controlled and stable operation of the proposed drive during all dynamics conditions. Fig. 9(a) shows the drive performance during start with motor speed of 270 r/min. The high inrush current during start is limited to permissible value by gradually increasing V_{dc}. To achieve speed control of proposed SRM drive from 480 to 1500 r/min, the converter output voltage is varied ranging from 100 to 300 V dc. Fig. 9(b) shows the motor dynamics when dc link is varied from 170 to 250 V such that speed change is observed from 860 to 1240 r/min. The speed

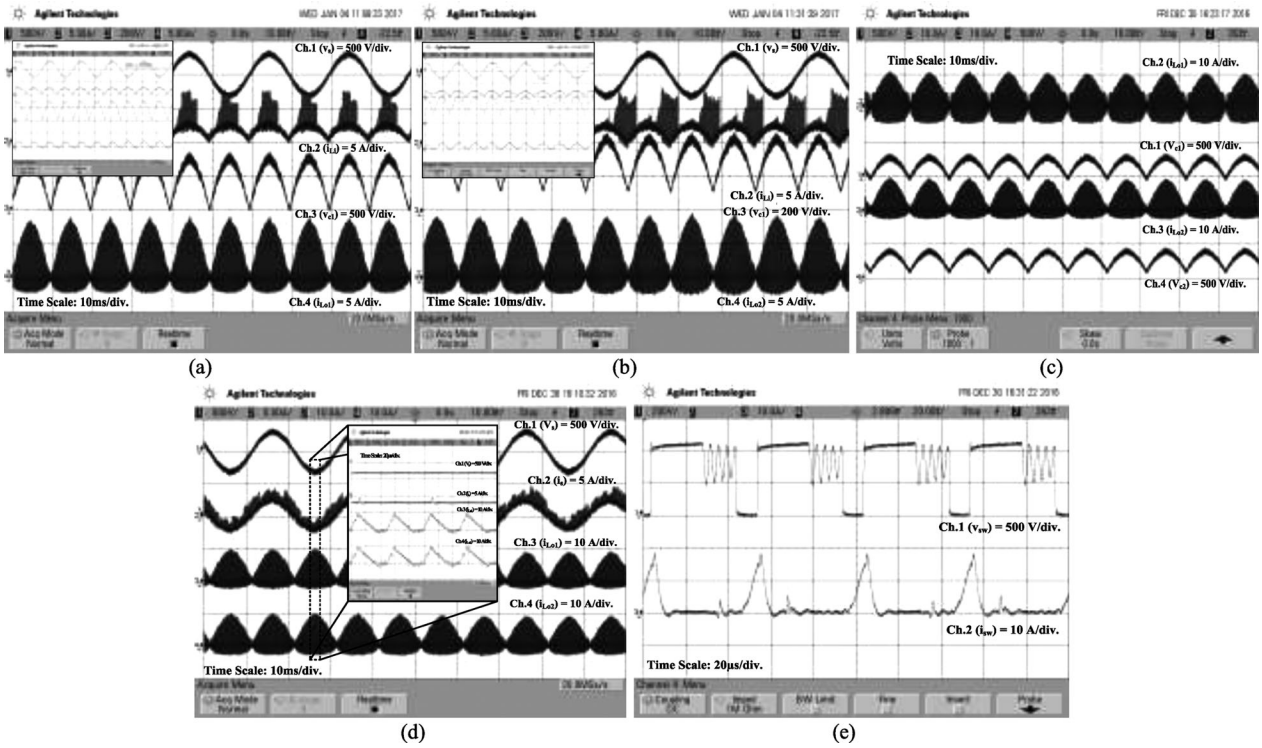


Fig. 8. Test results showing (a) current and voltage waveform through circuit components in SEPIC converter with high-resolution view (top right corner), (b) current and voltage waveform through circuit components in Cuk converter with high-resolution view (top right corner), (c) discontinuous current through output inductors L_{o1} and L_{o2} with continuous capacitor voltages (V_{c1} and V_{c2}), (d) PFC operation of proposed converter with enlarged view of waveform showing large freewheeling period which ensures DCM of operation, and (e) peak voltage and current stress across switching device during rated condition.

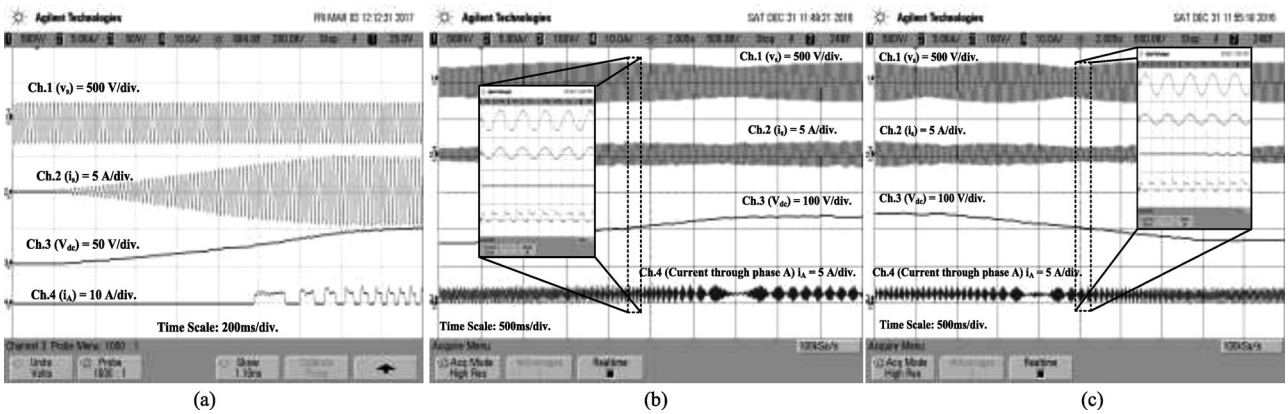


Fig. 9. Test results show the dynamic performance of proposed drive during: (a) starting, (b) change in dc link voltage from 170 to 250 V, and (c) change in dc link voltage from 250 to 170 V.

control is well obtained with this change in dc bus voltage. Similarly, the speed control is also demonstrated in Fig. 9(c) with sudden dip in dc link voltage from 250 to 170 V. During these dynamics conditions, enlarged views of are also shown in respective figures.

D. PFC and Improved Power Quality at AC Mains

The performance of proposed drive is examined on the basis of power quality indices measured from power quality analyzer (Fluke Make). The input voltage variation v_s is considered from 170 to 270 V ac such that variation in input current i_s is observed from 1.710 to 0.565 A. Fig. 10(a)–(c) shows obtained results at rated conditions as $v_s = 220$ V ac and dc link as 300 V dc. The input current THD is observed as 3.6% which is well under acceptable limit. Moreover, the motor draws rated power as 388 W. While considering the voltage dip, the supply voltage is considered as 170 V ac. Fig. 10(d)–(f) shows the obtained power quality indices at $v_s = 170$ V ac and dc link as 300 V dc. The input current THD is obtained as 3.1%. Similarly, an increase in supply voltage is considered as 270 V ac; therefore, the input current THD at $v_s = 270$ V and $V_{dc} = 300$ V is obtained as

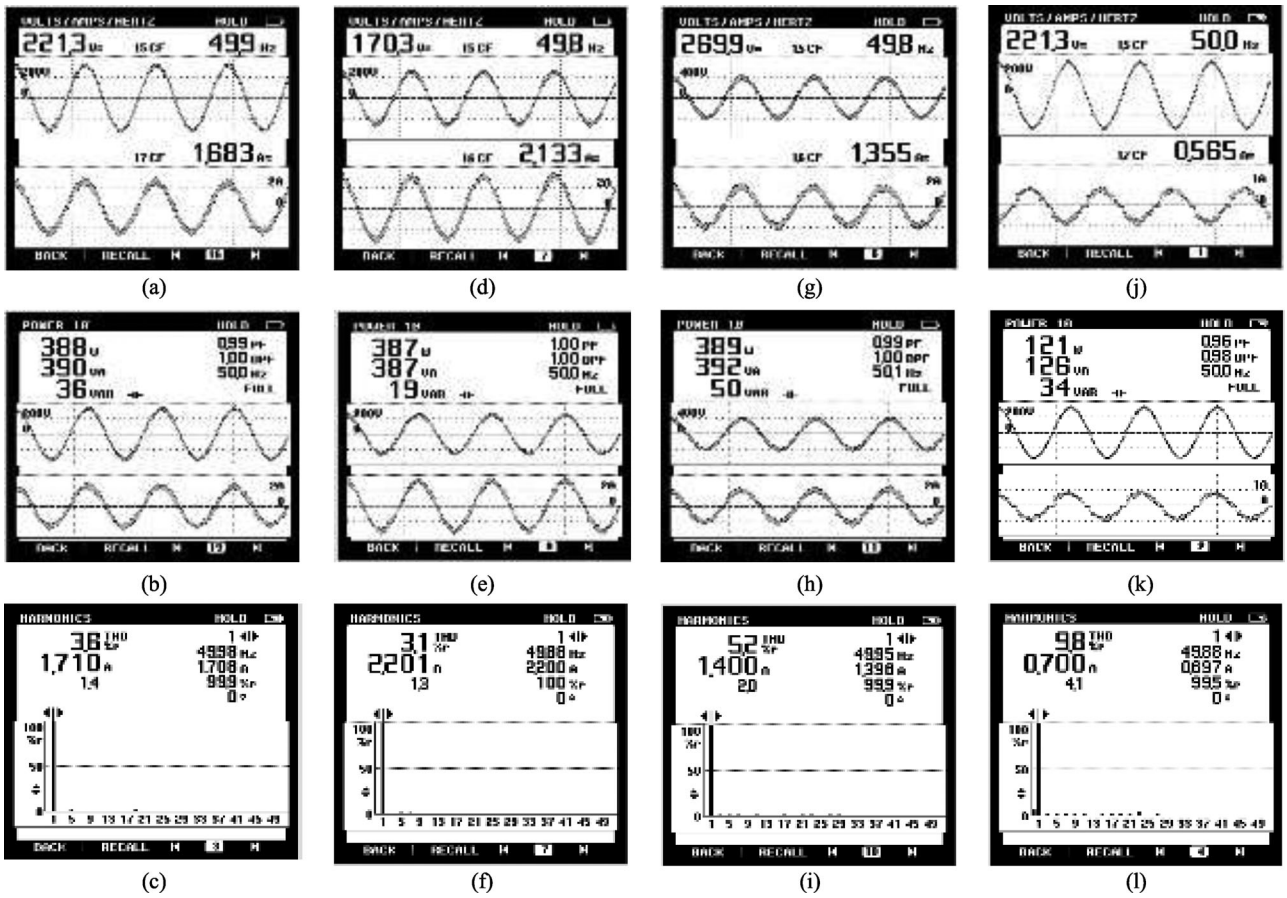
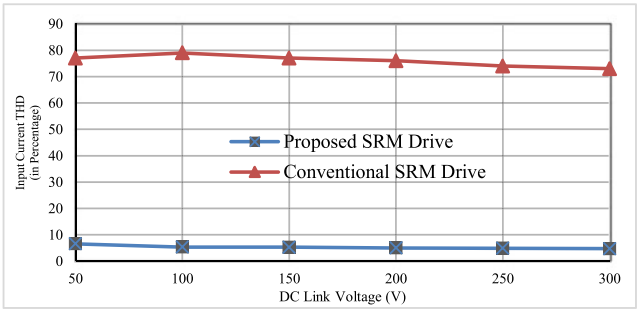


Fig. 10. Test result of proposed SRM drive on the basis of power quality indices with (a)–(c) $v_s = 220$ V, $V_{dc} = 300$ V, and P_{out} (output power) $= 388$ W, (d)–(f) $v_s = 170$ V, $V_{dc} = 300$ V, and P_{out} (output power) $= 387$ W, (g)–(i) $v_s = 270$ V, $V_{dc} = 300$ V, and P_{out} (output power) $= 389$ W, and (j)–(l) $v_s = 220$ V, $V_{dc} = 100$ V, and P_{out} (output power) $= 121$ W.

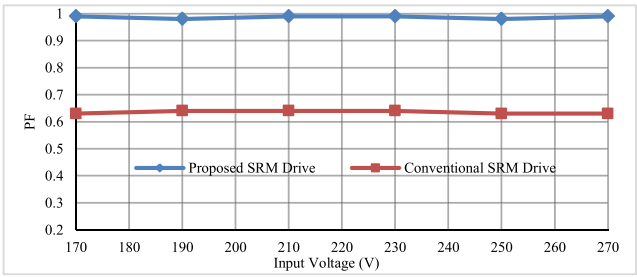
5.2% which is shown in Fig. 10(g)–(i). The motor performance is also evaluated at minimum dc link voltage as $V_{dc} = 100$ V with motor input power as 121 W. Moreover, input current THD is recorded as 9.8% as shown in Fig. 10(j)–(l). Thus, test results obtained present the excellent motor performance with improved power quality at supply mains.

E. Comparative Analysis of the Proposed Converter

The conventional SRM drive is fed with DBR, followed by a two bulky capacitors connected in series, which draws short duration peaky current pulse with poor power factor. However, the speed regulation is not possible in conventional configuration due to unregulated dc link voltage. Test results show that the input current THD obtained in the proposed drive is lying between 3.1% and 9.8% for complete range of dc bus voltage, i.e., from 100 to 300 V dc as shown in Fig. 11(a). Fig. 11(b) shows test results for supply voltage variation as 170–270 V ac. The proposed converter has featured balanced dual output voltages which appear as a best selection for a midpoint converter-fed SRM drive. The maximum voltage difference between two output voltages is obtained as 2.2 V, which is shown in Fig. 11(c). Fig. 11(d) shows a comparison on the basis of duty cycle and dc link voltage variation from 100 to 300 V dc. The duty cycle required in case of conventional Cuk and SEPIC converter configuration is more as compared to proposed Cuk–SEPIC-based configuration, which demonstrates the high voltage conversion ratio of the proposed converter. One of the demerits of the proposed converter is increased component count with additional diode, inductor, and capacitor. In order to calculate the efficiency of the proposed drive, the losses in each section of the drive are calculated. The separately measured losses include PFC converter loss, a midpoint converter-fed SRM drive loss, and loss associated with coupled dc motor operating as dc generator. The PFC converter losses are calculated by estimating converter input and output power using supply voltage, supply current, and converter output voltage and output current. The SRM losses include fixed core losses and variable copper loss. The midpoint converter is operated at fundamental frequency, thus switching losses can be neglected. Moreover, conduction loss in midpoint converter is considered which account 0.04% of the full load power. The losses in dc motor are calculated to determine output power of SRM. Fig. 11(e) shows the efficiency at different sections of the proposed drive. Table II presents a comparison of the proposed converter with simple buck boost, SEPIC, Cuk, and Zeta converters on the basis of component count, switching stress, and voltage conversion ratio.



(a)



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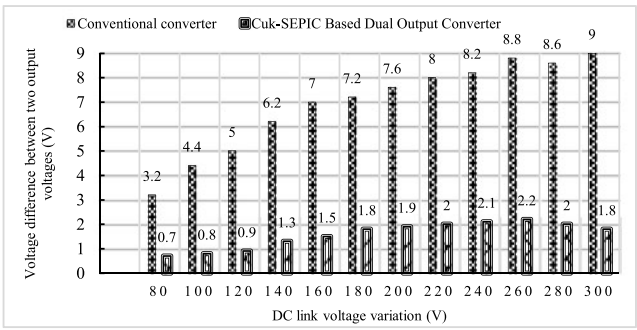
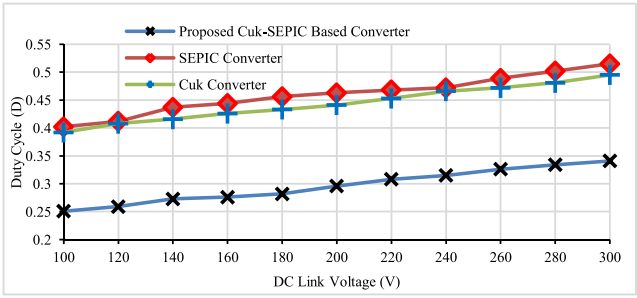
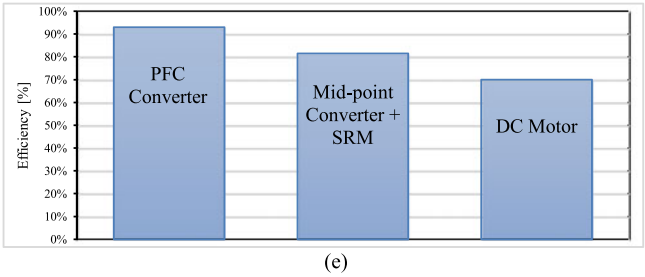


(c)



(d)



(e)

Fig. 11. Comparative study of proposed SRM drive with conventional drive on the basis: (a) input current THD at dc link voltage variation as 50–300 V dc, (b) input power factor at supply voltage variation as 170–270 V ac, (c) voltage difference between converter two output voltages at different dc link, (d) duty cycle variation at different dc link voltages, and (e) efficiency comparison at different sections of complete drive.

TABLE II
COMPARISON BETWEEN THE PROPOSED CONVERTER AND BASIC CONVERTER TOPOLOGIES

Attributes	Buck–Boost Converter [5], [6]	Cuk Converter [13], [15]	Sepic Converter [14], [15]	Zeta Converter [25]	Proposed Converter
Ultrafast Diode	1	1	1	1	2
Input Inductor	1	1	1	1	1
Output Inductor	0	1	1	1	2
Output Capacitor	1	1	1	1	2
Dual Output	No	No	No	No	Yes
Switching Device	1	1	1	1	1
Switch Stress	High	High	High	High	Low
Conduction Loss	High	High	High	High	Low
Voltage conversion ratio	Low	Medium	Medium	Medium	High

VII. CONCLUSION

The PFC-based dual output converter was proposed to feed SRM drive. This converter was derived while combining two basic converter configurations, i.e., Cuk converter and SEPIC converter. The proposed converter has featured self-balancing nature as both basic converters have same voltage conversion ratio. This converter is best suited as per the requirement of two balanced output voltages with one neutral point N. To obtain inherent PFC, a voltage follower approach was adopted. The output inductors were selected while ensuring the discontinuous inductor current. A prototype was developed to validate the performance of the proposed SRM drive. Moreover, test results demonstrated the DCM of operation as per the design. The observed power quality indices reflected the power quality improvement with reduced THD as per the given IEEE-519 standard. The motor performance was recorded for both dynamic and steady-state conditions and obtained test results depicted the excellent motor performance with improved power quality at supply side.

APPENDIX

The motor specifications for the four-phase, 8/6 pole SRM are as follows: rated power (P_{rated}) = 400 W; rated speed (ω_{rated}) = 1500 r/min; rated dc link voltage (V_{dc}) = 300 V; number of stator pole = 8; number of rotor pole = 6; number of phases = 4; phase resistance (R) = 0.7 Ω, unaligned inductance (L_u) = 12 mH, aligned inductance (L_a) = 110 mH; proportional gain (K_p) = 0.01; integral gain (K_i) = 0.0008; and saturation limit for duty cycle = 0.6. AC mains: single-phase 220 V, 50 Hz.

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