Design and Implementation of Modified SEPIC, ZETA, Cuk, Quasi Z-Source Converter for BLDC Drive System – A Comparative Analysis

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Abstract - For the system to work properly, it needs a suitable DC-DC converter. High output voltage and power, low harmonic distortion, low ripple content at both current and voltage, and high efficiency gain with fewer component requirements are just a few of the parameters for a good converter. A lot of the converters are made to meet some of the aforementioned requirements. With increased potential for BLDC drive-based Electric Vehicle (EV) applications, the converter chosen in this article is one that will be suitable for those applications. Before recommending a converter for a certain usage, its performance must be evaluated. Various converter topologies are considered. The validation process goes into great detail for the design topology, components used, equations created, loss calculations, and output performances. The majority of converters perform better than expected when choosing the right component values. Applications that work well are provided together with the findings of the converters and the related values.

***Keywords* - DC - DC converter, Modified SEPIC, ZETA, Quasi Z-Source, Cuk, BLDC and EV.**

INTRODUCTION - A lot of research is presently being done in order to create a sustainable DC to DC converter for use in Electric Vehicle (EV) applications. In the 1890s, the first electric vehicle emerged. However, throughout the past century, major efforts have been made to improve performance control in order to complete the adoption of EVs in the automotive sector. This research also focuses on the controlling performance improvement of EVs using batteries. The majority of EV components include an energy storage system, a motor, converter topologies, and control schemes. The motors used in electric vehicle applications include the Induction Motor (IM), Synchronous Motor (SM), Switched Reluctance Motor (SRM), DC motor, and Brush-Less DC (BLDC) Motor. Among these motors, the IM and SM have some efficiency limitations, while the SRM and DC motor causes sparking and acoustic noise, respectively. The motors discussed above have the following benefits over BLDC. It has a high power density, a strong starting torque, enhanced speed-torque characteristics, no acoustic noise or sparking, no winding on the rotary part, up to a 95% efficiency rate, and other benefits. So it makes sense to use a BLDC motor in electric vehicles. Extruder drive motors, actuators for industrial robots, feed drives for CNC machine tools, and linear and servo motors in the industrial field are further applications for BLDC motors. The following is a summary of the literature survey on selection converters. Fig. 1 displays the basic building blocks of the suggested approach.

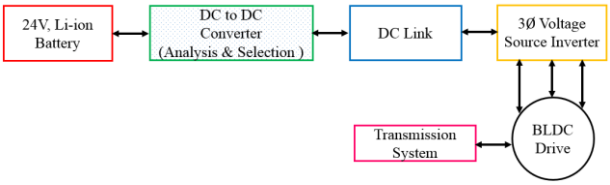


Fig. 1. General building blocks of the proposed approach

As suggested in [1], an SRM drive with a PFC-based converter combines Cuk and SEPIC converters. The SRM drive is commonly powered by a basic diode bridge rectifier, which draws peaky current with a low power factor and a high input-current THD. The next component is a sizable capacitor. The drawbacks include acoustic noise and having extra components. Power Factor Correction (PFC)-based Bridge-Less Luo (BL-Luo) converter-based BLDC motor drive was presented in [2]

One voltage sensor is used for the BLDC motor and PFC at ac mains speed control. The voltage follower control is used with a BL-Luo converter that is operating in the discontinuous inductor current mode. Because it permits low-frequency switching of the voltage source inverter for the motor's electronic commutation and lowers switching losses, a method of variable dc-link voltage is employed to control the BLDC motor's speed. The

suggested BLDC motor drive is designed to operate with better ac mains power quality and a range of speeds. A new single-phase AC-DC PFC bridgeless rectifier with a multiplier stage was invented in [3] with the goal of improving efficiency at low input voltage and reducing switch-voltage stress. To achieve an input current with a nearly unity power factor and minimum Total Harmonic Distortion (THD), the recommended architecture was designed to operate in Discontinuous Conduction Mode (DCM). The efficiency, THD, and power factor of a modified full-bridge SEPIC rectifier were evaluated using the architecture that was demonstrated. A modified Power Factor Correction Cuk Converter (PFCCC)-operated Voltage Source Inverter (VSI)-fed BLDC motor drive was developed in [4] for agricultural water pumping applications. To boost efficiency and PF and decrease the consequences of the system's low PF, PFC circuits are added to the AC input side of the water pumping system. Power Factor Correction (PFC) converters, such as the Zeta DC-DC converter in [5], are used to modify voltage to alter the speed of Permanent Magnet Brush-Less DC Motors (PMBLDCM).

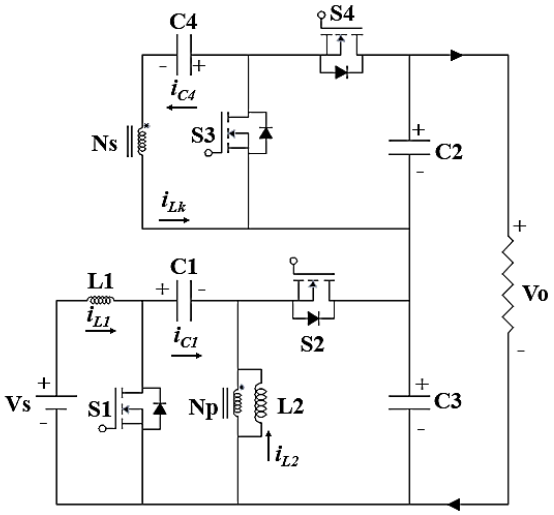
The recommended drive's detailed design, modelling, and performance are shown for an air conditioner using a PMBLDC motor rated at 0.817 kW and 1500 rpm. A novel bidirectional interleaved hybrid converter using linked inductors (CIs) was proposed in [6] in order to maximise the performance of the power train in battery electric vehicles (BEVs). Realize the integration of the DC/DC converter and DC/AC inverter in the BEV power train, acting as a backup generator to send emergency power straight to the home, with good performance in every operating mode. It can lower system costs and volume while boosting effectiveness and dependability. The interleaving structure is used in this case to increase output power, minimise input current and output voltage ripple, reduce power loss, and increase efficiency. The use of CIs of energy storage inductors enhances the performance of the proposed converter. Supercapacitors (SCs) and batteries may be used in an EV design to deliver dependable and quick energy transfer, as discussed in [7].

Power is moved between the abovementioned energy sources and the EV via a DC link coupled to a bidirectional interleaved dc-dc converter. The converter is investigated statistically and qualitatively, and as part of a comprehensive design process, a simple control system implementation is provided. A brand-new boost-based DC-DC converter without a transformer was proposed in study by [8]. Utilizing n levels of voltage multiplier cells and a charge-pump circuit (CPC), the voltage gain of the proposed converter was increased (VMC). By building a lab prototype with a power of 300 W, input and output voltages of 30 V and 310 V, respectively, and a switching frequency of 40 kHz, the performance of the converter is confirmed. The hybrid converter topology, also known as the SEPIC converter fed three-level Neutral-Point-Clamped (NPC) inverter topology, was developed to eliminate torque ripples. The outcomes of this study led to the development of a system that, as detailed in [9], significantly reduces torque ripple when compared to a system based on a two-level NPC inverter.[10]

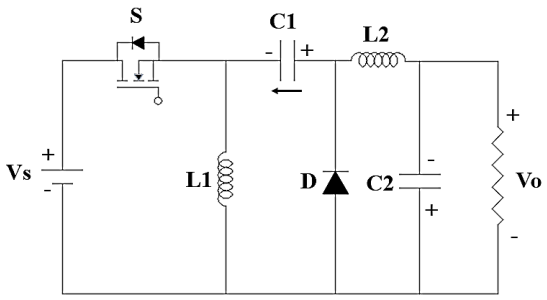
Identifying 2-kW BLDC-based EV applications with low ripple and high current output is the main objective of this work. The outcomes of several converter topologies' simulations are then contrasted. According to Modified SEPIC results, they are quite competitive with other converters. The rest of the paper is structured as follows: Output answers and reasons are presented after component design equations, simulated values, and design studies of various converter topologies. The paper then discusses ripple content analysis and comparative research.

II. DESIGN ANALYSIS OF CONVERTER TOPOLOGIES

The design considerations and analysis for the investigation of suitable low ripple and high power converters, the following topologies are taken into account: Modified SEPIC, ZETA, cuk, and Quasi Z-source converters. These converters' circuit configurations are shown in Fig. 2.



(a)



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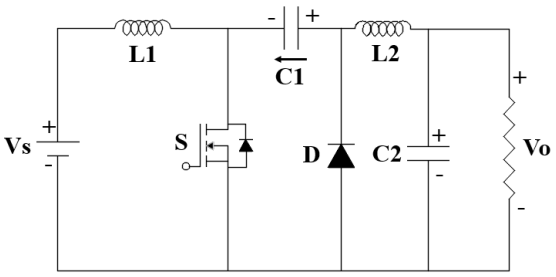

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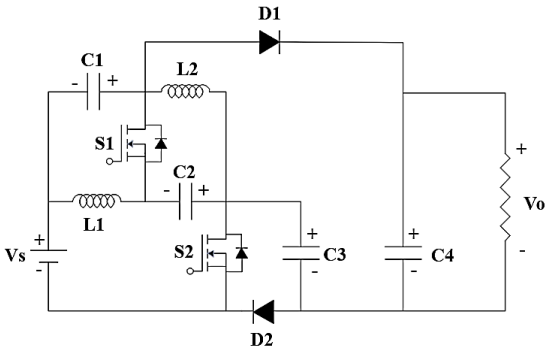


(d)

Fig. (2). Different converter topologies such as (a). Modified SEPIC topology (b). ZETA converter topology, (c). Cuk converter topology (d). Quazi Z-Source converter topology.

A. Modified SEPIC

The Modified SEPIC applications are high power, high current and static gain applications [11]. The Modified SEPIC consists of coupled inductor, leakage inductor L_1, magnetizing inductor L_2, four MOSFET switch S_1-S_4, two intermediate capacitors C_1 and C_4, output capacitor C_2 and C_3 and load resistor R. Fig. 2(a) displays the Modified SEPIC topology's circuit configuration.

Design Equations of Modified SEPIC

The Leakage and Magnetizing Inductance, L_1 & L_2 can be expressed as,

$$L = \frac{V_S D}{f_S * \Delta I_L} \quad (1)$$

For ΔI_L, assuming for design calculation as 4.8% of I_{Load}.

$$L_1 = L_2 = \frac{24 * 0.67}{33.3 * 0.048} = 10\ mH$$

Where, V_s - Source voltage (v), D - duty cycle, fs - switching frequency (kHz), ΔI_L - change in load currents. The Intermediate capacitors, C_1 & C_4 can be calculated from the following equation.

$$C = \frac{V_O D}{R * fs * \Delta I_C} \quad (2)$$

For ΔV_C, assuming for design calculation as 2% of V_o.

$$C_1 = C_4 = \frac{48 * 0.67}{1 * 33.3 * 0.96} = 1000\ \mu F$$

Where, V_o - output voltage (v), D - duty cycle, fs - switching frequency (kHz), ΔV_C - change in capacitive voltage. The Output filter capacitors, C_2 & C_3 are large enough to filter the output ripples.

$$C_2 = C_3 = 1200\ \mu F \text{ (Kept as constant)}$$

Component values are derived and used in the Modified SEPIC simulation, which is shown in Table 1, based on the aforementioned formulae. The output response of Modified SEPIC is illustrated in Fig. 3. The input voltage, V_s, is specified as 24 volts, and the supply current, I_s, is 95A. The converter produced a 41.2v output voltage and a 41.12A output current. It is 1.99 times for the voltage conversion ratio. The converter has an efficiency rate of 73.8%.

Table 1. Values used in simulation of Modified SEPIC

S.No	Components	Values
1	Leakage Inductor, L_1	10 mH
2	Intermediate Capacitor, C_1 & C_4	1000 µF
3	Magnetizing Inductor, L_2	10 mH
4	Output Capacitor, C_2 & C_3	1200 µF
5	Switch x 4	MOSFET
6	Resistive Load, R	100 Ω
7	Switching frequency, fs	33 kHz

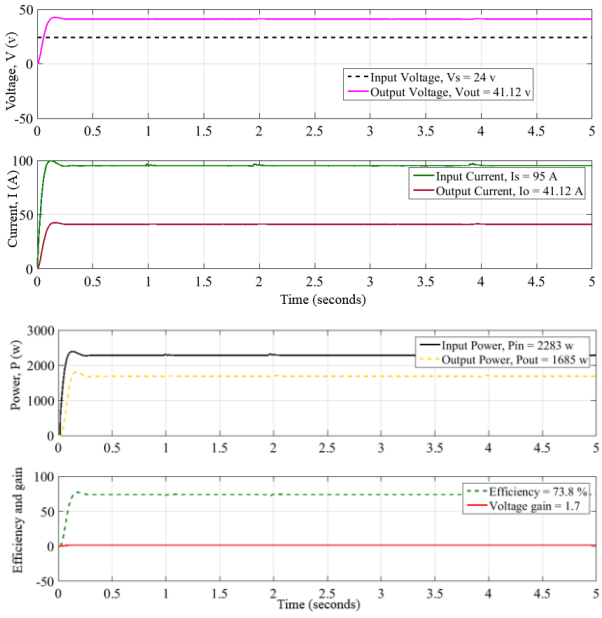


Fig. 3 Output response of Modified SEPIC

B. ZETA converter

The applications of ZETA converters are SMPS and automotive battery recharge from solar PV cells [12]. It consists of a single MOSFET switch, inductors L1 and L2, intermediate capacitors C1, output capacitor C2, and a load resistor R. Fig. 2(b) depicts the ZETA converter topology's circuit architecture.

Design Equations of ZETA converter

A straightforward Zeta converter design example is provided in the following section. The converter's input voltage is Vs = 24v, and its output must remain at 72v. The load resistance may be between 50 and 100Ω. The duty cycle D can be calculated by,

$$D = \frac{V_o}{V_d + V_o} \tag{4}$$

The inductors L_1 and L_2 can be obtained from the equation (13) and (14).

$$L_1 \geq \frac{(1-D)^2 * R_o}{2Df_s} \tag{5}$$

$$L_2 \geq \frac{(1-D) * R_o}{2f_s} \tag{6}$$

The sizing of capacitor C_1 can be expressed as,

$$C_1 \geq \frac{D * I_o}{\Delta V_{C1} * f_s}$$

Similarly, the sizing of capacitor C_2 can be expressed as,

$$C_2 \geq \frac{(1-D) * V_o}{8 * \Delta V_{C1} * L_2 * f_s^{\,2}} \tag{7}$$

Based on the above equations, component values are calculated and used in the simulation of ZETA converter, which is presented in Table 2.

Table 2. Components values used in simulation of ZETA converter

S.No	Components	Values
1	Inductors, L_1 & L_2	1.6 mH
2	Capacitor, C_1	150 µF
3	Output Capacitor, C_2	720 µF
4	Resistive Load, R	100 Ω
5	Switching frequency, fs	25 kHz

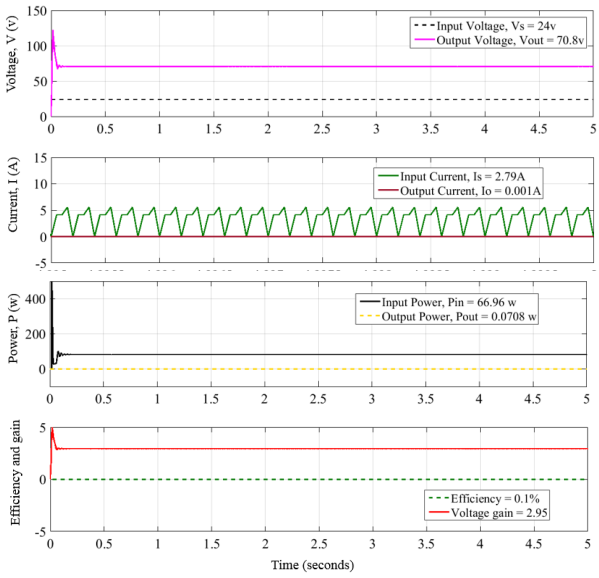


Fig. 4. Output response of ZETA converter

The output response of ZETA converter is illustrated in Fig. 4. The input voltage, V_s, is specified as 24 volts, and the supply current, I_s, is 2.79A. The converter produced a 70.8v output voltage and a 0.001A output current. It is 2.95 times for the voltage conversion ratio. The converter has an efficiency rate of 0.1%.

C. Cuk converter

In hybrid solar-wind energy systems, a Cuk converter is used as a regulator to maintain a constant output voltage where the input voltage is affected by the speed of the sun and wind. The voltage regulation for the DC application systems uses a Cuk converter [13] & [14]. The cuk converter consists of single MOSFET switch, inductors L_1 and L_2, intermediate storage capacitor C_1, output capacitor, C_2 and load resistor R. Fig. 2(c) depicts the Cuk converter's topology's circuit configuration.

Design Equations of CUK converter

The average value of input voltage is expressed as,

$$V_{in} = \frac{2\sqrt{2}V_s}{\pi} \tag{8}$$

The duty cycle ratio, D can be given as,

$$\frac{V_o}{V_s} = \frac{D}{1-D} \tag{9}$$

The input inductance, L_1 is calculated from,

$$L_1 = \frac{DV_{in}}{\Delta I L_1 f_s} \quad (10)$$

The output inductance, L_2 is calculated from,

$$L_2 = \frac{(1-D)DV_{dc}}{\Delta I L_2 f_s} \quad (11)$$

The intermediate capacitor, C_1 can be expressed as,

$$C_1 = \frac{DI_{dc}}{\Delta V_{C1} f_s} \quad (12)$$

The output capacitor, C_2 can be expressed as,

$$C_2 = \frac{I_{dc}}{\omega * \Delta V_{C2}} \quad (13)$$

Based on the above equations, component values are calculated and used in the simulation of Cuk converter, which is presented in Table 3.

Table 3. Values used in simulation of Cuk converter

S.No.	Components	Values
1	Inductors, L_1 & L_2	18 mH
2	Capacitor, C_1	200 µF
3	Output Capacitor, C_2	720 µF
4	Resistive Load, R	100 Ω

The output response of cuk converter is illustrated in Fig. 5. The input voltage, V_s, is specified as 24 volts, and the supply current, I_s, is 0.33 A. The converter produced a 23.1v output voltage and a 0.23A output current. It is 0.96 times for the voltage conversion ratio. The converter has an efficiency rate of 67.6%.

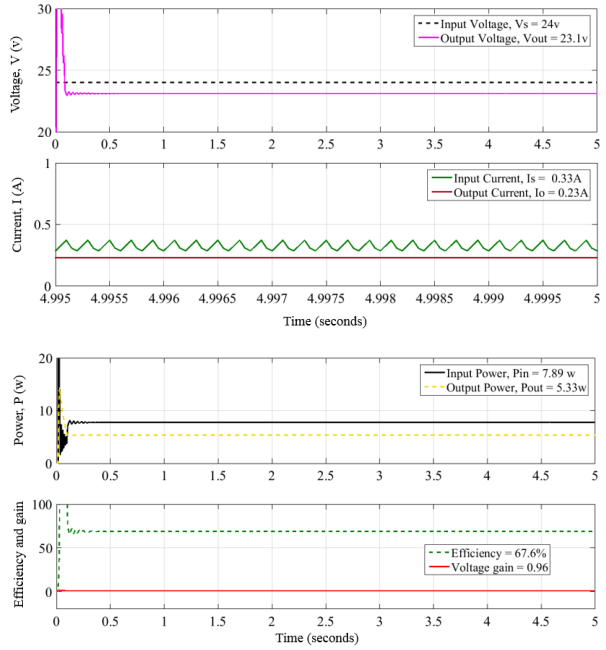


Fig. 5. Output response of Cuk converter

D. Quasi Z-source converter

The Quasi Z-source converter is compact, less expensive, and has a high efficiency [15]. It is used in wide range for high power with medium voltage applications.

It consists of two MOSFET switches, inductors L_1 and L_2, diodes D_1 and D_2, intermediate storage capacitor C_1, C_2, C_3 and C_4 and load resistor R. Fig. 2(d) depicts the circuit setup for the Quasi Z-source converter topology.

Design Equations of Quasi Z-source converter

The input inductor L_1 can be determined by,

$$L_1 \geq \frac{D(1-D)V_s}{\Delta i_{L1} f_s (1-2D)} \quad (14)$$

Similarly, inductor L_2 can be determined by,

$$L_2 \geq \frac{D(1-D)V_s}{\Delta i_{L2} f_s (1-2D)} \quad (15)$$

The Capacitors $C_{1\text{-}4}$ value can be determined by,

$$C_1 \geq \frac{I_{L2}(1-D)}{\Delta V_{C1} f_s} \quad (16)$$

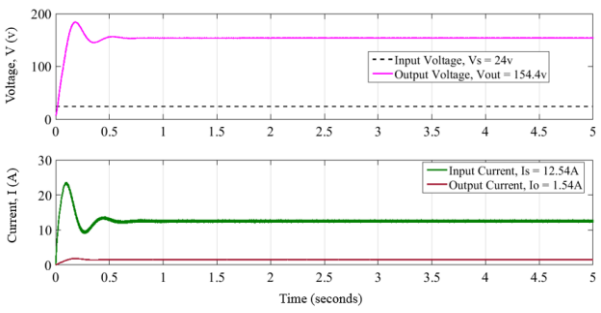
$$C_2 \geq \frac{I_{L2}(1-D)}{\Delta V_{C2} f_s} \quad (17)$$

$$C_3 \geq \frac{I_o}{\Delta V_{C3} f_s} \quad (18)$$

$$C_4 \geq \frac{I_o(1-D)}{\Delta V_{C4} f_s} \quad (19)$$

Table 4. Components values used in simulation of Quasi Z-source converter

S.No	Components	Values
1	Input Inductor, L_1	20 mH
2	Input Filter Capacitor, C_1	200 µF
3	Magnetizing inductor, L_2	20 mH
4	Storage Capacitors, C_2 & C_3	650 µF
5	Output Capacitor, C_4	1000 µF
6	Resistive Load, R	100 Ω



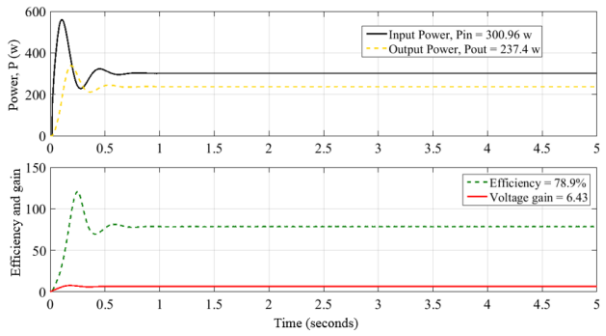


Fig. 6. Output response of Quazi Z-Source converter

The output response of Quazi Z-source converter is illustrated in Fig. 6. The input voltage, V_s, is specified as 24 volts, and the supply current, I_s, is 12.54 A.

The converter produced a 154.4v output voltage and a 1.54A output current. It is 6.43 times for the voltage conversion ratio. The converter has an efficiency rate of 78.9%.

III. COMPARATIVE ANALYSIS

For the purpose of comparison, all of the aforementioned converters are powered by 24v Li-ion batteries with a combined maximum current capacity of 110Ah.

The output responses are analysed in the subsequent part in order to determine the appropriate converter with the least output ripple and a high enough current to power 2kW BLDC motor-based electric vehicles. The output voltage that was obtained from the 24 volt battery supply is where the analysis begins.

Analysis of the voltage gain value is followed by consideration of input current ripple. The output load current is directly proportional to the input ripple voltage amplitude. At maximum output load, the input ripple amplitude reaches its maximum value. Additionally, the duty cycle of the converter affects the voltage ripple's amplitude. Without considerably raising the current stress and losses, one capacitor and one inductor can be added to provide the input current ripple cancellation. But by changing the remaining component values that are present in the converter topology, it is intended to reduce the current ripple. The input current ripple analysis is presented in Fig. 8 and output voltage waveform is given in Fig.7

In a DC circuit, output voltage ripple wastes energy and has a variety of unfavourable impacts, including component heating, noise and distortion, and the potential for poor operation of digital circuits. A voltage regulator and an electronic filter are both capable of eliminating ripple and it is presented in Fig.9 and Fig.10. Many issues may result from a strong ripple current. For instance, the switching power supply may interpret this current draw as a fault condition if the ripple exceeds around 5% of the DC output current, in which case the over-current safety circuits may cause the supply to be shut down.

The load could lead to instability in the control loops if the pulse rate of the load is harmonically connected to the power supply switching frequencies. High ripple currents have the potential to severely overload switching supply outputs and accelerate their failure.

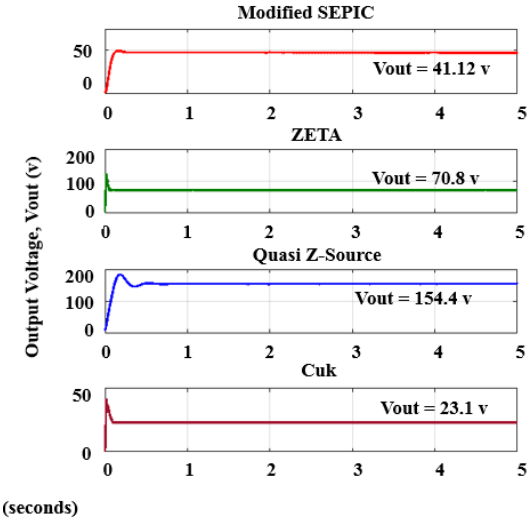


Fig. 7. Output voltage obtained from different converter topologies

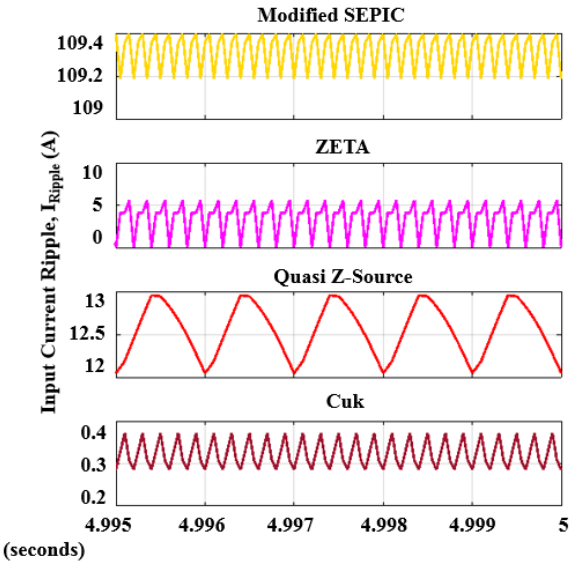


Fig. 8. Input current ripple analysis

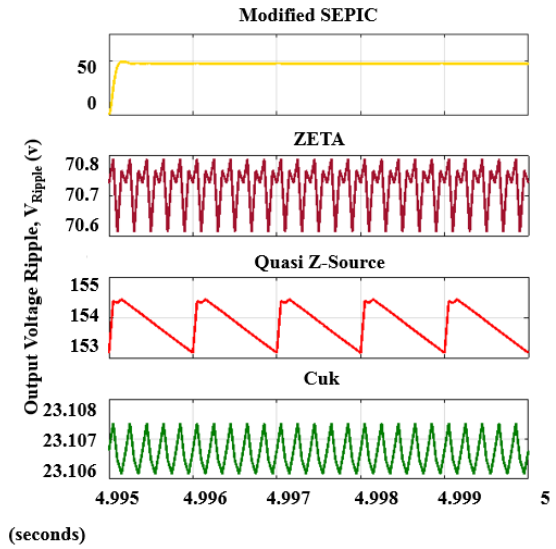


Fig. 9. Output voltage ripple analysis

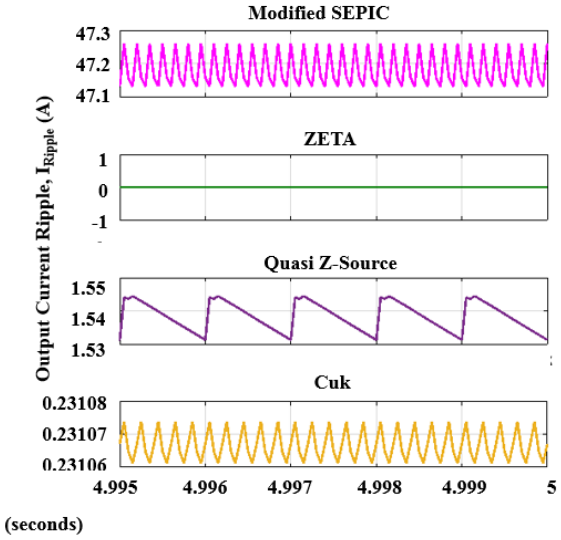


Fig. 10. Output current ripple analysis

The comparative analysis between the converter topologies values are tabulated in Table 5 and 6.

Table 5. Comparison of efficiency and voltage gain

	P_{in} ,w	P_{out}, w	η, %	n
Modified SEPIC	2283	1685	73.8	1.7
ZETA	66.96	0.0708	0.1	2.95
Cuk	7.89	5.33	67.6	0.96
Quasi Z-Source	300.96	237.4	78.9	6.43

IV. CONCLUSION

We conclude our analysis of a range of converter topology properties, including input and output voltage and current, ripple factor, efficiency, voltage gain, and component losses. The use of Modified SEPIC converters is suggested for BLDC-based EV applications.

The Modified SEPIC converter has a higher voltage gain ratio as a result. These are also incredibly tiny losses in comparison to other losses. The SEPIC's current output allows for a 2kW BLDC drive that can be used to power the vehicles.

Table 6. Comparative analysis of various converters

Input voltage, Vs = 24v and Switching frequency, fs = 25 kHz

Converter topologies	**Input current, A**	**Output voltage, v**	**Output current, A**	**Reduced Output ripple, %**	**No. of components**	**Applications**
Modified SEPIC	95	41.12	41.12	0.30	11	High Power, High Current and Static Gain Applications
ZETA	2.79	70.8	0.001	0.40	6	SMPS and automotive battery recharge from solar PV cells
Cuk	0.33	23.1	0.23	0.34	6	as a regulator to maintain a constant output voltage
Quasi Z-Source	12.54	154.4	1.54	0.42	10	Wide range for high power with medium voltage applications

REFERENCES

[1]. A. Anand and B. Singh, "Power Factor Correction in Cuk–SEPIC-Based Dual-Output-Converter-Fed SRM Drive", *IEEE Transactions of Industrial Electronics*, vol. 65, no. 2, pp. 1117-1127, Feb. 2018. https://doi.org/10.1109/TIE.2017.2733482.

[2]. Bhim Singh, Vashit Bist, Chandra A, and Al-Haddad K "Power Factor Correction in Bridgeless-Luo Converter fed BLDC Motor Drive", *IEEE Transactions of Industry Applications*, Vol. 51, No. 2, pp. 1179 - 1188, 2015. https://doi.org/10.1109/TIA.2014.2344502.

[3] Al-Gabri AM, Fardoun AA and Ismail EH, "Bridgeless PFC modified SEPIC rectifier with extended gain for universal input voltage applications", *IEEE Transactions of Power Electronics*, vol.30, no.8, pp.4272- 4282, 2015. https://doi.org/10.1109/TPEL.2014.2351806.

[4]. N. Kumarasabapathy & M. Ramasamy, "Modified isolated power factor correction Cuk-converter fed BLDC motor drive with Fuzzy Logic Controller for pumping applications" *Journal of the Chinese Institute of Engineers*, Vol. 43, no. 6, pp. 553 - 565, July 2020. https://doi.org/10.1080/02533839.2020.1777204.

[5]. Dinesh Gopal, Umasankar Periasamy and Mohana Periyasamy, "Fuzzy and PID Controllers for Buck-Boost Converter Fed Bridgeless BLDC Motor over Cloud", *International Conference on Intelligent Data Communication Technologies and Internet of Things (ICICI)*, pp. 1328-1337, Jan. 2019. https://doi.org/10.1007/978-3-030-03146-6_155.

[6]. Hedra Saleeb, Khairy Sayed, Ahmed Kassem and Ramadan Mostafa, "Control and analysis of bidirectional interleaved hybrid converter with coupled inductors for electric vehicle applications", *Electrical Engineering*, Springer Publications, Nov. 2019. https://doi.org/10.1007/s00202-019-00860-3.

[7]. Rodnei Regis de Melo, Fernando Lessa Tofoli, Sergio Daher and Fernando Luiz Marcelo Antunes, "Interleaved bidirectional DC - DC converter for electric vehicle applications based on multiple energy storage devices", *Electrical Engineering*, Springer Publications, May 2020. https://doi.org/10.1007/s00202-020-01009-3.

[8]. Hamed Pourfarzad, Mohammad Saremi and Tohid Jalilzadeh, "An extended high‐voltage‐gain DC-DC converter with reduced voltage stress on switches/diodes", *Electrical Engineering*, Springer Publications, June 2020. https://doi.org/10.1007/s00202-020-01040-4.

[9]. Vaiyapuri Viswanathan & Seenithangom Jeevananthan, "Hybrid converter topology for reducing torque ripple of BLDC motor", *IET Power Electronics*, Vol. 10, No. 12, pp. 1572-1587, 2017. https://doi.org/10.1049/iet-pel.2015.0905.

[10]. Jin Li, Jinjun Liu, Dushan Boroyevich, Paolo Mattavelli and Yaosuo Xue, "Three-level Active Neutral-Point-Clamped Zero-Current-Transition Converter for Sustainable Energy Systems", *IEEE Transactions on Power Electronics*, Vol. 26, no. 12, pp. 3680 - 3693, Dec. 2011. https://doi.org/10.1109/TPEL.2011.2161890.

[11]. Benlafkih Abdessamad, Krit Salah-ddine and Chafik Elidrissi Mohamed, "Design and Modeling of DC/DC Boost Converter for Mobile Device Applications", *International Journal of Science and Technology*, Vol. 2, no. 5, pp. 394 - 401, May 2013.

[12]. M. Gildersleeve, H.P. Forghani-zadeh, and G.A. Rincon-Mora, "A Comprehensive Power Analysis and a Highly Efficient, Mode-Hopping DC-DC Converter", *IEEE Asia-Pacific Conference on ASIC*, pp. 153-156, 2002.

[13]. Dong Liu, Yanbo Wang, Qi Zhang and Zhe Chen, "ZVZCS Full Bridge Three-Level DC/DC Converter with Reduced Device Count", *IEEE Transactions on Power Electronics*, Vol. 35, no. 10, pp. 9965 - 9970, Feb. 2020. https://doi.org/10.1109/TPEL.2020.2977227.

[14]. A.B. Jorgensen, "Derivation, Design and Simulation of ZETA converter", *IEEE TechRix*. https://doi.org/10.36227/techrxiv.16732825.v1.

[15]. V. Bist and B. Singh, "PFC Cuk converter-fed BLDC motor drive", *IEEE Transactions on Power Electronics*, Vol. 30, no. 2, pp. 871-887, Mar. 2014. https://doi.org/10.1109/TPEL.2014.2309706.