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Department of Electrical and Electronics Engineering

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16EE267-Project Work (Final Viva Voce); Batch 2019-2023

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Design and Development of Modified SEPIC Converter for BLDC Drive

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AIM & OBJECTIVE

AIM : To compare and analyze with various converters and to prove modified SEPIC Converter is suitable for BLDC drive system for better efficiency.

OBJECTIVE : The main objective of this project is to design and develop modified SEPIC converter which is suitable for BLDC based system with increased potential and high power rating of applications. It has better efficiency, minimal ripple output, low harmonic distortion and high current and voltage.

LITERATURE SURVEY

S.no	Title	Author	Inference
1	Design and implementation boost converter with constant voltage in dynamic load condition	R. Rakhmawati, Suhariningsih, D.Andriawan and F.D.Murdianto (2017),International Seminar on ATIC (iSemantic), 2017, pp. 273- 278.	Basic designing consideration and simulation work of boost converter.
2	An improved soft switching PWM FB dc/dc converter for reducing conduction loss	E. S. Kim and K. Y. Joe et al(1996), Proc.IEEE PESC Rec.,pp. 651–657, 1996.	Overview of pulse width modulated full bridge DC-DC converter and implementing soft switching approach with minimized conduction losses on the converter
3	Zero voltage and zero current switching full bridge PWM converter for high power applications	J. G. Cho, J. Sabate, G. Hua, and F. C. Lee(2006)	Methodology to overcomes limitations of the ZVS-FB-PWM converter such as high circulating energy, severe parasitic ringing on the rectifier diodes, and limited ZVS load range for lagging leg switches.

EXISTING SYSTEM

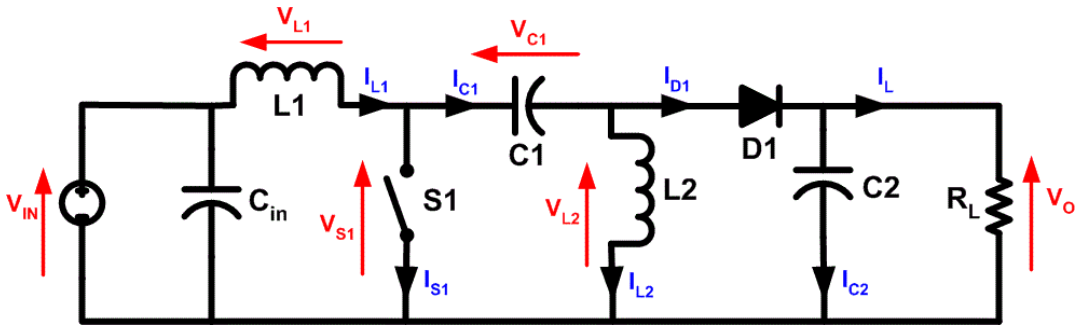


Figure: Existing System for SEPIC Converter

- Like the buck–boost converter, the SEPIC has a pulsating output current.
- The similar Cuk converter does not have this disadvantage, but it can only have negative output polarity, unless the isolated Cuk converter is used.
- Since the SEPIC converter transfers all its energy via the series capacitor, a capacitor with high capacitance and current handling capability is required.
- The fourth-order nature of the converter also makes the SEPIC converter difficult to control, making it only suitable for very slow varying applications.
- Complex Design: The design of a SEPIC converter is more complex than that of a conventional buck or boost converter. This complexity makes it difficult to troubleshoot and may require specialized skills to design.
- More Components: The SEPIC converter requires more components than a conventional buck or boost converter.

PROPOSED SYSTEM

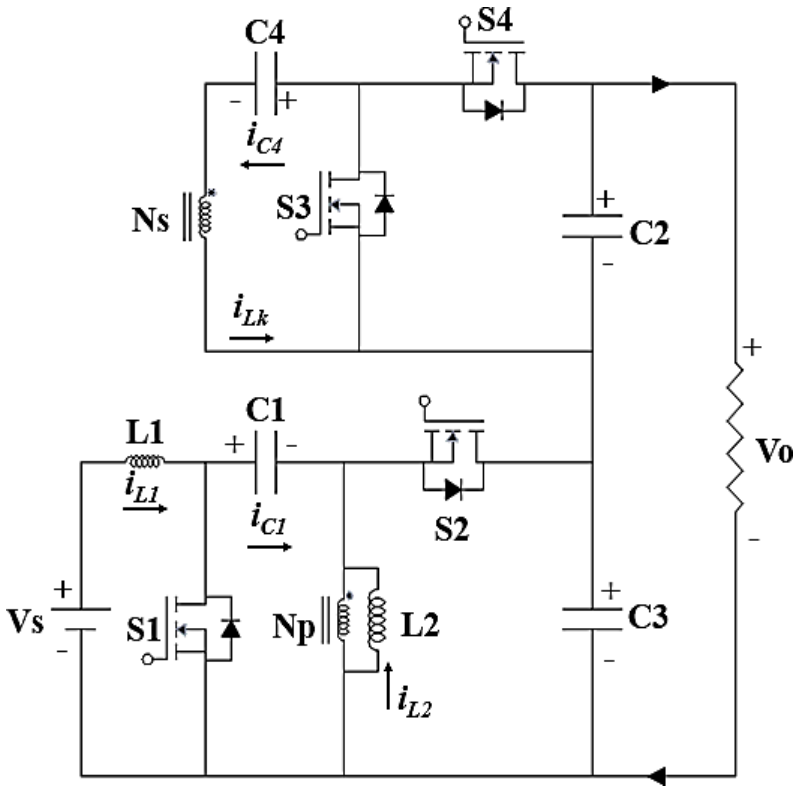
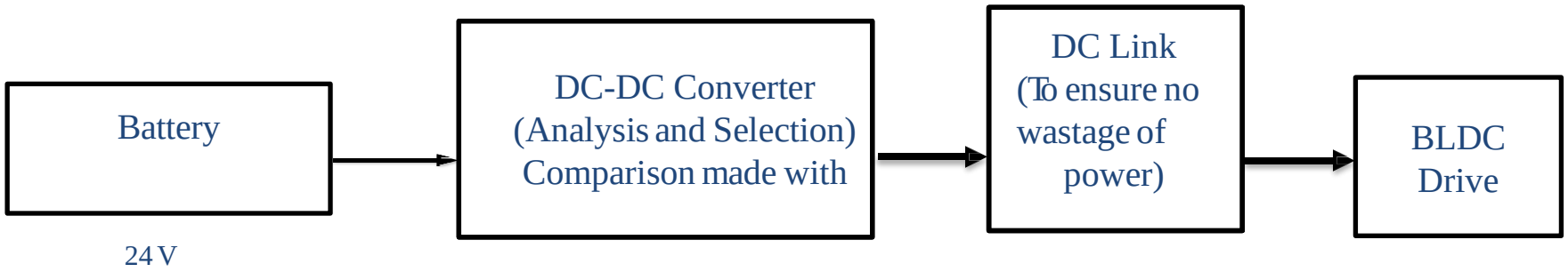


Figure: Circuit Diagram of Modified SEPIC Converter

- Better Efficiency: A modified SEPIC converter can offer higher efficiency compared to the conventional SEPIC converter. This is achieved by reducing the voltage stress on the switch and minimizing the switching losses.
- Improved Power Density: The modified SEPIC converter can achieve higher power density than the conventional SEPIC converter due to the reduced size and weight of the circuit.
- Wide Input Voltage Range: A modified SEPIC converter can operate over a wide input voltage range, making it suitable for a variety of applications. This is because it can maintain a constant output voltage regardless of input voltage variations.
- Reduced EMI Noise: The modified SEPIC converter can be designed with improved EMI filtering techniques, which can reduce the electromagnetic interference (EMI) noise generated by the circuit.

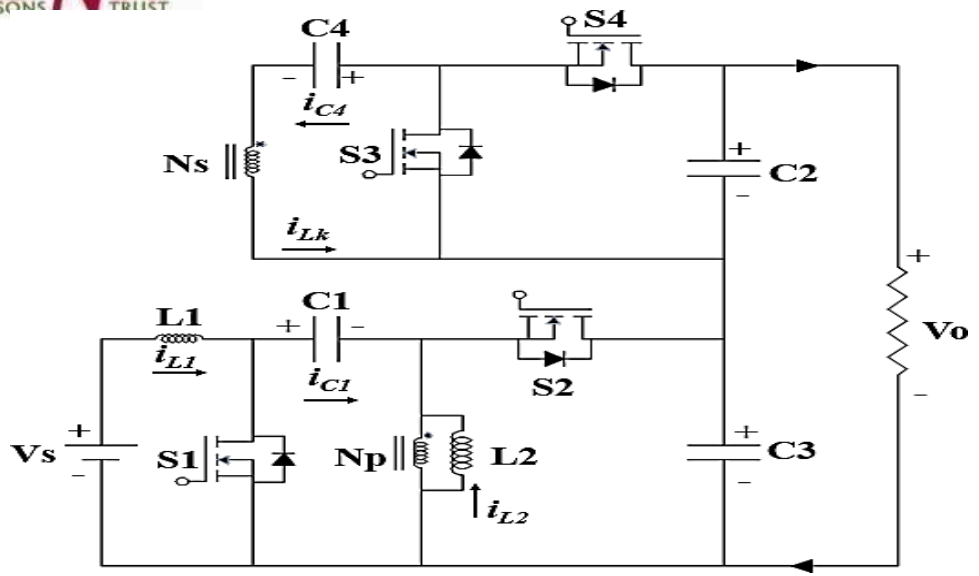
PROPOSED BLOCK DIAGRAM



1. **Modified SEPIC Converter**
2. Zeta Converter
3. Quasi Z-source Converter
4. Cuk Converter

Figure: Block diagram

MODIFIED SEPIC



S.No	Components	Values
1	Leakage Inductor, L1	10 mH
2	Intermediate Capacitor, C1 &C	1000 µF
3	Magnetizing Inductor,L2	10 mH
4	Output Capacitor,C2&C3	1200 µF
5	Switching frequency, fs	33 kHz
6	Resistive Load,R	100 Ω
7	Switch x 4	MOSFET

Design Equations of Modified SEPIC

The Leakage and Magnetizing Inductance, L1 & L2 can be expressed as,

$$L = \frac{V_S D}{f_S * \Delta I_L} \quad (1)$$

For ΔIL, assuming for design calculation as 4.8% of **I Load.**

$$L_1 = L_2 = \frac{24 * 0.67}{33.3 * 0.048} = 10\ mH$$

Where, Vs - Source voltage (v), D - duty cycle, fs - switching frequency (kHz), ΔIL– change in load currents.

The Intermediate capacitors, C1 & C4 can be calculated from the following equation.

$$C = \frac{V_O D}{R * fs * \Delta I_C} \quad (2)$$

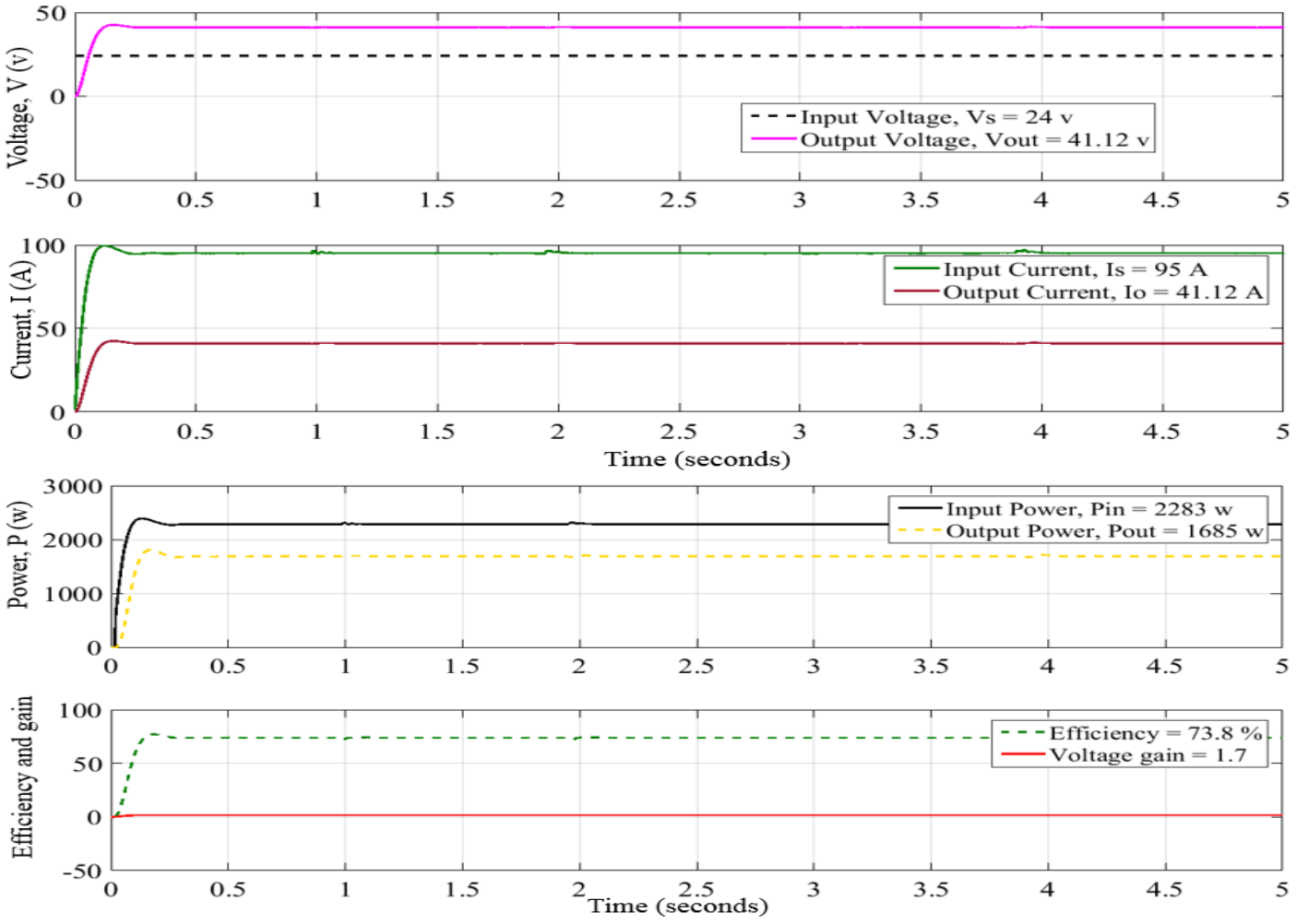
For ΔVC, assuming for design calculation as 2% of **Vo**.

$$C_1 = C_4 = \frac{48 * 0.67}{1 * 33.3 * 0.96} = 1000\ \mu F$$

Where, Vo- output voltage (v), D - duty cycle, fs - switching frequency (kHz), ΔVC - change in capacitive voltage. The Output filter capacitors, C2 & C3 are large enough to filter the output ripples.

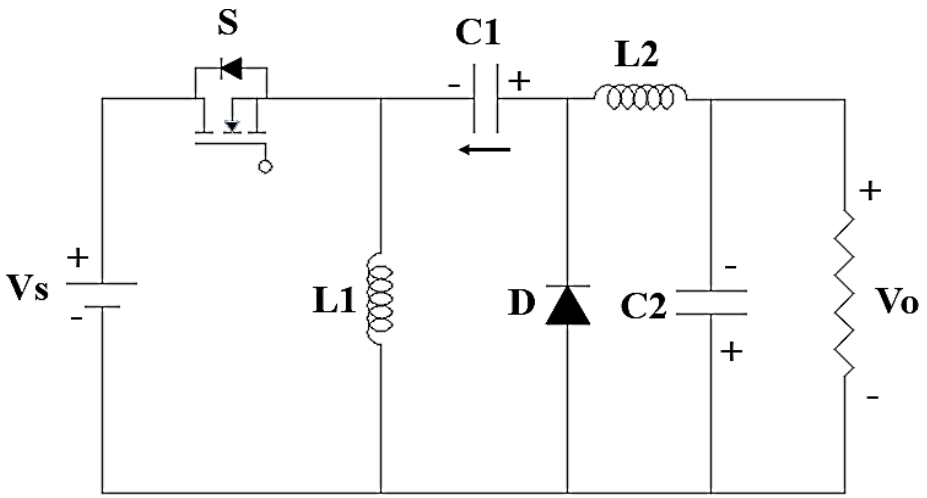
$$C_2 = C_3 = 1200\ \mu F \text{ (Kept as constant)}$$

MODIFIED SEPIC



Design Parameter	Rating
Input Parameters	
Input Voltage,Vs	**24 V**
Switching Frequency, f	**25 kHz**
Obtained Output	
Output Voltage,Vout	**41.12 V**
Output Current, Iout	**41.12A**
Overall Efficiency,ŋ	**73.8%**

ZETA CONVERTER



S.No	Components	Values
1	Inductors, L1 & L2	1.6 mH
2	Capacitor, C1	150 µF
3	Output Capacitor, C2	720 µF
4	Resistive Load, R	100 Ω
5	Switching frequency, fs	25 kHz

Design Equations of ZETA converter

A straightforward Zeta converter design example is provided in the following section. The converter's input voltage is Vs = 24v, and its output must remain at 72v. The load resistance may be between 50 and 100Ω. The duty cycle D can be calculated by,

$$D = \frac{V_o}{V_d + V_o} \qquad (4)$$

The inductors L1 and L2 can be obtained from the equation (5) and (6).

$$L_1 \geq \frac{(1-D)^2 * R_o}{2Df_s} \qquad (5)$$

$$L_2 \geq \frac{(1-D) * R_o}{2f_s} \qquad (6)$$

The sizing of capacitor C1 can be expressed as,

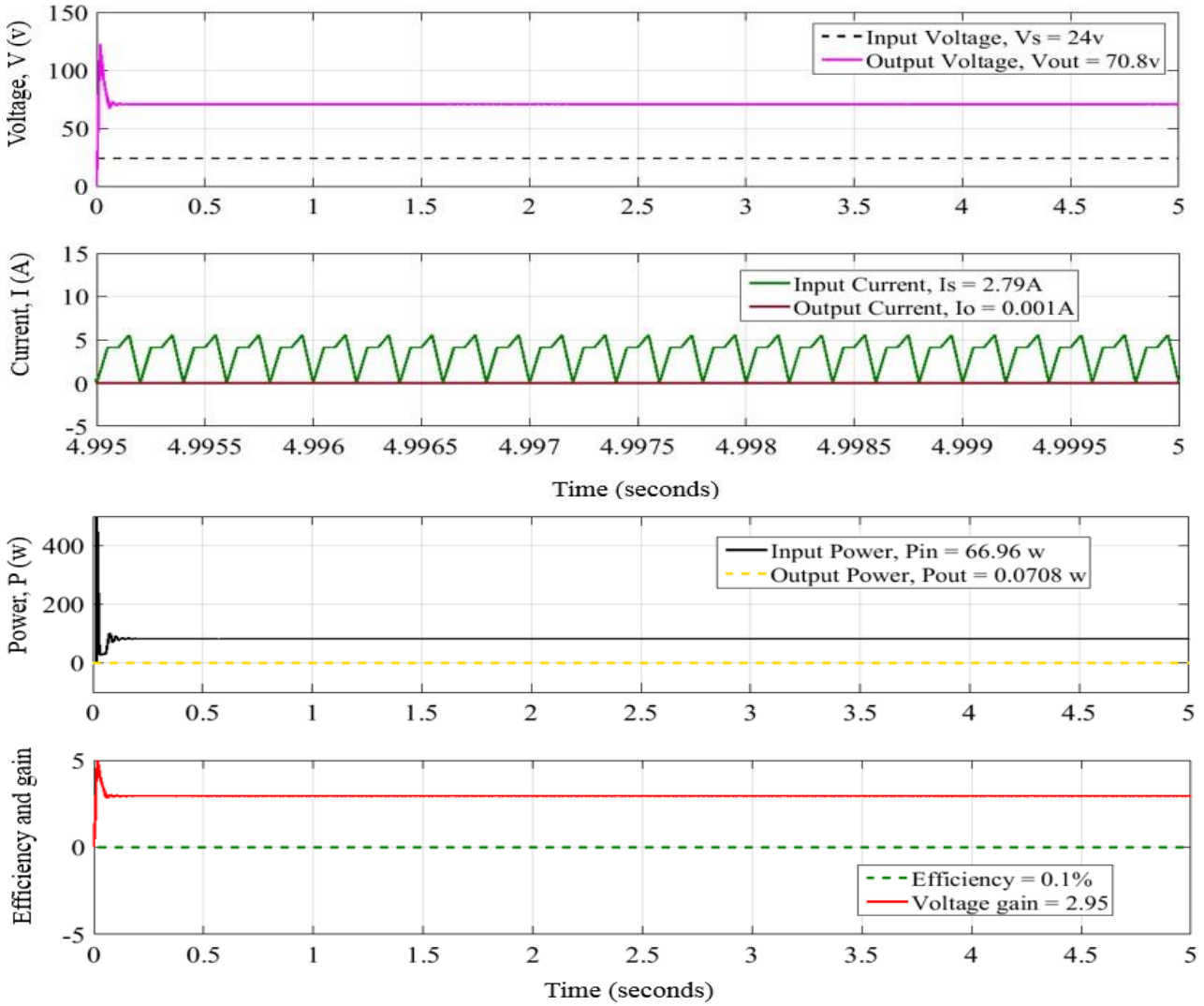
$$C_1 \geq \frac{D * I_o}{\Delta V_{C1} * f_s}$$

Similarly, the sizing of capacitor C2 can be expressed as,

$$C_2 \geq \frac{(1-D) * V_o}{8 * \Delta V_{C1} * L_2 * {f_s}^2}$$

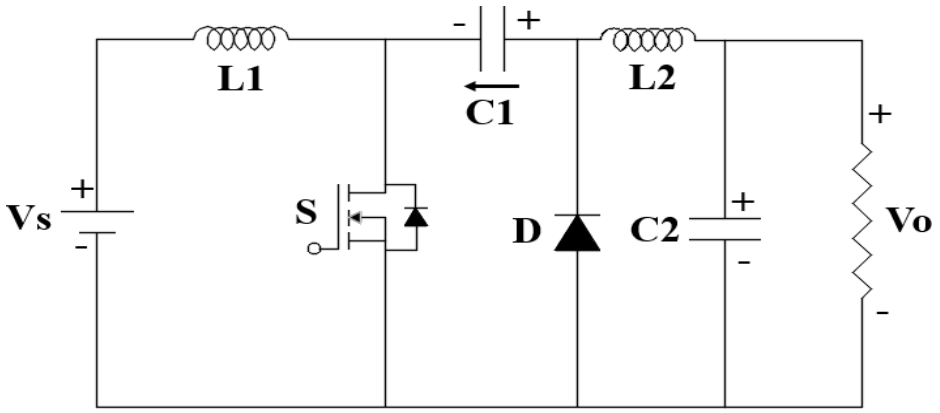
Based on the above equations, component values are calculated and used in the simulation of ZETA converter

ZETA CONVERTER



Design Parameter	Rating
Input Parameters	
Input Voltage,Vs	**24 V**
Switching Frequency, f	**25 kHz**
Obtained Output	
Output Voltage,Vout	**70.8 V**
Output Current, Iout	**0.001A**
Overall Efficiency,ɳ	**0.1%**

CUK CONVERTER



S.NO	COMPONENT	VALUE
1	Inductors, L1 & L2	18 mH
2	Capacitor, C1	200 µF
3	Output Capacitor, C2	720 µF
4	Resistive Load, R	100 Ω

Design Equations of CUK converter

The average value of input voltage is expressed as,

$$V_{in} = \frac{2\sqrt{2}V_s}{\pi} \quad (8)$$

The duty cycle ratio, D can be given as,

$$\frac{V_o}{V_s} = \frac{D}{1-D} \quad (9)$$

The input inductance, L1 is calculated from, 10

$$L_1 = \frac{DV_{in}}{\Delta I L_1 f_s} \quad (10)$$

The output inductance, L2 is calculated from,

$$L_2 = \frac{(1-D)DV_{dc}}{\Delta I L_2 f_s} \quad (11)$$

The intermediate capacitor, C1 can be expressed as,

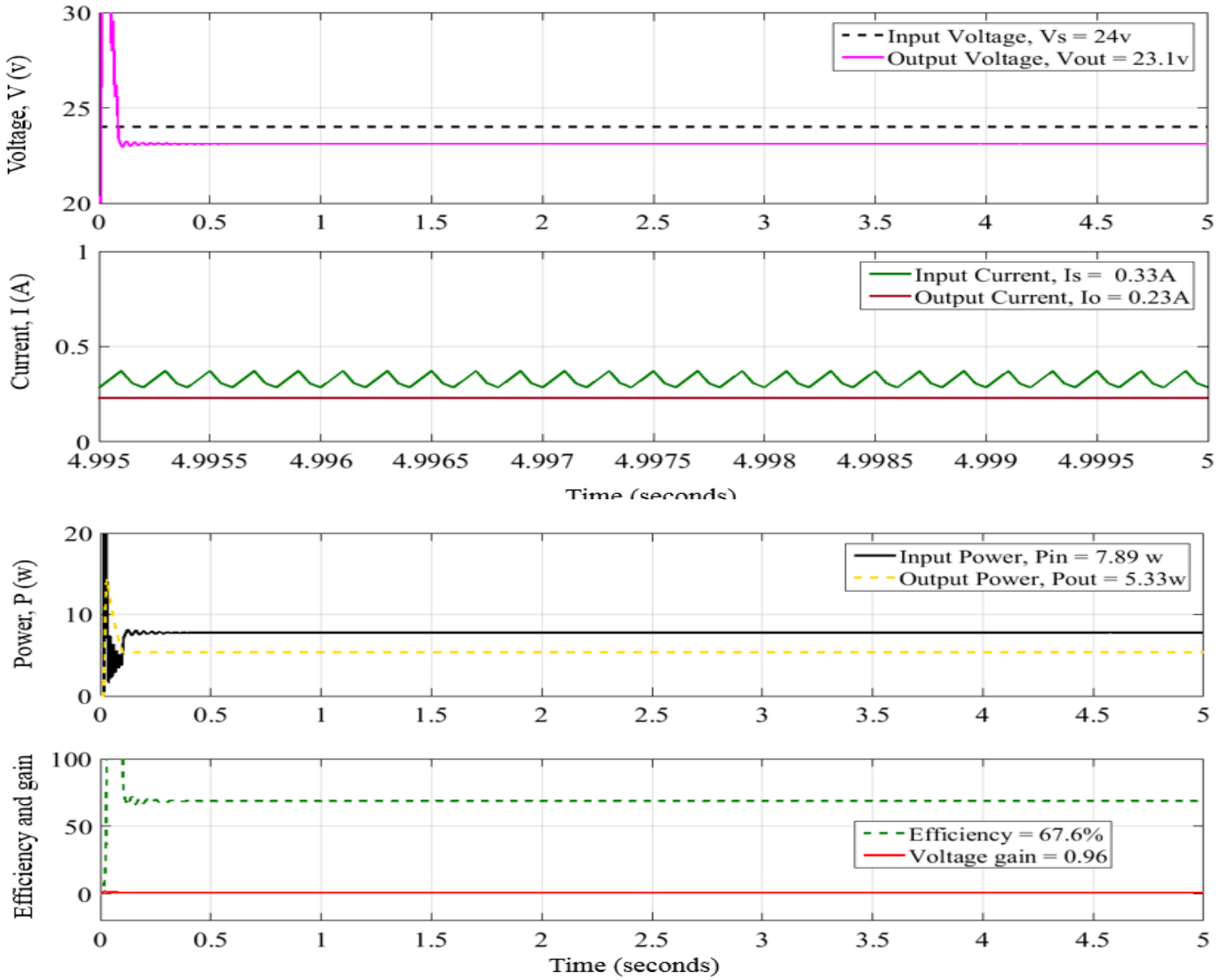
$$C_1 = \frac{DI_{dc}}{\Delta V_{C_1} f_s} \quad (12)$$

The output capacitor, C2 can be expressed as,

$$C_2 = \frac{I_{dc}}{\omega * \Delta V_{C2}} \quad (13)$$

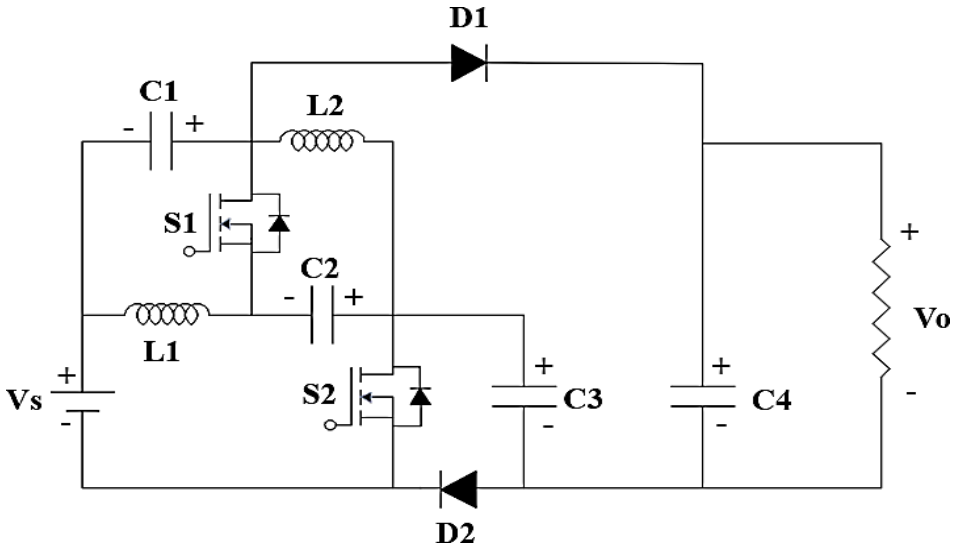
Based on the above equations, component values are calculated and used in the simulation of Cuk converter, which is presented in Table 3.

CUK CONVERTER



Design Parameter	Rating
Input Parameters	
Input Voltage,Vs	**24 V**
Switching Frequency, f	**25 kHz**
Obtained Output	
Output Voltage,Vout	**23.1 V**
Output Current, Iout	**0.23A**
Overall Efficiency,ɳ	**67.6%**

QUASI Z-SOURCE CONVERTER



S.NO	Components	Values
1	Input Inductor, L1	20 mH
2	Input Filter Capacitor, C1	200 µF
3	Magnetizing inductor, L2	20 mH
4	Storage Capacitors, C2 & C3	650 µF
5	Output Capacitor, C4	1000 µF
6	Resistive Load, R	100 Ω

Design Equations of Quasi Z-source converter

The input inductor L1 can be determined by,

$$L_1 \geq \frac{D(1-D)V_S}{\Delta i_{L1} f_S (1-2D)} \qquad (14)$$

Similarly, inductor L2 can be determined by,

$$L_2 \geq \frac{D(1-D)V_S}{\Delta i_{L2} f_S (1-2D)} \qquad (15)$$

The Capacitors C1-4 value can be determined by,

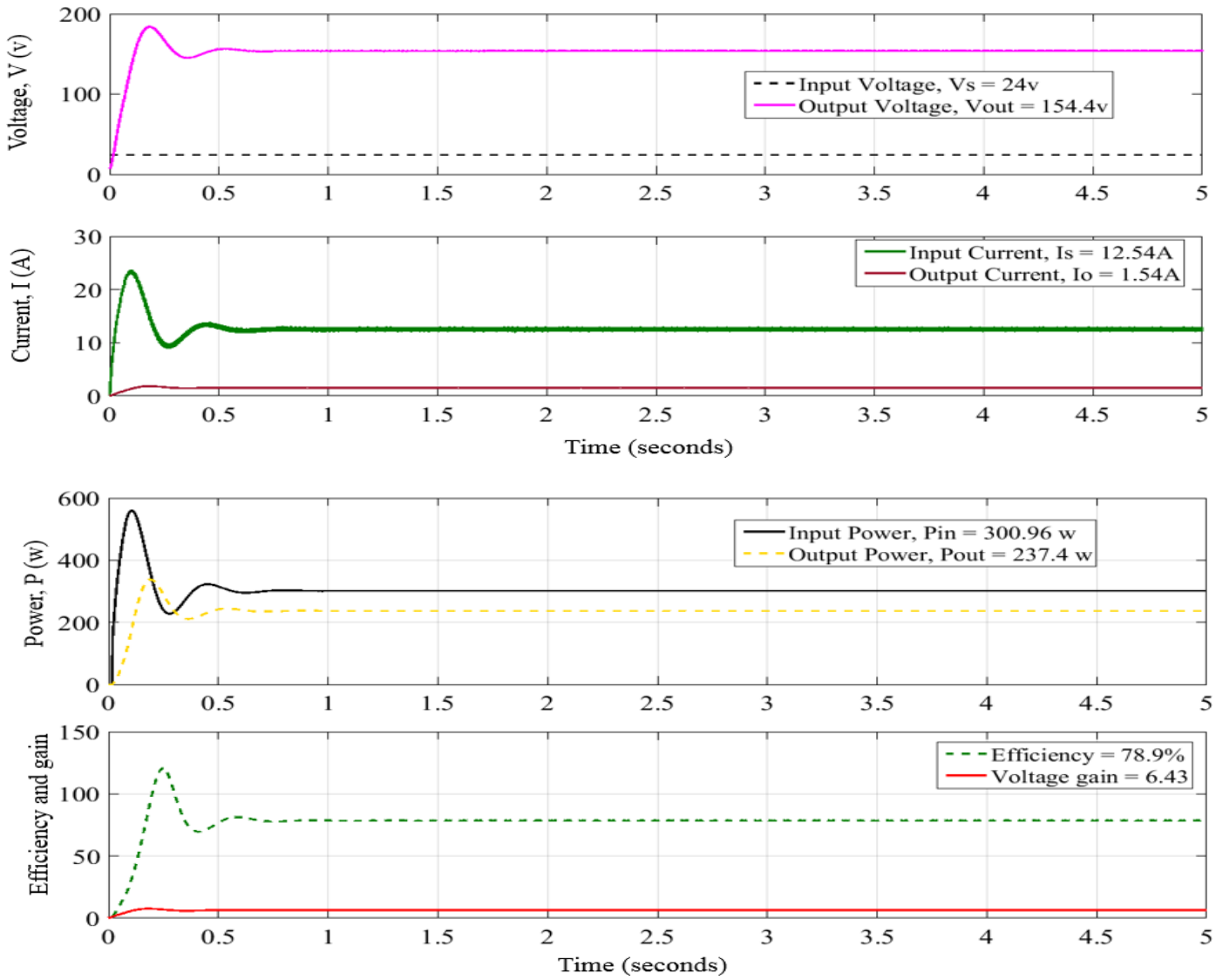
$$C_1 \geq \frac{I_{L2}(1-D)}{\Delta V_{C1} f_s} \qquad (16)$$

$$C_2 \geq \frac{I_{L2}(1-D)}{\Delta V_{C2} f_s} \qquad (17)$$

$$C_3 \geq \frac{I_o}{\Delta V_{C3} f_s} \qquad (18)$$

$$C_4 \geq \frac{I_o(1-D)}{\Delta V_{C4} f_s} \qquad (19)$$

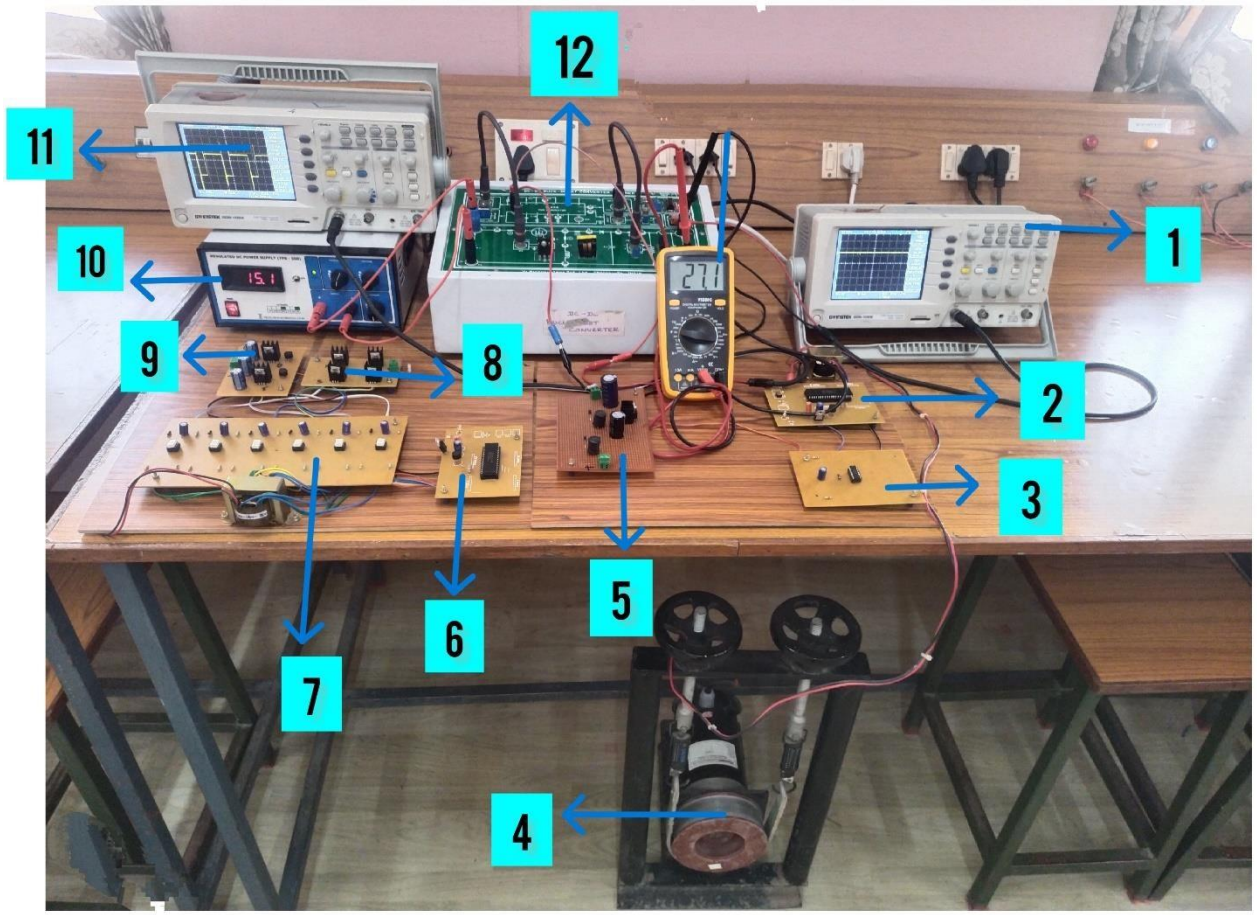
QUASI Z-SOURCE CONVERTER



Design Parameter	Rating
Input Parameters	
Input Voltage,Vs	**24 V**
Switching Frequency, f	**25 kHz**
Obtained Output	
Output Voltage,Vout	**154.4 V**
Output Current, Iout	**1.54A**
Overall Efficiency,ɳ	**78.9%**

HARDWARE SNAPSHOT AND SPECIFICATION

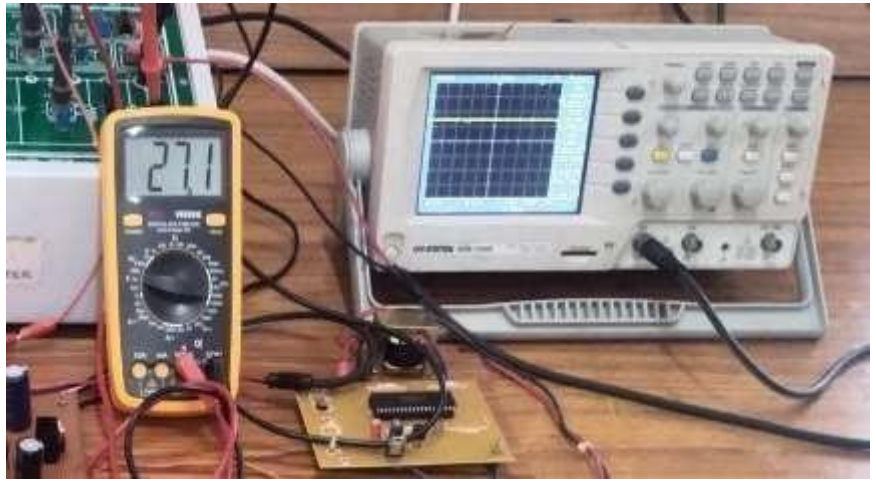
HARDWARE SNAPSHOT

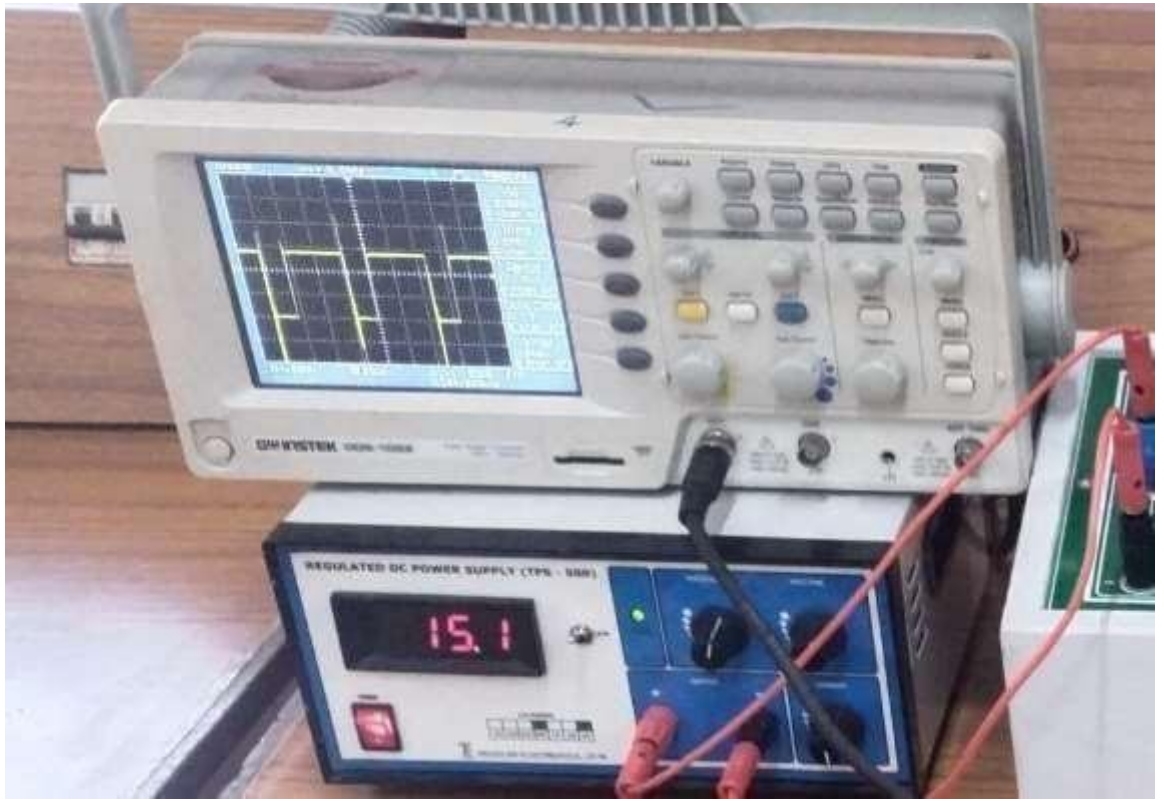


Component Names

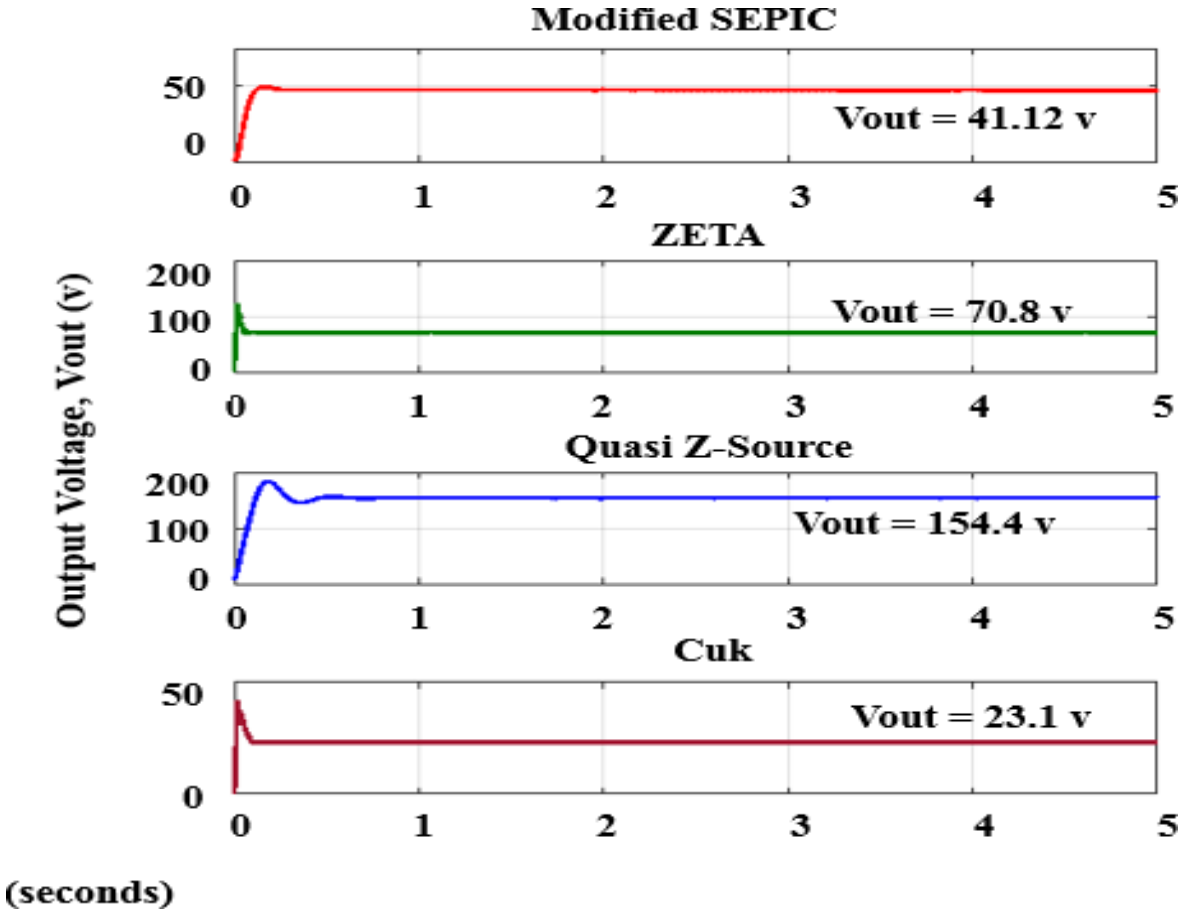
1. Input Waveform
2. Gate Input Signal
3. Gate Drive IC
4. BLDC Motor
5. Driver Circuit
6. Microcontroller
7. Switching Control
8. MOSFET Switches
9. Bridge Rectifier
10. Voltage Regulator
11. Output Waveform
12. Buck-Boost Converter

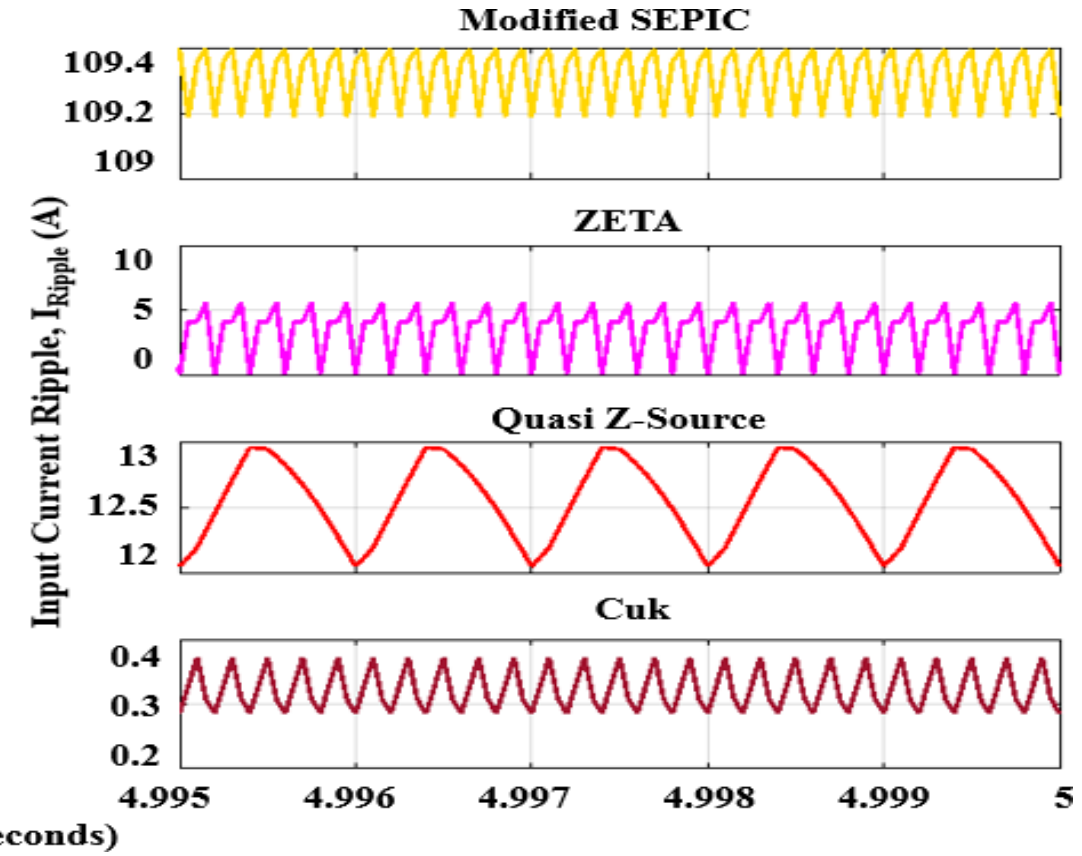
HARDWARE OUTPUT



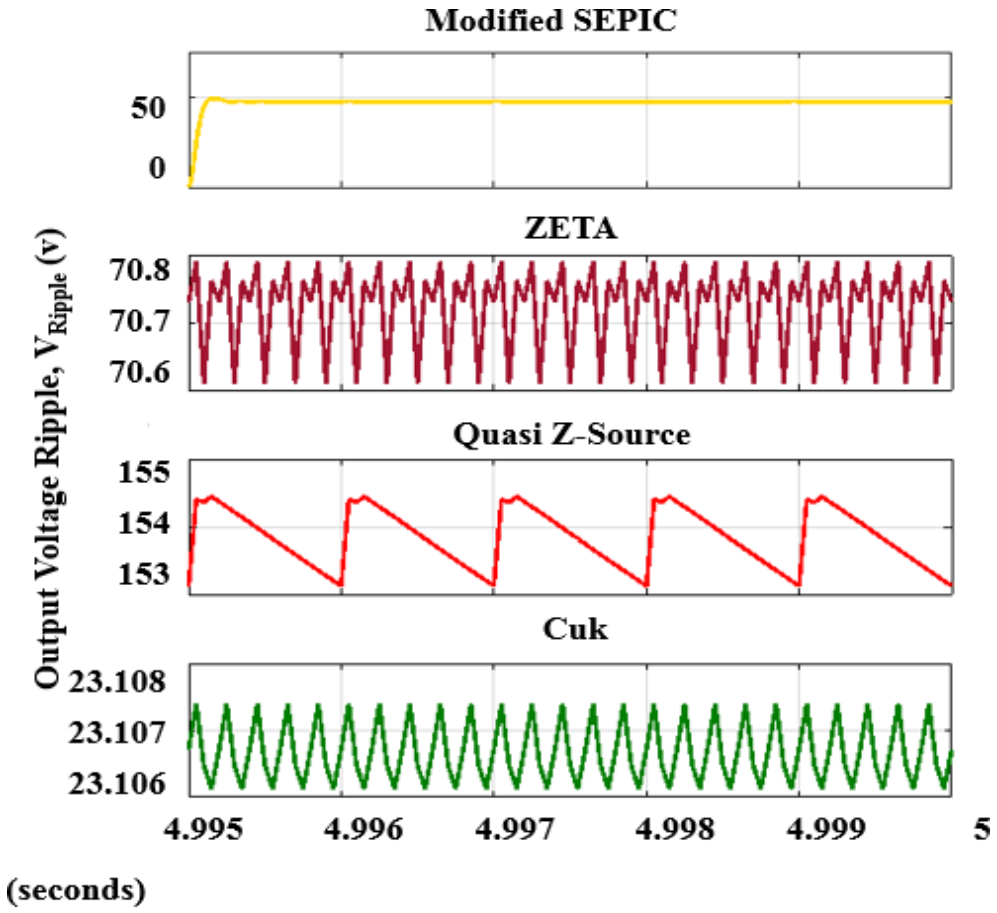


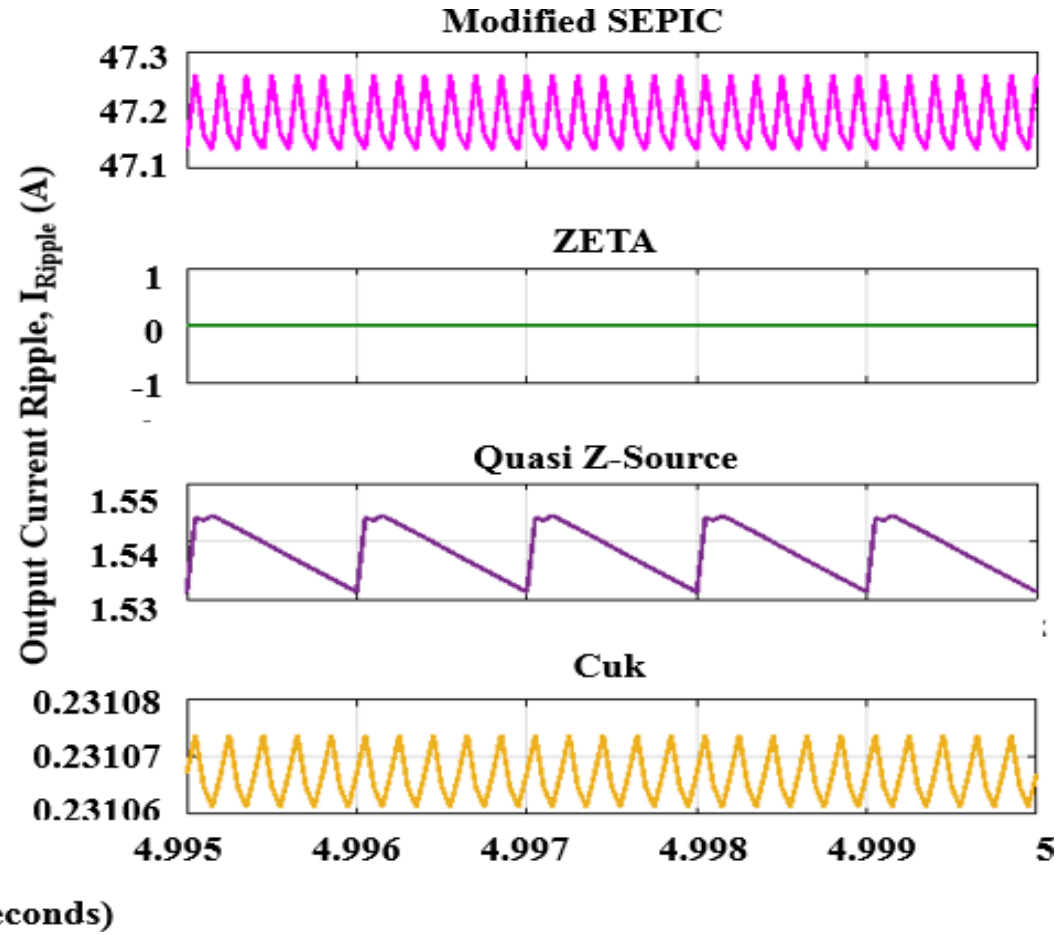
COMPARSION ON VARIOUS CONVERTERS





COMPARSION ON VARIOUS CONVERTERS





COMPARISON RESULTS BETWEEN VARIOUS CONVERTERS

Converter topologies	Input current, A	Output voltage, V	Output current, A	Reduced Output ripple%	No. of components
Modified SEPIC	95	41.12	41.12	0.30	11
ZETA	2.79	70.8	0.001	0.40	6
Cuk	0.33	23.1	0.23	0.34	6
Quasi Z-source	12.54	154.4	1.54	0.42	10

CONCLUSION & FUTURE SCOPE

CONCLUSION

Modified SEPIC Converter is designed & developed and is compared with various converters like Zeta, Cuk and Quasi-Z source converters. Modified SEPIC converter produces output voltage and output current as 41.2v and 41.12A respectively, it is 1.99 times of the voltage conversion ratio, output ripple is observed as 0.30% with an efficiency of 73.8%.

FUTURE SCOPE

A modified SEPIC converter can have several potential future scopes, including:

- **High power applications:** The SEPIC converter is typically used in low-power applications, but a modified SEPIC converter could potentially be designed for high power applications, such as electric vehicle charging stations or renewable energy systems.
- **Higher efficiency:** A modified SEPIC converter could be designed to increase its efficiency by reducing losses in the circuit, such as switching losses.
- **Multi-output converter:** A modified SEPIC converter can be designed to provide multiple outputs, which could be useful in applications that require different voltage levels.
- **Renewable energy systems:** A modified SEPIC converter can be used in renewable energy systems, such as solar or wind power, to convert the DC voltage generated by the panels or turbines to a voltage suitable for charging batteries.

REFERENCE

YEAR	AUTHOR	ARTICLES	LINK
Feb 2018	A. Anand and B. Singh	"Power Factor Correction in Cuk– SEPIC-Based Dual-Output-Converter-Fed SRM Drive", IEEE Transactions of Industrial Electronics, vol. 65, no. 2, pp. 1117- 1127	https://doi.org/10.1109/TIE.2017.2733482.
2015	Bhim Singh, Vashit Bist, Chandra A, and Al-Haddad K	"Power Factor Correction in Bridgeless-Luo Converter fed BLDC Motor Drive", IEEE Transactions of Industry Applications, Vol. 51, No. 2, pp. 1179 – 1188	https://doi.org/10.1109/TIA.2014.2344502.
July 2020	N. Kumarasabapathy & M. Ramasamy,	"Modified isolated power factor correction Cuk-converter fed BLDC motor drive with Fuzzy Logic Controller for pumping applications" *Journal of the Chinese Institute of Engineers*, Vol. 43, no. 6, pp. 553 - 565	https://doi.org/10.1080/02533839.2020.1777204

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May 2020	Rodnei Regis de Melo, Fernando Lessa Tofoli, Sergio Daher and Fernando Luiz Marcelo Antunes	"Interleaved bidirectional DC - DC converter for electric vehicle applications based on multiple energy storage devices", *Electrical Engineering*, Springer Publications	https://doi.org/10.1007/s00202-020-01009-3.
2017	Vaiyapuri Viswanathan & Seenithangom Jeevananthan	"Hybrid converter topology for reducing torque ripple of BLDC motor", *IET Power Electronics*, Vol. 10, No. 12, pp. 1572-1587	https://doi.org/10.1049/iet-pel.2015.0905.

PUBLICATION
IEEE Conference

2023 IEEE Sponsored Third International Conference on Advances in Electrical, Computing, Communication and Sustainable Technologies (ICAECT 2023)

05-06 January 2023, Bhilai, Chhattisgarh

Design and Implementation of Modified SEPIC, ZETA, Cuk, Quasi Z Source Converter for BLDC Drive System –AComparativeAnalysis

Thank you