# CBCS SCHEME

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15CS72

## Seventh Semester B.E. Degree Examination, Jan./Feb. 2021 **Advanced Computer Architectures**

Time: 3 hrs.

Max. Marks: 80

Note: Answer any FIVE full questions, choosing ONE full question from each module.

## Module-1

- a. Describe with a neat diagram different shared memory multiprocessor models.
  - b. A 400 MHz processor was used to execute a program with the following instruction mix and clock cycle counts:

Instruction Type	Instruction Count	Clock Cycle Count
Integer Arithmetic	450000	1
Data Transfer	320000	2
Floating Point	150000	2
Control Transfer	80000	2

Determine the effective CPI, MIPS rate and execution time for this program.

(07 Marks)

## OR

a. Explain the different types of data dependences. Draw the dependence graph for the following code segment:

 $S_1$ : Load  $R_1$ , A

 $/R_i \leftarrow Memory(A)/$ 

 $S_2$ : Add  $R_2$ ,  $R_1$ 

 $/R_2 \leftarrow (R_1) + (R_2)$ 

 $S_3$ : Move  $R_1$ ,  $R_3$ 

 $/R_1 \leftarrow (R_3)/$ 

S<sub>4</sub>: Store B, R<sub>1</sub>

 $/Memory(B) \leftarrow (R_1)/$ 

(08 Marks)

b. List the different types of static connection networks and explain any three in detail.

(08 Marks)

## Module-2

a. Differentiate between CISC and RISC architecture.

(06 Marks)

b. Explain in detail Inclusion, coherence and Locality properties.

(10 Marks)

## OR

a. Explain with a neat diagram Hierarchical Memory Technology.

(08 Marks)

Explain the architecture of VLIW processor and its pipeline operation.

(08 Marks)

#### Module-3

- What is arbitration? Describe central arbitration and distributed arbitration with relevant
  - Explain direct mapping cache organization. Mention its advantages and disadvantages.

(07 Marks)

OR

1 of 2

Important Note: 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.

2. Any revealing of identification, appeal to evaluator and /or equations written eg, 42+8 = 50, will be treated as malpractice.

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6 a. Consider the following reservation table for a three-stage pipeline.

	1	2	3	4	5	6	7	8
$S_1$	X					X		X
$S_2$		X		X		Y		
$S_3$			X		X		X	

- (i) What are the forbidden latencies and initial collision vector?
- (ii) Draw the state transition diagram.
- (iii) List all simple cycles and greedy cycles.
- (iv) Determine MAL.
- (v) Determine the pipeline throughput.

(10 Marks)

b. List the different mechanisms for instruction pipelining. Explain any one in detail. (06 Marks)

#### Module-4

- a. What is cache coherence problem? What are the different causes of cache inconsistencies? Explain n detail. (10 Marks)
  - b. Explain store and forward routing and wormhole routing related to message routing.

(06 Marks)

#### OR

- 8 a. Describe with relevant sketches three types of cache directory protocols. (10 Marks)
  - b. Explain the context switching policies.

## (06 Marks)

#### Module-5

- Explain synchronous message passing and asynchronous passing related to message passing model. (08 Marks)
  - b. Explain object oriented programming model.

## (08 Marks)

## OR

- 10 a. Explain the concept of operand forwarding with suitable example. (08 Marks)
  - b. Describe in brief Tomasulo's algorithm.

(08 Marks)