Girish Mururu

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My current research involves enhancing the performance of systems using compilers and studying nondeterminism in systems and in other areas of system software

Education

Ph.D. Computer Science, Georgia Institute of Technology, Atlanta, Georgia GPA 3.90 (Expected: May 2020)

M.S. Computer Science, Georgia Institute of Technology, Atlanta, Georgia Dec. 2014 GPA 3.92 B.E. Computer Science, R.V. College of Engineering, Bengaluru, India GPA 9.35 June 2011

Expertise

Programming Languages: C, C++, Java, Python, COQ, ASM, MFC, Perl

LLVM, Clang, Curator Programming:

> Tools: Git, GDB, WINDBG, Latex, Emacs, Eclipse, Perforce, Visual Studio, Ant, Maven

Operating Systems Used Linux, MacOS, Windows

> Algorithms, Compilers, Systems, Computer Architecture, Networks Courses In:

Work Experience

intern | Cloud Platform Architecture, VMware, Palo Alto, California Summer 2016

- > Implemented a wrapper library, Panda, for distributed services
- > Used curator and corfuDB as underlying libraries for Panda
- > Provided a single interface such that the underlying libraries can be switched without breaking dependencies

Curator CorfuDB Eclipse Maven Git

intern | Parallel Languages Compiler, Intel, Nashua, NH

Summer 2015

- > Worked on proof of concept of proposed changes to C and C++ languages
- > Developed support for task parallelism in Clang/LLVM for C and C++

C C++ Clang LLVM Git

Graphics Software Engineer, Intel, Bengaluru, India

June 2011 - July 2013

- > Worked on development of different display protocols such as HDMI, DP
- > Implemented new features such as smooth scaling in intel display driver
- > Worked on the proof of concept for new display protocol USBAV protocol
- > Implemented interrupt handling for the Intel Gen 6 processor (Skylake)

C WINDBG Visual Studio MFC Perforce

intern | Graphics Software, Intel, Bengaluru, India

Spring 2011

- > Designed and developed a tool to validate display configuration of the Intel Gen 3 processor (Ivvbridge)
- > Enabled OEMs to design suitable display contours through the tool

C WINDBG Visual Studio MFC

intern | Embedded Software, ITTIAM Systems, Bengaluru, India

> Designed and developed a statistics-collection module for multi-threaded applications in embedded systems

C Visual Studio

m Georgia Institute of Technology, Atlanta, Georgia

Beacons: compiler aided scheduling

(Current)

- > Worked on increasing the throughput of servers
- > Analyzed and classified the regions of the code with huge memory footprint using
- > Used machine learning for region timing analysis
- > Worked on user level scheduler that acts on beacons from processes
- > Collaborated with Christopher Porter, Ada Gavrilovska, and Santosh Pande

C++ LLVM Polly Git R Python

BlankIt: Attack Surface Reduction via Demand Driven Loading

(Current)

- > Worked on reducing the library code surface avaiable at runtime
- > Used machine learning to predict the call chain within the library
- > Unblanked/Blankded only the required code during execution
- > Collaborated with Christopher Porter, Prithayan Barua, and Santosh Pande

C++ LLVM IntelPin Python Git

Pinit: Influencing OS Scheduling via Compiler-Induced Affinities

(Current)

- > Worked on increasing the throughput of servers by minimally pinning the applications during execution to avoid cache misses
- > Used compiler analysis for finding the regions of the code that can be pinned
- > Collaborated with Vincent Ni, Ada Gavrilovska, and Santosh Pande

C++ LLVM Polly Python Git

Generating Robust Parallel Programs via Model Driven Prediction of Compiler Optimizations (Current)

- > Proposed a systematic way of generating a performance model that captures the sensitivity of non-determinism to different architectural artifacts
- > Leveraged the model to detect the right compiler flag for an application that can eliminate data race conditions
- > Collaborated with Kaushik Ravichandran, Ada Gavrilovska and Santosh Pande C | Python | PAPI | Intel Vtune |

Quantifying and Reducing Execution Variance in STM via Model Driven Commit Optimization CGO 19, PPoPP 2018 (Poster)

- > Worked on minimizing the variance in the execution time of threads participating in transactions
- > Built a framework for guiding the STM based on the training model
- Collaborated with Ada Gavrilovska and Santosh Pande

C Python TL2 STM SynQuake

Transformers: The Advent of Dark Silicon

PACT 2015 (Poster)

- > Proposed and developed a technique to leverage the phenomenon of dark silicon to transform between multiple micro-architectures
- > Collaborated with Anshul Bansal

C++ Macsim

Mini-Projects

Aug 2013 - Dec 2014

- > Quantum Distributed Computing: Demonstrated distributed services such as leader election, distributed locking in Quantum computing
- > Cluster Fair Scheduling: Implemented distributed fair job scheduling using sockets in Java
- > Redundant Array Bounds (Team of 2): Developed a framework for generating safe C code by inserting array bound checks
- > Network Packet Capture (Team of 2): Developed a Linux loadable kernel module and a PCAP module for capturing network packets
- > GTThreads: Converted a process-wide completely-fair scheduler into thread-wide completely fair scheduler
- > Out-of-order Pipelined Processor: Constructed a simulator that uses Tomasulo's

Java C++ LLVM Python C Git

R. V. College of Engineering, Bengaluru, India

OASM: One pass Assembler

(May 2010)

- > Proposed and developed a new algorithm for one pass assembler
- > Collaborated with Girish Kumar

▼ Teaching Experience

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Head Teaching Assistant, Compilers: Theory & Practice (OMSCS), Summer 2017, Spring 2017, Fall 2017

- > Answered the gueries of students on piazza and during office hours
- > Designed a framework for the project, compiler for the Tiger language

Head Teaching Assistant, Compilers & Interpreters, Fall 2016, Fall 2018

- > Answered the gueries of students during office hours and also on piazza
- > Guided students in implementing a complete compiler for the Tiger language

Teaching Assistant, Embedded Software (OMSCS), Spring 2016

- > Answered the gueries of students on piazza and during office hours
- > Designed one of the projects in Vex